HS54095

Silicon N Channel MOS FET
High Speed Power Switching

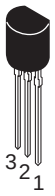
REJ03G1668-0200
Rev.2.00
Dec 10, 2009

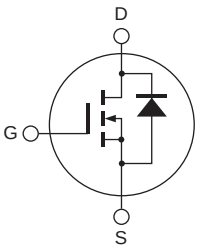
Features

- Low on-resistance
  $R_{DS(on)}$ = 13.5 Ω typ. (at I_D = 0.1 A, V_{GS} = 10 V, Ta = 25°C)
- Low drive current
- High density mounting

Outline

RENESAS Package code: PRSS0003DA-A
(Package name: TO-92(1))





1. Gate
2. Drain
3. Source

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	600	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	0.2	A
Drain peak current	$I_{D\ (pulse)}^{Note1}$	0.8	A
Body-drain diode reverse drain current	I_{DR}	0.2	A
Body-drain diode reverse drain peak current	$I_{DR\ (pulse)}^{Note1}$	0.8	A
Channel dissipation	Pch	0.75	W
Channel to ambient thermal impedance	θ_{ch-a}	166.7	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

Electrical Characteristics

(Ta = 25°C)

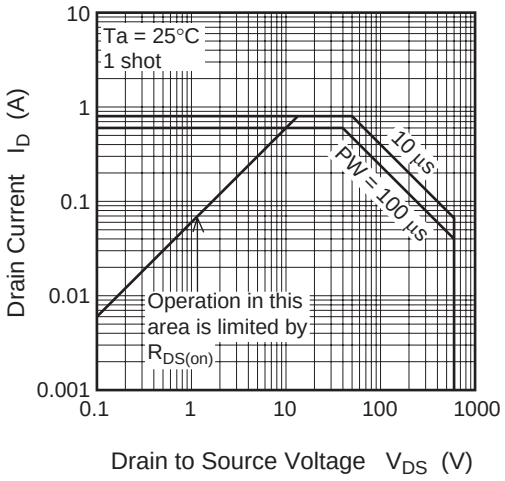
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	I_D = 10 mA, V_{GS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 600 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±30 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	3	—	5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	13.5	16.5	Ω	I_D = 0.1 A, V_{GS} = 10 V Note2
Input capacitance	Ciss	—	66	—	pF	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	8.7	—	pF	
Reverse transfer capacitance	Crss	—	1.3	—	pF	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 0.1 A V_{GS} = 10 V R_L = 3000 Ω Rg = 10 Ω
Rise time	t_r	—	15	—	ns	
Turn-off delay time	$t_{d(off)}$	—	51	—	ns	
Fall time	t_f	—	175	—	ns	
Total gate charge	Qg	—	4.8	—	nC	V_{DD} = 480 V V_{GS} = 10 V I_D = 0.2 A
Gate to source charge	Qgs	—	0.6	—	nC	
Gate to drain charge	Qgd	—	3.2	—	nC	
Body-drain diode forward voltage	V_{DF}	—	0.77	1.30	V	I_F = 0.2 A, V_{GS} = 0 Note2
Body-drain diode reverse recovery time	t_{rr}	—	220	—	ns	I_F = 0.2 A, V_{GS} = 0 di_F/dt = 50 A/μs

Notes: 2. Pulse test

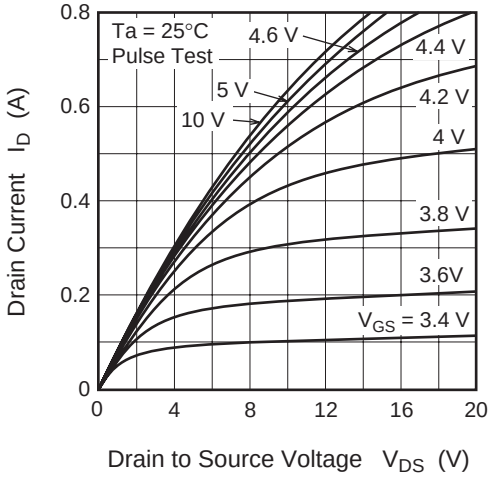
3. Since this device is equipped with high voltage FET chip (V_{DSS} ≥ 600 V), high voltage may be supplied. Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.
4. This device is sensitive to electrostatic discharge. It is recommended to adopt appropriate cautions when handling this product.

Main Characteristics

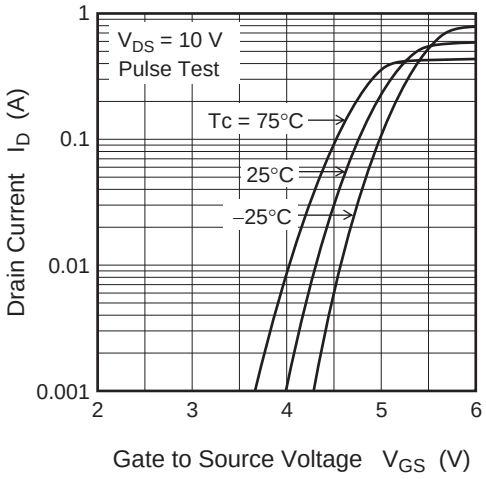
Maximum Safe Operation Area



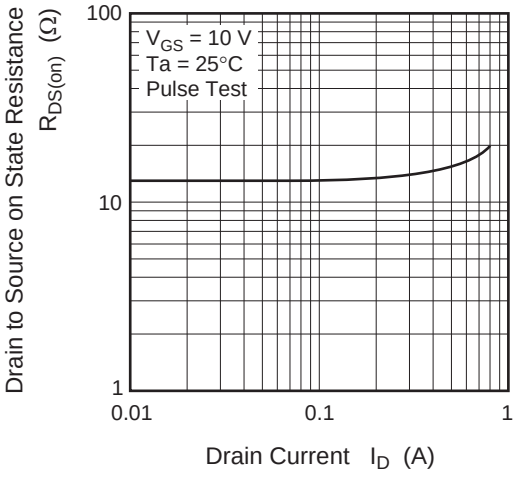
Typical Output Characteristics



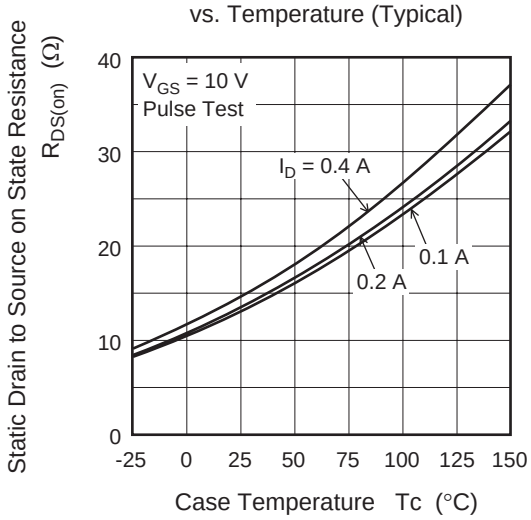
Typical Transfer Characteristics



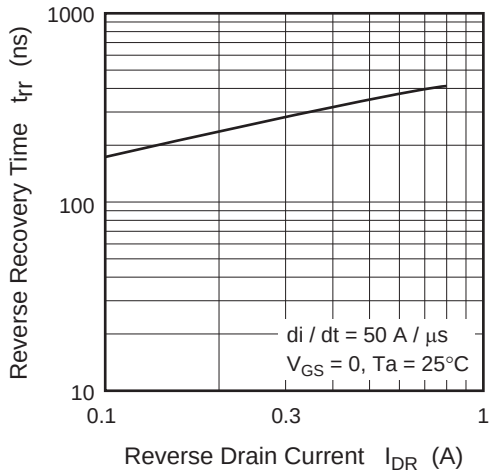
Static Drain to Source on State Resistance vs. Drain Current (Typical)



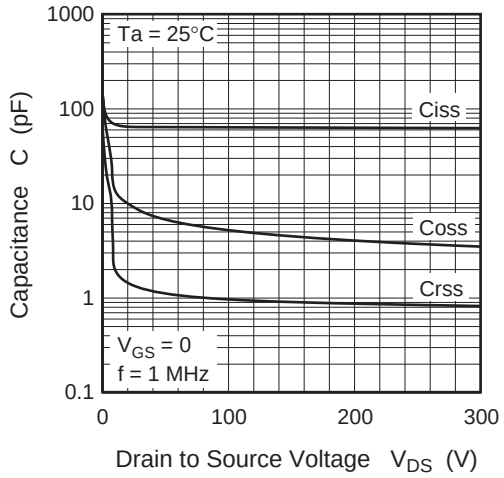
Static Drain to Source on State Resistance vs. Temperature (Typical)



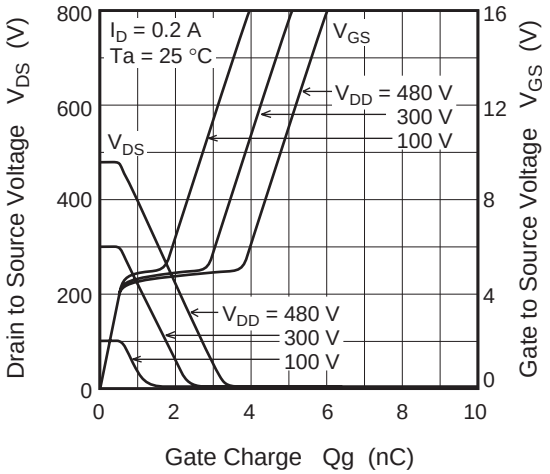
Body-Drain Diode Reverse Recovery Time (Typical)



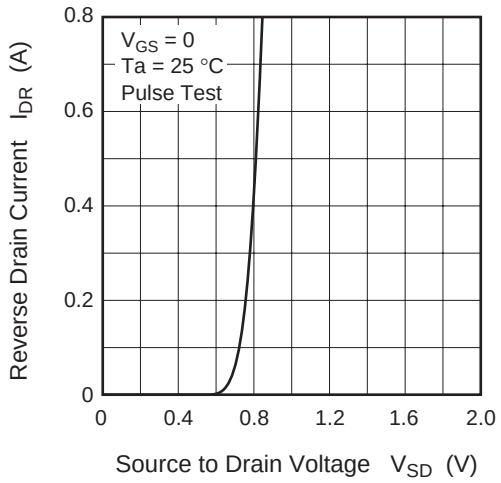
Typical Capacitance vs.
Drain to Source Voltage



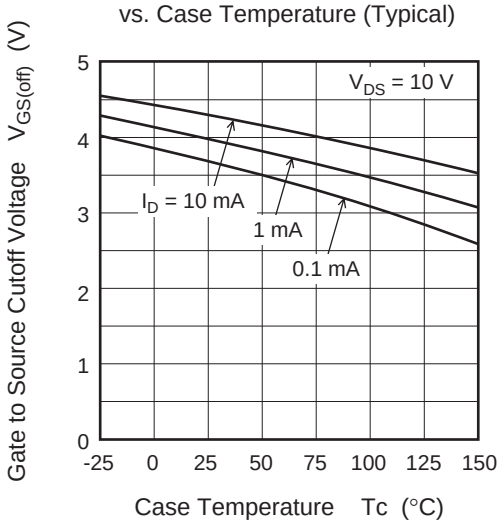
Dynamic Input Characteristics (Typical)



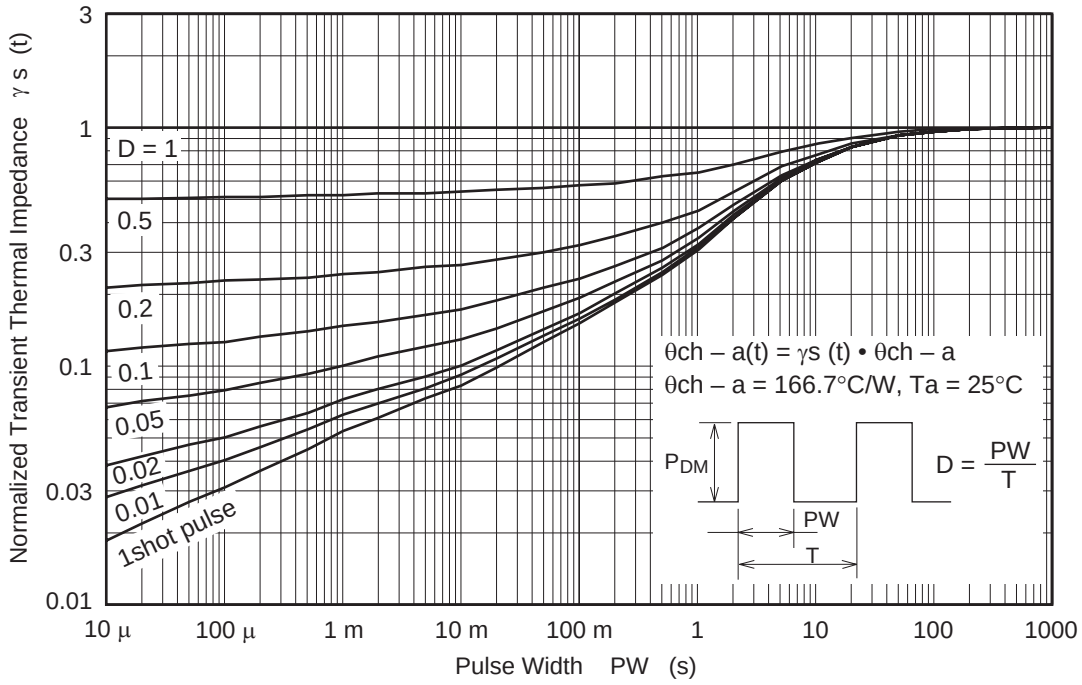
Reverse Drain Current vs.
Source to Drain Voltage (Typical)



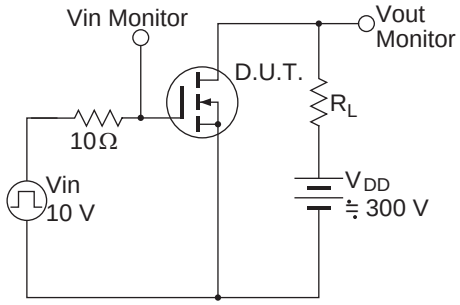
Gate to Source Cutoff Voltage
vs. Case Temperature (Typical)



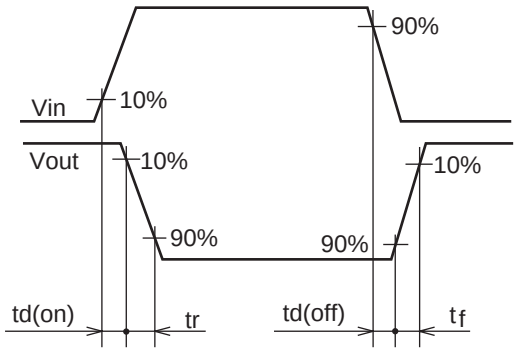
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



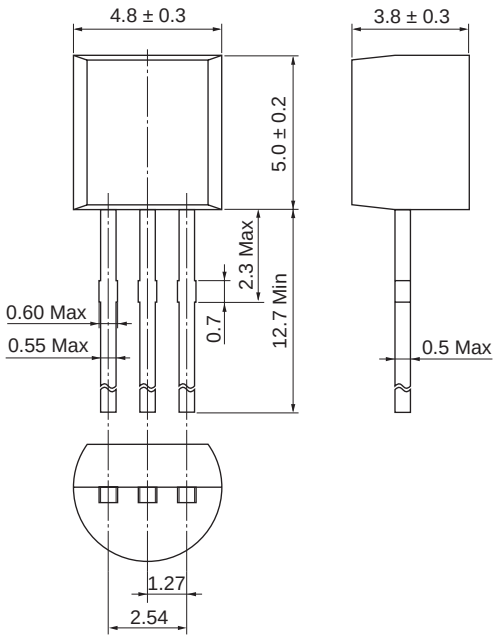
Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
TO-92(1)	SC-43A	PRSS0003DA-A	TO-92(1) / TO-92(1)V	0.25g

Unit: mm



Since HS54095 is equipped with high voltage FET chip (V_{DSS} ≥ 600 V), high voltage may be supplied.
Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.

Ordering Information

Part No.	Quantity	Shipping Container
HS54095TZ-E	2500 pcs	Hold Box, Radial Taping

Note: Leads is forming applied as following figure.

Unit: mm