TO :

Date : May, 27, 2010

# Customer Acceptance Specification

## 10” Color TFT-LCD Module

Model: **HSD100IXN1**

**-A****

相關文件：

| Accepted by: | |
|---|---|
| Signature | Date |
| | |
| Proposed by: Technical Service Division | |
| Signature | Date |
| | |

Note:
1. Please contact HannStar Display Corp. before designing your product based on this module specification.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by HannStar for any intellectual property claims or other problems that may result from application based on the module described herein.

# Record of Revisions

| Rev. | Date | Sub-Model | Description of change |
|---|---|---|---|
| 1.0 | May, 27, 2010 | A** | Formal Product Specification was first released |

# Contents

# 1.0 GENERAL DESCRIPTION

## 1.1 Introduction

HannStar Display model HSD100IXN1-A** is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back light system. This TFT LCD has a 10 (4:3) inch diagonally measured active display area with XGA (1024 horizontal by 768 vertical pixel) resolution.

## 1.2 Features

- 10 (4:3 diagonal) inch configuration
- 6 bits driver with 1channel TTL interface
- RoHS and Halogen-Free Compliance

## 1.3 Applications

- Digital Photo frame
- Multimedia applications and Others AV system

## 1.4 General information

| Item | | Specification | Unit |
|---|---|---|---|
| Outline Dimension | | 215.5 x 166.5 x 5.0 (Typ.) | mm |
| Display area | | 202.752 (H) x 152.064 (V) | mm |
| Number of Pixel | | 1024 RGB (H) x 768(V) | pixels |
| Pixel pitch | | 0.198(H) x 0.198(V) | mm |
| Pixel arrangement | | RGB Vertical stripe | |
| Display mode | | Normally white | |
| Surface treatment | | Antiglare, Hard-Coating (3H) | |
| Weight | | 330 (Typ.) | g |
| Back-light | | Single LED (Side-Light type) | |
| Power Consumption | Logic System | 0.75 (Max.) | W |
| | B/L System | 2.64 (Max.) | W |

## 1.5 Mechanical Information

| Item | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Module Size | Horizontal (H) | 215.2 | 215.5 | 215.8 | mm |
| | Vertical (V) | 166.2 | 166.5 | 166.8 | mm |
| | Depth (D) | – | 5.0 | 5.3 | mm |
| Weight | | – | 330 | – | g |

# 2.0 ABSOLUTE MAXIMUM RATINGS

## 2.1 Electrical Absolute Rating

### 2.1.1 TFT LCD Module

| Item | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Digital Supply voltage | VCC | -0.5 | 5 | V | |
| Analog Supply voltage | AVDD | -0.5 | 13.5 | V | |
| Supply voltage | V1~V7 | 0.4AVDD | AVDD+0.3 | V | |
| | V8~V14 | -0.3 | 0.6AVDD | V | |
| Digital input voltage | - | -0.5 | VCC+0.5 | V | |

### 2.1.2 Back-Light Unit

| Item | Symbol | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|
| LED current | $I_L$ | 220 | — | mA | (1) (2)(3) |
| LED voltage | $V_L$ | 10.5 | — | V | (1) (2)(3) |

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) Ta =25±2℃

(3) Test Condition: LED current 220 mA. The LED lifetime could be decreased if operating $I_L$ is larger than 220mA.

## 2.2 Environment Absolute Rating

| Item | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Operating Temperature | $T_{opa}$ | -20 | 70 | ℃ | |
| Storage Temperature | $T_{stg}$ | -30 | 80 | ℃ | |

## 3.0 OPTICAL CHARACTERISTICS

### 3.1 Optical specification

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Contrast | | CR | Θ=0 Normal viewing angle | 480 | 600 | — | | (1)(2) |
| Response time | Rising | $T_R$ | | — | 2.4 | 4.8 | msec | (1)(3) |
| | Falling | $T_F$ | | — | 5.6 | 11.2 | | |
| White luminance (Center) | | $Y_L$ | | 200 | 250 | — | $cd/m^2$ | (1)(4) ($I_L$=220mA) |
| Color chromaticity (CIE1931) | White | $W_x$ | | 0.260 | 0.310 | 0.360 | | (1)(4) |
| | | $W_y$ | | 0.280 | 0.330 | 0.380 | | |
| Viewing angle | Hor. | $\Theta_L$ | CR>10 | 65 | 75 | — | | |
| | | $\Theta_R$ | | 65 | 75 | — | | |
| | Ver. | $\Theta_U$ | | 50 | 60 | — | | |
| | | $\Theta_D$ | | 60 | 70 | — | | |
| Brightness uniformity | | $B_{UNI}$ | Θ=0 | 70 | - | — | % | (5) |
| Optima View Direction | | 6 O' clock | | | | | | (6) |

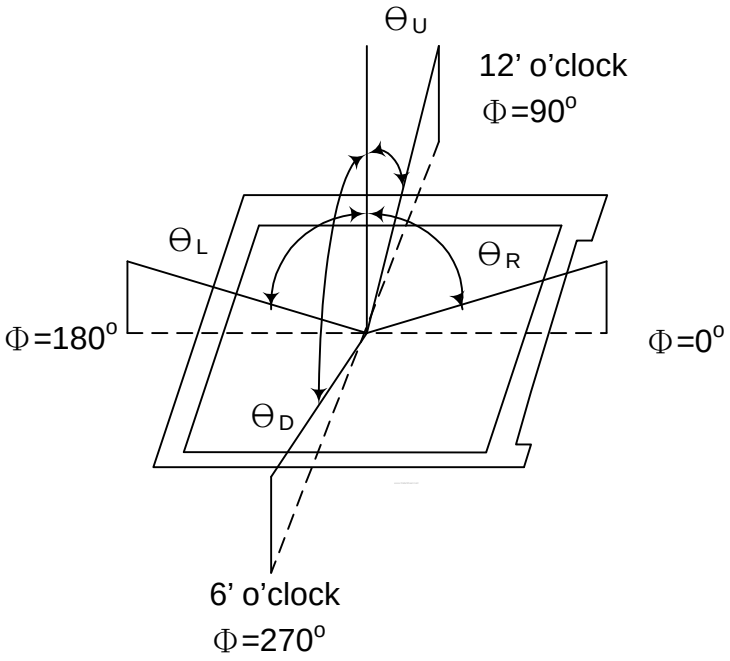
### 3.2 Measuring Condition

- Measuring surrounding：dark room
- LED current $I_L$：220mA
- Ambient temperature：25±2°C
- 15min. warm-up time.

### 3.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.
- Measuring spot size：20 ~ 21 mm

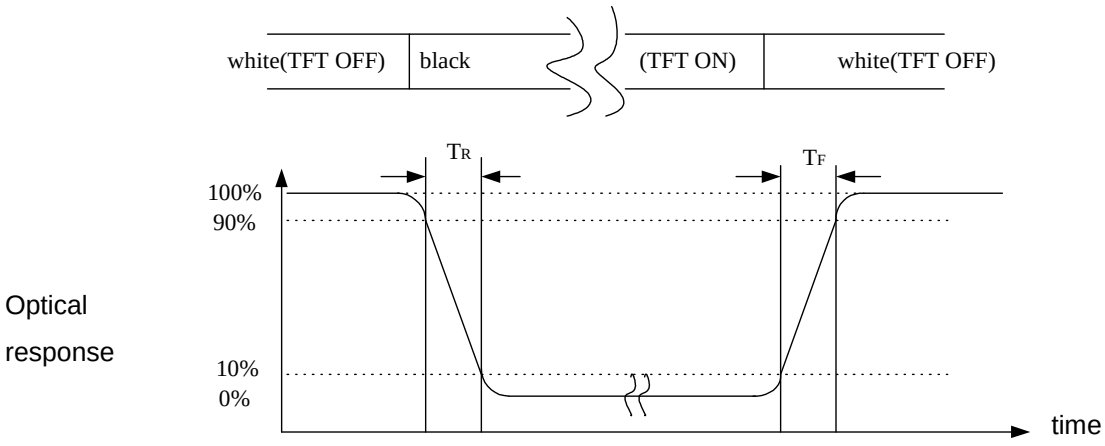
**Note (1)** Definition of Viewing Angle:



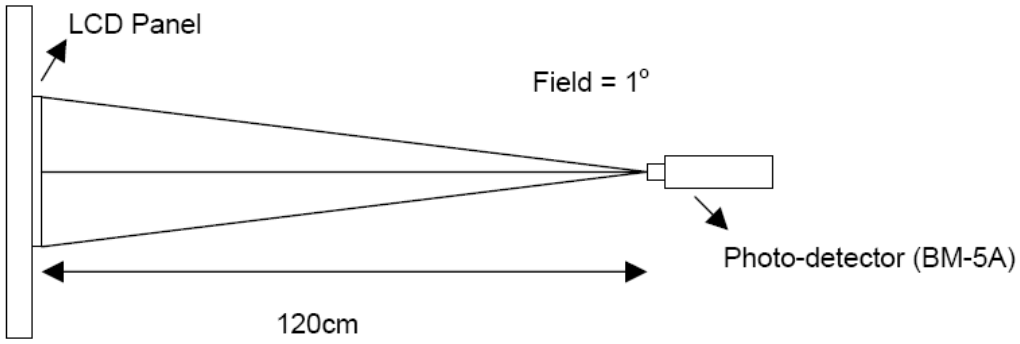

**Note (2)** Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

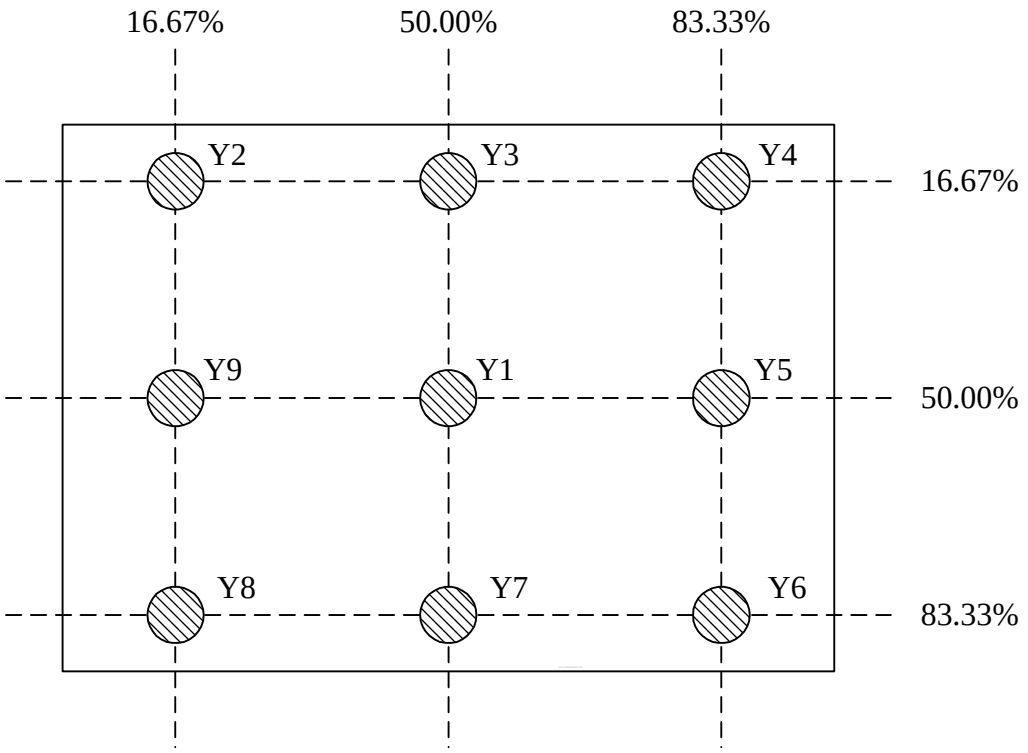
**Note (3)** Definition of Response Time : Sum of $T_R$ and $T_F$




**Note (4)** Definition of optical measurement setup



**Note (5)** Definition of brightness uniformity

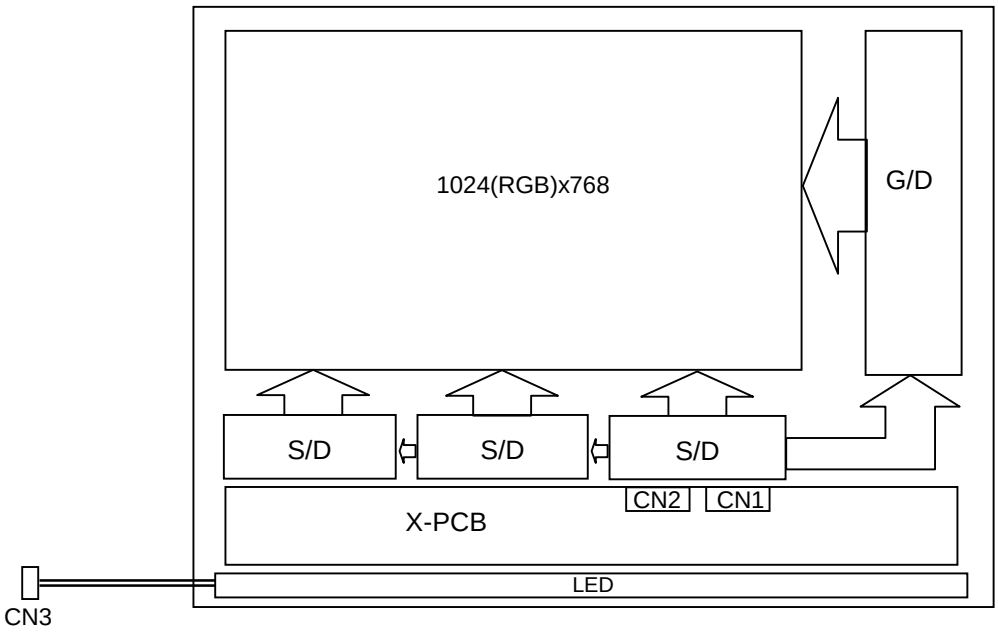



$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

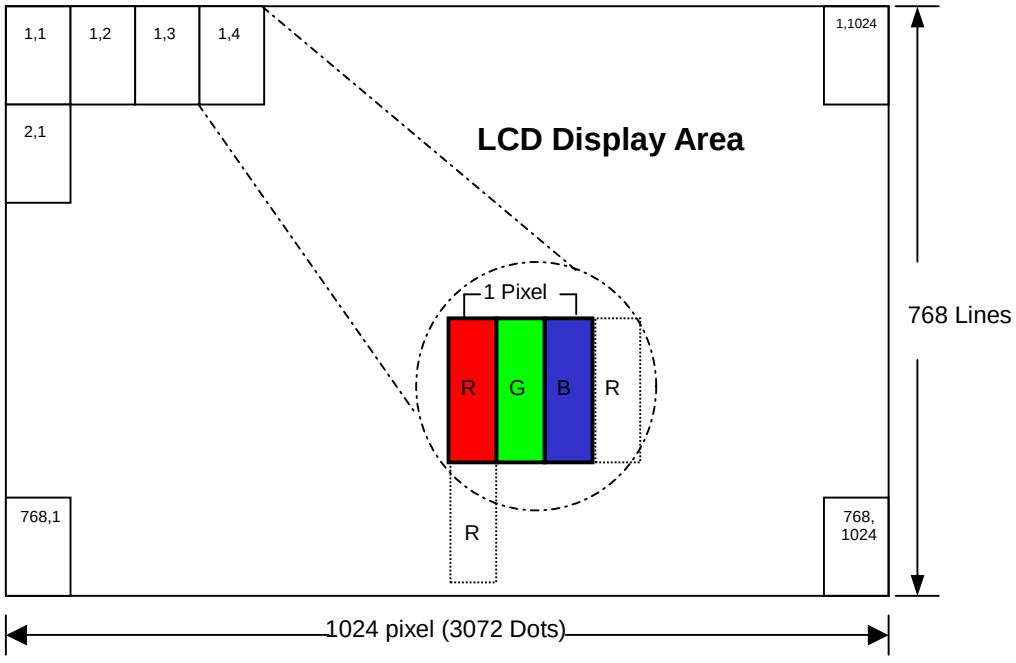
**Note (6)**：Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.

# 4.0 BLOCK DIAGRAM

## 4.1 TFT LCD Module:




## 4.2 Pixel Format



## 5.0 INTERFACE PIN CONNECTION

### 5.1 TFT LCD Module：

**CN1** (Input signal): 30pin, 0.5mm pitch, 196033-30041-3 (P-TWO or equivalent)

| Pin No. | Signal | Description |
|---|---|---|
| 1 | POL | Polarity Setting |
| 2 | STVD | Vertical Line start pulse I/O signal |
| 3 | OE123R | Vertical Line output Enable signal |
| 4 | G-CLKR | Vertical Line Clock |
| 5 | STVU | Vertical Line start pulse I/O signal |
| 6 | GND | Digital Power Ground |
| 7 | EDGSEL | Define clock edge select input, default EDGSEL=L.<br>EDGSEL=L Latch data by rising edge of clock<br>EDGSEL=H Latch data by rising and falling edges of clock |
| 8 | VCC | Digital Voltage Input |
| 9 | V9 | Gamma Voltage Input |
| 10 | VGL | Gate OFF Voltage |
| 11 | V2 | Gamma Voltage Input |
| 12 | VGH | Gate ON Voltage |
| 13 | V6 | Gamma Voltage Input |
| 14 | UDC | Shift up/down control signal<br>UDC = "H", up shift:<br>STVD (Input) →G1 ~ G600→STVU (Output)<br>UDC= "L", down shift:<br>STVU (Input) →G600~G1→STVD (Output) |
| 15 | VCOM | Common Voltage |
| 16 | AGND | Analog Power Ground |
| 17 | AVDD | Analog Voltage Input |
| 18 | V14 | Gamma Voltage Input |
| 19 | V11 | Gamma Voltage Input |
| 20 | V8 | Gamma Voltage Input |
| 21 | V5 | Gamma Voltage Input |
| 22 | V3 | Gamma Voltage Input |
| 23 | GND | Digital Power Ground |
| 24 | R5 | Red Data Bus Input (MSB) |
| 25 | R4 | Red Data Bus Input |
| 26 | R3 | Red Data Bus Input |
| 27 | R2 | Red Data Bus Input |
| 28 | R1 | Red Data Bus Input |
| 29 | R0 | Red Data Bus Input (LSB) |
| 30 | GND | Digital Power Ground |

**CN2** (Input signal): 30pin, 0.5mm pitch,196033-30041-3 (P-TWO or equivalent)

| Pin No. | Signal | Description |
|---|---|---|
| 1 | GND | Digital Power Ground |
| 2 | G5 | Green Data Bus Input (MSB) |
| 3 | G4 | Green Data Bus Input |
| 4 | G3 | Green Data Bus Input |
| 5 | G2 | Green Data Bus Input |
| 6 | G1 | Green Data Bus Input |
| 7 | G0 | Green Data Bus Input (LSB) |
| 8 | DIO2_COF3 | Horizontal Line start pulse I/O signal (STHR) |
| 9 | REV | Data Invert signal |
| 10 | GND | Digital Power Ground |
| 11 | CLK | Pixel clock |
| 12 | VCC | Digital Voltage Input |
| 13 | DIO1_COF1 | Horizontal Line start pulse I/O signal (STHL) |
| 14 | LD | Polarity latch and re-flash new data to output |
| 15 | B5 | Blue Data Bus Input (MSB) |
| 16 | B4 | Blue Data Bus Input |
| 17 | B3 | Blue Data Bus Input |
| 18 | B2 | Blue Data Bus Input |
| 19 | B1 | Blue Data Bus Input |
| 20 | B0 | Blue Data Bus Input (LSB) |
| 21 | LRC | Select left or right shift, normally pulled high.<br>SHL="1": DIO1→ OUT1,2,3→OUT4,5,6→ OUT1198,1199,1200 = DIO2<br>SHL="0": DIO1= OUT1,2,3 ← OUT4,5,6← OUT1198,1199,1200←DIO2 |
| 22 | V1 | Gamma Voltage Input |
| 23 | V4 | Gamma Voltage Input |
| 24 | V7 | Gamma Voltage Input |
| 25 | V10 | Gamma Voltage Input |
| 26 | V12 | Gamma Voltage Input |
| 27 | V13 | Gamma Voltage Input |
| 28 | AVDD | Analog Voltage Input |
| 29 | AGND | Analog Power Ground |
| 30 | VCOM | Common Voltage |

## 5.2 Back-Light Unit

CN3 LED Power Source (**BHSR-02VS-1**) or equivalent

Mating Connector: (**SBHT-002T-P0.5**) or equivalent

| Terminal no. | Symbol | Function |
|---|---|---|
| 1 | $V_L$ | LED power supply (high voltage) |
| 2 | $G_L$ | LED power supply (low voltage) |

# 6.0 ELECTRICAL CHARACTERISTICS

## 6.1 TFT LCD Module

| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Supply Voltage | Vcc | 3.0 | 3.3 | 3.6 | V | Note (2), Note (3) |
| | $V_{GH}$ | 16.55 | 17 | 17.45 | V | Note (2), Note (3) |
| | $V_{GL}$ | -7.35 | -7 | -6.65 | V | Note (2), Note (3) |
| | $AV_{DD}$ | 9.22 | 9.48 | 9.75 | V | Note (2), Note (3) |
| VCOM | $V_{COMin}$ | - | 3.19 | - | V | |
| Input signal voltage | $V_{iH}$ | 0.7 Vcc | - | Vcc | V | Note (1) |
| | $V_{iL}$ | 0 | - | 0.3 Vcc | V | |
| Current of power supply | $I_{CC}$ | - | 8.3 | - | mA | Vcc = 3.3V (Black) |
| | $I_{ADD}$ | - | 70 | - | mA | $AV_{DD}$= 9.5 V (Black) |
| | $I_{GH}$ | - | 0.3 | - | mA | $V_{GH}$= 17 V |
| | $I_{GL}$ | - | 0.6 | - | mA | $V_{GL}$= -7 V |
| Input level of V1~V5 | Vx | AVDD/2 | - | AVDD-0.1 | V | |
| Input level of V6~V10 | Vx | 0.1 | - | AVDD/2 | V | |

Note (1): HSYNC, VSYNC, DE, Digital Data

Note (2): Be sure to apply the power voltage as the power sequence spec.

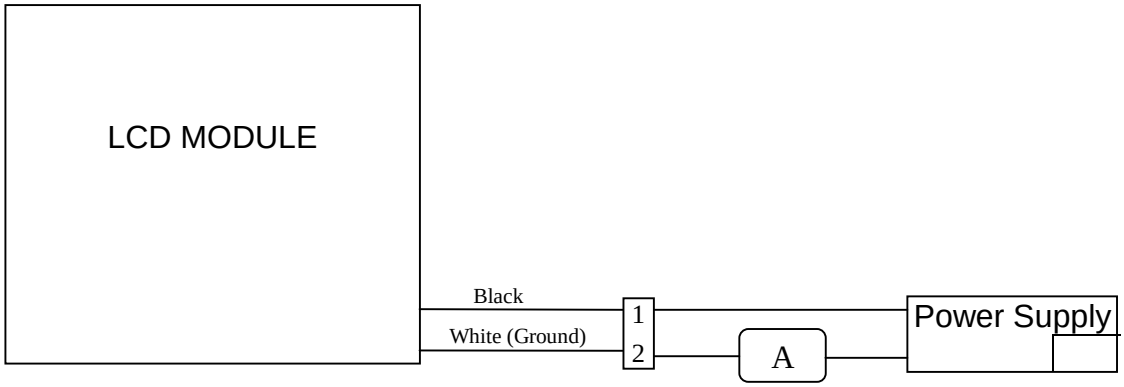
Note (3): DGND=AGND=0V

## 6.2 Back-Light Unit

The back-light system is an edge-lighting type with 33 LED.

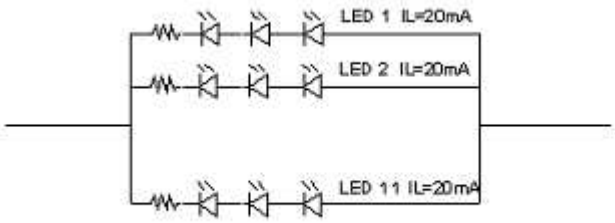
The characteristics of the LED are shown in the following tables.

| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| LED current | $I_L$ | — | 220 | — | mA | (2) |
| LED voltage | $V_L$ | — | 10.5 | — | V | |
| Operating LED life time | Hr | 20000 | — | — | Hour | (1)(2) |



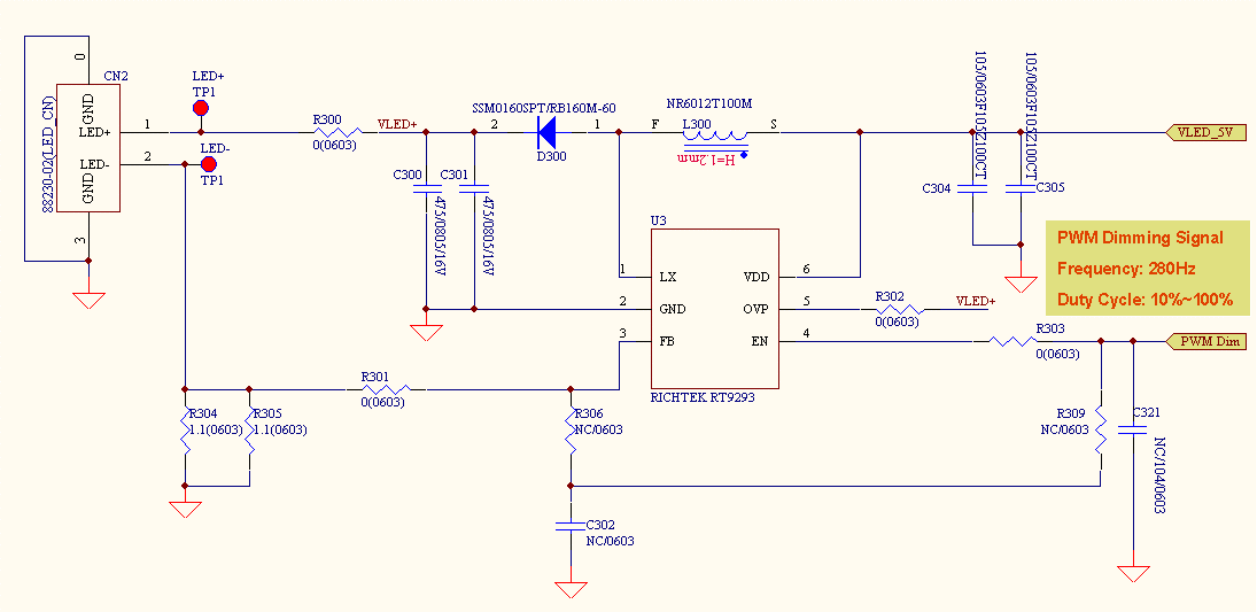

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=220mA. The LED lifetime could be decreased if operating IL is larger than 220mA. The constant current driving method is suggested.




**LED Light Bar Circuit**

Note (3) Suggested Schematic of LED Back-Light Driver




**Suggested Schematic of LED Back-Light Driver**

## 6.3 AC Characteristics

### Source Driver Timing

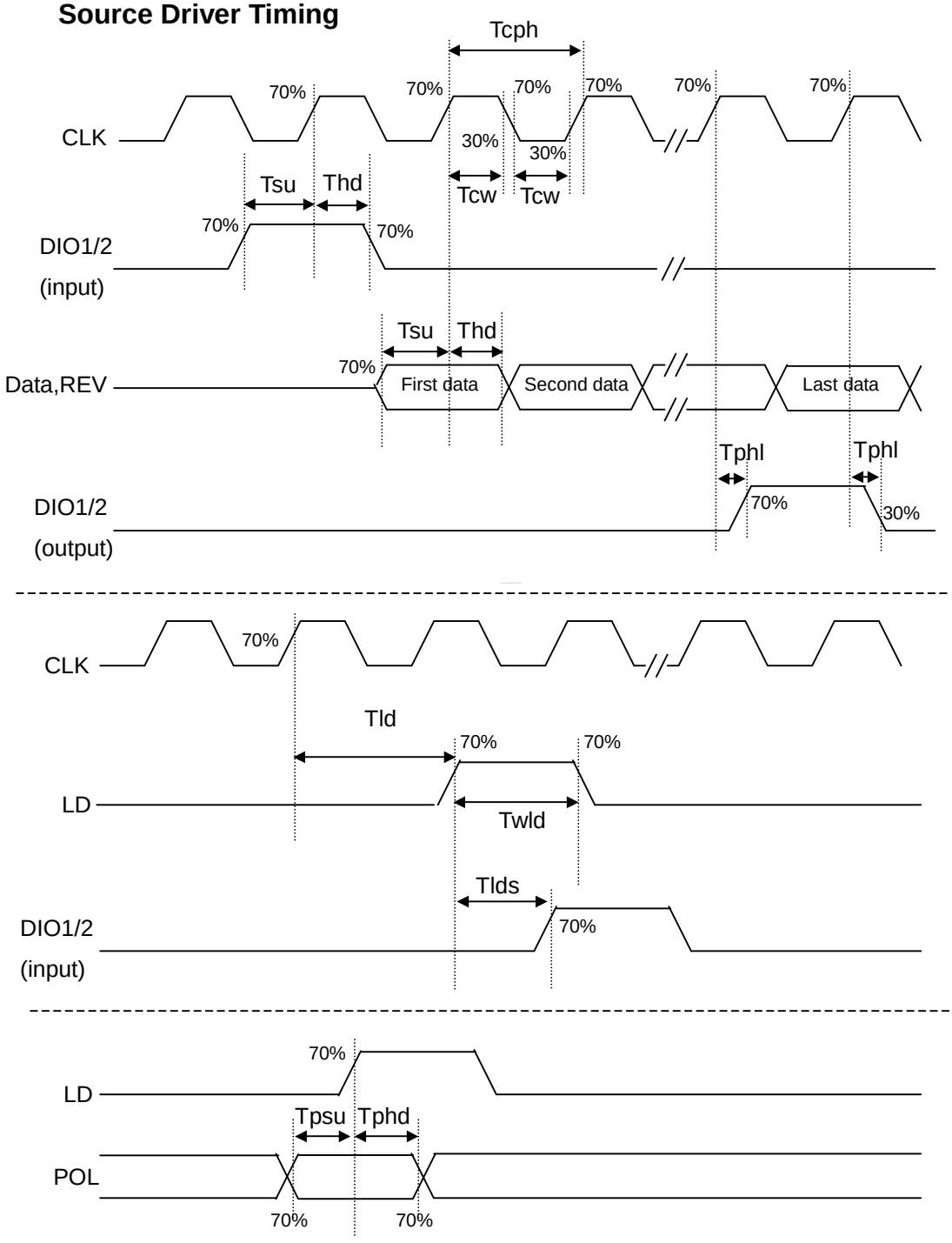
| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| CLK frequency | Fclk | - | 56 | 60 | MHz | - |
| CLK pulse width | Tcw | 6 | - | - | ns | - |
| Data set-up time | Tsu | 4 | - | - | ns | - |
| Data hold time | Thd | 2 | - | - | ns | - |
| Propagation delay of DIO2/1 | Tphl | 6 | 10 | 15 | ns | CL=25pF ( Output ) |
| Time that the last data to LD | Tld | 1 | - | - | Tcph | - |
| Pulse width of LD | Twld | 2 | - | - | Tcph | - |
| Time that LD to DIO1/2 | Tlds | 5 | - | - | Tcph | - |
| POL set-up time | Tpsu | 6 | - | - | ns | POL to LD |
| POL hold time | Tphd | 6 | | | ns | POL to LD |

### Gate Driver Timing

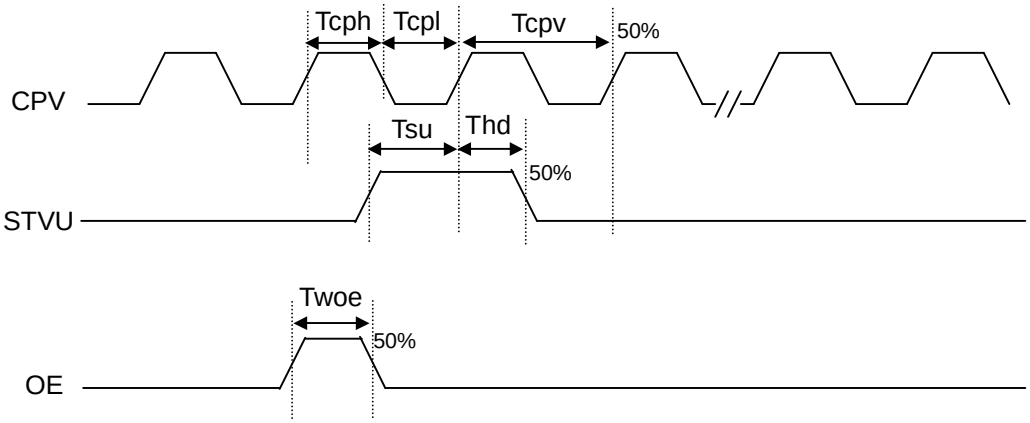
| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| CPV period | Tcpv | 5 | - | - | us | - |
| CPV pulse width | Tcpvh, Tcpvl | 2.5 | - | - | us | 50% duty cycle |
| OE pulse width | Twoe | 1 | - | - | us | - |
| Data setup time | Tsu | 200 | - | - | ns | - |
| Data hold time | Thd | 300 | - | - | ns | - |

## 6.4 Timing Diagram of Interface Signal

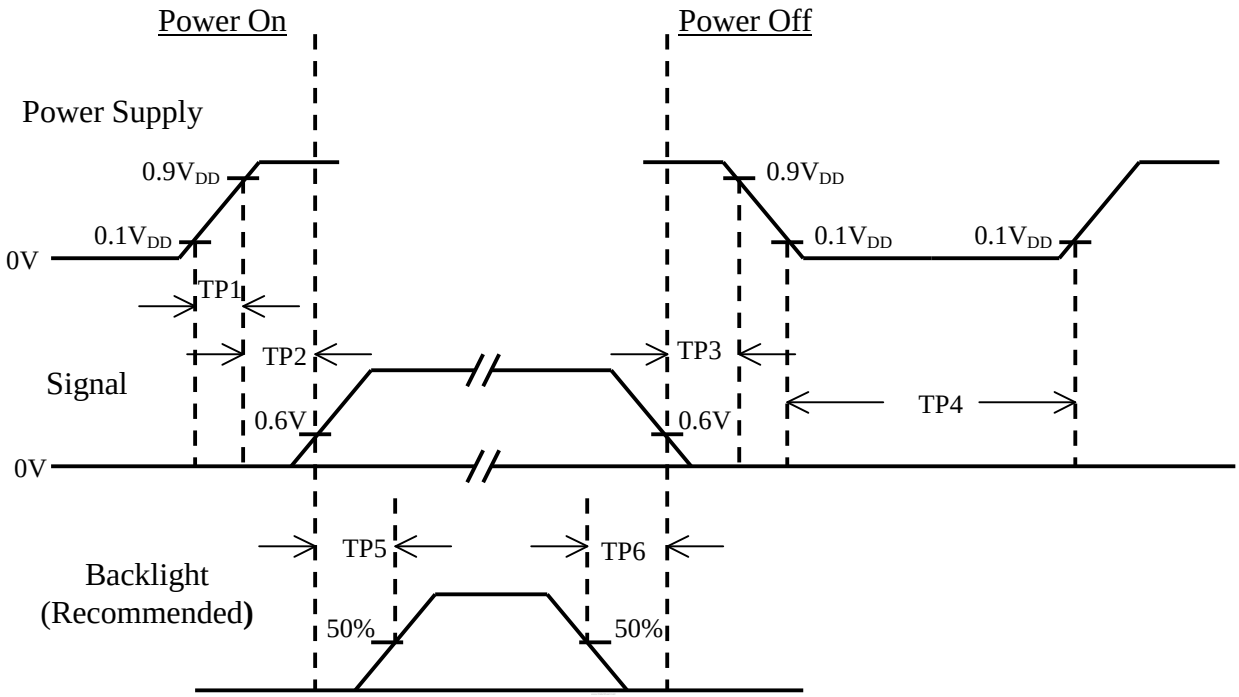
### Source Driver Timing



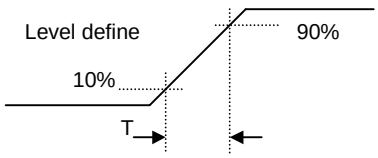
## Gate Driver Timing



### 6.5 Power On / Off Sequence




| Item | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| TP1 | 0.5 | -- | 10 | msec | |
| TP2 | 0 | -- | 50 | msec | |
| TP3 | 0 | -- | 50 | msec | |
| TP4 | 500 | -- | -- | msec | |
| TP5 | 200 | -- | -- | msec | |
| TP6 | 200 | -- | -- | msec | |

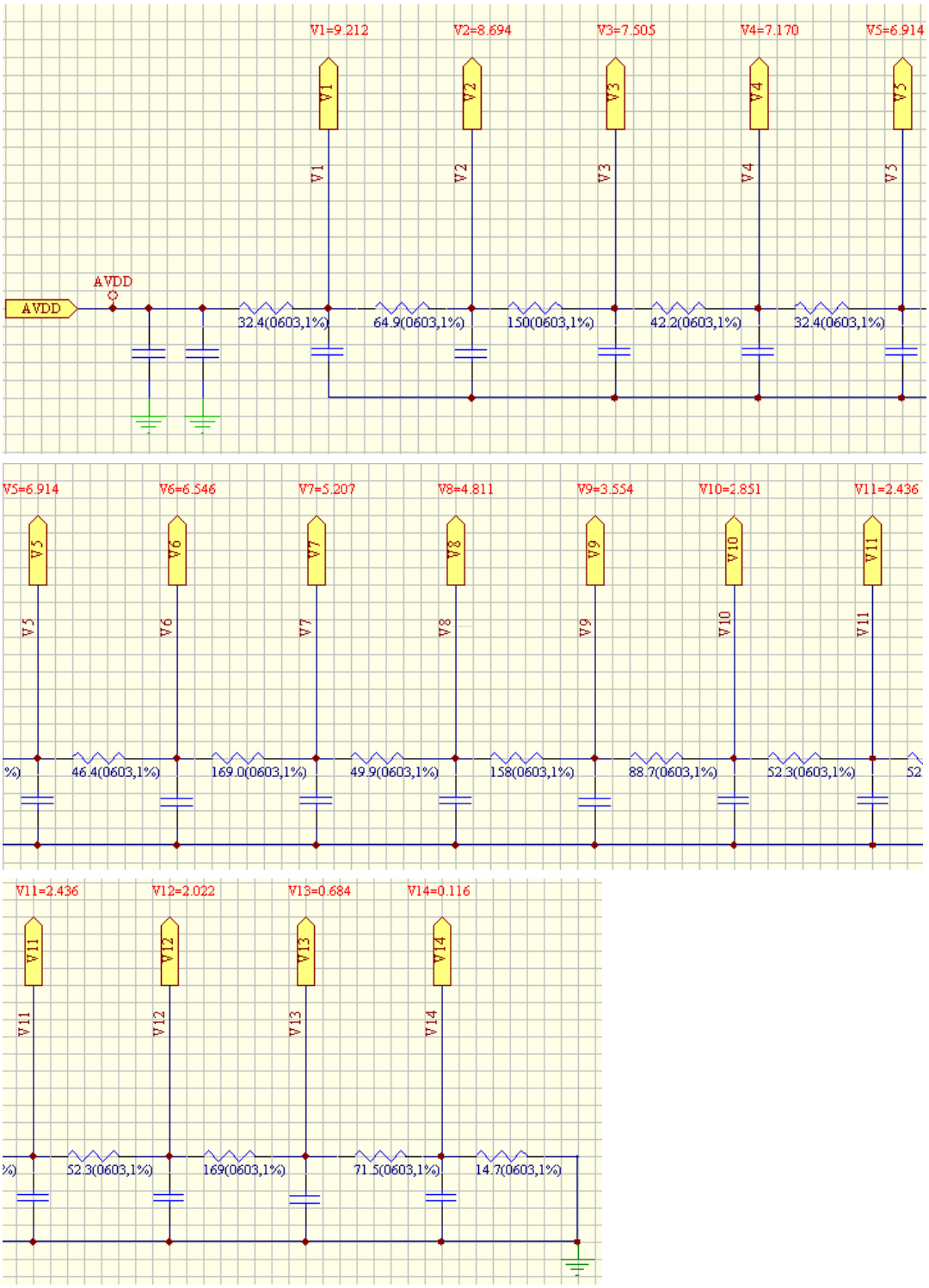



Power On Sequence: VCC-> AVDD -> VGL -> VGH -> Data -> B/L

Power Off Sequence: B/L-> Data -> VGH -> VGL -> AVDD -> VCC

Notes: Data include R0~R7, G0~G7, B0~B7, HSD, VSD, DCLK, SHLR, UPDN, DE MODE, RSTB, STBYB, SHLR, UPDN, DITH

## 6.6 Gamma circuit




*Suggested Gamma Circuit(AVDD=9.5V).

## 7.0 Reliability test items

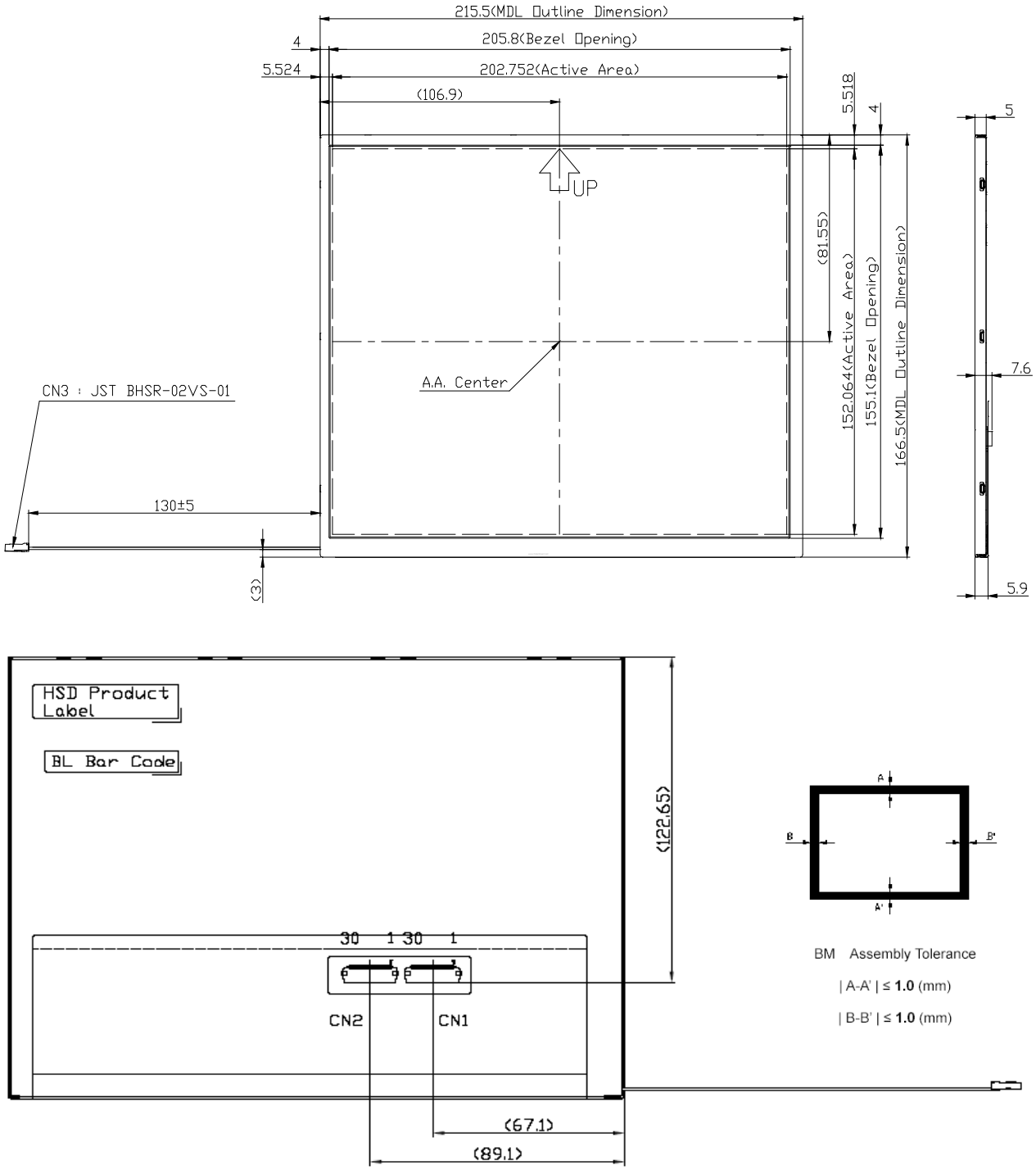
| No. | Item | Conditions | Remark |
|---|---|---|---|
| 1 | High Temperature Storage | Ta=+80°C, 240hrs | |
| 2 | Low Temperature Storage | Ta=-30°C, 240hrs | |
| 3 | High Temperature Operation | Ta=+70°C, 240hrs | |
| 4 | Low Temperature Operation | Ta=-20°C, 240hrs | |
| 5 | High Temperature and High Humidity (operation) | Ta=+60°C, 90%RH, 240hrs | |
| 6 | Thermal Cycling Test (non operation) | -30°C(30min) → +80°C(30min), 200cycles | |
| 7 | Electrostatic Discharge | ±200V,200pF(0Ω) 1 time/each terminal | |
| 8 | Vibration | 1.Random:<br>1.04Grms, 5~500Hz, X/Y/Z,<br>30min/each direction<br>2. Sine:<br>Freq. Range: 8~33.3Hz<br>Stoke: 1.3mm<br>Sweep: 2.9G, 33.3~400Hz<br>X/Z: 2hr, Y: 4hr, cyc: 15min | |
| 9 | Shock | 100G, 6ms, ±X, ±Y, ±Z<br>3 time for each direction | JIS C7021, A-10<br>(Condition A) |
| 10 | Vibration (with carton) | Random: 0.015G^2/Hz, 5~200Hz<br>-6dB/Octave, 200~400Hz<br>XYZ each direction: 2hr | |
| 11 | Drop (with carton) | Height: 60cm<br>1 corner, 3 edges, 6 surfaces | JIS Z0202 |

Note: There is no display function NG issue occurred, all the cosmetic specification is judged before the reliability stress.

# 8.0 OUTLINE DIMENSION

## 8.1 Outline Dimension

**Unit : mm**




**Note : General Tolerance : +/- 0.3mm**

# 9.0 LOT MARK

## 9.1 Lot Mark

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Code 1,2,3,4,5,6: HannStar internal flow control code.
Code 7: production location.
Code 8: production year.
Code 9: production month.
Code 10,11,12,13,14,15: serial number.

Note (1) Production Year: Code 8 is defined by the last number of the year, for example

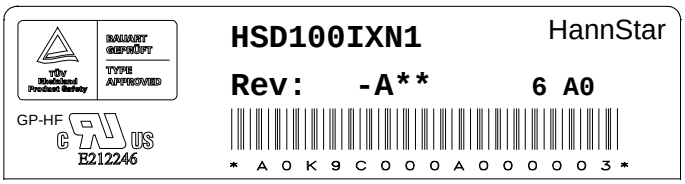
| Year | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 |
|---|---|---|---|---|---|---|---|---|---|---|
| Mark | 6 | 7 | 8 | 9 | 0 | 1 | 2 | 3 | 4 | 5 |

Note (2) Production Month

| Month | Jan. | Feb. | Mar. | Apr. | May. | Jun. | Jul. | Aug. | Sep. | Oct | Nov. | Dec. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mark | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C |

## 9.2 Detail of Lot Mark

(1) Below label is attached on the backside of the LCD module. See Section 8.0: Outline Dimension.
(2) The detail of Lot Mark is attached as below.
(3) This is subject to change without prior notice.

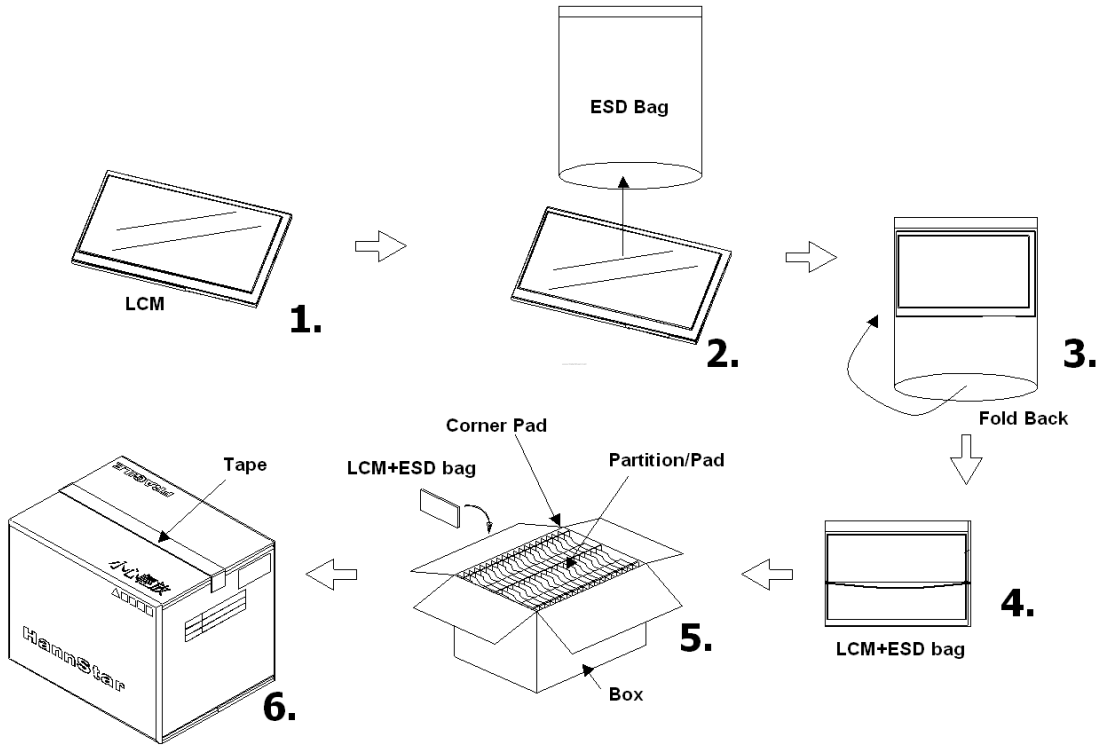


## 10.0 PACKAGE SPECIFICATION

### 10.1 Packing form

| LCM Model | LCM Qty. in the box | Inner Box Size (mm) | Notice |
|---|---|---|---|
| HSD100IXN1-A | 60 pcs/box | Ref.538 x 302 x 417$^{H}$ | |

### 10.2 Packing assembly drawings




| | Material | Notice |
|---|---|---|
| Box | Corrugated Paper Board | (AB Flute) |
| Partition/Pad | Corrugated Paper Board | (B Flute) |
| Corner Pad | Corrugated Paper Board | (AB Flute) |
| ESD bag | PE | |

# 11.0 GENERAL PRECAUTION

## 11.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

## 11.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

## 11.3 Breakage of LCD Panel

11.3.1. If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

11.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

11.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

11.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

## 11.4 Electric Shock

11.4.1. Disconnect power supply before handling LCD module.

11.4.2. Do not pull or fold the LED cable.

11.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

## 11.5 Absolute Maximum Ratings and Power Protection Circuit

11.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

11.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

11.5.3. It's recommended to employ protection circuit for power supply.

## 11.6 Operation

11.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

11.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

11.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

11.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

11.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

### 11.7 Mechanism

Please mount LCD module by using mounting holes arranged in four corners tightly.

### 11.8 Static Electricity

11.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

11.8.2 Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

### 11.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

### 11.10 Disposal

When disposing LCD module, obey the local environmental regulations.

**HSD100IXN1-A10**

**3.1 Optical specification**

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Contrast | | CR | Θ=0 Normal viewing angle | 480 | 600 | — | | (1)(2) |
| Response time | Rising | $T_R$ | | — | 2.4 | 4.8 | msec | (1)(3) |
| | Falling | $T_F$ | | — | 5.6 | 11.2 | | |
| White luminance (Center) | | $Y_L$ | | 200 | 250 | — | $cd/m^2$ | (1)(4) ($I_L$=120mA) |
| Color gamut | | S | | — | 60 | — | % | |
| Color chromaticity (CIE1931) | White | $W_x$ | | 0.280 | 0.310 | 0.340 | | (1)(4) |
| | | $W_y$ | | 0.300 | 0.330 | 0.360 | | |
| | Red | Rx | | 0.579 | 0.609 | 0.639 | | |
| | | Ry | | 0.326 | 0.356 | 0.386 | | |
| | Green | Gx | | 0.289 | 0.319 | 0.349 | | |
| | | Gy | | 0.557 | 0.587 | 0.617 | | |
| | Blue | Bx | | 0.124 | 0.154 | 0.184 | | |
| | | By | | 0.056 | 0.086 | 0.116 | | |
| Viewing angle | Hor. | $\Theta_L$ | CR>10 | 65 | 75 | — | | |
| | | $\Theta_R$ | | 65 | 75 | — | | |
| | Ver. | $\Theta_U$ | | 50 | 60 | — | | |
| | | $\Theta_D$ | | 60 | 70 | — | | |
| Brightness uniformity | | $B_{UNI}$ | Θ=0 | 70 | — | — | % | (5) |
| Optima View Direction | | 6 O’ clock | | | | | | (6) |

### 5.3 TFT LCD Module：

**CN** (Input signal): 60pin, 0.5mm pitch, 106C60-102000-G2-R (Starconn or equivalent)

| Pin No. | Signal | Description |
|---|---|---|
| 1 | POL | Polarity Setting |
| 2 | STVD | Vertical Line start pulse I/O signal |
| 3 | OE123R | Vertical Line output Enable signal |
| 4 | G-CLKR | Vertical Line Clock |
| 5 | STVU | Vertical Line start pulse I/O signal |
| 6 | GND | Digital Power Ground |
| 7 | EDGSEL | Define clock edge select input, default EDGSEL=L.<br>EDGSEL=L Latch data by rising edge of clock<br>EDGSEL=H Latch data by rising and falling edges of clock |
| 8 | VCC | Digital Voltage Input |
| 9 | V9 | Gamma Voltage Input |
| 10 | VGL | Gate OFF Voltage |
| 11 | V2 | Gamma Voltage Input |
| 12 | VGH | Gate ON Voltage |
| 13 | V6 | Gamma Voltage Input |
| 14 | UDC | Shift up/down control signal<br>UDC = "H", up shift:<br>STVD (Input) →G1 ~ G600→STVU (Output)<br>UDC= "L", down shift:<br>STVU (Input) →G600~G1→STVD (Output) |
| 15 | VCOM | Common Voltage |
| 16 | AGND | Analog Power Ground |
| 17 | AVDD | Analog Voltage Input |
| 18 | V14 | Gamma Voltage Input |
| 19 | V11 | Gamma Voltage Input |
| 20 | V8 | Gamma Voltage Input |
| 21 | V5 | Gamma Voltage Input |
| 22 | V3 | Gamma Voltage Input |
| 23 | GND | Digital Power Ground |
| 24 | R5 | Red Data Bus Input (MSB) |
| 25 | R4 | Red Data Bus Input |
| 26 | R3 | Red Data Bus Input |
| 27 | R2 | Red Data Bus Input |
| 28 | R1 | Red Data Bus Input |
| 29 | R0 | Red Data Bus Input (LSB) |
| 30 | GND | Digital Power Ground |

| Pin No. | Signal | Description |
|---|---|---|
| 31 | GND | Digital Power Ground |
| 32 | G5 | Green Data Bus Input (MSB) |
| 33 | G4 | Green Data Bus Input |
| 34 | G3 | Green Data Bus Input |
| 35 | G2 | Green Data Bus Input |
| 36 | G1 | Green Data Bus Input |
| 37 | G0 | Green Data Bus Input (LSB) |
| 38 | DIO2_COF3 | Horizontal Line start pulse I/O signal (STHR) |
| 39 | REV | Data Invert signal |
| 40 | GND | Digital Power Ground |
| 41 | CLK | Pixel clock |
| 42 | VCC | Digital Voltage Input |
| 43 | DIO1_COF1 | Horizontal Line start pulse I/O signal (STHL) |
| 44 | LD | Polarity latch and re-flash new data to output |
| 45 | B5 | Blue Data Bus Input (MSB) |
| 46 | B4 | Blue Data Bus Input |
| 47 | B3 | Blue Data Bus Input |
| 48 | B2 | Blue Data Bus Input |
| 49 | B1 | Blue Data Bus Input |
| 50 | B0 | Blue Data Bus Input (LSB) |
| 51 | LRC | Select left or right shift, normally pulled high.<br>SHL="1": DIO1→ OUT1,2,3→OUT4,5,6→<br>OUT1198,1199,1200 = DIO2<br>SHL="0": DIO1= OUT1,2,3 ← OUT4,5,6←<br>OUT1198,1199,1200←DIO2 |
| 52 | V1 | Gamma Voltage Input |
| 53 | V4 | Gamma Voltage Input |
| 54 | V7 | Gamma Voltage Input |
| 55 | V10 | Gamma Voltage Input |
| 56 | V12 | Gamma Voltage Input |
| 57 | V13 | Gamma Voltage Input |
| 58 | AVDD | Analog Voltage Input |
| 59 | AGND | Analog Power Ground |
| 60 | VCOM | Common Voltage |

### 6.6 Back-Light Unit

The back-light system is an edge-lighting type with 33 LED.

The characteristics of the LED are shown in the following tables.

| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| LED current | $I_L$ | — | 220 | — | mA | (2) |
| LED voltage | $V_L$ | — | 10.5 | 11 | V | |
| Operating LED life time | Hr | 20000 | — | — | Hour | (1)(2) |

**Source Driver Timing**

| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| CLK frequency | Fclk | 48 | 56 | 60 | MHz | Frame rate at 60Hz |
| CLK pulse width | Tcw | 6 | - | - | ns | - |
| Data set-up time | Tsu | 4 | - | - | ns | - |
| Data hold time | Thd | 2 | - | - | ns | - |
| Propagation delay of DIO2/1 | Tphl | 6 | 10 | 15 | ns | CL=25pF ( Output ) |
| Time that the last data to LD | Tld | 1 | - | - | Tcph | - |
| Pulse width of LD | Twld | 2 | - | - | Tcph | - |
| Time that LD to DIO1/2 | Tlds | 5 | - | - | Tcph | - |
| POL set-up time | Tpsu | 6 | - | - | ns | POL to LD |
| POL hold time | Tphd | 6 | | | ns | POL to LD |

**Gate Driver Timing**

| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| CPV period | Tcpv | 5 | - | - | us | - |
| CPV pulse width | Tcpvh, Tcpvl | 2.5 | - | - | us | 50% duty cycle |
| OE pulse width | Twoe | 1 | - | - | us | - |
| Data setup time | Tsu | 200 | - | - | ns | - |
| Data hold time | Thd | 300 | - | - | ns | - |

## 8.1 Outline Dimension