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HannStar Product Information

**Model : HSD150SX87
- A**

- Note:
1. Please contact HannStar Display Corp. before designing your product based on this module specification.
 2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by HannStar for any intellectual property claims or other problems that may result from application based on the module described herein.



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Record of Revisions

Rev.	Updated No.	Date	Description of change
0.1	—	Mar.03,2003	Tentative specification for HSD150SX87-A was first issued.
0.2	—	Mar.18,2003	1. Modify the typical values of the viewing angle and the brightness unifomity in the page 7. 2. Increase the in-rush current condition in the page 16. 3. Modify the AC timing specification in the page 19. 4. Increase the graphic of the initial condition of the AC timing specification in the page 23.
0.3	—	Mar.22,2003	1.modify page 19. 2.Modify viewing angle in page 7. 3.Add suggest timing in page 25



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1.0 GENERAL DESCRIPTIONS

1.1 Introduction

HannStar Display model **HSD150SX87-A** is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, the voltage reference, common voltage, DC-DC converter, column, and row driver circuit. This TFT LCD has a 15-inch diagonally measured active display area with XGA resolution (768 vertical by 1024 horizontal pixel array).

1.2 Features

- 15" XGA TFT LCD panel
- 2 CCFLs Backlight system
- Supported XGA (V:768 lines, H:1024 pixels) resolution
- Supported to 75Hz refresh rate
- Without LCD Timing Controller

1.3 General information

Item	Specification	Unit
Outline dimension	321.0× 249.0× 10.5 (typ.)	Mm
Display area	304.1(H) x 228.1(V) (15.0" diagonal)	Mm
Number of Pixel	1024(H) x 768(V)	Pixels
Pixel pitch	0.297(H) x 0.297(V)	Mm
Pixel arrangement	RGB Vertical stripe	
Display color	6-bits driver	
Display mode	Normally white	
Surface treatment	Antiglare, Hard-Coating(3H)	
Weight	900(typ.)	G
Back-light	2-CCFLs, Top & bottom edge side	
Input signal	Source and Gate Driver control signals	
Power consumption	12 W(typ.), with back light	W
Optimum viewing direction	6 o'clock	

1.4 Applications

- Desktop monitors
- Display terminals for AV applications
- Monitors for industrial applications

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1.5 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal(H)	--	321.0	--	mm
	Vertical(V)	--	249.0	--	mm
	Depth(D)	--	10.5	--	mm
Weight (without inverter)		--	900	--	g

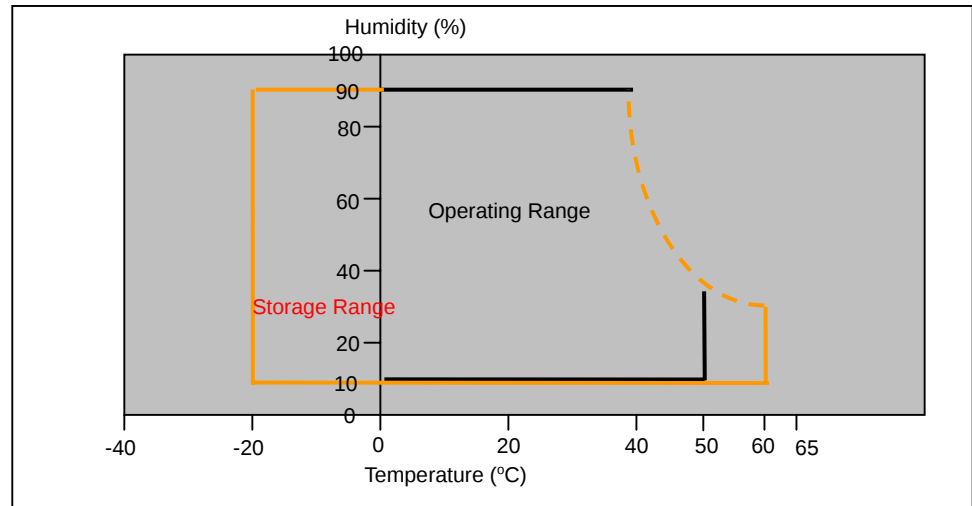
2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Absolute Rating of Environment

Item	Symbol	Min.	Max.	Unit	Note
Storage temperature	T _{STG}	-20	60	°C	
Operating temperature	T _{OPR}	0	50	°C	
Vibration(non-operating)	V _{NOP}	--	1.5	G	(1)
Shock(non-operating)	S _{NOP}	--	70	G	(2)
Storage humidity	H _{STG}	10	90	%RH	(3)
Operating humidity	H _{OP}	10	80	%RH	(3)
Low pressure(operating)	P _{LOP}	697	--	HPa	(4)
Low pressure(non-operating)	P _{LNOP}	116	--	HPa	(5)

- Note
- (1) **5-500-5Hz** sine wave, X,Y,Z each directions, 30 min/cycle.
 - (2) 11ms, ±X, ±Y, ±Z direction, one time each. For this shock test, it is necessary to fill the silicon rubber between the shock jig as buffer.
 - (3) Max wet bulb temp. =39°C
 - (4) **2 hrs.** (10000 feet)
 - (5) **24hrs.** (50000 feet)

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2.2 Electrical Absolute Rating:

2.2.1 TFT LCD Module:

Item	Symbol	Condition	Value		Unit
			min.	max.	
Input Power Voltage	V_{DD}	Normal	+3.0	+3.8	V(DC)
Logic Signal input voltage	V_{SIG}	Normal	-0.3	$V_{DD} + 0.3$	V

2.2.2 Back Light Unit:

Item	Symbol	Min.	Max.	Unit	Note
Lamp voltage	V_L	0	2000	V(rms)	(1)
Lamp current	I_L	-	9.0	mA	(1)
Lamp frequency	f_L	0	100	KHz	(1)

Note: (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

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3.0 OPTICAL CHARACTERISTICS

3.1 Measuring Condition

- Measuring surrounding : dark room
- Lamp current I_{BL} : $(8.0) \pm 0.1 \text{mA}$, lamp freq. $F_L = 55 \text{ KHz}$
- $V_{DD1} = 3.3\text{V}$, $f_v = 60\text{Hz}$, $f_{DCLK} = 32.5\text{MHz}$
- Surrounding temperature : $25 \pm 2^\circ\text{C}$
- 30min. Warm-up time.

3.2 Measuring Equipment

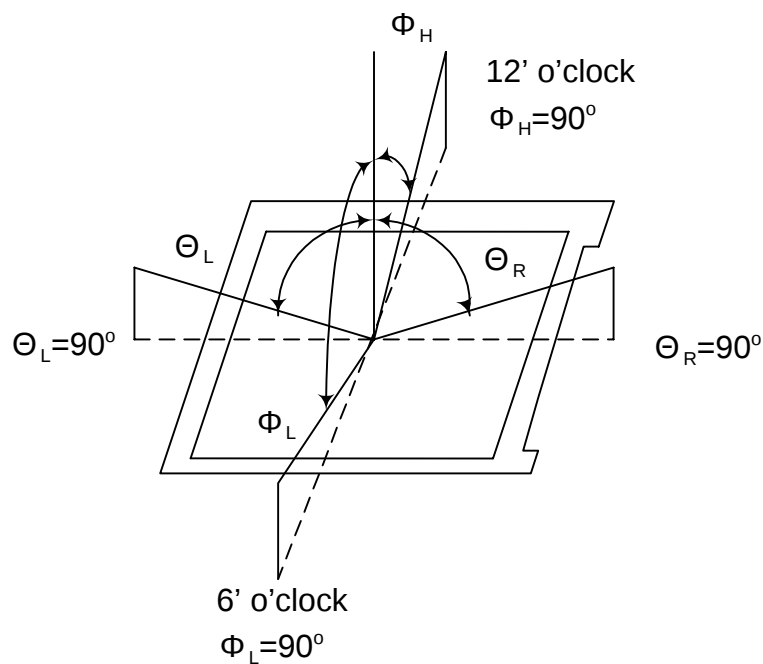
- LCD-7000 of Otsuka Electric Corp., which utilized MCPD-7000 for Chromaticity and BM-5A for other optical characteristics.
- Measuring spot size : 10~12mm

3.3 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast		CR	Θ=0° ϕ=0° Normal viewing angle	300	450	--		(1)(2)
Response time	Rising	TR +TF		--	16	--	msec	(1)(3)
	Falling							
White luminance (center of screen)		Y _L		200	250		cd/m ²	(1)
Color chromaticity (CIE1931)	Red	R _x		0.604	0.634	0.664		(1)(4)
		R _y		0.309	0.339	0.369		
	Green	G _x		0.255	0.285	0.315		
		G _y		0.557	0.587	0.617		
	Blue	B _x		0.114	0.144	0.174		
		B _y		0.045	0.075	0.105		
	White	W _x	0.28	0.31	0.34			
		W _y	0.3	0.33	0.36			
Viewing angle	Hor.	Θ _L	CR>10	--	65	--		
		Θ _R		--	65	--		
	Ver.	Θ _H		--	45	--		
		Θ _L		--	55	--		
	Hor.	Θ _L	CR>5	--	75	--		
		Θ _R		--	75	--		
	Ver.	Θ _H		--	50	--		
		Θ _L		--	65	--		
Brightness uniformity		B _{UNI}	Θ=0° ϕ=0°	75	--	--	%	(5)

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Note (1) Definition of Viewing Angle:

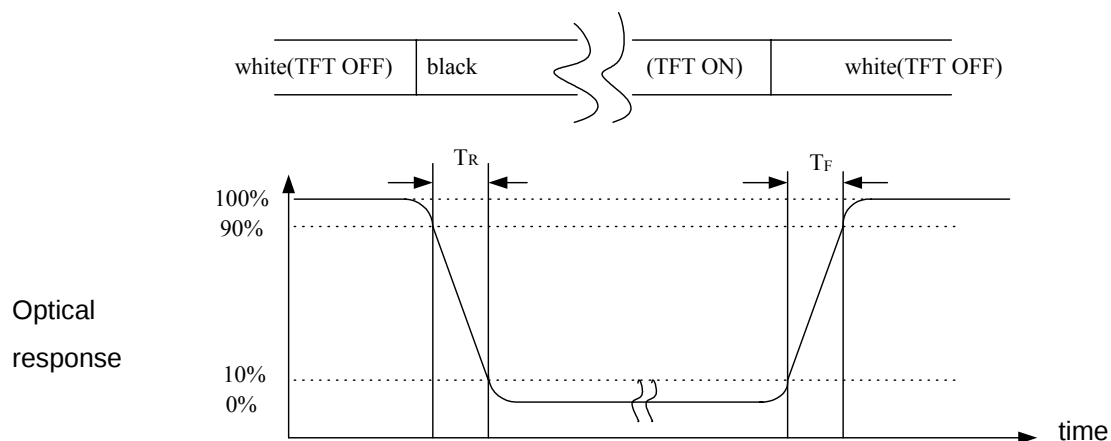


Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

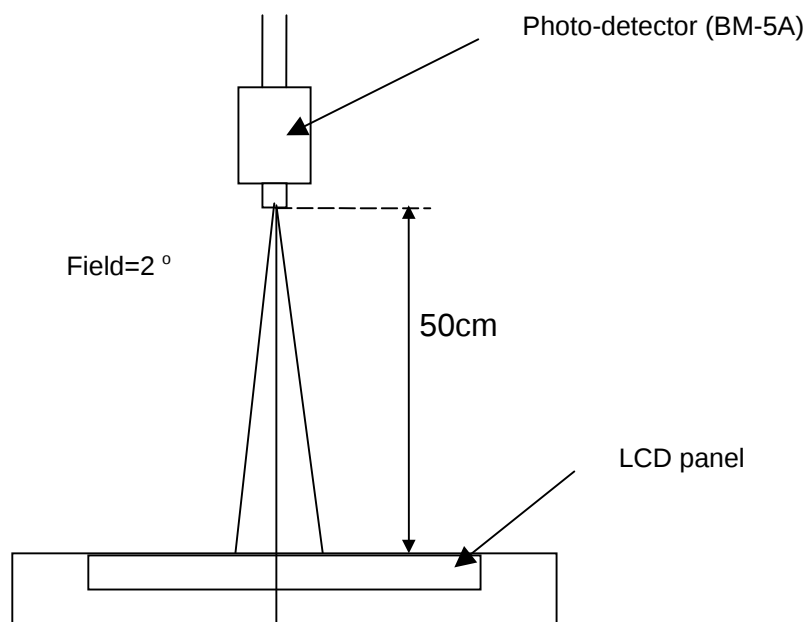
$$CR = \frac{\text{Luminance with all pixels white (L63)}}{\text{Luminance with all pixels black (L0)}}$$

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Note (3) Definition of Response Time: Sum of T_R and T_F



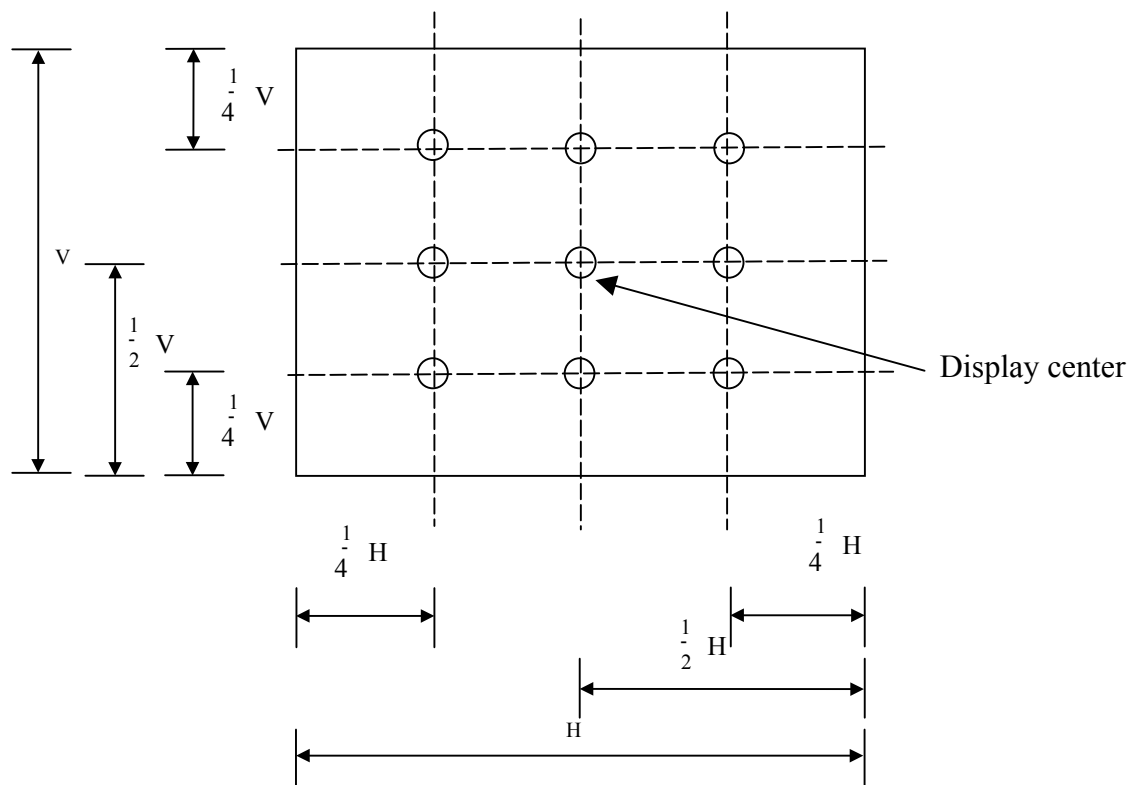
Note (4) Optical characteristic measurement setup



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Note (5) Definition of brightness uniformity

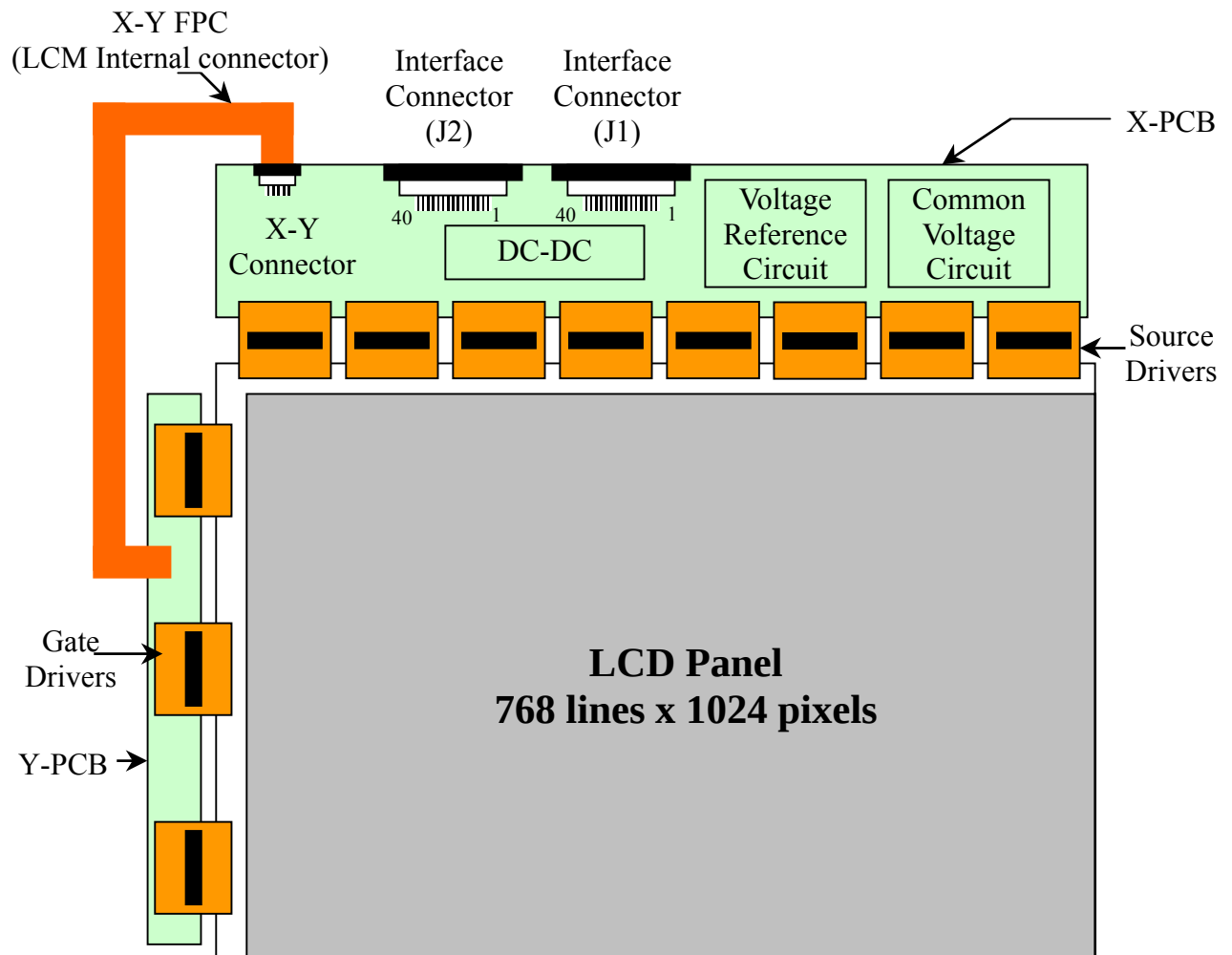
Luminance uniformity $= (\text{Min Luminance}) / (\text{Max Luminance}) \times 100\%$



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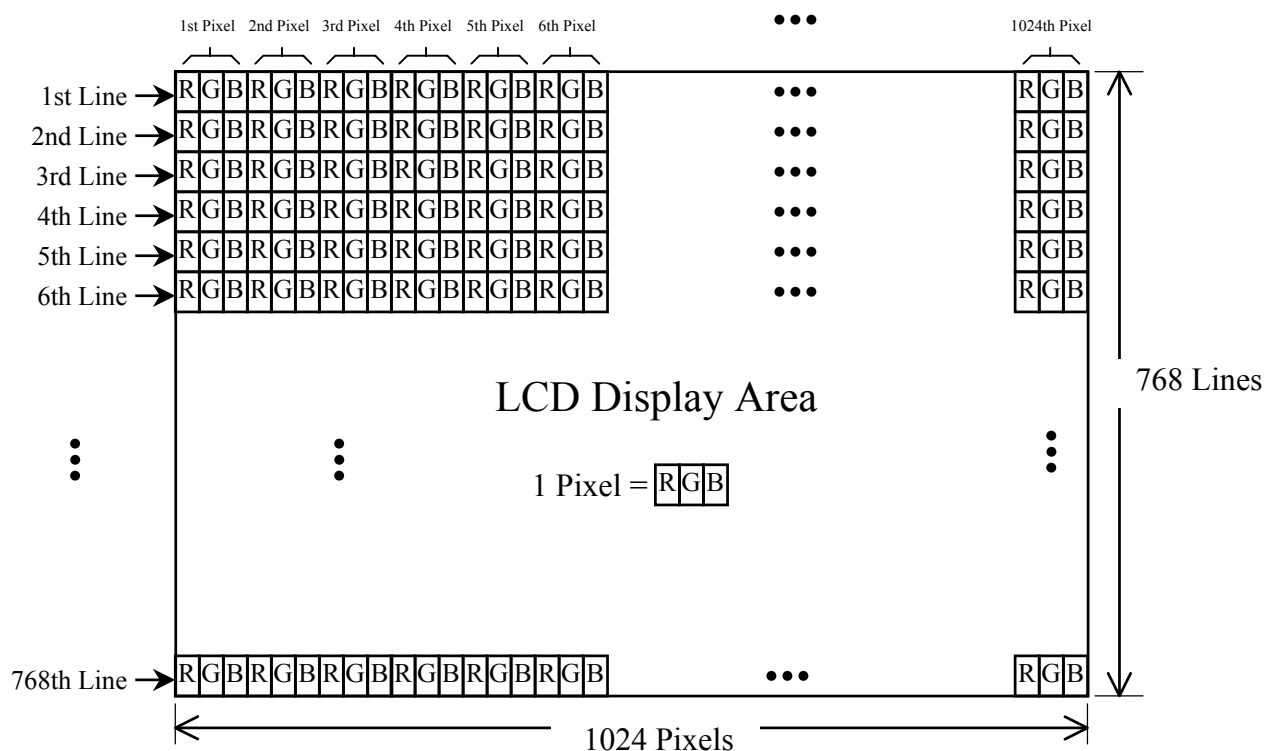
4.0 BLOCK DIAGRAM

4.1 LCD Module Block Diagram:



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4.2 Pixel Format



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4.3 Relationship between Displayed Color and Input Data

	Display	MSB R5 R4 R3 R2 R1 R0	LSB G5 G4 G3 G2 G1 G0	MSB B5 B4 B3 B2 B1 B0	LSB	Gray scale level
Basic color	Black	L L L L L L	L L L L L L	L L L L L L	L L L L L L	-
	Blue	L L L L L L	L L L L L L	H H H H H H	H H H H H H	-
	Green	L L L L L L	H H H H H H	L L L L L L	L L L L L L	-
	Light Blue	L L L L L L	H H H H H H	H H H H H H	H H H H H H	-
	Red	H H H H H H	L L L L L L	L L L L L L	L L L L L L	-
	Purple	H H H H H H	L L L L L L	H H H H H H	H H H H H H	-
	Yellow	H H H H H H	H H H H H H	L L L L L L	L L L L L L	-
Gray scale of Red	White	H H H H H H	H H H H H H	H H H H H H	H H H H H H	-
	Black	L L L L L L	L L L L L L	L L L L L L	L L L L L L	L0
	Dark ↑ ↓ Light	L L L L L L	L L L L L L	L L L L L L	L L L L L L	L1
		L L L L L L	L L L L L L	L L L L L L	L L L L L L	L2
		:	:	:	:	L3...L60
		:	:	:	:	
		H H H H L L	L L L L L L	L L L L L L	L L L L L L	L61
		H H H H H L	L L L L L L	L L L L L L	L L L L L L	L62
Gray scale of Green	Red	H H H H H H	L L L L L L	L L L L L L	L L L L L L	Red L63
	Black	L L L L L L	L L L L L L	L L L L L L	L L L L L L	L0
	Dark ↑ ↓ Light	L L L L L L	L L L L L L	L L L L L L	L L L L L L	L1
		L L L L L L	L L L L L L	L L L L L L	L L L L L L	L2
		:	:	:	:	L3...L60
		:	:	:	:	
		L L L L L L	H H H H L L	L L L L L L	L L L L L L	L61
		L L L L L L	H H H H H L	L L L L L L	L L L L L L	L62
Gray scale of Blue	Green	L L L L L L	H H H H H H	L L L L L L	L L L L L L	Green L63
	Black	L L L L L L	L L L L L L	L L L L L L	L L L L L L	L0
	Dark ↑ ↓ Light	L L L L L L	L L L L L L	L L L L L L	L L L L L L	L1
		L L L L L L	L L L L L L	L L L L L L	L L L L L L	L2
		:	:	:	:	L3...L60
		:	:	:	:	
		L L L L L L	H H H H L L	L L L L L L	L L L L L L	L61
		L L L L L L	H H H H H L	L L L L L L	L L L L L L	L62
Gray scale of White and Black	Blue	L L L L L L	L L L L L L	H H H H H H	H H H H H H	Blue L63
	Black	L L L L L L	L L L L L L	L L L L L L	L L L L L L	L0
	Dark ↑ ↓ Light	L L L L L L	L L L L L L	L L L L L L	L L L L L L	L1
		L L L L L L	L L L L L L	L L L L L L	L L L L L L	L2
		:	:	:	:	L3...L60
		:	:	:	:	
		H H H H L L	H H H H L L	L L L L L L	L L L L L L	L61
		H H H H H L	H H H H H L	L L L L L L	L L L L L L	L62
	White	H H H H H H	H H H H H H	H H H H H H	H H H H H H	White L63

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5.0 I/O CONNECTION PIN ASSIGNMENT

5.1 Interface FPC Connector (40-pins x 2) (Hirose: FH12-40S-0.5SH)

I/F FRC Connector (J1)			I/F FRC Connector (J2)		
Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC	No Connecting	1	VDD	Digital Power Input (DC +3.3V)
2	NC	No Connecting	2	VDD	Digital Power Input (DC +3.3V)
3	GND	Ground	3	GND	Ground
4	GND	Ground	4	GND	Ground
5	EB5	Even-dot Blue Data bit 5 (MSB)	5	OB5	Odd-dot Blue Data bit 5 (MSB)
6	EB4	Even-dot Blue Data bit 4	6	OB4	Odd-dot Blue Data bit 4
7	EB3	Even-dot Blue Data bit 3	7	OB3	Odd-dot Blue Data bit 3
8	EB2	Even-dot Blue Data bit 2	8	OB2	Odd-dot Blue Data bit 2
9	EB1	Even-dot Blue Data bit 1	9	OB1	Odd-dot Blue Data bit 1
10	EB0	Even-dot Blue Data bit 0 (LSB)	10	OB0	Odd-dot Blue Data bit 0 (LSB)
11	GND	Ground	11	GND	Ground
12	EG5	Even-dot Green Data bit 5 (MSB)	12	OG5	Odd-dot Green Data bit 5 (MSB)
13	EG4	Even-dot Green Data bit 4	13	OG4	Odd-dot Green Data bit 4
14	EG3	Even-dot Green Data bit 3	14	OG3	Odd-dot Green Data bit 3
15	EG2	Even-dot Green Data bit 2	15	OG2	Odd-dot Green Data bit 2
16	EG1	Even-dot Green Data bit 1	16	OG1	Odd-dot Green Data bit 1
17	EG0	Even-dot Green Data bit 0 (LSB)	17	OG0	Odd-dot Green Data bit 0 (LSB)
18	GND	Ground	18	GND	Ground
19	ER5	Even-dot Red Data bit 5 (MSB)	19	OR5	Odd-dot Red Data bit 5 (MSB)
20	ER4	Even-dot Red Data bit 4	20	OR4	Odd-dot Red Data bit 4
21	ER3	Even-dot Red Data bit 3	21	OR3	Odd-dot Red Data bit 3
22	ER2	Even-dot Red Data bit 2	22	OR2	Odd-dot Red Data bit 2
23	ER1	Even-dot Red Data bit 1	23	OR1	Odd-dot Red Data bit 1
24	ER0	Even-dot Red Data bit 0 (LSB)	24	OR0	Odd-dot Red Data bit 0 (LSB)
25	GND	Ground	25	GND	Ground
26	CPH1	Pixel Clock Input	26	CPH2	Pixel Clock Input
27	GND	Ground	27	GND	Ground
28	GND	Ground	28	GND	Ground
29	STH	Horizontal Start Pulse	29	NC	No Connecting
30	LOAD	Source Driver Latch Pulse	30	NC	No Connecting
31	POL	Source Driver Output Polarity control	31	NC	No Connecting
32	REV	Data Reverse Control Signal	32	NC	No Connecting
33	GND	Ground	33	NC	No Connecting
34	GND	Ground	34	NC	No Connecting
35	STV	Vertical Start Pulse	35	NC	No Connecting
36	NC	No Connecting	36	NC	No Connecting
37	CPV	Vertical Clock Input	37	NC	No Connecting
38	OE	Gate Driver Output Enable Signal	38	NC	No Connecting
39	GND	Ground	39	GND	Ground
40	GND	Ground	40	GND	Ground

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5.2 Back Light Unit (CCFL) Connectors:



CN3, 4: CCFL Power Source (BHR-03VS-1/Japan Solderless Terminal MFG Co., LTD)

Mating connector: SM02 (8.0)B-BHS-1/ Japan Solderless Terminal MFG Co., LTD

Terminal No.	Symbol	Function
1	VL	CCFL power supply (high voltage)
2	NC ¹⁾	No connection
3	GL	CCFL power supply (low voltage)

Note 1) Please connects NC pin to nothing. Don't connect it to ground nor to other signal Input. (NC pin should be open.)

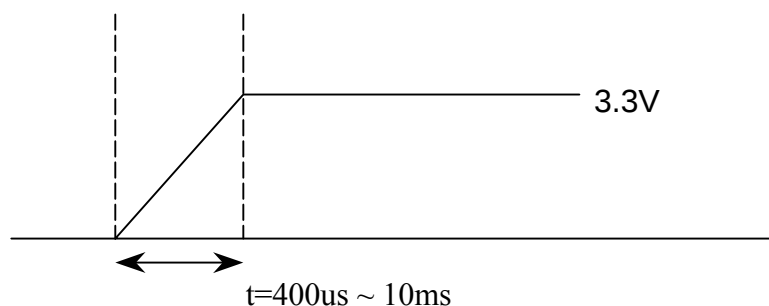
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6.0 ELECTRICAL CHARACTERISTICS

6.1 Electrical System of LCD Module:

Item	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Voltage	V_{DD}		+3.0	+3.3	+3.6	V(DC)
Input Rush Current	I_{rush}	$V_{DD} = +3.3V$ Each $I_{out} = \max.$			1.5(*)	A
Input Signal voltage	V_{IH}	High Level	2.4	3.3	$V_{DD}+0.2$	V
	V_{IL}	Low Level	0	-	0.9	V

* Inrush current conditions



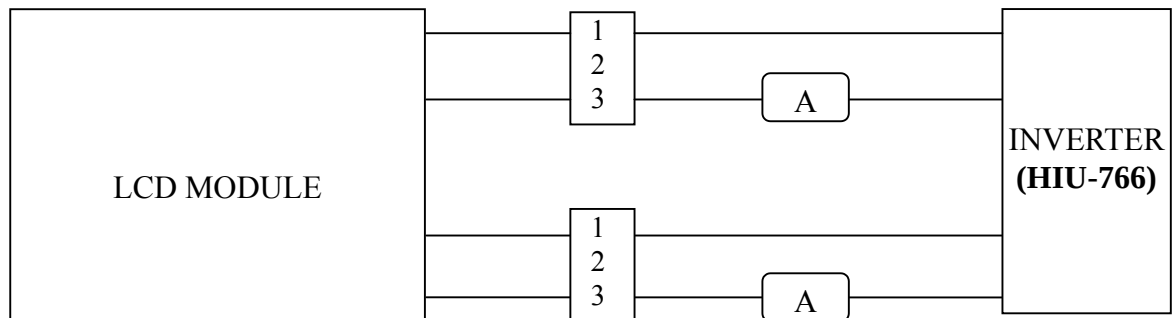
6.2 Back-Light Unit:

The backlight system is an edge-lighting type with 2-CCFL (Cold Cathode Fluorescent Lamp). The characteristics of four lamps are shown in the following tables.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Lamp current	I_L	4.0	8.0	9.0	mA(rms)	(1)
Lamp voltage	V_L	640	670	700	V(rms)	$I_L = 8.0 \text{ mA}$
Frequency	f_L	45	55	80	KHz	(2)
Lamp life time	Hr	30,000	--	-	Hour	(3)
Startup voltage	V_s	1400	-	-	V(rms)	at 25°C
		1050				at 0°C

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Note: (1) Lamp current is measured with current meter for high frequency as shown below.
Specified values are for a lamp.



- (2) Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency shall be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.
- (3) Life time (Hr) can be defined as the time in which it continues to operate under the condition:
Temp. = $25 \pm 3^\circ\text{C}$, $I_L = 8.0\text{mA(rms.)}$ and $f_L = 55\text{ KHz}$ until one of the following event occurs:
1. When the brightness becomes 50%.
 2. When the startup voltage (V_s) at 0°C becomes higher than the maximal value of V_s specified above.

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6.3 AC Electrical Characteristics:

6.3.1 AC Timing: (VDD1=3.0V~3.6V, TOPR=25 oC) 5)

Item	Symbol	Min.	Typ.	Max.	Unit	Signals	Note
Reference Signal (Pixel Clock)	F1 T1=CLK T2=T1*2	50 12.5 25	65 15.384 30.769	80 20 40	MHz n-Sec n-Sec		
Reference Signal (DENB)	Line Periodic	T3=Line	526	672	900	T2	1), 2), 4)
	Line Active	T4	512	512	512	T2	
	Line Blank	T5	14	160	388	T2	
	Frame Periodic	T6	773	806	950	Lines	
	Frame Active	T7	768	768	768	Lines	
	Frame Blank	T8	5	---	---	Lines	
Vertical Periodic	Periodic	T6	773	806	950	Lines	STV 2)
	Pulse Width	T9	1	1	---	Lines	
	Set-up Time	T13	700	800	---	n-Sec	
	Hold Time	T14	700	800	---	n-Sec	
Horizontal Periodic	Period	T15	---	1	---	Lines	OE CPV LOAD STH
	Pulse Width	T16A	1			u-Sec	
		T16B	1			u-Sec	
		T16C	2	64	100	T2	
		T16D	25	30.769	40	n-Sec	
	Rising Time	T17A		40	60		
		T17B		40	60		
		T17C	2	4		n-Sec	
		T17D	2	4			
	Falling Time	T18A		40	60		
		T18B		40	60		
		T18C	2	4		n-Sec	
		T18D	2	4			
	Set-up Time	T19A T19B	7 7	10 10	---	n-Sec	LOAD STH
	Hold Time	T20A T20B	7 7	10 10	---	n-Sec	

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Item	Symbol	Min.	Typ.	Max.	Unit	Signals	Note
6Horizontal Periodic	Period	T21	---	2	---	Lines	POL
	Pulse Width	T22	---	1	---	Lines	
	Rising Time	T23	---	---	8	n-Sec	
	Falling Time	T24	---	---	8	n-Sec	
	Set-up Time	T25	6	---	---	n-Sec	
	Hold Time	T26	2	---	---	n-Sec	
Clock	Period	T2	25.00	30.769	40	n-Sec	CPH1 CPH2
	Rising Time	T27	---	---	8	n-Sec	
	Falling Time	T28	---	---	8	n-Sec	
Image Data And Data Reverse Control Pin	Setup time	T29	6	---	---	n-Sec	ER(5:0) EG(5:0) EB(5:0) OR(5:0) OG(5:0) OB(5:0) REV
	Hold time	T30	2	---	---	n-Sec	
Relative Signals	LOAD rising- STH rising	T31	6	---	---	T2	
	CPV rising- LOAD rising	T32	3.5	3.7	4.5	u-Sec	

Frame Rate Recommend using :

V signals	F _V	---	60.00	85	Hz		6)
H signals	F _H	39.5	48.35	70	KHz		

Note 1) Refer to VESA standard.

Note 2) In case of using the long frame period, the deterioration of display quality, noise etc. may be occurred.

Note 3) Do not fix CPH1 and CPH2 to “H” or “L” level while the V_{DD} (+3.3V) is supplied. If CPH1 and CPH2 is fixed to “H” level or “L” level for certain period while the V_{DD} (+3.3V) is supplied, the panel may be damaged.

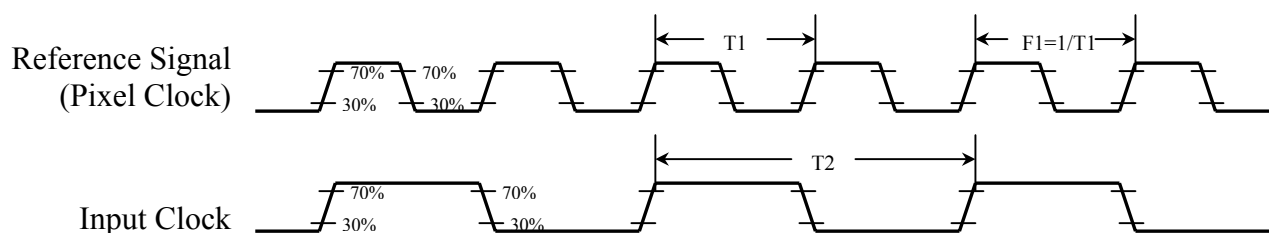
Note 4) Do not change t3 and t6 values in the operation. When t1 or t4 is changed, the panel is displayed as black.

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- Note 5) Please adjust LCD operating signal timing and FL driving frequency, to optimize the display quality. There is a possibility that flicker is observed by the interference of LCD operating signal timing and FL driving condition (especially driving frequency).
- Note 6) All of the timing have to meet “ 6.3.1 AC timing chart – Pixel frequency must less than 40MHz”, frame rate 85Hz can be acceptable.

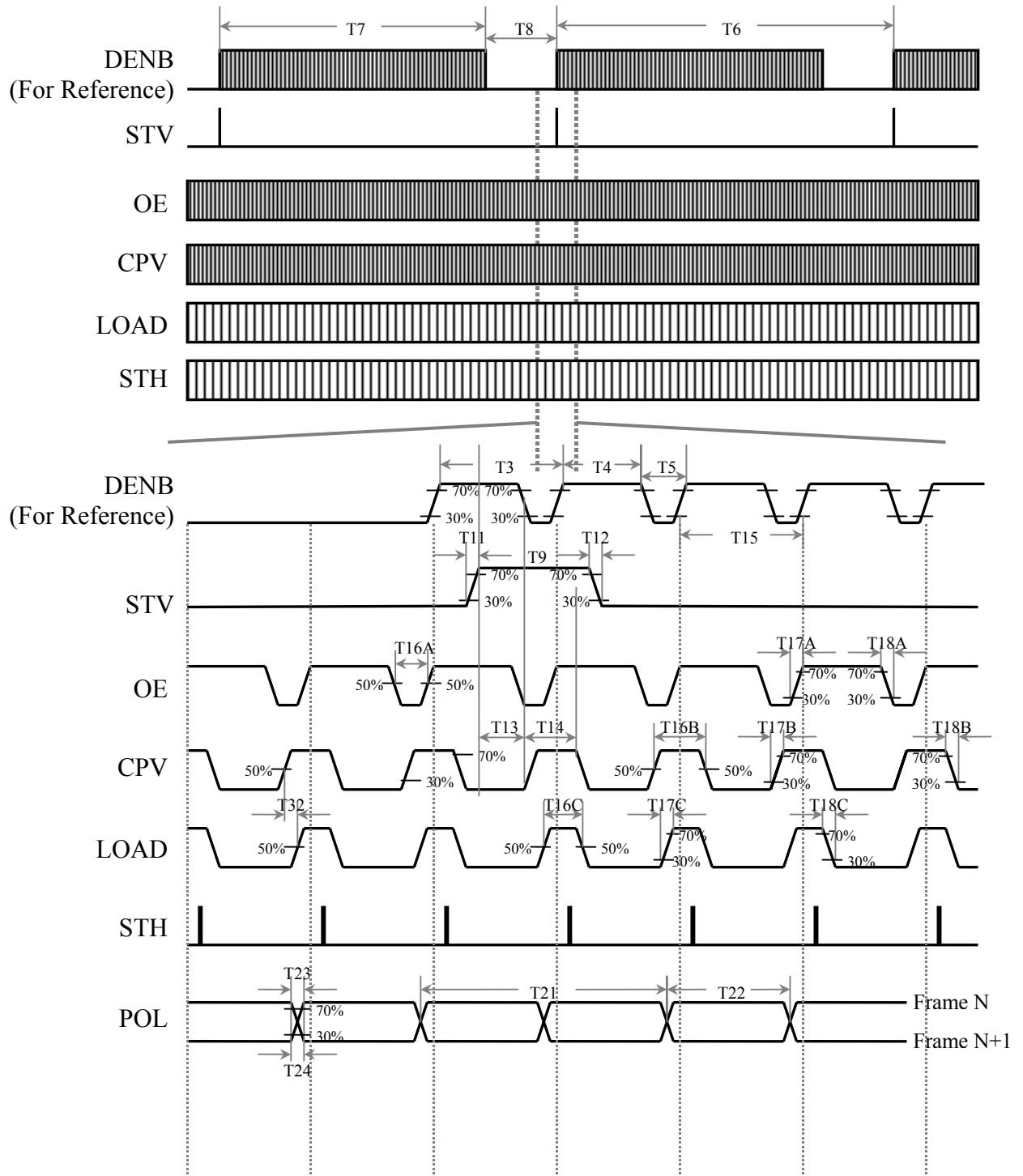
6.3.2 AC Timing Charts:

(1). Reference Signal (pixel clock):



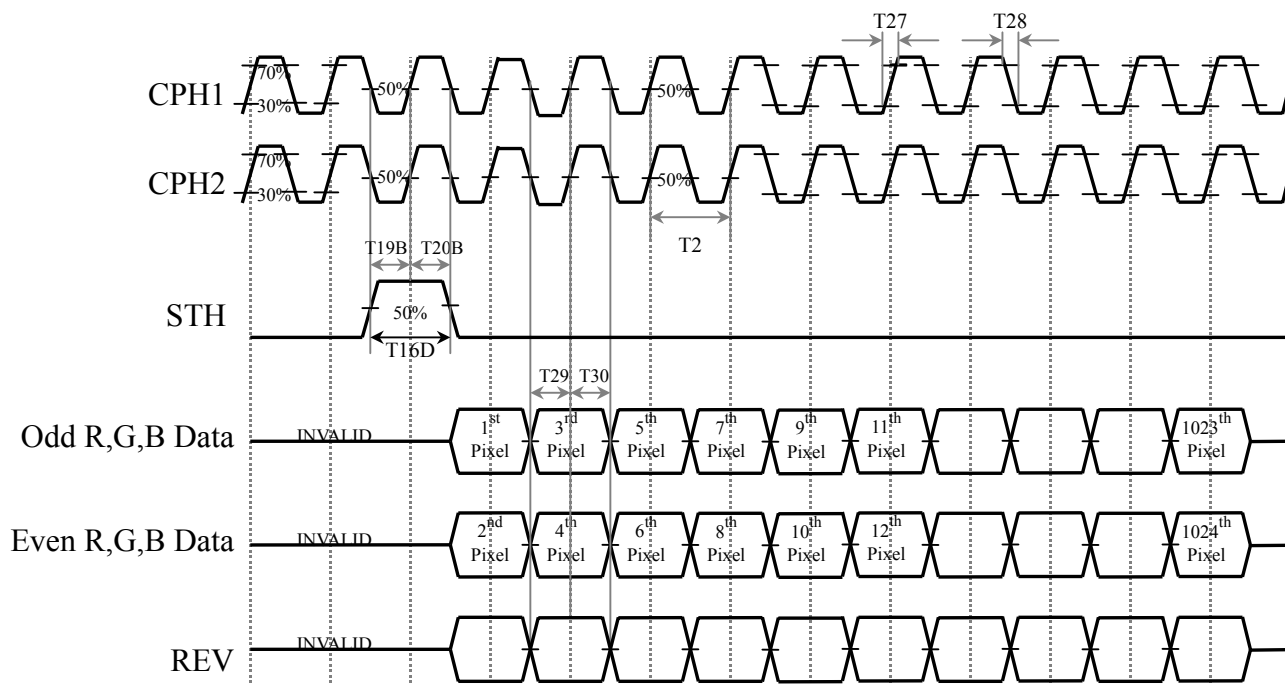
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(2). Vertical Periodic (STV1, STV2, OE, CPV):

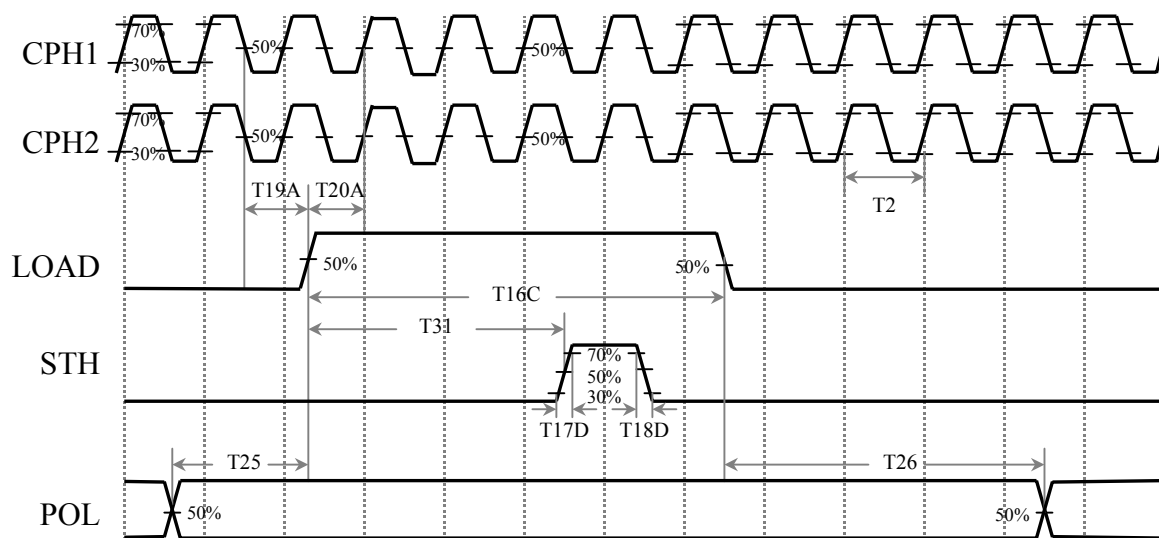


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(3). Horizontal Periodic 1 (STH, CPH, DATA):

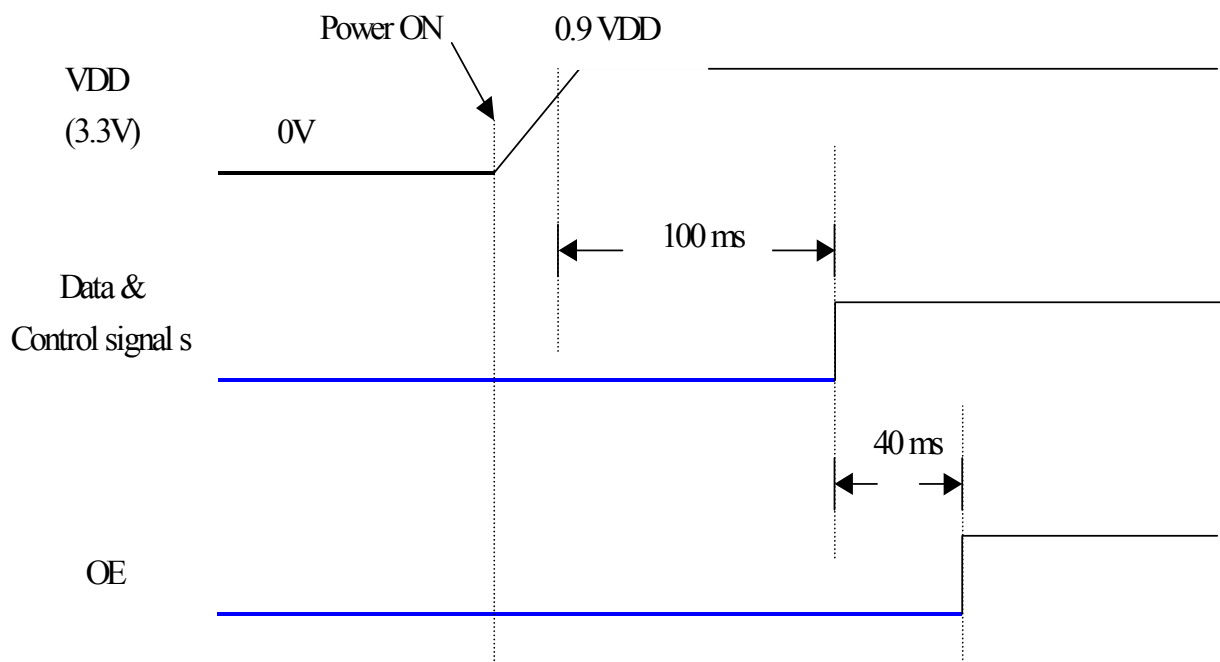


(4). Horizontal Periodic 2 (CPH, LOAD, STH, POL):



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(5). Initial Condition:

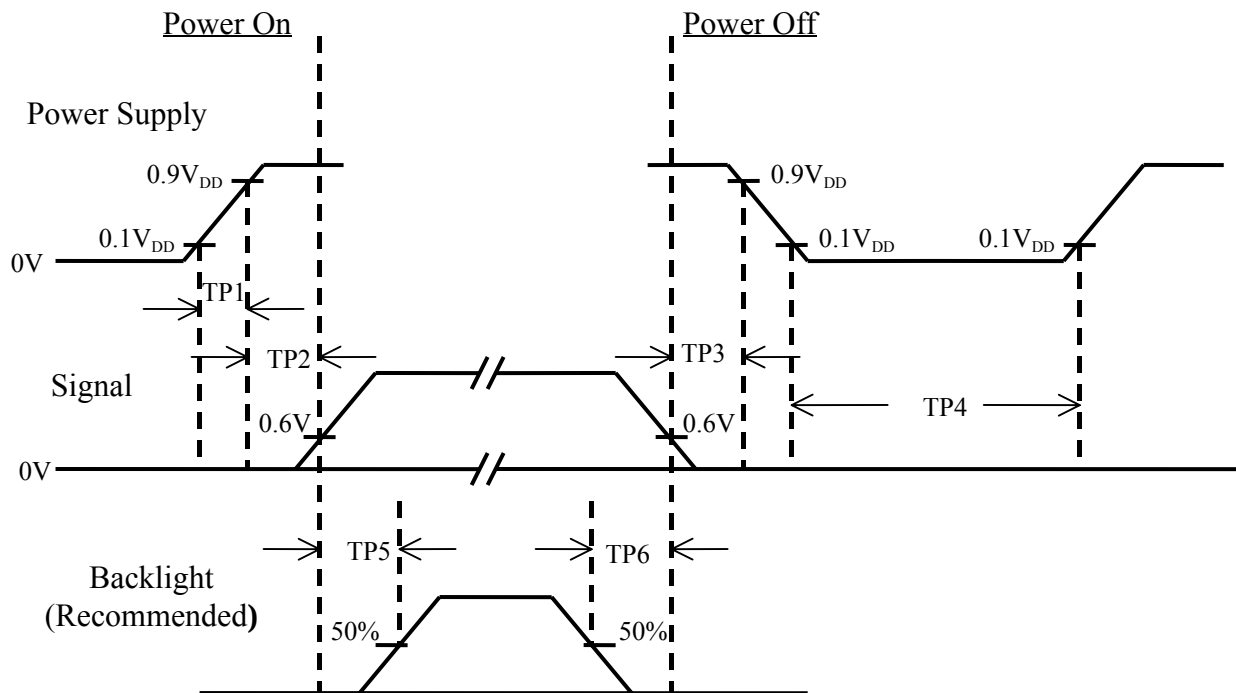


* Input Power (VDD) should be 0V(GND) before Power-ON.

* All signals (including control signals and data) should be kept **low** before it is active.

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6.4 Power On / Off Sequence :



Item	Min.	Typ.	Max.	Unit	Remark
TP1	0.4	-	10	msec	
TP2	100	-	200	msec	
TP3	0	-	50	msec	
TP4	1	-	-	sec	
TP5	200	-	-	msec	
TP6	200	-	-	msec	

Note : (1) The supply voltage of the external system for the module input should be the same as the definition of V_{DD}.

(2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.

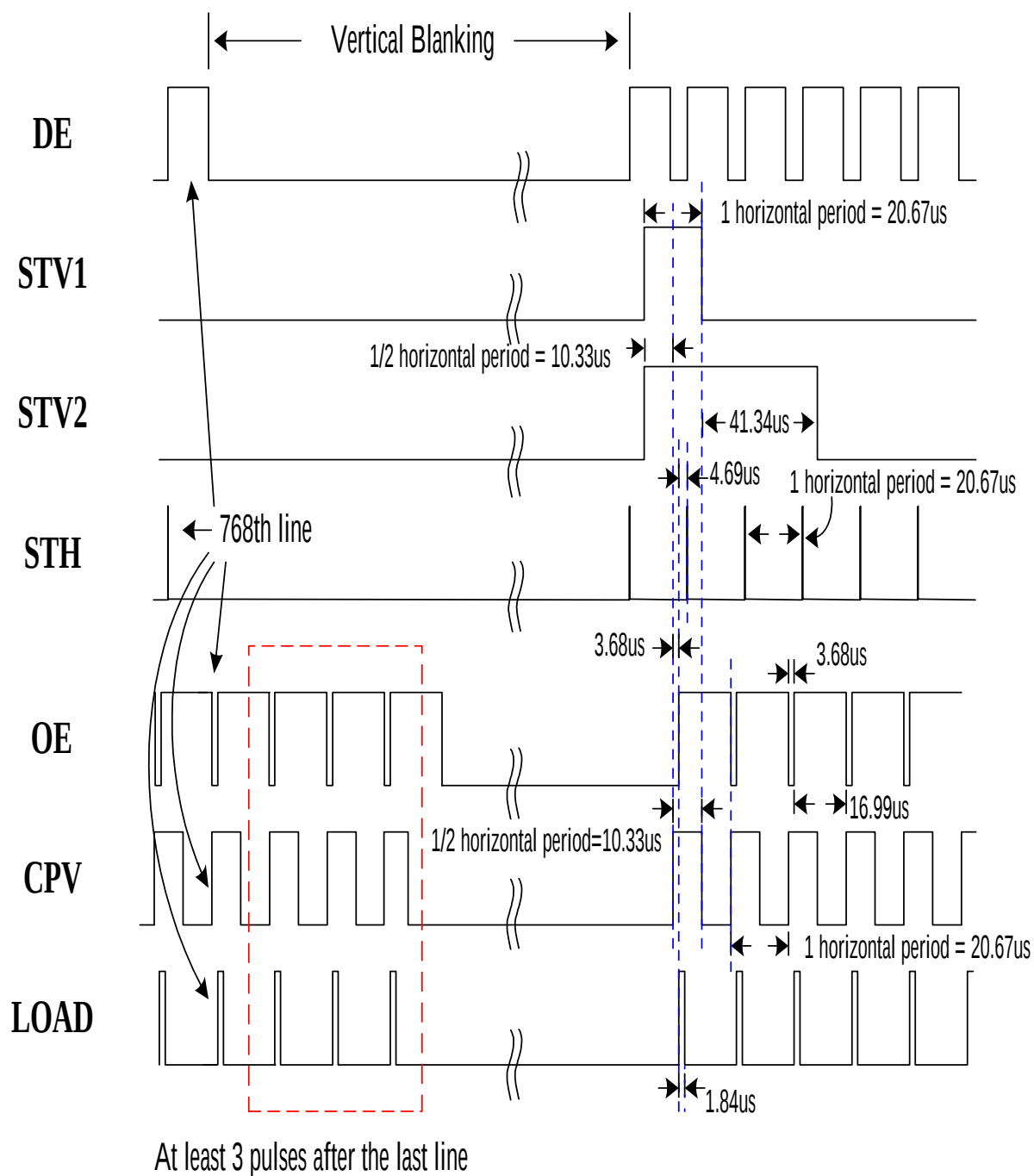
(3) In case of V_{DD} = off level, please keep the level of input signal on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

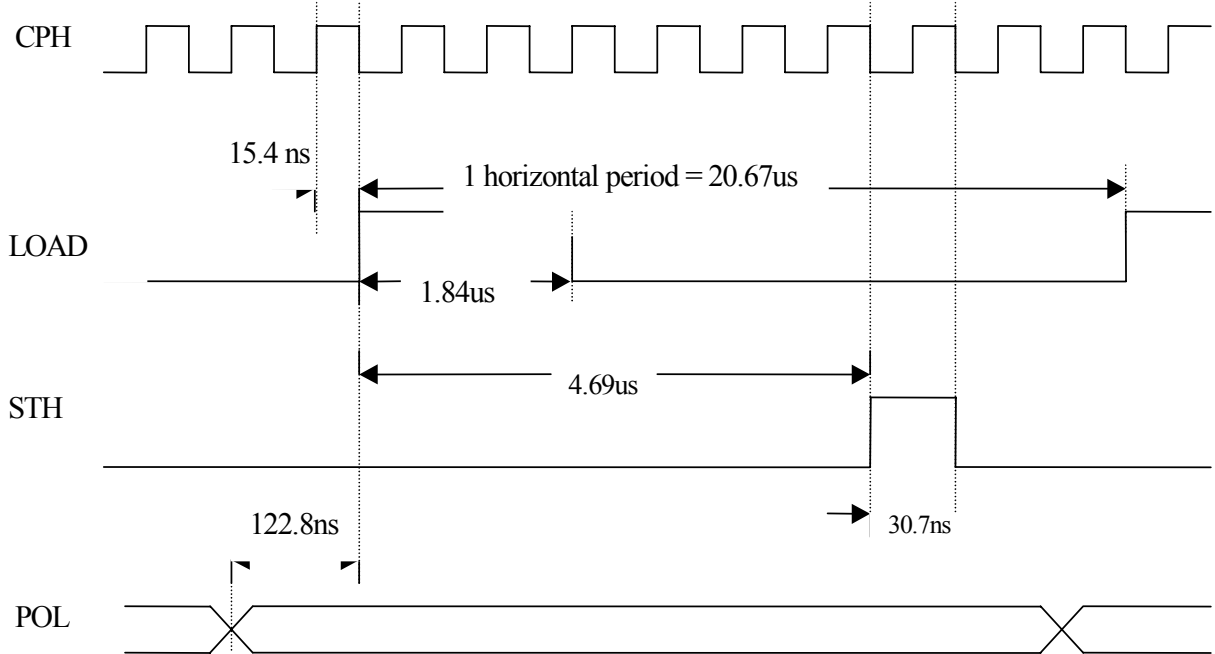
(5) Interface signal shall not be kept at high impedance when the power is on.

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7.0 Suggested Timing (VESA – 1024x768/60Hz) :



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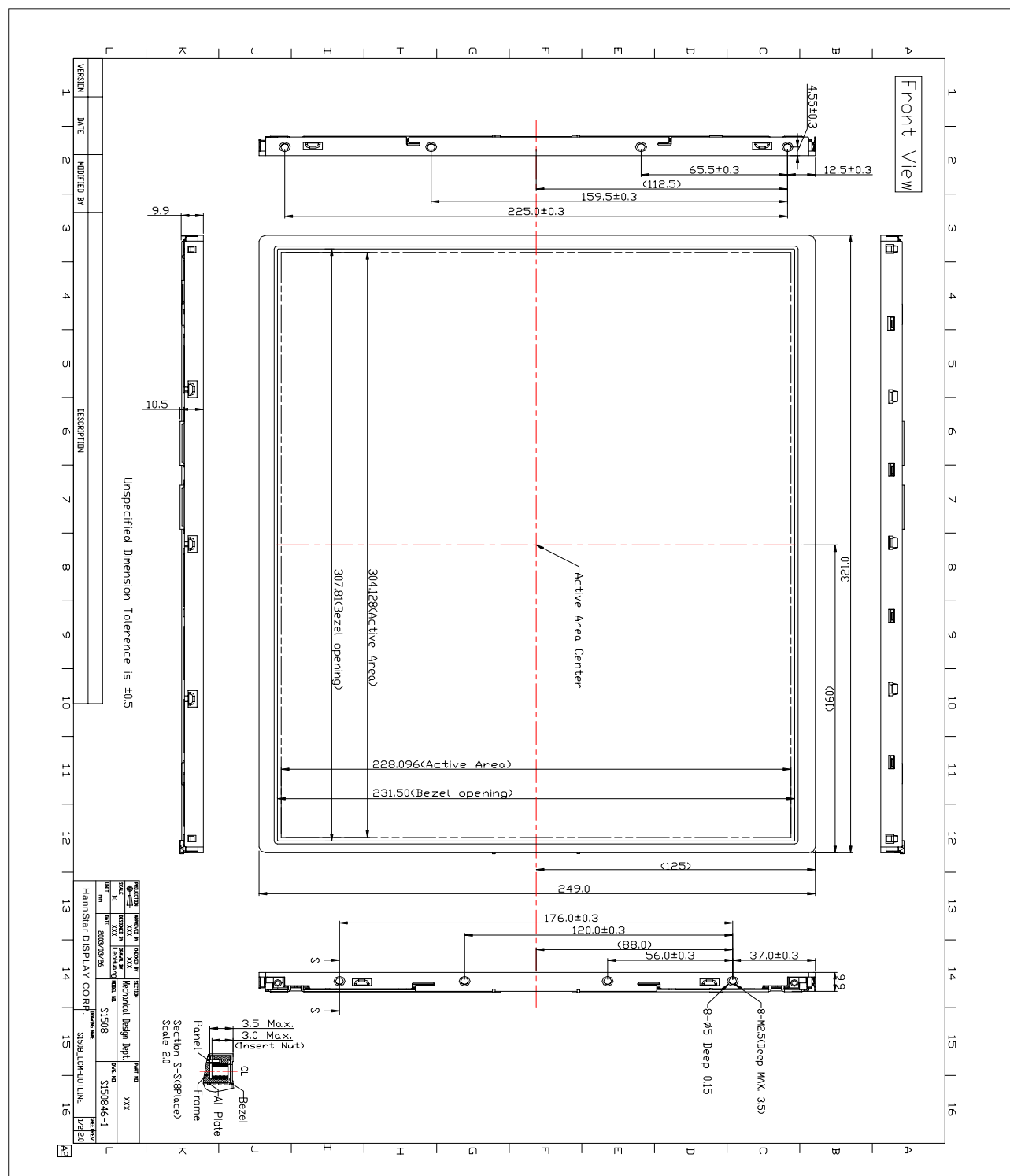


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8.0 OUTLINE DIMENSION

8.1 Front View:

Date: 2003.02.26



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8.2 Back View:

Date: 2003.02.26

