AE-12

TENTATIVE

HOLTEK 台灣華邦電子股份有限公司 HOLTEK MICROELECTRONICS INC.

HT—82230	11. 25. 1991
8 SEC PCM SPEECH WITH CPU MODE	PAGE: 1

A. General Description—

The HT—82230 is a single-chip PCM voice synthesis LSI implemented in CMOS technology . It is designed to work with minimum number of external component and provides 8 seconds of voice capacity with 7 bits resolution at 6 KHz sampling rate. It include 2 kind of operation mode: One is KEY mode; that with 16 retrigger key and can select 12 kind of voice The other is CPU mode; that can interfac with CPU. There are two sub-modes under CPU mode: One is similar to KEY mode , ie. CPU can select K1～K16 16 kind of voice, another mode is that CPU can program the voice directly, that is, it can select 192K bits ROM memory which represent 64 sections of voice data.

Blocks within the IC include: On—chip ROM for voice data storage, 7 bits current mode D/A converter and control logic. All blocks are already prepared for fabrication except voice data, the customer's voice data is programed into masked ROM by changing one mask during IC fabrication.

The 8 seconds voice capacity can be separated into maximum 64 sections with free length combination. Play of each section is triggered by either a control key or CPU data input. Two LED indicator output and one end pules outputs for external driving are also provided (refer to function description). The HT—82230 is offered in 18—pin, 20—pin or 24—pin DIP package.

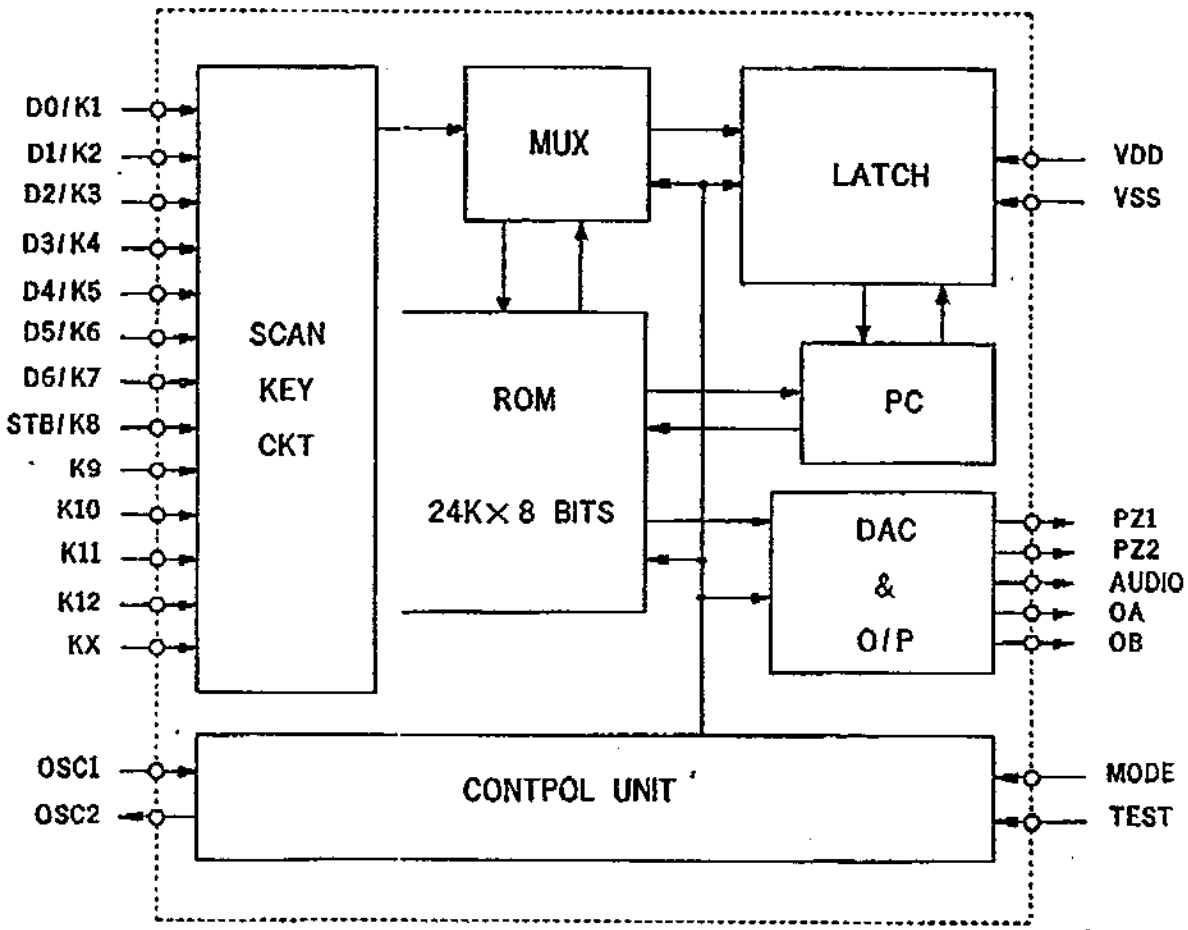
B. Features—

- Low stand-by current (1uA typ).
- Current mode D/A output.
- 64 sections programmable.
- 8 seconds of speech capacity.
- 24K × 8 bits ROM.
- Direct piezo driving output.
- 12 retriggerable direct output priority coding (TTL/CMOS input compatible).
- Two kinds of operation mode
  (1.) key mode. (2.) CPU mode
- One key for sequential playing (KX).
- Max 16 keys sequential playing function.
- Max 64 voice section.
- Operating voltage : 2.4V—5.3V.

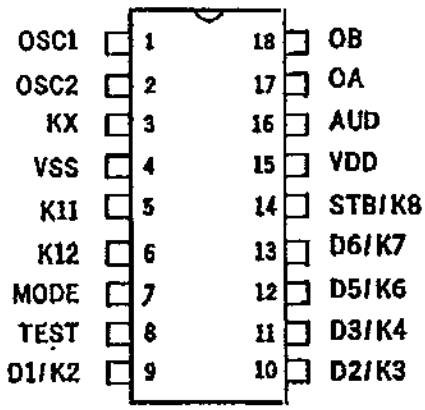
C. Application—

- Toys.
- Public address system.
- Alter & Warning system.
- Sound effect generator.
- Production with speech interface.

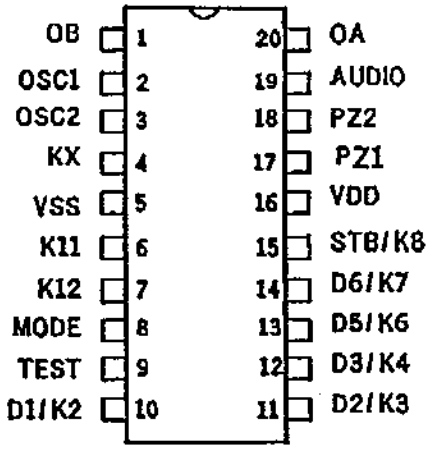
D. Block Diagram—



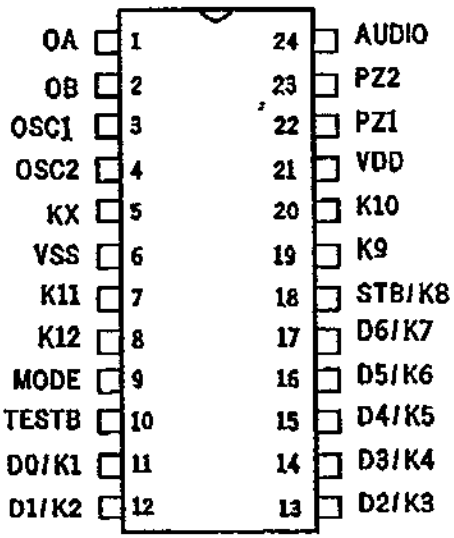
E. Pin Assignment—



HT—82230
18—PIN DIP



HT—82230
20—PIN DIP



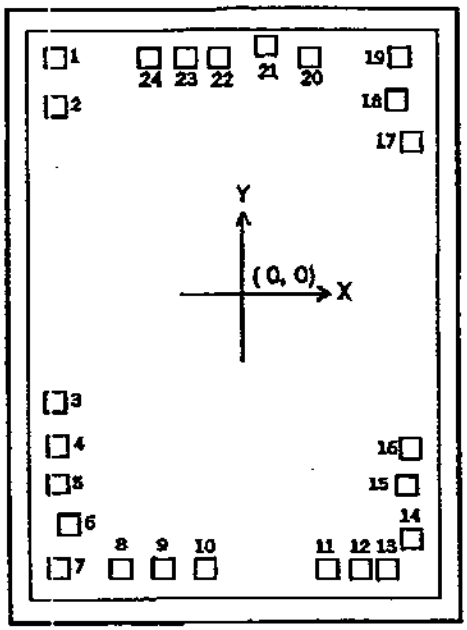
HT—82230
24—PIN DIP

F. Pin Description—

(24 pin version.)

Pin No.	Pin Name	I/O	Description
1	OA	O	LED driver (KEY mode); Busy pin (CPU mode).
2	OB	O	LED driver (KEY mode); End pulse (CPU mode).
3	OSC1	I	Oscillator input pin.
4	OSC2	O	Oscillator output pin.
5	KX	I	Sequential playing key (KEY mode).
6	VSS		Negative power supply (GND).
7	KI1	I	Key input pin (KEY mode).
8	KI2	I	Key input pin (KEY mode).
9	MODE	I	CPU mode (VSS); KEY mode (floating or VDD).
10	TESTB	I	For test only.
11	D0/K1	I	Data input (CPU mode); key input (KEY mode).
12	D1/K2	I	Data input (CPU mode); key input (KEY mode).
13	D2/K3	I	Data input (CPU mode); key input (KEY mode).
14	D3/K4	I	Data input (CPU mode); key input (KEY mode).
15	D4/K5	I	Data input (CPU mode); key input (KEY mode).
16	D5/K6	I	Data input (CPU mode); key input (KEY mode).
17	D6/K7	I	Data input (CPU mode); key input (KEY mode).
18	STB/K8	I	strobe pin (CPU mode); key input (KEY mode).
19	K9	I	Key input (KEY mode).
20	K10	I	Key input (KEY mode).
21	VDD		Positive power supply.
22	PZ1	O	Puzzler output driver 1.
23	PZ2	O	Puzzler output driver 2.
24	AUD	O	Voice output pin.

G. Pad Assignment & Position —



* This IC substrate should be connected to VSS in PCB layout artwork.

Chip Size : 2740 X 4530 (μ m)^2

Unit : (μ m)

Pad No	Symbol	X	Y	Pad No	Symbol	X	Y
1	OSC2	−1103.5	1995.5	13	D5/K6	698.5	−1995.0
2	KX	−1122.5	1744.5	14	D6/K7	1112.5	−1810.0
3	VSS	−1169.0	−1121.0	15	STB/K8	1099.0	−1584.5
4	K11	−1122.5	−1331.5	16	K9	1112.5	−1364.5
5	K12	−1122.0	−1580.0	17	K10	1112.5	1575.5
6	MODE	−1109.0	−1800.0	18	VDD	1059.5	1797.0
7	TESTB	−1184.0	−1995.0	19	PZ1	1094.0	1995.0
8	D0/K1	−853.5	−1995.0	20	PZ2	723.0	1995.0
9	D1/K2	−543.5	−1995.0	21	AUD	146.0	2023.0
10	D2/K3	−232.5	−1995.0	22	OA	−49.0	1995.0
11	D3/K4	77.5	−1995.0	23	OB	−344.0	1995.0
12	D4/K5	388.5	−1995.0	24	OSC1	−539.0	1995.0

H. Absolute Maximum Ratings —

(Ta = 25 °C)

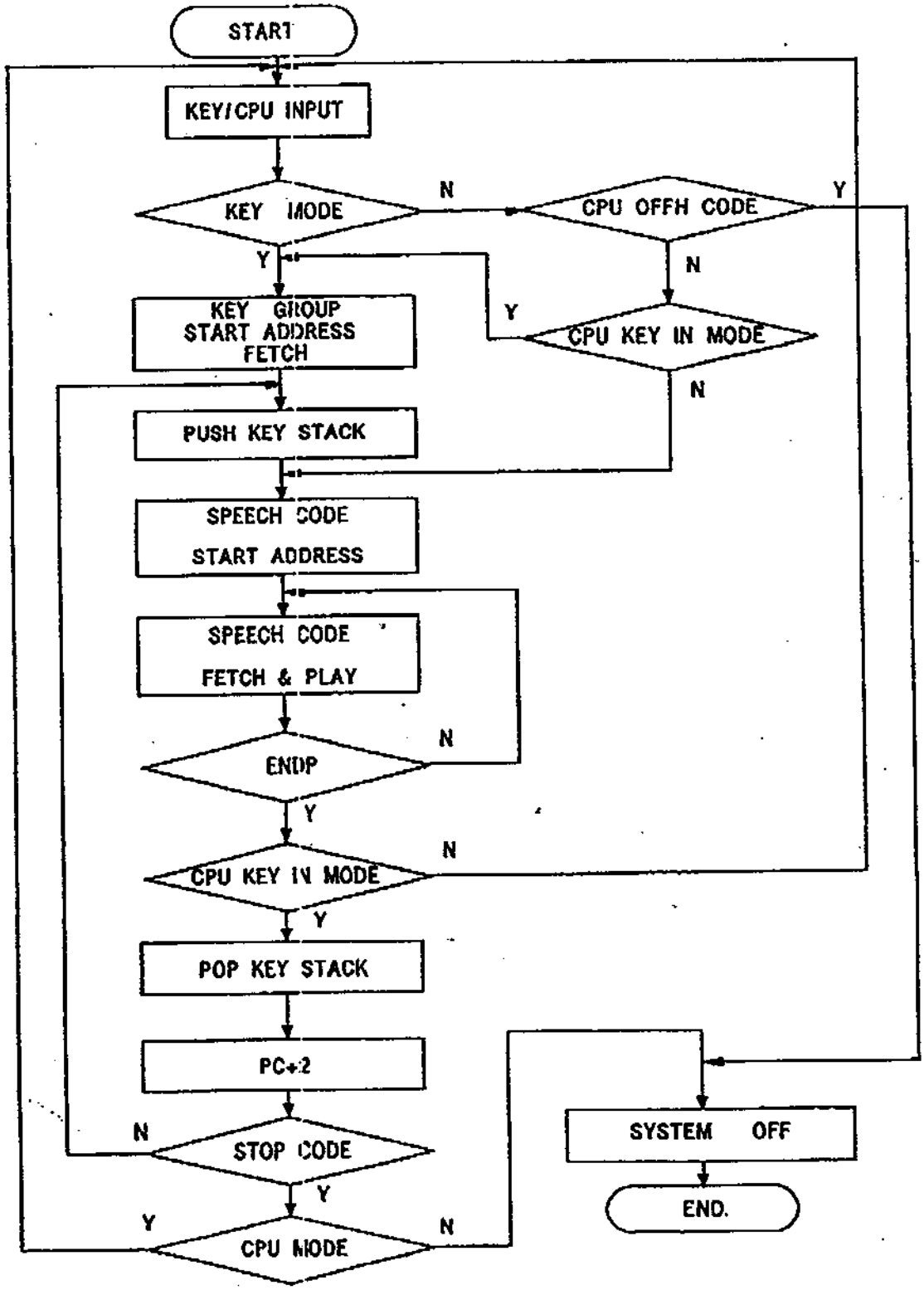
Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage	V_{DD}	−0.3	6.0	V
Input Voltage	V_I	V_{SS}−0.3	V_{DD}+0.3	V
Storage Temperature	T_{STG}	−50	125	°C
Operating Temperature	T_{OP}	0	70	°C

I. Electrical Characteristics —

(Ta = 25 °C)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
		VDD	Condition				
V_{DD}	Operating Voltage	—	—	2.4	—	5.3	V
I_{DD}	Operating Current	5V	No Load	—	0.6	3	mA
I_O	Max. AUD Output Current	5V	V_{OH}=0.6V	−2	−3	—	mA
I_{OL1}	OUTA Sink Current	5V	V_{OL}=1.0V	3	5	—	mA
I_{OL2}	OUTB Sink Current	5V	V_{OL}=1.0V	3	5	—	mA
I_{SW}	K1~K12 Current	5V	V_{IL}=0V	—	10	50	uA
V_{IH}	'H' Input Voltage	—	—	0.7V_{DD}	—	—	V
V_{IL}	'L' Input Voltage	—	—	—	—	0.3V_{DD}	V
fosc	System Frequency	5V	Rosc=12K	—	1.58	—	MHz
I_{STB}	Stand-by Current	5V	—	—	.2	5	uA

J. Flowchart—

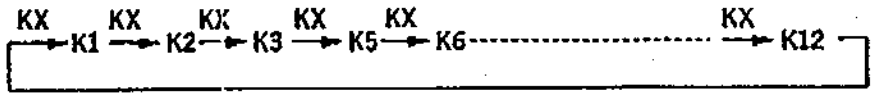

START
KEY/CPU INPUT
KEY MODE
N
CPU OFFH CODE
Y
Y
N
KEY GROUP START ADDRESS FETCH
Y
CPU KEY IN MODE
N
PUSH KEY STACK
SPEECH CODE START ADDRESS
SPEECH CODE FETCH & PLAY
N
ENDP
Y
N
CPU KEY IN MODE
Y
POP KEY STACK
PC+2
N
STOP CODE
Y
Y
CPU MODE
N
SYSTEM OFF
END.

K. Functional Description—

The HT—82230 with 2 operation mode: KEY mode & CPU mode.

1. KEY mode function:

When MODE key be connected to VDD or floating, the K1~K12 as retriggerable direct key input, and OA, OB as LED driver pins. K1~K12 can generate 12 kind of voice. KX key is a sequential playing key, when it be triggered, the IC wil playing K1 voice repeatly until trigger signal be removed. If KX key be retriggered again, the IC will playing the next voice. Its function as belows:



Under KEY mode OA, OB can drive LED directly, and can be optioned as follow:

OA— volume indicator.

— 2Hz 1/4 duty.

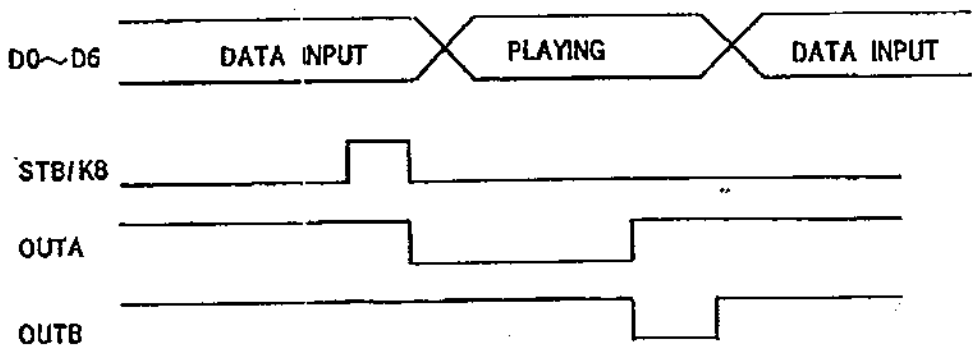
— Busy output (low active).

OB— $\overline{2Hz}$, 1/4 duty . (OUTA)

— END pulse. (Low pulse 90ms, fs=6 KHz)

2. CPU mode function:

When MODE key be connected to VSS, the D0—D6 as data input pins. STB/K8 pin as chip strobe, OA as busy pin, OB as end pin. The Timing as follows:



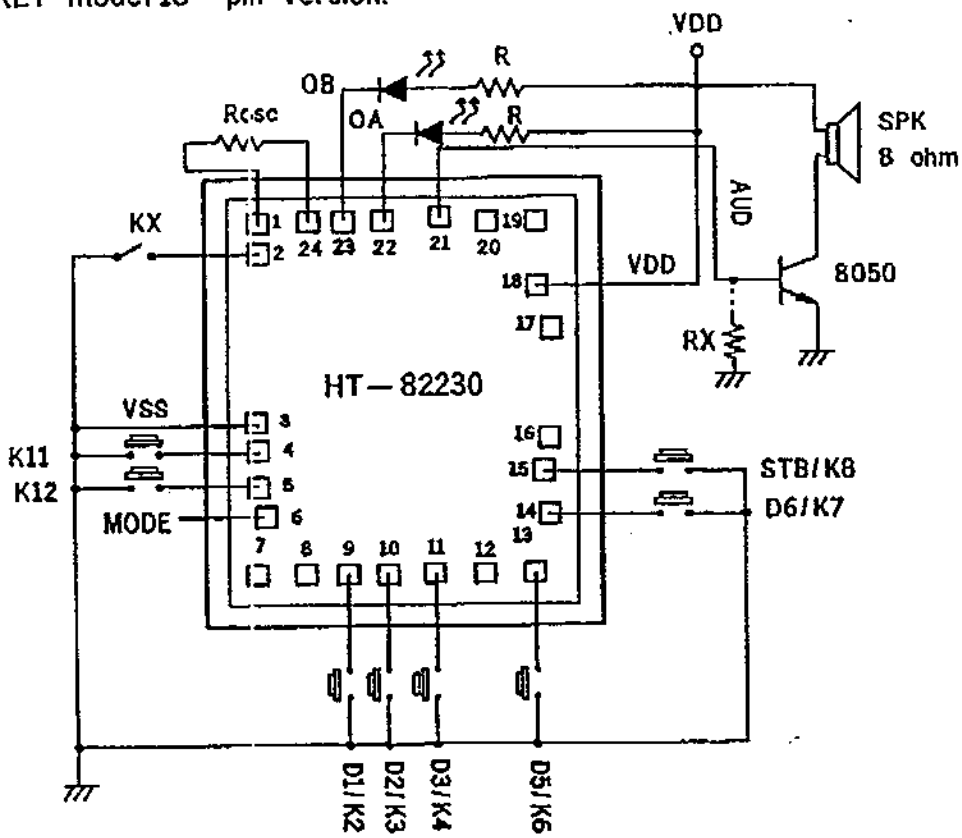
Note: When D6=1, it option as key—in mode, it can select K1～K16 voice.

When D6=0, it option as program mode, it can select 0～63 sections voice.

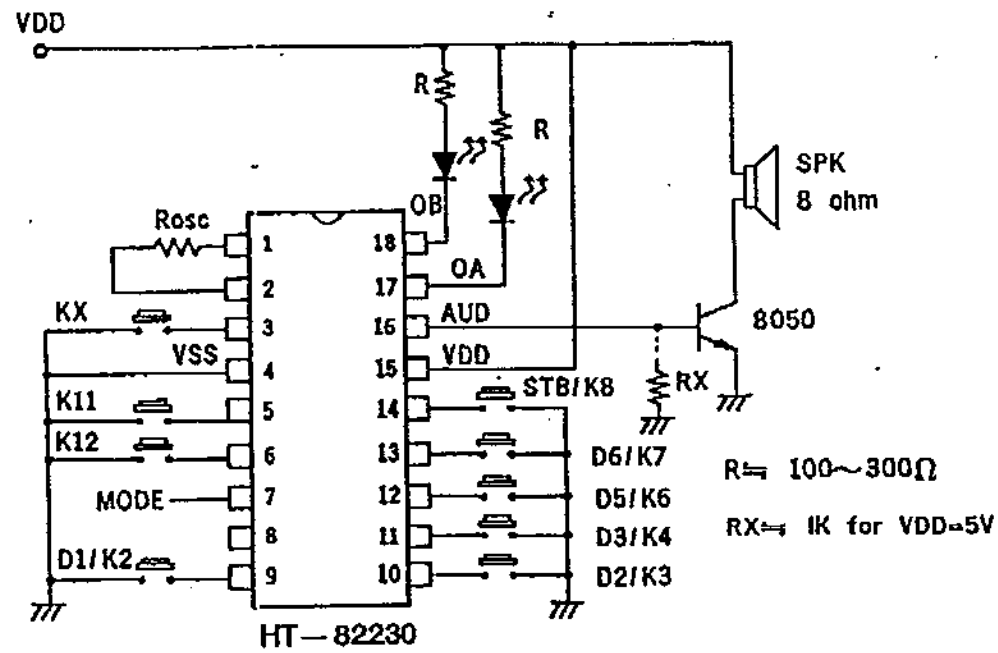
KEY—IN MODE					CPU PROGRAM MODE						
D3	D2	D1	D0	Function	D5	D4	D3	D2	D1	D0	Function
0	0	0	0	KEY16	0	0	0	0	0	0	Section0 (space).
0	0	0	1	KEY1	0	0	0	0	0	1	Section1 (up).
0	0	1	0	KEY2	0	0	0	0	1	0	Section2 (down).
					0	0	0	0	1	1	Section3
					0	0	0	1	0	0	Section4
1	1	1	1	KEY15							
					0	0	1	1	1	1	Section15
											Section16
					1	1	1	1	1	1	Section63

L. Application Circuit—

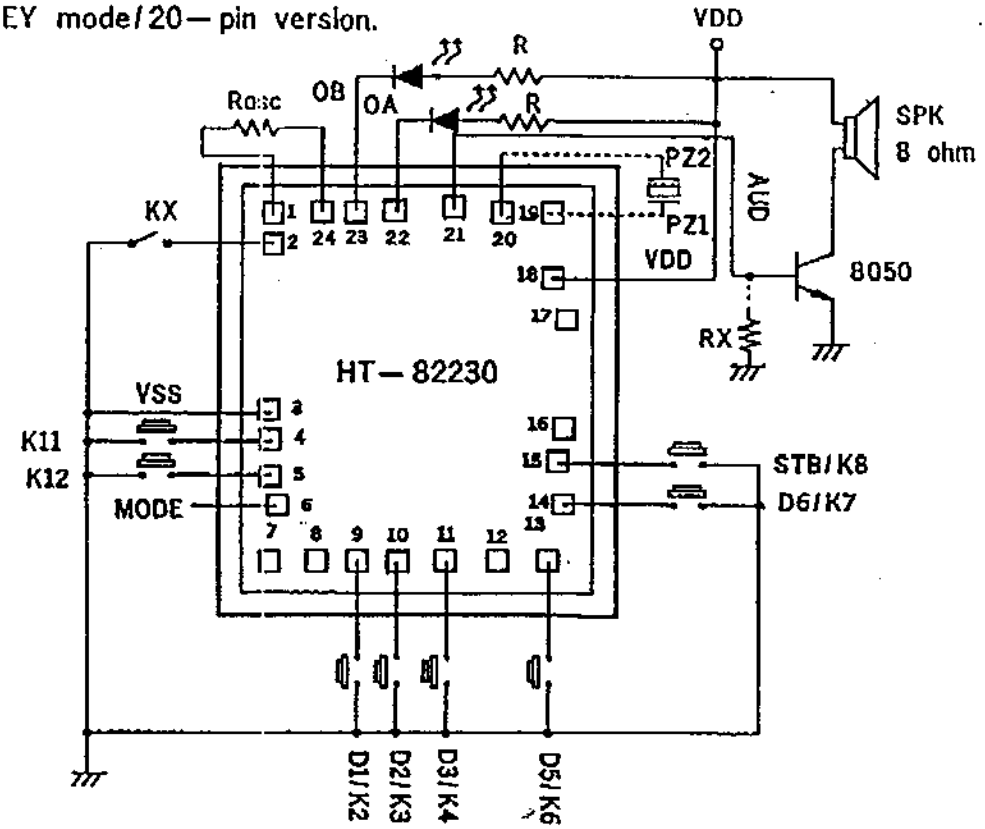
(a.) KEY mode/18—pin version.



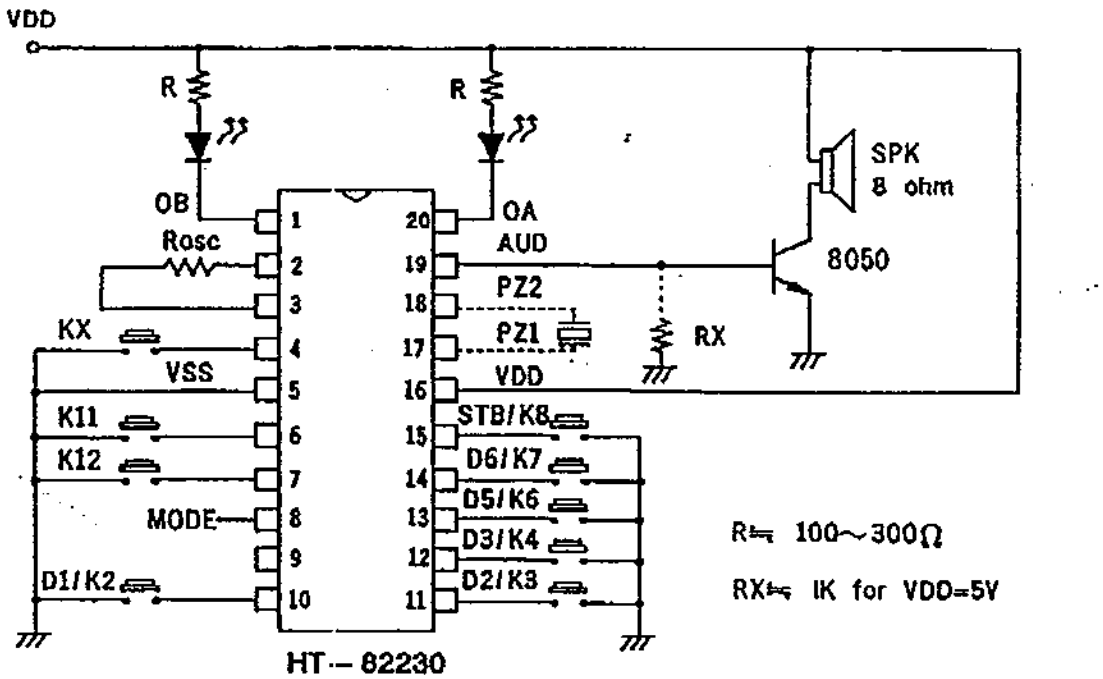
* This IC substrate should be connected to VSS in PCB layout artwork.



(b.) KEY mode/20—pin version.



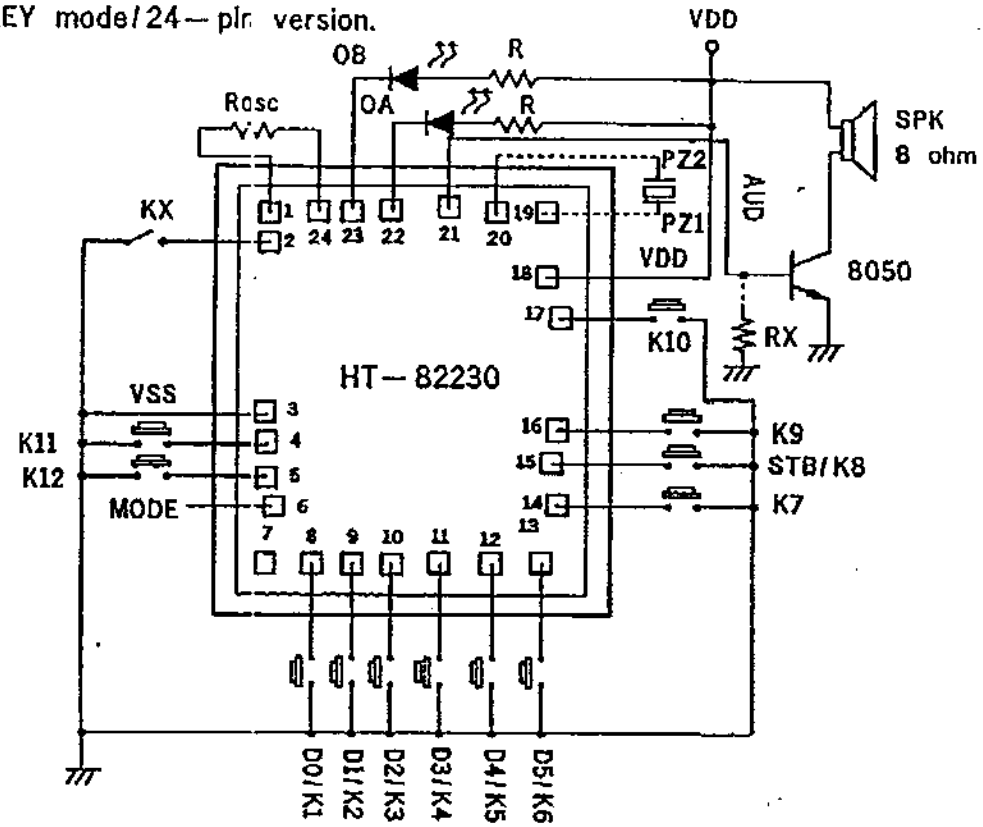
★ This IC substrate should be connected to VSS in PCB layout artwork.



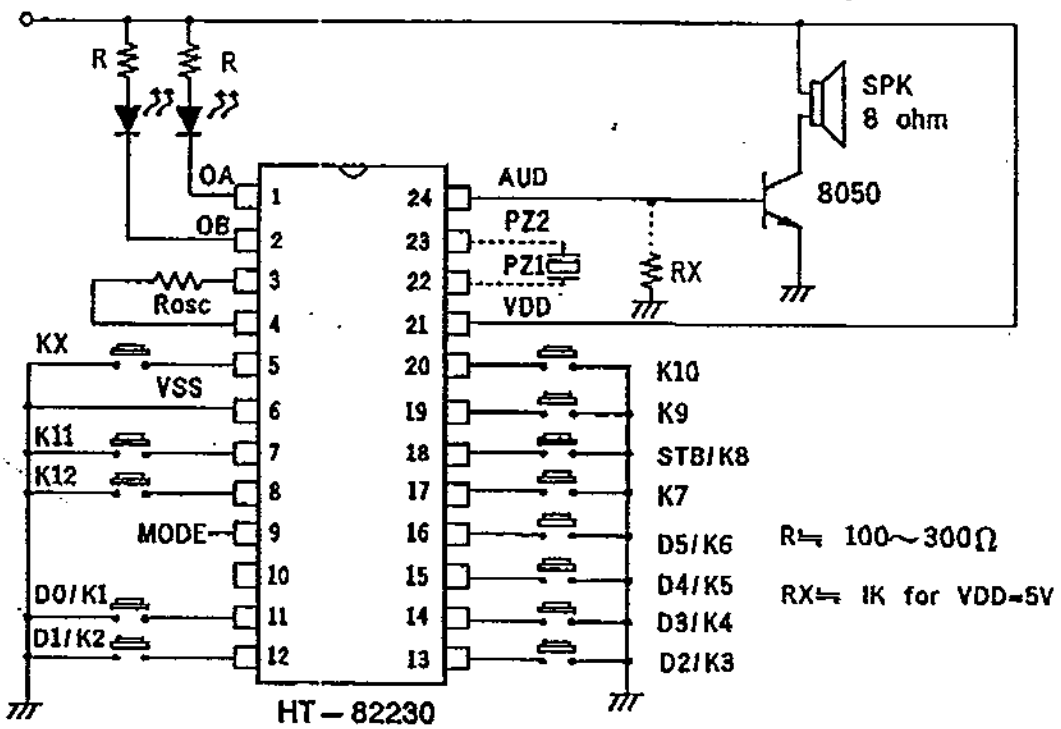
R≒ 100~300Ω

RX≒ IK for VDD=5V

(c.) KEY mode/24—pin version.



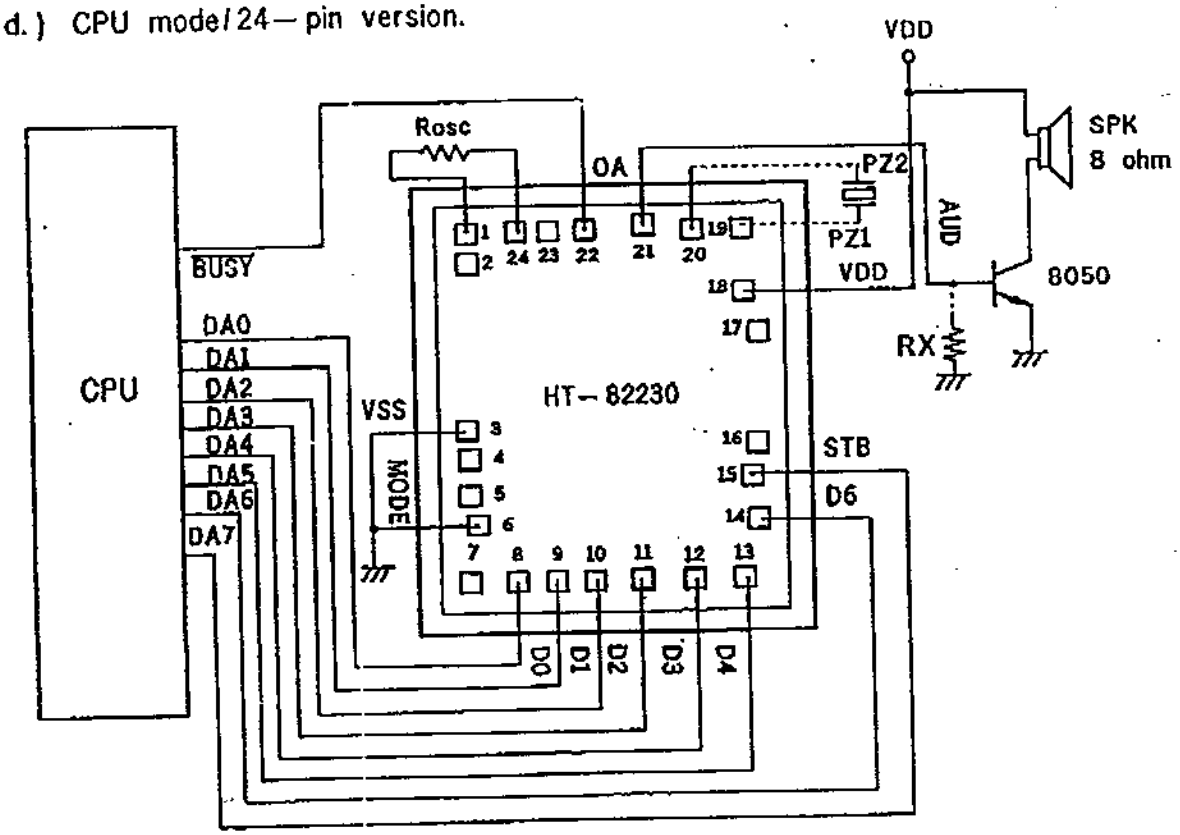
VDD • This IC substrate should be connected to VSS in PCB layout artwork.



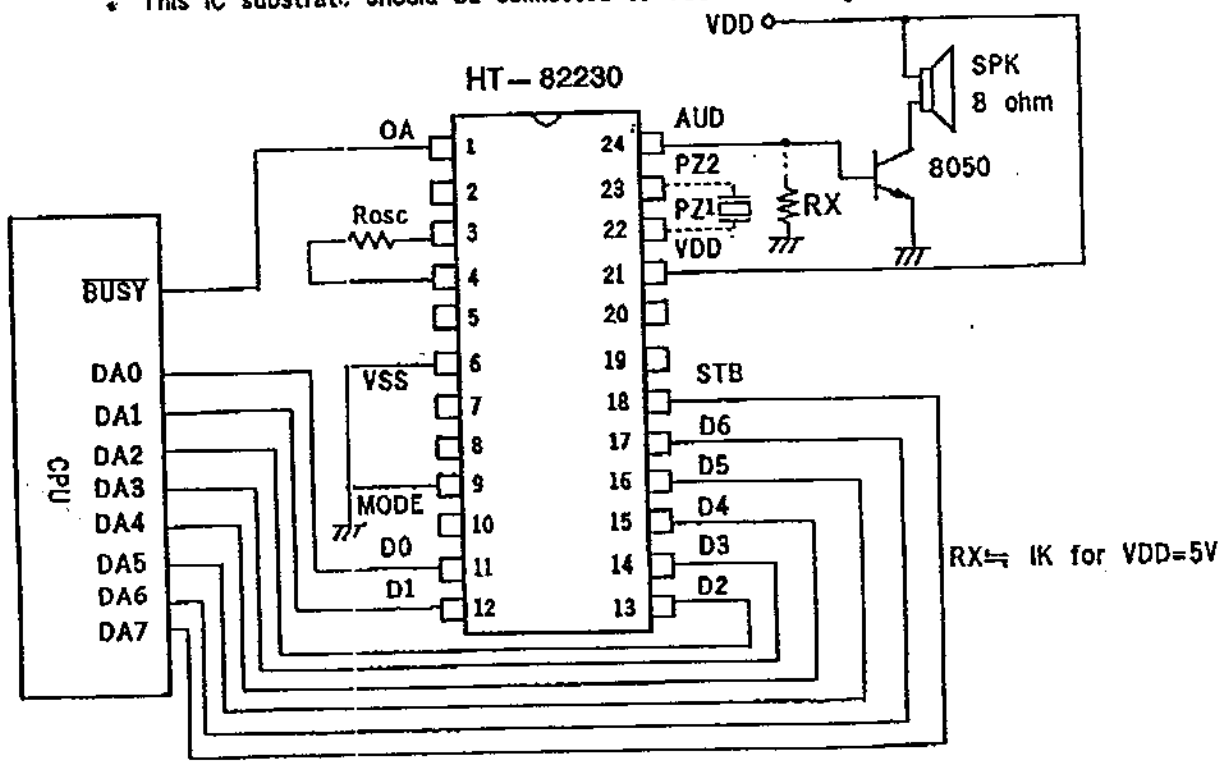
R≒ 100～300Ω

RX≒ 1K for VDD=5V

(d.) CPU mode/24—pin version.

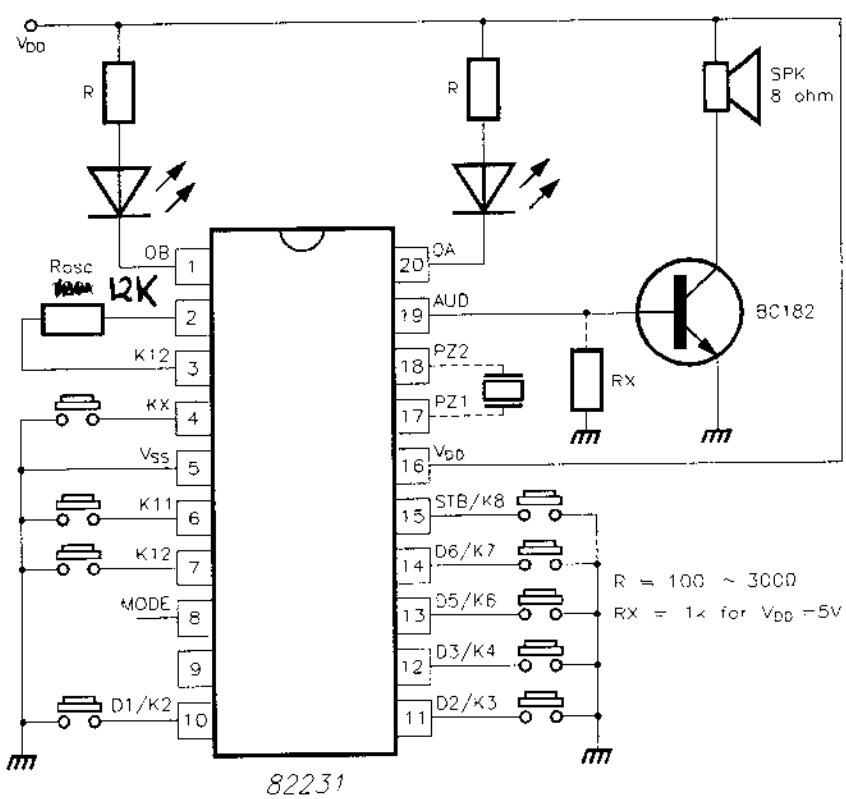


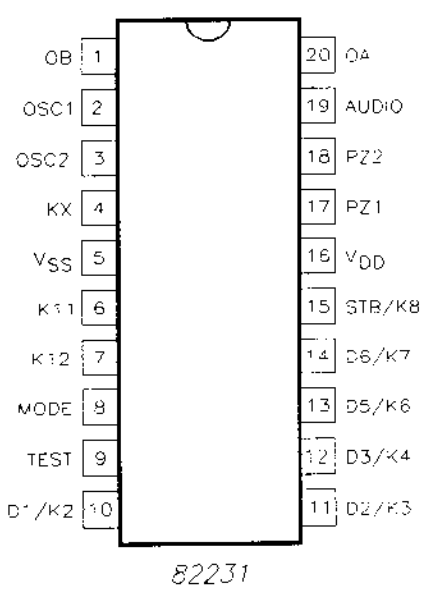
* This IC substrate should be connected to VSS in PCB layout artwork.



RX≒ IK for VDD=5V

AE12.


VDD
R
R
SPK
8 ohm
Rosc
12K
OB 1
2
K12 3
KX 4
VSS 5
K11 6
K12 7
MODE 8
9
D1/K2 10
20 OA
19 AUD
18 PZ2
17 PZ1
16 VDD
15 STB/K8
14 D6/K7
13 D5/K6
12 D3/K4
11 D2/K3
BC182
RX
R = 100 ~ 300Ω
RX = 1K for VDD =5V
82231


OB 1
OSC1 2
OSC2 3
KX 4
VSS 5
K11 6
K12 7
MODE 8
TEST 9
D1/K2 10
20 OA
19 AUDIO
18 PZ2
17 PZ1
16 VDD
15 STB/K8
14 D6/K7
13 D5/K6
12 D3/K4
11 D2/K3
82231