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TITLE : HT10X21-413

Product Specification for Customer

Rev. B

HYDIS Technologies

REVISION HISTORY

REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
O		Initial Release	09.07.10	S.W.KANG
A	E0909-F009	Polarizer is changed	09.09.18	S.W.KANG
B		Product description is modified.	09.09.26	S.W.KANG

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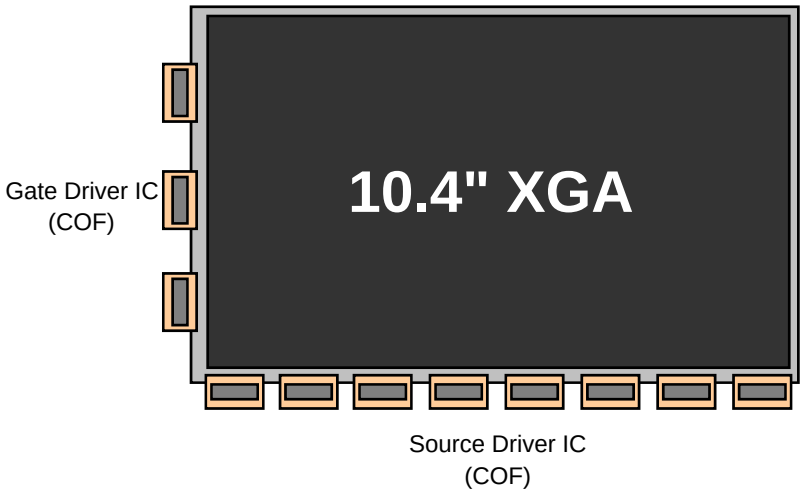
1.0 GENERAL DESCRIPTION

1.1 Introduction

HT10X21-413 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as active switching devices. This module has a 10.4 inch diagonally measured active area with XGA resolutions (1024 horizontal by 768 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe. This module consists of a TFT-LCD panel manufactured by HYDIS and driver tabs of data and gate.



1.2 Features : Without PCB & BLU

1) Unit : Panel + Source IC, Gate Driver IC (Without PCB & BLU)
2) High contrast ratio and wide viewing angle
3) Upper : Clear/ Lower : Clear
4) RoHS Product
5) High temperature operation enable (High reliability Liquid Crystal)

1.3 Application

Industrial and Digital Information Display

1.3 General Specifications

PARAMETER	SPECIFICATION	UNIT	REMARK
Active area	210.432 X 157.824	mm	
Number of pixels	1024(H) × 768(V)	pixels	
Pixel pitch	0.2055(H) × 0.2055(V)	mm	
Pixel arrangement	RGB Vertical stripe		
Liquid Crystal clearing temperature	≥ 104	℃	
Display mode	Normally Black		
Panel transmittance	4.8	%	
Surface treatment	Upper : Clear / Lower : Clear		
Color filter Chromaticity	X=0.312 , Y=0.342		

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit.

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARK
Operating Temperature	T_{OP}	-20	+85	℃	Note 1
Storage Temperature	Tsp	-20	+85	℃	Note 1
Main Component ' Operation Temperature	T_{OP}	0	+70	℃	Note 2

Note 1. This range was defined by a result of customer test.
Because the range of reliability temperature would depend on customer system such as backlight, heating system, etc.

Note 2. Basically, HYDIS could guarantee our units(Panel + COF) according to each of component specification within following temperature.

So this LCD(Panel + COF) unit could guarantee absolute maximum rating with the minimum reliability temperature of component.
For more detail, refer to HYDIS reliability test of page 25.

3.0 ELECTRICAL SPECIFICATIONS

3.1 Recommended electrical specification

PARAMETER		MIN.	TYP.	MAX.	UNIT	REMARK
Digital Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Analog Power Supply Voltage	AVDD	8.7	9.0	9.3	V	
γ 1-corrected Power Supply Voltage	GMA1	8.4	8.7	9.0	V	
γ 2-corrected Power Supply Voltage	GMA2	6.82	7.12	7.42	V	
γ 3-corrected Power Supply Voltage	GMA3	6.22	6.52	6.82	V	
γ 4-corrected Power Supply Voltage	GMA4	5.68	5.98	6.28	V	
γ 5-corrected Power Supply Voltage	GMA5	4.38	4.68	4.98	V	
γ 6-corrected Power Supply Voltage	GMA6	4.04	4.34	4.64	V	
γ 7-corrected Power Supply Voltage	GMA7	2.74	3.04	3.34	V	
γ 8-corrected Power Supply Voltage	GMA8	2.20	2.50	2.80	V	
γ 9-corrected Power Supply Voltage	GMA9	1.60	1.90	2.20	V	
γ 10-corrected Power Supply Voltage	GMA10	0.12	0.32	0.62	V	
Panel Common Power Supply	Vcom	3.45	3.65	3.85	V	Note 1, 2
Gate Driver Positive Power Supply	Von	24.1	24.4	24.7	V	
Gate Driver Negative Power Supply	Voff	-7.6	-7.9	-8.2	V	
Permissible Input Ripple Voltage	Vripple	-	-	100	mA	At VDD = 3.3V

Note 1 : Panel common power (VCOM) has to optimize at flicker pattern with variable voltage circuit.
This circuit has to be composed of variable resister.
Note 2 : Flicker pattern is one pixel skip green pattern. Green 6bits data is 100000. The other data is 000000.

R	G	B	R	G	B	R	G	B	R	G	B	
R	G	B	R	G	B	R	G	B	R	G	B	
R	G	B	R	G	B	R	G	B	R	G	B	
R	G	B	R	G	B	R	G	B	R	G	B	

Figure. Flicker pattern

※ The others electrical specifications are refered to APPENDIX

4.0 OPTICAL SPECIFICATION

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and TOPCONE BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement... VDD shall be 3.3 +/-0.3V at 25°C. Optimum viewing angle direction is 6 o'clock.

PARAMETER		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Viewing Angle Range	Horizontal	Θ_3	CR > 10	-	89	-	Deg.	Note 1
		Θ_9		-	89	-	Deg.	
	Vertical	Θ_{12}		-	89	-	Deg.	
		Θ_6		-	89	-	Deg.	
Panel Transmittance					4.8		%	
Luminance Contrast ratio		CR	Θ = 0°	-	500	-		Note 2
White Chromaticity		x_w	Ta= 25° C Θ = 0°	-	0.312	-		Note 3
		y_w		-	0.342	-		
Color Reproduction				-	40	-	%	
Response Time		$T_r + T_d$		-	-	40	ms	Note 4
Cross Talk		CT		-	-	2.0	%	Note 5

Note : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1 shown in Appendix).

2. Contrast measurements shall be made at viewing angle of Θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix)
Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 4 shall be defined as the spectral data of Color filter. Final color chromaticity could be changed by customer' light source.

4. The electro-optical response time measurements shall be made as FIGURE 3 shown in Appendix by switching the "data" input signal OFF and ON. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

5. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark. (See FIGURE 4 shown in Appendix).

5.0 PIN ASSIGNMENTS

5.1 Drive IC Part Name : TMC57384CF11 (Source Drive IC)
HM10G005H-C5M (Gate Drive IC)

5.1.1 XD1

Input side			Input side	
No.	Descriptions		No.	Descriptions
1	NC		42	VDD1(*1)
2	Repair1		43	VDD1(*2)
3	Repair2		44	VSS1
4	CPV		45	GMA5
5	GND		46	GMA4
6	GND		47	GMA3
7	VDD		48	GMA2
8	STV		49	GMA1
9	VOFF		50	VSS2
10	VOFF		51	CLK
11	VON		52	TP1
12	VCOM		53	POL
13	OUTPUT [1)]		54	REV1
14	EIO2 [2)]		55	REV2
15	D55		56	D25
16	D54		57	D24
17	D53		58	D23
18	D52		59	D22
19	D51		60	D21
20	D50		61	D20

21	D45		62	D15
22	D44		63	D14
23	D43		64	D13
24	D42		65	D12
25	D41		66	D11
26	D40		67	D10
27	D35		68	D05
28	D34		69	D04
29	D33		70	D03
30	D32		71	D02
31	D31		72	D01
32	D30		73	D00
33	RS(LCH)		74	EIO1 [2)]
34	LP		75	OUTPUT [1)]
35	VDD2		76	NC
36	L/P		77	Repair2
37	GMA10		78	Repair1
38	GMA9		79	NC
39	GMA8		80	NC
40	GMA7		81	NC
41	GMA6		82	NC

5.1.2. XD2 ~ XD7

Input side			Input side	
No.	Descriptions		No.	Descriptions
1	NC		42	VDD1(*1)
2	Repair1		43	VDD1(*2)
3	Repair2		44	VSS1
4	CPV		45	GMA5
5	GND		46	GMA4
6	GND		47	GMA3
7	NC		48	GMA2
8	NC		49	GMA1
9	NC		50	VSS2
10	NC		51	CLK
11	NC		52	TP1
12	NC		53	POL
13	OUTPUT [1)]		54	REV1
14	EIO2 [2)]		55	REV2
15	D55		56	D25
16	D54		57	D24
17	D53		58	D23
18	D52		59	D22
19	D51		60	D21
20	D50		61	D20

21	D45		62	D15
22	D44		63	D14
23	D43		64	D13
24	D42		65	D12
25	D41		66	D11
26	D40		67	D10
27	D35		68	D05
28	D34		69	D04
29	D33		70	D03
30	D32		71	D02
31	D31		72	D01
32	D30		73	D00
33	RS(LCH)		74	EIO1 [2)]
34	LP		75	OUTPUT [1)]
35	VDD2		76	NC
36	L/P		77	Repair2
37	GMA10		78	Repair1
38	GMA9		79	NC
39	GMA8		80	NC
40	GMA7		81	NC
41	GMA6		82	NC

5.1.3 XD8

Input side			Input side	
No.	Descriptions		No.	Descriptions
1	NC		42	VDD1(*1)
2	Repair1		43	VDD1(*2)
3	Repair2		44	VSS1
4	NC		45	GMA5
5	GND		46	GMA4
6	GND		47	GMA3
7	NC		48	GMA2
8	NC		49	GMA1
9	NC		50	VSS2
10	NC		51	CLK
11	NC		52	TP1
12	NC		53	POL
13	OUTPUT [1)]		54	REV1
14	EIO2 [2)]		55	REV2
15	D55		56	D25
16	D54		57	D24
17	D53		58	D23
18	D52		59	D22
19	D51		60	D21
20	D50		61	D20

21	D45		62	D15
22	D44		63	D14
23	D43		64	D13
24	D42		65	D12
25	D41		66	D11
26	D40		67	D10
27	D35		68	D05
28	D34		69	D04
29	D33		70	D03
30	D32		71	D02
31	D31		72	D01
32	D30		73	D00
33	RS(LCH)		74	EIO1 [2)]
34	LP		75	OUTPUT [1)]
35	VDD2		76	NC
36	L/P		77	Repair2
37	GMA10		78	Repair1
38	GMA9		79	VCOM
39	GMA8		80	VCOM
40	GMA7		81	NC
41	GMA6		82	NC

Note 1) Output pins(#13, #75) are to confirm the first & final data of each drive IC.
Note 2) XD1 EIO2 pin(#14) is connected start pulse of timing controller & the other EIO2 pins are connected before EIO1 pins.

5.2 Pin Description

5.2.1 Source Drive IC

Pin Name	I/O	Description	Function
D00~D05 D10~15 D20~25	I	Data input for port-1	Input gray scale data(6bit) multiple 2 pixels(6dot) 36 bit length image data. Dn0: LSB , Dn5:MSB
D30~35 D40~45 D50~55	I	Data input for port-2	
EIO1 EIO2	O I	Start pulse	For start pulse I/O of internal shift register EIO1: Left shift output , EIO2: Left shift input
L/R	I	Shift direction	Right shift : H Left shift : L This must be grounded.
CLK	I	Shift clock	Write the data into data register at the rising edge. CLK should be input continuously.
VDD1(*1) VDD1(*2)	I	Analog supply voltage	VDD1(*1) supplies reference voltage of analog circuit. Then stable voltage should be supplied. VDD1(*2) supplies output circuits etc.
VDD2	I	Digital supply voltage	For supply digital power to the device.
GMA1~GMA10	I	γ-corrected power supplies	Maintain the reference voltage during output gray scale voltage.
TP1	I	Latch input	Latch the registered data and transfer to the D/A converter at the rising edge. Gray scale voltage output at the falling edge.
POL	I	Polarity control	POL="L" : The reference voltages for Odd number outputs are GMA1~GAM5 Even number outputs are GMA6~GAM10 POL="H" : The reference voltages for Odd number outputs are GMA6~GAM10 Even number outputs are GMA1~GAM5
REV1 REV2	I	Data inversion	Select the input data invert or not. REV1: for port-1 inverting control REV2: for port-2 inverting control REV1,2="H" : data are inverted REV1,2="L" : data are not inverted

OUTPUT	O	LC drive Output	Output of supplied voltage to each final data of each drive IC
RS(LCH)	I	LCD drive capability selector	Switch LCD drive capability RS="H" : for the heavy load RS="L" : for the specification load Recommendation = "L"
LP	I	Low power mode selector	Select the charge/discharge current level LP="H" : normal current level LP="L" : low current level Recommendation = "L"
VSS1 VSS2	I	Ground	Connect this pin to the ground of the system

5.2.2 Gate Drive IC

Pin Name	I/O	Description	Function
CPV	I	Shift clock input	This pin inputs a shift clock to the internal shift register. The shift operation is performed in synchronization with the rising edge of this input.
STV	I	Shift pulse input	This pin is read at the rising edge of shift clock CPV, and scan signals are output from the driver output pins.
VCOM	I	Driver positive power supply	The driver output: high level
VDD	I	Logic power supply	For supply digital power to the device
VSS GND	I	Ground	Connect this pin to the ground of the system
VEE	I	Negative power supply for internal operation	The driver output: low level
Repair1 Repair2	-	Panel repair line	
VCOM	I	Panel common voltage	
NC	-	No connection	

6.0 SIGNAL TIMING SPECIFICATION

6.1 Signal timing specification (VESA)

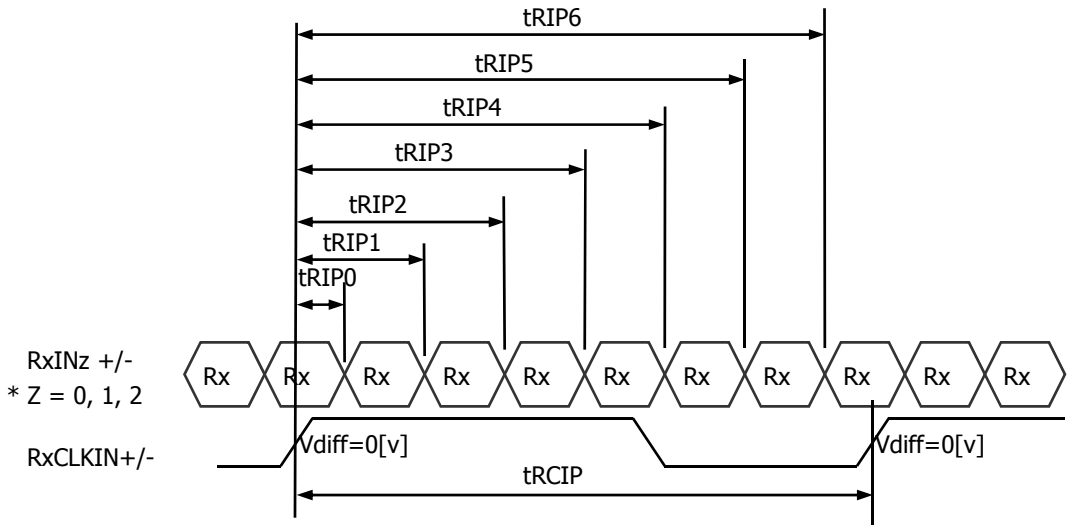
The HT10X21-411 is operated by the only DE (Data enable) mode.

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Frame Period	T1	-	806	-	lines
Vertical Display Period	T2	768	768	768	lines
One Line Scanning Period	T3	-	1344	-	clocks
Horizontal Display Period	T4	1024	1024	1024	clocks
Clock Frequency	1/T5	-	65	-	MHz

6.2 LVDS Rx Interface Timing Parameter

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
CLKIN Period	tRCIP	12.5	15.38	-	nsec	
Input Data 0	tRIP0	-0.4	0.0	+0.4	nsec	
Input Data 1	tRIP1	tRICP/7-0.4	tRICP/7	tRICP/7+0.4	nsec	
Input Data 2	tRIP2	2 ×tRICP/7-0.4	2 ×tRICP/7	2 ×tRICP/7+0.4	nsec	
Input Data 3	tRIP3	3 ×tRICP/7-0.4	3 ×tRICP/7	3 ×tRICP/7+0.4	nsec	
Input Data 4	tRIP4	4 ×tRICP/7-0.4	4 ×tRICP/7	4 ×tRICP/7+0.4	nsec	
Input Data 5	tRIP5	5 ×tRICP/7-0.4	5 ×tRICP/7	5 ×tRICP/7+0.4	nsec	
Input Data 6	tRIP6	6 ×tRICP/7-0.4	6 ×tRICP/7	6 ×tRICP/7+0.4	nsec	

* Vdiff = (RINz+)-(RINz-), (RCLKIN+)-(RCLKIN-)



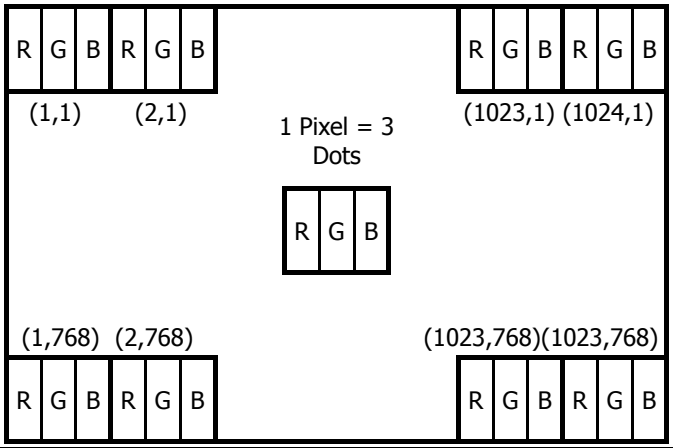
6.3 LVDS Interface

LVDS Transmitter : THC63LVDM83A or equivalent

INPUT SIGNAL	TRANSMITTER		INTERFACE		DF19KR-20P-1H	REMARK
	PIN NO.	PIN NO.	SYSTEM (Tx)	TFT-LCD (Rx)	PIN NO.	
R0	51	48 47	OUT0- OUT0+	IN0- IN0+	5 6	
R1	52					
R2	54					
R3	55					
R4	56					
R5	3					
G0	4					
G1	6	46 45	OUT1- OUT1+	IN1- IN1+	7 8	
G2	7					
G3	11					
G4	12					
G5	14					
B0	15					
B1	19					
B2	20	42 41	OUT2- OUT2+	IN2- IN2+	9 10	
B3	22					
B4	23					
B5	24					
HSYNC	27					
VSYNC	28					
DE	30					
MCLK	31	40	CLKOUT-	CLKIN-	11	
		39	CLKOUT+	CLKIN+	12	

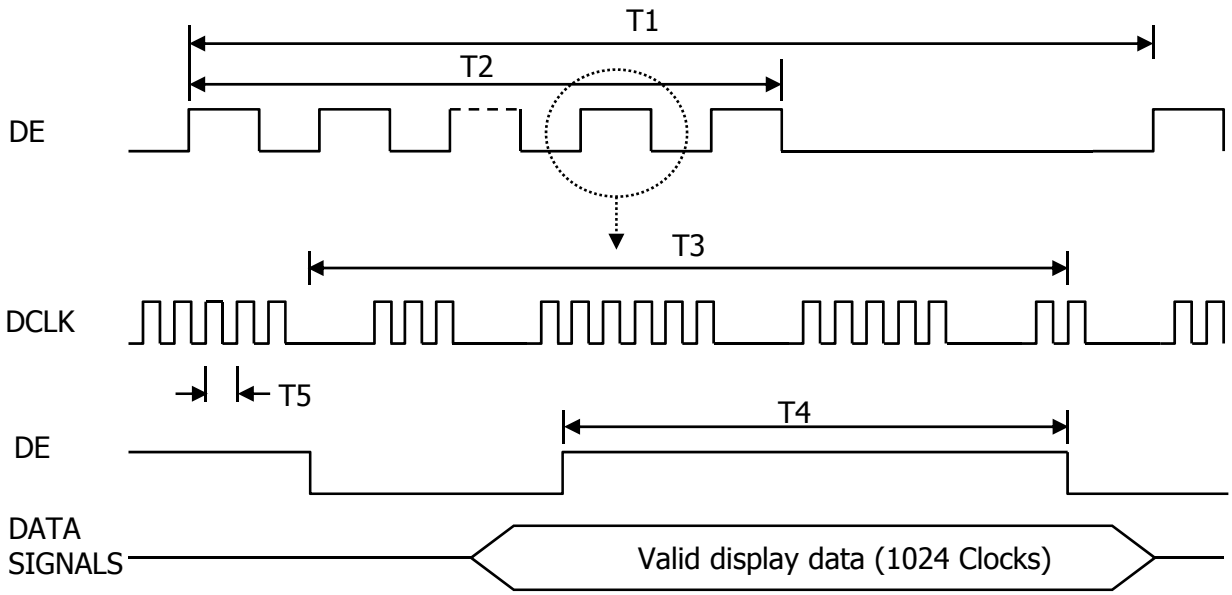
6.4 Data Input Format

Display position of input data



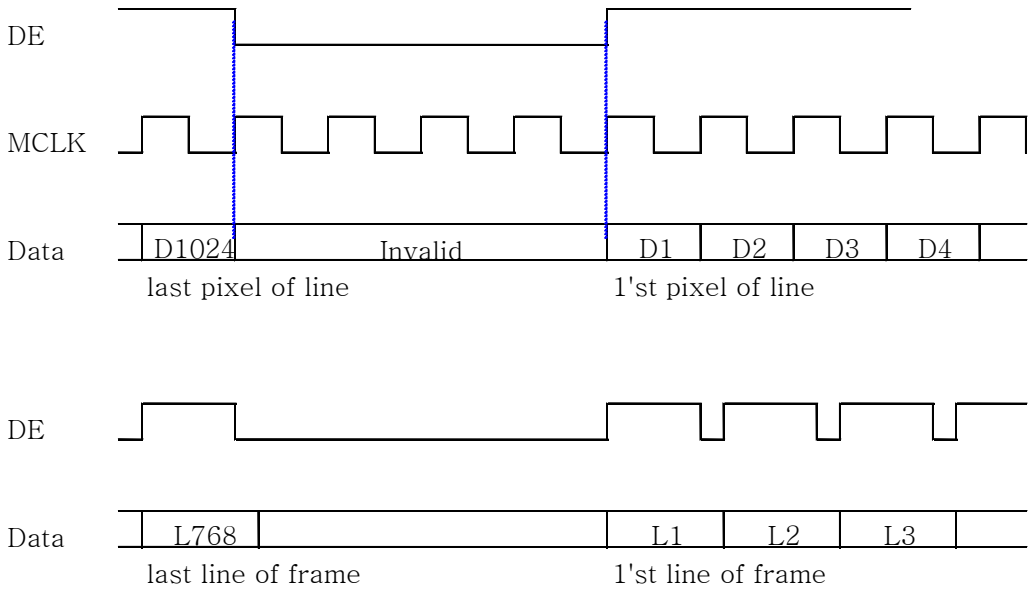
7.0 SIGNAL TIMING WAVEFORMS OF INTERFACE SIGNAL (DE MODE)

7.1 Timing Waveforms of Interface Signal

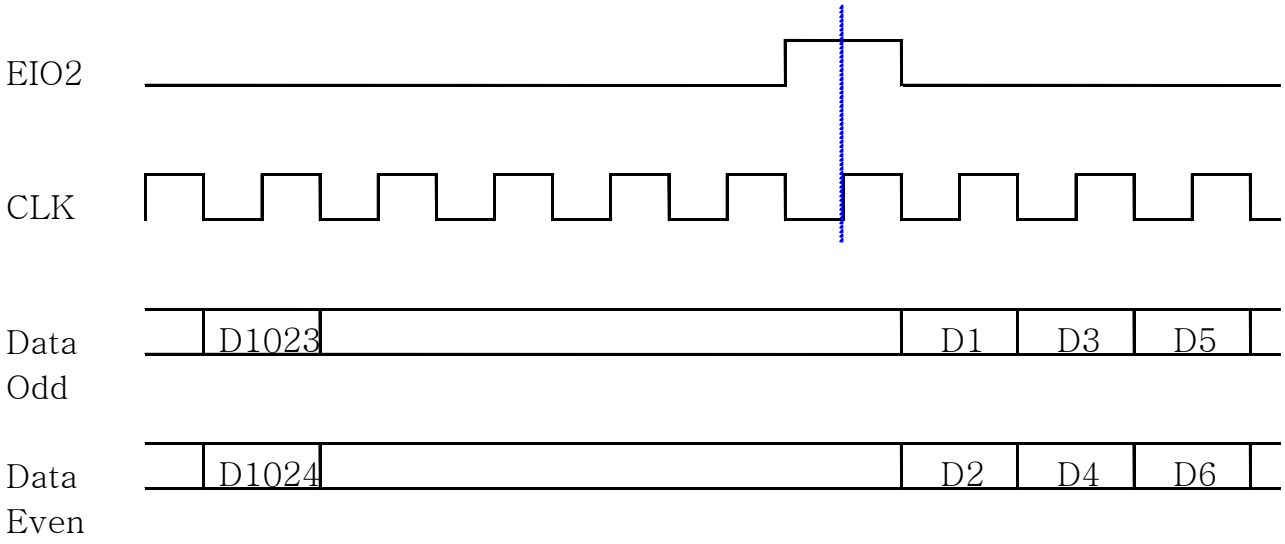


7.2 Recommended timing controller waveforms

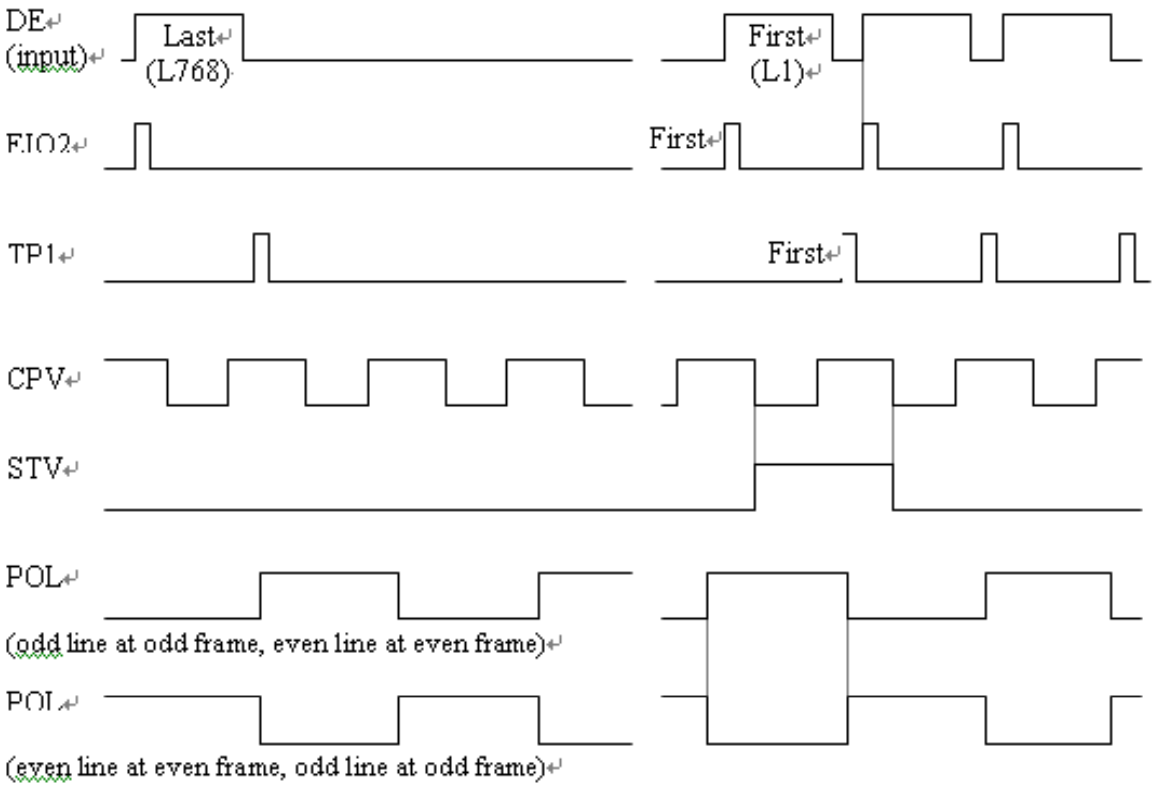
7.2.1. Input Timing Waveforms (Video data from Host)

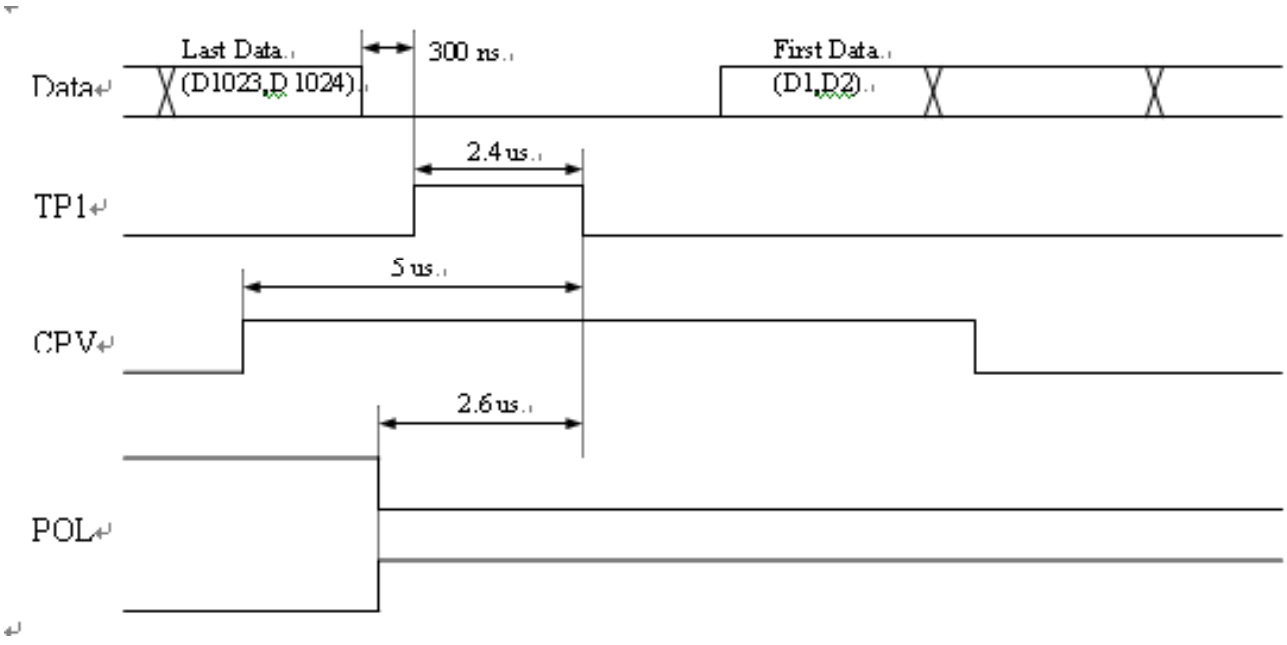


7.2.2 Recommended Output data waveforms (Timing controller to Panel)



7.2.3 Recommended timing controller output waveforms (At 60Hz)





※ The others timing specifications are refered to APPENDIX

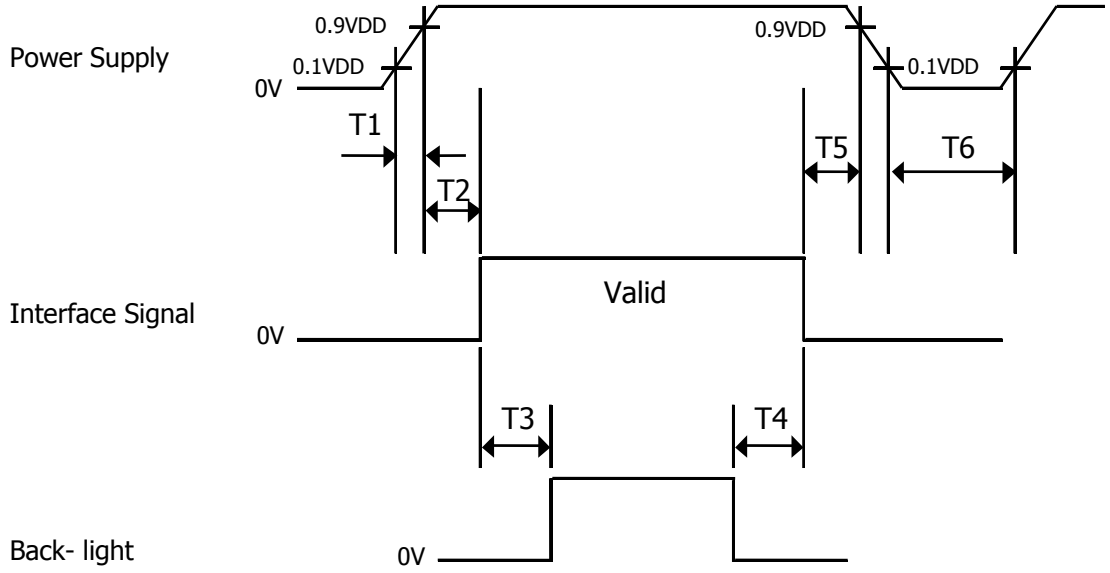
8.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

Each color is displayed in sixty-four gray scales from a 6 bit data signal input. A total of 262,144 colors are derived from the resultant 18 bit data.

Colors & Gray Scale		Red Data						Green Data						Blue Data					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↓						↓						↓					
	▽	↓						↓						↓					
	Brighter	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	△	↓						↓						↓					
	▽	↓						↓						↓					
	Brighter	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	▽	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↓						↓						↓					
	▽	↓						↓						↓					
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Gray Scale Of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1
	Darker	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0
	△	↓						↓						↓					
	▽	↓						↓						↓					
	Brighter	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1
	▽	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.0 Recommended POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below



1) 0 < T1 ≤ 10 ms
2) 0 < T2 ≤ 50 ms
3) 100 ms ≤ T3
4) 100 ms ≤ T4
5) 0 ≤ T5 ≤ 50ms
6) 1 sec ≤ T6

Notes : 1. When the power supply VDD is 0V, Keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.

10.0 HYDIS RELIABLITY TEST

This condition is the internal standard of HYDIS. (This condition is not related to customer evaluation)
HYDIS conducts the test with following reliability temperature which HYDIS could guarantee.

NO	TEST ITEM	CONDITIONS
1	High temperature storage test	Ta = 70°C, 240 hrs
2	Low temperature storage test	Ta = -20°C, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs
4	High temperature operation test	Ta = 70 °C, 240 hrs
5	Low temperature operation test	Ta = 0 °C, 240 hrs
6	Thermal shock	Ta = -20 °C ↔ 60 °C (30 min), 100 cycle

11.0 HANDLING & CAUTIONS

11.1 Cautions when taking out the module

1) Pick the pouch only, when taking out module from a shipping package.

11.2 Cautions for handling the module

1) As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
2) As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
3) As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
4) Do not pull the interface connector in or out while the LCD module is operating.
5) Put the module display side down on a flat horizontal plane.
6) Handle connectors and cables with care.

11.3 Cautions for the operation

1) When the module is operating, do not lose MCLK, DE signals. If any one of these signals were lost, the LCD panel would be damaged.
2) Obey the supply voltage sequence. If wrong sequence were applied, the module would be damaged.

11.4 Cautions for the atmosphere

1) Dewdrop atmosphere should be avoided.
2) Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer-packing pouch and under relatively low temperature atmosphere is recommended.

11.5 Cautions for the module characteristics

1) Do not apply fixed pattern data signal to the LCD module at product aging.
2) Applying fixed pattern for a long time may cause image sticking.

11.6 Other cautions

1) Do not disassemble and/or re-assemble LCD module.
2) Do not re-adjust variable resistor or switch etc.
3) When returning the module for repair or etc, please pack the module not to be broken.
4) We recommend using the original shipping packages.

12.0 APPENDIX

12.1 Drive IC detail specification

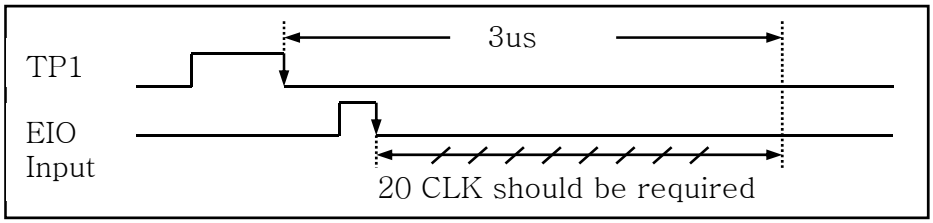
12.1.1. X-Drive IC Function Description

12.1.1.1. Acquisition of image data

EIO2= "H" is acquired at the first CLK rising edge after EIO2 is biased high. After EIO2 is biased low, acquisition of image data into internal latch begins at the next CLK rising edge. Once all data for 384 outputs are input, device become stand-by automatically and it refrains from acquiring more data despite any CLK inputs until input EIO2 again.

12.1.1.2. Remark for EIO and CLK signal input

EIO must be input only one pulse during 1H period.
CLK must be input more than 20 pulses (on XGA driven by 8 chips) from falling edge of EIO input to 3us after falling edge of TP1.



12.1.1.3.Extend Outputs

Connect the EIO1 pin of previous device to the EIO2 pin of the next device and all input pins except EIO1 and EIO2 are connected commonly by each device.

12.1.1.4.Relationship between the input data and output voltage

Output voltage are defined by the input data value and 10γ correction voltage(GMA1-10).
Supporting dot inversion driving, the polarities of input gray scale voltage of even pins and odd pins that Refer to common electrode voltage can be reversed.

(1) γcorrective reference voltage input(GMA1-10)

Should be input externally. Maintain the stable reference voltage during output gray scale voltage.
Refer to "Recommended Operating Conditions" for the order of each voltage.

(1) Image signal data mapping

Data format : 6bit x 2RGB
Input width : 36bit (2 pixels data)

MSB					LSB
Dx5	Dx4	Dx3	Dx2	Dx1	Dx0

12.1.1.5.Relationship between input data and output pins

This relationship is irrespective of L/R condition

Output	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	. . .	OUT384
Data	D00~D05	D10~D15	D20~D25	D30~D35	D40~D45	D50~D55	. . .	D50~D55

12.1.2. Y-Drive IC operation

The output of LCD control (OUT1 to OUT768) are driven "VCOM" or "VEE" level controlled by the input signals (STV,CPV). The STV data is latched and transferred to OUT1 on the rising edge of CPV, and OUT1 data is shifted to OUT2 and new STV data is also transferred to OUT1 on the next rising edge of CPV. In this way, the data is shifted synchronized to the rising edge of CPV.

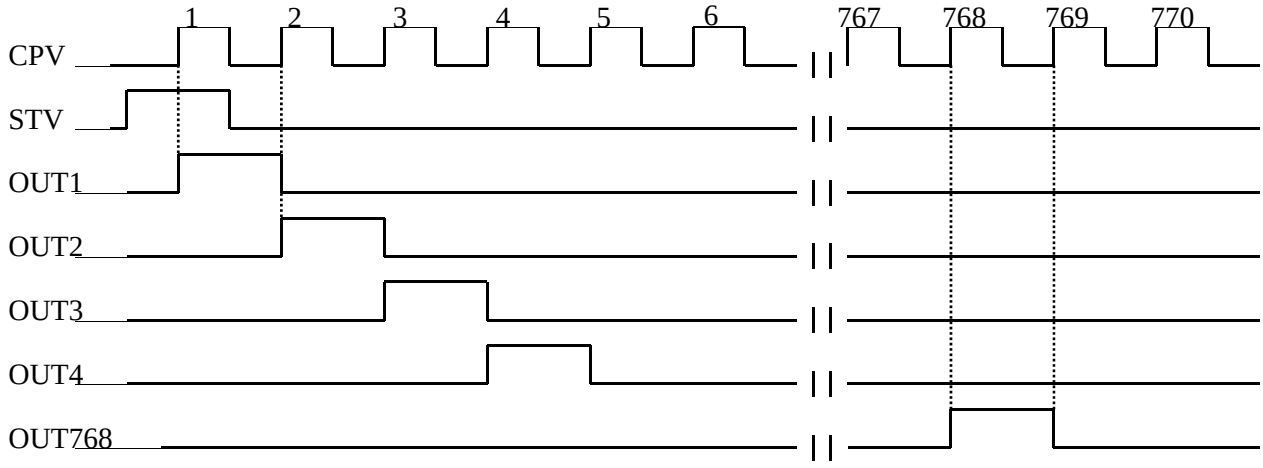
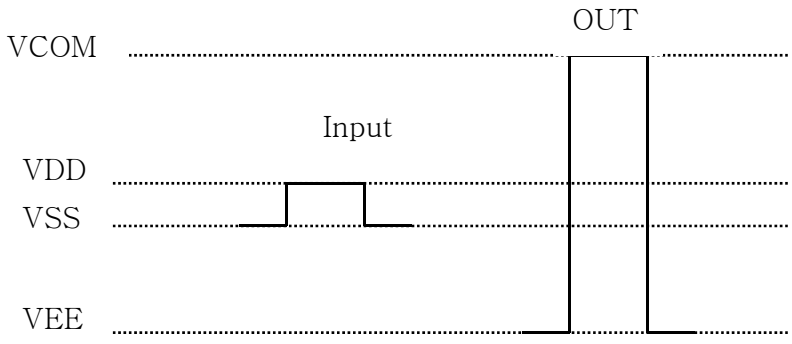


Fig. 12.1.6 Timing Chart

12.1.2.1 LCD control output voltage of Y-Drive IC

The negative voltage output for the liquid crystal control is available. (Example)



The voltage of input signals (CPV, STV) is VSS("L") of VDD("H").
The voltage of output signals (OUT1 ~ OUT768) is VEE or VCOM

12.1.3.Relation between input data and output voltage at X-Drive IC)

12.1.3.1.γcorrection curve

The relationship between input data and γvoltage is shown in below Figure.

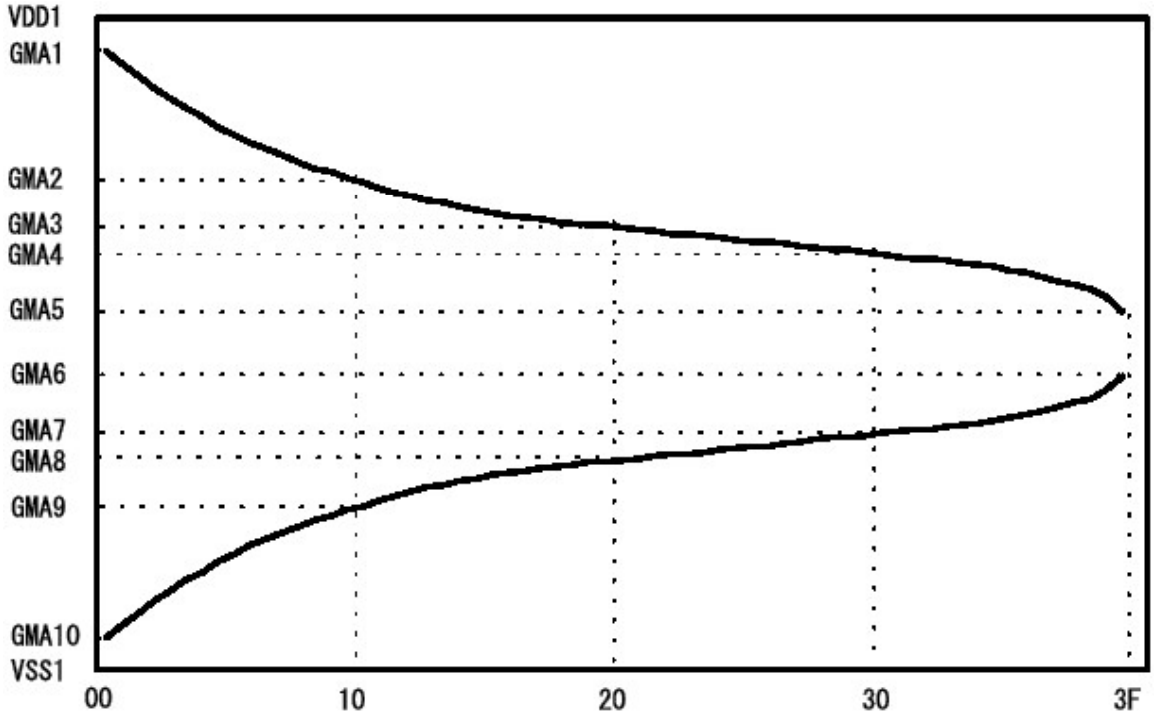


Figure 12.1.3-1 γ correction Curve

12.1.3.2. GMA resistors

Resistors as specified in below table are connected in series to each γcorrection reference power supplies. If γcorrection reference power supply of LCD panel matches each resistance ratio, the parts of GMA external power supplies are not required.

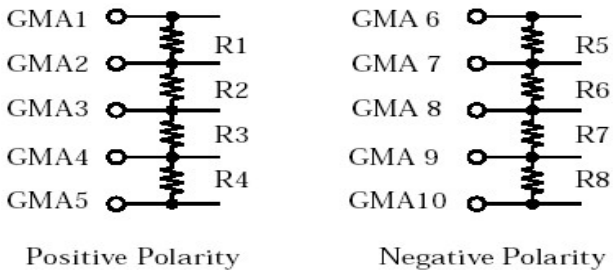


Figure 12.1.3-2 GMA1~GMA10 Connection

Resistor	Ratio
R1、R8	2419
R2、R7	937
R3、R6	697
R4、R5	1547

Table 12.1.3-1 Resistor Ratio

12.1.3.3. Relation between input data and output voltage

The relationship between input data and output voltage that is converted by GMA voltage is shown in below table. The input data are described in Hexa-decimal.

Data(H)	Output Voltage	Data(H)	Output Voltage
00	GMA1	20	GMA3
01	GMA2+(GMA1-GMA2) * 3360/3885	21	GMA4+(GMA3-GMA4) * 1050/1120
02	GMA2+(GMA1-GMA2) * 3010/3885	22	GMA4+(GMA3-GMA4) * 980/1120
03	GMA2+(GMA1-GMA2) * 2695/3885	23	GMA4+(GMA3-GMA4) * 910/1120
04	GMA2+(GMA1-GMA2) * 2415/3885	24	GMA4+(GMA3-GMA4) * 840/1120
05	GMA2+(GMA1-GMA2) * 2170/3885	25	GMA4+(GMA3-GMA4) * 770/1120
06	GMA2+(GMA1-GMA2) * 1925/3885	26	GMA4+(GMA3-GMA4) * 700/1120
07	GMA2+(GMA1-GMA2) * 1680/3885	27	GMA4+(GMA3-GMA4) * 630/1120
08	GMA2+(GMA1-GMA2) * 1435/3885	28	GMA4+(GMA3-GMA4) * 560/1120
09	GMA2+(GMA1-GMA2) * 1225/3885	29	GMA4+(GMA3-GMA4) * 490/1120
0A	GMA2+(GMA1-GMA2) * 1015/3885	2A	GMA4+(GMA3-GMA4) * 420/1120
0B	GMA2+(GMA1-GMA2) * 805/3885	2B	GMA4+(GMA3-GMA4) * 350/1120
0C	GMA2+(GMA1-GMA2) * 630/3885	2C	GMA4+(GMA3-GMA4) * 280/1120
0D	GMA2+(GMA1-GMA2) * 455/3885	2D	GMA4+(GMA3-GMA4) * 210/1120
0E	GMA2+(GMA1-GMA2) * 280/3885	2E	GMA4+(GMA3-GMA4) * 140/1120
0F	GMA2+(GMA1-GMA2) * 105/3885	2F	GMA4+(GMA3-GMA4) * 70/1120
10	GMA2	30	GMA4
11	GMA3+(GMA2-GMA3) * 1400/1505	31	GMA5+(GMA4-GMA5) * 2415/2485
12	GMA3+(GMA2-GMA3) * 1295/1505	32	GMA5+(GMA4-GMA5) * 2345/2485
13	GMA3+(GMA2-GMA3) * 1190/1505	33	GMA5+(GMA4-GMA5) * 2275/2485
14	GMA3+(GMA2-GMA3) * 1085/1505	34	GMA5+(GMA4-GMA5) * 2205/2485
15	GMA3+(GMA2-GMA3) * 980/1505	35	GMA5+(GMA4-GMA5) * 2135/2485
16	GMA3+(GMA2-GMA3) * 875/1505	36	GMA5+(GMA4-GMA5) * 2030/2485
17	GMA3+(GMA2-GMA3) * 770/1505	37	GMA5+(GMA4-GMA5) * 1925/2485
18	GMA3+(GMA2-GMA3) * 665/1505	38	GMA5+(GMA4-GMA5) * 1820/2485
19	GMA3+(GMA2-GMA3) * 560/1505	39	GMA5+(GMA4-GMA5) * 1715/2485
1A	GMA3+(GMA2-GMA3) * 455/1505	3A	GMA5+(GMA4-GMA5) * 1610/2485
1B	GMA3+(GMA2-GMA3) * 350/1505	3B	GMA5+(GMA4-GMA5) * 1470/2485
1C	GMA3+(GMA2-GMA3) * 280/1505	3C	GMA5+(GMA4-GMA5) * 1295/2485
1D	GMA3+(GMA2-GMA3) * 210/1505	3D	GMA5+(GMA4-GMA5) * 1120/2485
1E	GMA3+(GMA2-GMA3) * 140/1505	3E	GMA5+(GMA4-GMA5) * 735/2485
1F	GMA3+(GMA2-GMA3) * 70/1505	3F	GMA5

Table Table 12.1.3-2 Positive polarity (Data00~3F)

Data(H)	Output Voltage	Data(H)	Output Voltage
00	GMA10	20	GMA8
01	GMA10+(GMA9-GMA10)*525/3885	21	GMA8+(GMA7-GMA8) * 70/1120
02	GMA10+(GMA9-GMA10)*875/3885	22	GMA8+(GMA7-GMA8) * 140/1120
03	GMA10+(GMA9-GMA10)*1190/3885	23	GMA8+(GMA7-GMA8) * 210/1120
04	GMA10+(GMA9-GMA10)*1470/3885	24	GMA8+(GMA7-GMA8) * 280/1120
05	GMA10+(GMA9-GMA10)*1715/3885	25	GMA8+(GMA7-GMA8) * 350/1120
06	GMA10+(GMA9-GMA10)*1960/3885	26	GMA8+(GMA7-GMA8) * 420/1120
07	GMA10+(GMA9-GMA10)*2205/3885	27	GMA8+(GMA7-GMA8) * 490/1120
08	GMA10+(GMA9-GMA10)*2450/3885	28	GMA8+(GMA7-GMA8) * 560/1120
09	GMA10+(GMA9-GMA10)*2660/3885	29	GMA8+(GMA7-GMA8) * 630/1120
0A	GMA10+(GMA9-GMA10)*2870/3885	2A	GMA8+(GMA7-GMA8) * 700/1120
0B	GMA10+(GMA9-GMA10)*3080/3885	2B	GMA8+(GMA7-GMA8) * 770/1120
0C	GMA10+(GMA9-GMA10)*3255/3885	2C	GMA8+(GMA7-GMA8) * 840/1120
0D	GMA10+(GMA9-GMA10)*3430/3885	2D	GMA8+(GMA7-GMA8) * 910/1120
0E	GMA10+(GMA9-GMA10)*3605/3885	2E	GMA8+(GMA7-GMA8) * 980/1120
0F	GMA10+(GMA9-GMA10)*3780/3885	2F	GMA8+(GMA7-GMA8) * 1050/1120
10	GMA9	30	GMA7
11	GMA9+(GMA8-GMA9) * 105/1505	31	GMA7+(GMA6-GMA7) * 70/2485
12	GMA9+(GMA8-GMA9) * 210/1505	32	GMA7+(GMA6-GMA7) * 140/2485
13	GMA9+(GMA8-GMA9) * 315/1505	33	GMA7+(GMA6-GMA7) * 210/2485
14	GMA9+(GMA8-GMA9) * 420/1505	34	GMA7+(GMA6-GMA7) * 280/2485
15	GMA9+(GMA8-GMA9) * 525/1505	35	GMA7+(GMA6-GMA7) * 350/2485
16	GMA9+(GMA8-GMA9) * 630/1505	36	GMA7+(GMA6-GMA7) * 455/2485
17	GMA9+(GMA8-GMA9) * 735/1505	37	GMA7+(GMA6-GMA7) * 560/2485
18	GMA9+(GMA8-GMA9) * 840/1505	38	GMA7+(GMA6-GMA7) * 665/2485
19	GMA9+(GMA8-GMA9) * 945/1505	39	GMA7+(GMA6-GMA7) * 770/2485
1A	GMA9+(GMA8-GMA9) * 1050/1505	3A	GMA7+(GMA6-GMA7) * 875/2485
1B	GMA9+(GMA8-GMA9) * 1155/1505	3B	GMA7+(GMA6-GMA7) * 1015/2485
1C	GMA9+(GMA8-GMA9) * 1225/1505	3C	GMA7+(GMA6-GMA7) * 1190/2485
1D	GMA9+(GMA8-GMA9) * 1295/1505	3D	GMA7+(GMA6-GMA7) * 1365/2485
1E	GMA9+(GMA8-GMA9) * 1365/1505	3E	GMA7+(GMA6-GMA7) * 1750/2485
1F	GMA9+(GMA8-GMA9) * 1435/1505	3F	GMA6

Table 12.1.3-3 Negative polarity (Data00~3F)

12.1.4. Electrical Characteristics

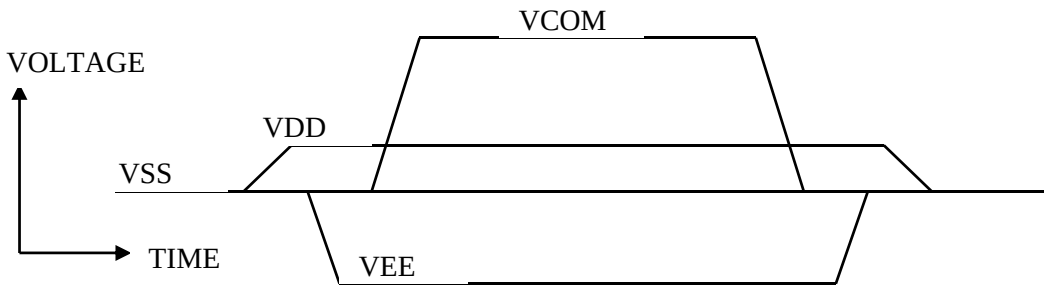
Basically, the ground-level voltage is VSS=VSS1=VSS2=GND=0V.

12.1.4.1. Absolute maximum rating over operating free-air temperature (unless otherwise noted)

	Parameter	Applied Port	Rating	Unit
X-Drive IC	Supply Voltage at Logic Port	VDD2	-0.5 to + 5.0	V
	Supply Voltage at Driver Port	VDD1	-0.5 to + 12.0	V
	Input Voltage	GMA1 to GMA10	-0.5 to VDD1 + 0.5	V
		Except GMA	-0.5 to VDD2 + 0.5	V
	Output Voltage	EIO1, EIO2	-0.5 to VDD2 + 0.5	V
		OUT1 to OUT3072	-0.5 to VDD1 + 0.5	V
Y-Drive IC	Power Supply	VDD	-0.3 to + 7.0	V
	Power Supply	VCOM	-0.3 to + 40.0	V
	Power Supply	VEE	-20.0 to + 0.3	V
	Power Supply	VCOM-VEE	-0.3 to VDD + 0.3	V
Storage Temperature (Tstg)			-55 to 125	°C

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these of any other conditions beyond those indicated under recommended operation conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Keep the power on sequence of VDD2, Control input, VDD1 and GMA1 to GMA10.
During power off, this must be reversed.

The order of power on is VDD→VEE→Input signal→VCOM and the order of power off is reverse as shown below figure.



12.1.4.2. Operating condition

	Parameter	Applied Port	Condition	Min.	Typ.	Max.	Unit
X-DriveIC	Supply Voltage	VDD1		6.5		10.5	V
	Supply Voltage	VDD2		3.0		3.6	V
	γ-corrected Supply Voltage	GMA1 ~ GMA5	Note	1/2VDD1		VDD1-0.2	V
		GMA6 ~ GMA10		VSS1+0.2		1/2VDD1	V
	CLK Frequency	CLK				70	MHz
	Output Load Capacitance (CL)	OUT1 ~ OUT3072				75	pF
Y-DriveIC	Power Supply	VDD		3.0	3.3	3.6	V
	Power Supply	VCOM		10		25	V
	Power Supply	VEE		-15		-5	V
	Power Supply	VCOM-VEE		17		35	V
	CPV Frequency	CPV				150	KHz
Operating free-air Temperature Range				-10		75	°C

Note : Relation of γ-corrected input voltage
VDD1>GMA1, GMn ≥GMAn+1 (n=1 to 9), GMA10>VSS1

12.1.4.3. DC characteristics of X-Drive IC

Parameter	Applied port	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level Input Voltage	D00~D05,D10~D15, D20~D25,D30~D35,	VIH1		0.7VDD2		VDD2	V
Low-level Input Voltage	D40~D45,D50~D55, CLK,TP1,REV1,	VIL1		0		0.3VDD2	V
Input Leakage Current	REV2,EIO1,EIO2, POL,LP,RS(LCH)	IIL		-1		1	uA
Output Current *1)	OUT1~OUT3072	ICHG	Vx=VDD1-0.2V Vout=Vx-1.0V VDD1=6.5V		-200	-150	uA
		IDIS	Vx=VSS1+0.2V Vout=Vx+1.0V VDD1=6.5V	150	210		
Output Voltage Pin to Pin Deviation *2)	OUT1~OUT3072	ΔVO	*4)		±5	±15	mV
			*5)		±13	±25	
Average Output Voltage Variation *3)	OUT1~OUT3072	ΔVA			±10		mV

<Note>

*1) Vx=Output Voltage(Out1~Out3072), Vout=Output pin voltage during measurement
*2) Define as the deviation among pins of positive and negative polarities amplitude difference during same data output on all pins.
*3) Define ad the variation of output voltage deviation ΔVO averages among chips.
4) Vout=VDD1-0.2V to VDD1(1/2)+0.5V, VSS1+0.2V to VDD1*(1/2)-0.5V
5) Vout=VDD1(1/2)+0.5V to VDD1*(1/2)-0.5V

Total Gamma Resistance	GMA1~GMA5 GMA6~GMA10	RGMA		2800	5600	8400	Ω
Output Voltage Dynamic Range	OUT1 ~ OUT3072	VOUT		VSS1+0.2		VDD1-0.2	V
Driver Port Dynamic Current Consumption	VDD1-VSS1	Didd1	*6)		1.0	3	mA
Driver Port Static Current Consumption	VDD1-VSS1	Sidd1	*7)		0.1	0.4	mA
Logic Port Dynamic Current Consumption	VDD2-VSS2	Didd2	*8)		2	3	mA
Logic Port Static Current Consumption	VDD2-VSS2	Sidd2	*9)		1	7	uA

<Note>

*6) TP1=20uS, fCLK=36MHz, No output Load, VDD1=10.5V,
Black raster display, GMA1=10.3V, GMA10=0.2V
*7) No output Load, VDD1=10.5V, Black raster display, GMA1=10.3V, GMA10=0.2V
*8) TP1=20uS, fCLK=36MHz, Dot checkerboard display
*9) Stop clock and input signals, VDD2=3.6V

12.1.4.4. DC characteristics of Y-Drive IC

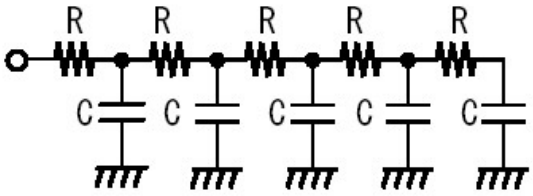
Item	Symbol	Condition	Min	Typ	Max	Unit	Terminal
"0" Input Voltage	VIL		VSS		0.1*VDD	V	All Input Terminals
"1" Input Voltage	VIH		0.9*VDD		VDD	V	All Input Terminals
"0" Input Voltage	VOL	IOL=40uA	VSS		0.25	V	STV
"1" Input Voltage	VOH	IOH=40uA	VDD-0.25		VDD	V	STV
"0" Input Resistance	ROL	Vout=VEE+0.5V			500	Ω	OUT1~ OUT263
"1" Input Resistance	ROH	Vout=Vcom-0.5V			500	Ω	OUT1~ OUT263
Input Current	Iin		-5.0		+5.0	uA	All Input Terminals

12.1.4.5. AC characteristics of X-Drive IC

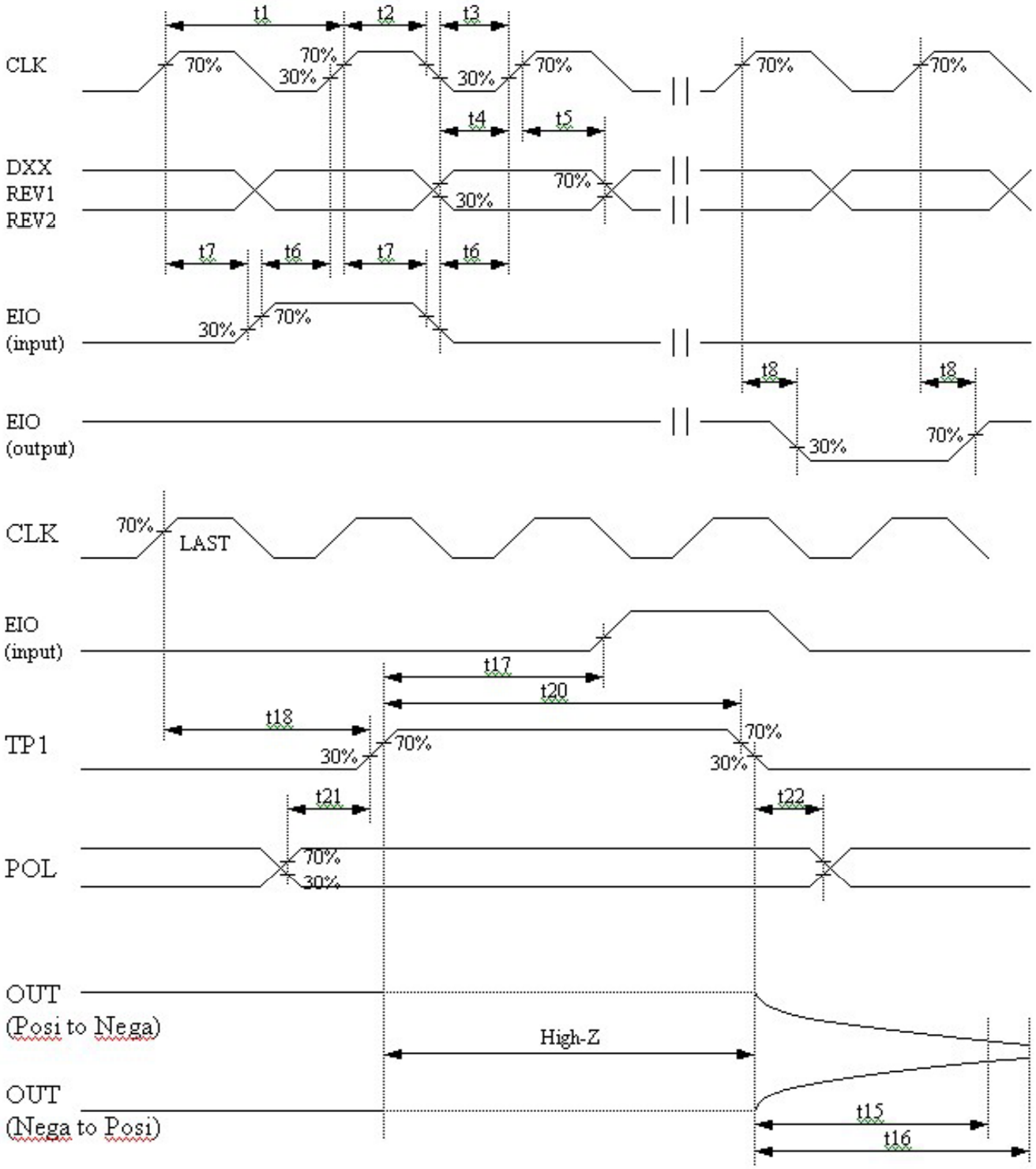
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK Cycle Time	t1		14			nS
CLK High Time	t2		2.0			nS
CLK Low	t3		2.0			nS
Data to REV Setup Time	t4		2.0			nS
Data to REV Hold Time	t5		0			nS
Start Pulse Setup Time	t6		2.0			nS
Start Pulse Hold Time	t7		0			nS
Start Pulse Signal Delay Time	t8	CL=25pF			88	nS
Driver Output Delay Time-1	t15	CL=75pF R=5 kΩ (Note1 & 3)			8	uS
Driver Output Delay Time-1	t16	CL=75pF R=5 kΩ (Note2 & 3)			10	uS
TP1 Signal to EIO(input) Signal Setup Time	t17		5			CLK cycle
Last data CLK to TP1(L) Hold Time	t18		2			CLK cycle
TP1 Signal High Time	t20		400			nS
POL TP1 Signal Setup Time	t21		-5			nS
POL TP1 Signal Hold Time	t22		6.0			nS

Note1) The period that driver output voltage reaches ±(VDD1*0.1) of expected output voltage.
Note2) The period that driver output voltage reaches expected output voltage with 6-bit accuracy.
Note3) Output load condition is defined below schematic.

R = 1KΩ
C = 15pF



12.1.4.6. X-Drive IC Timing Chart

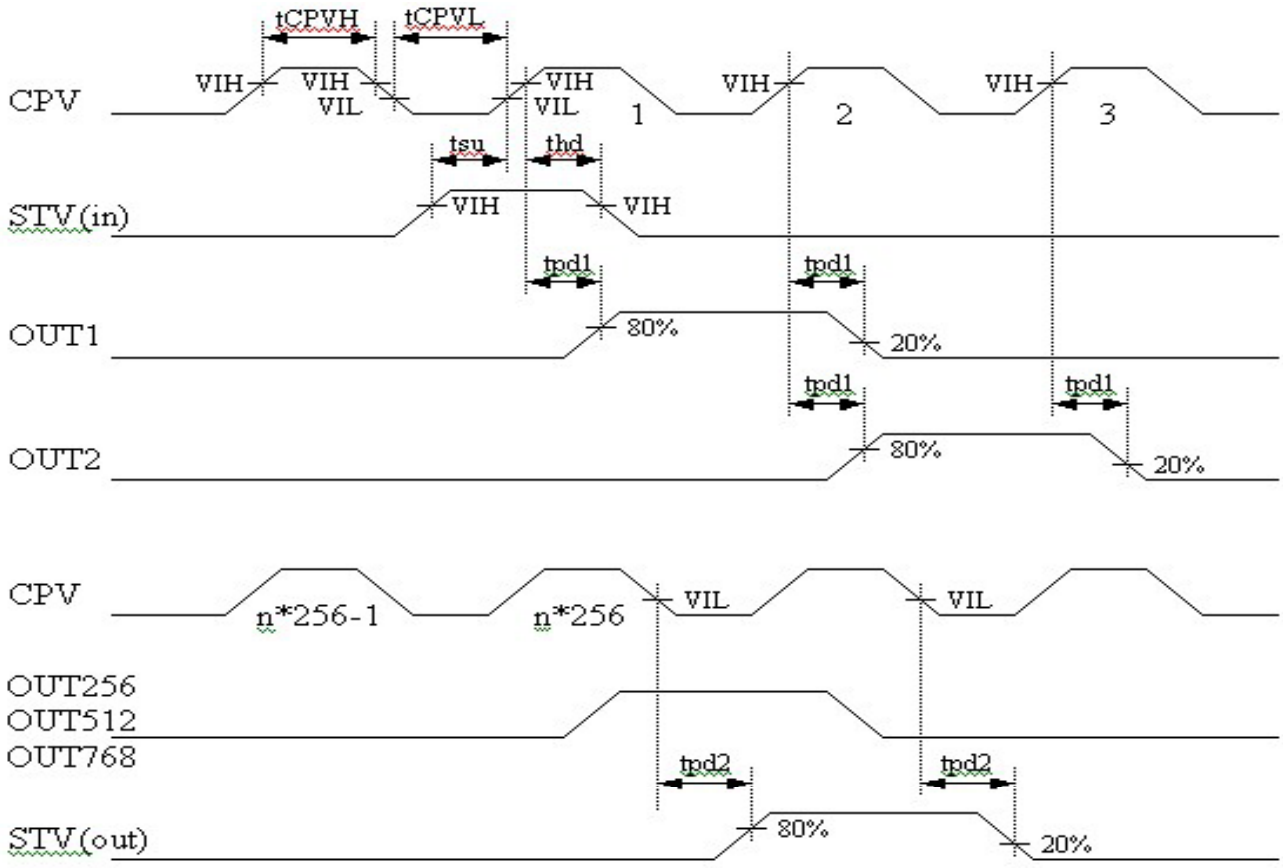


12.1.4.7. AC characteristics of Y-Drive IC

Item	Symbol	Condition	Min	Max	Unit
Operating Frequency	fCP			100	kHz
CPV Clock Pulse Width	tCPVH, tCPVL		1		us
Data Set Up Time	tsu		700		ns
Data Hold Time	thd		700		ns
Output Delay Time1	tpd1	CL=300pF			ns
Output Delay Time2	tpd2	CL=30pF			ns

Measurement condition : Input = VIL/VIH
Output = 20%/80%

12.1.4.8. Y-Drive IC Timing Chart



12.2 HYDIS Test Method

Figure 1. Measurement Set Up

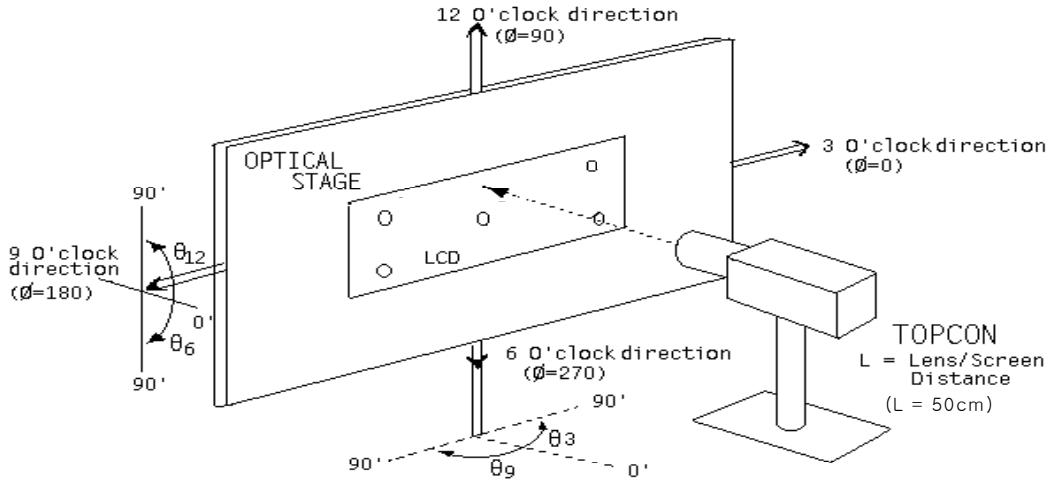


Figure 2. Average Luminance Measurement Locations & Uniformity Measurement Locations

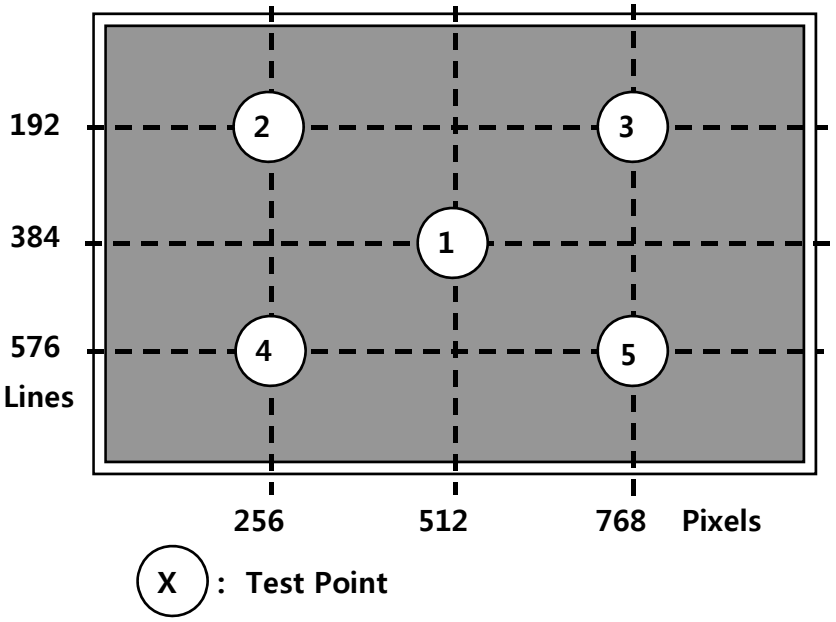


Figure 3. Response Time Testing

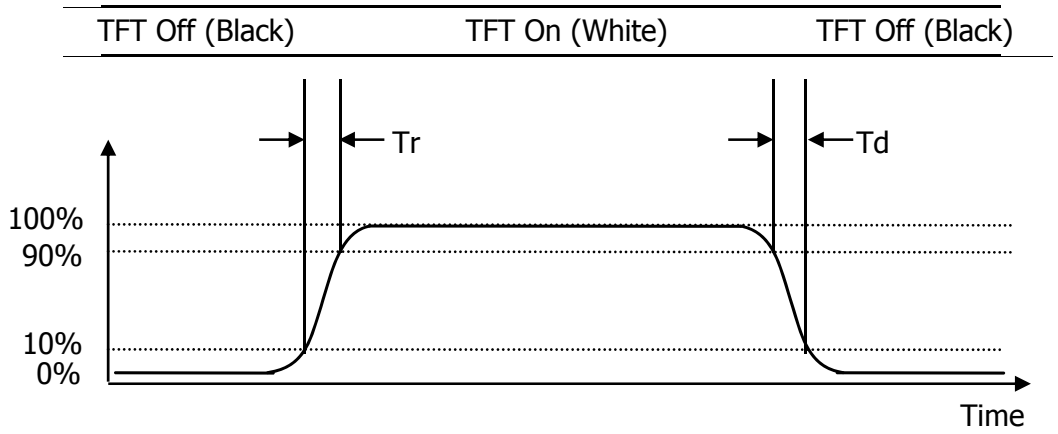
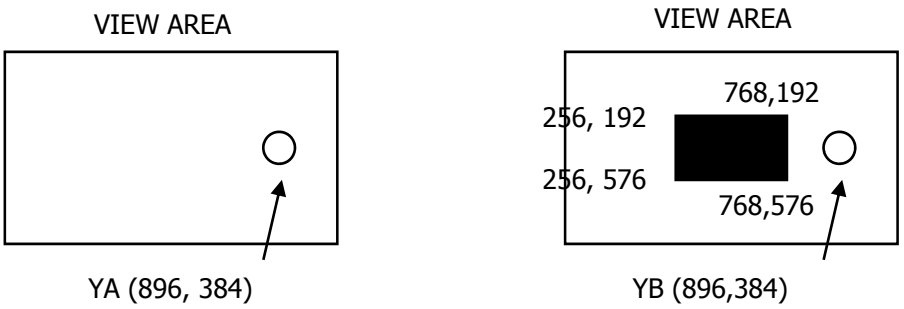


Figure 4. Cross Modulation Test Description



$$\text{Cross-Talk} = \left| \frac{YB - YA}{YA} \right| \times 100$$

Where: Y_A = Initial luminance of measured area (cd/m^2)

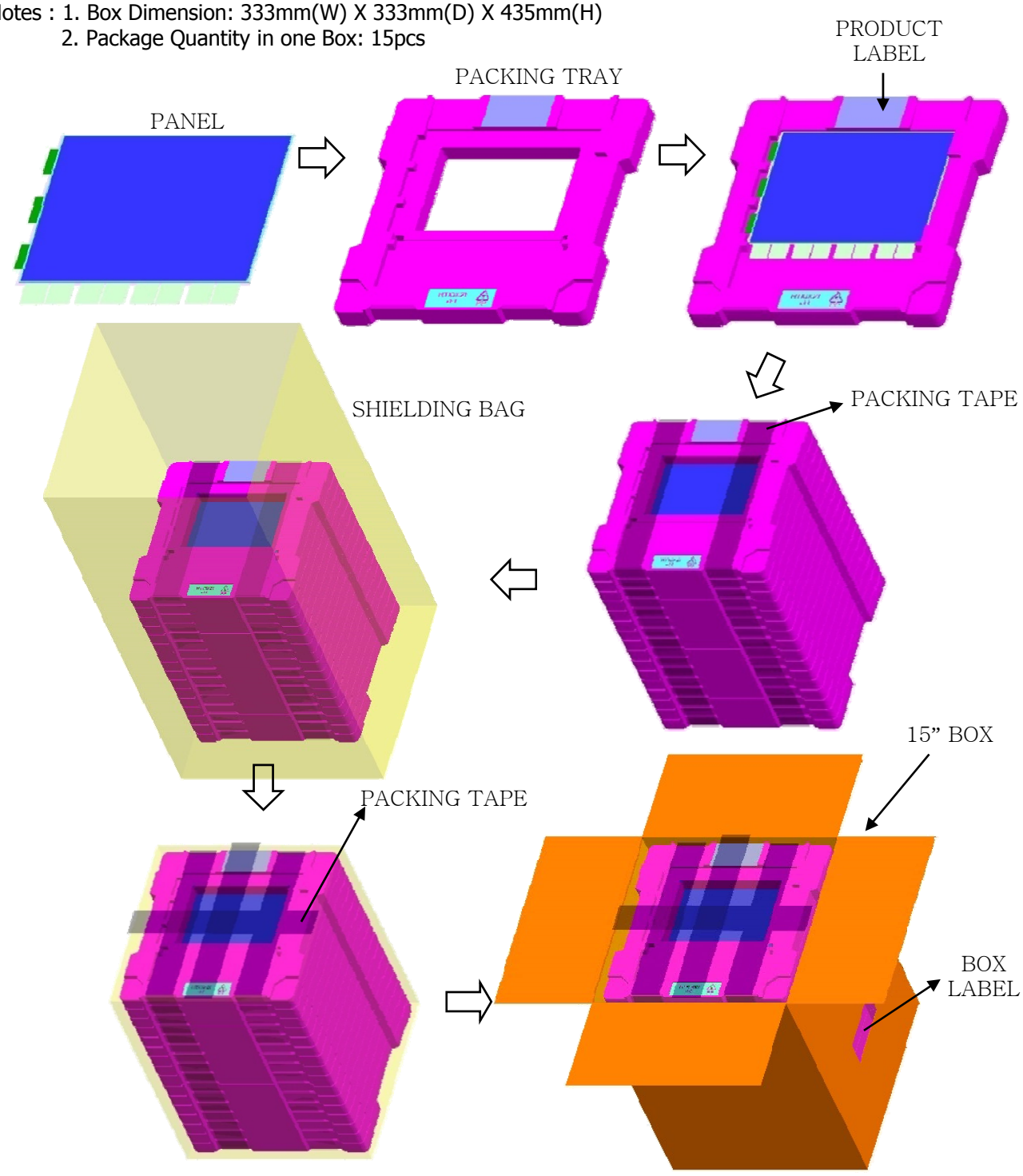
Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns.

13.0 PACKING

13.1 Packing Order

Notes : 1. Box Dimension: 333mm(W) X 333mm(D) X 435mm(H)
2. Package Quantity in one Box: 15pcs

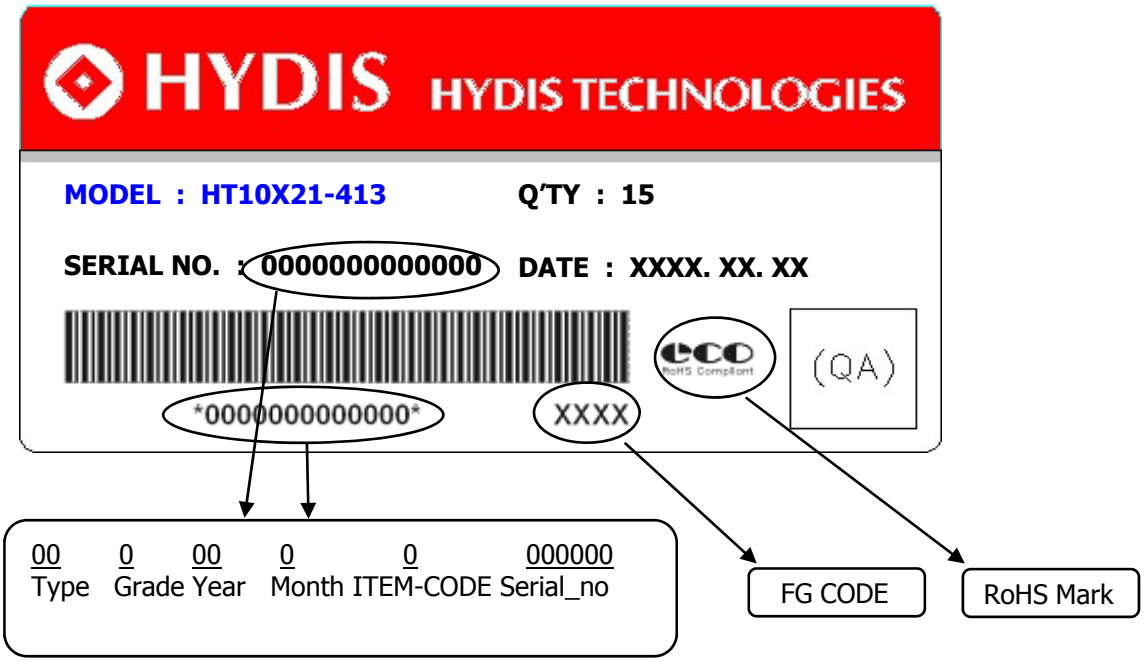


14.0 Environment & Safety

14.1 Packing Label

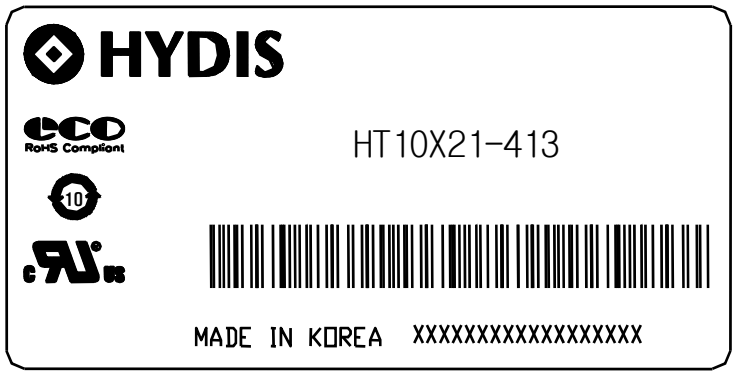
1) Label Size: 108 mm (L) × 56 mm (W)

2) Contents
Model : HT10X21-413 TFT-LCD
Q`ty : Q'ty in one box
Serial No. : Box Serial No. See next figure for detail description.
Date : Packing Date
FG Code : FG Code of Product



14.3 Product Label

1) Picture



1	2	3	4	5	6	7
X X	X	X	X X	X	X X X X	X X X X X X

2) HYDIS Barcode

No 1. Control Number

No 2. Rank / Grade

No 3. Line Classification (HYDIS : H)

No 4. Year (5 : 2005, 6 : 2006, …)

No 5. Month (1, 2, 3,…, 9, X, Y, Z)

No 6. FG Code

No 7. Serial Number

15.0 TFT-LCD Panel Outline Dimension (Front view)