HT1608
2×20 Channel LCD Driver

Features

- Power supply
  - +5V for internal logic circuit
  - –5V for LCD driver circuit
- 40 internal LCD drivers available
- Bias voltage: static to 1/5 bias
- LCD driver with serial/parallel conversion function
- Common or segment driver output by selection

Applications

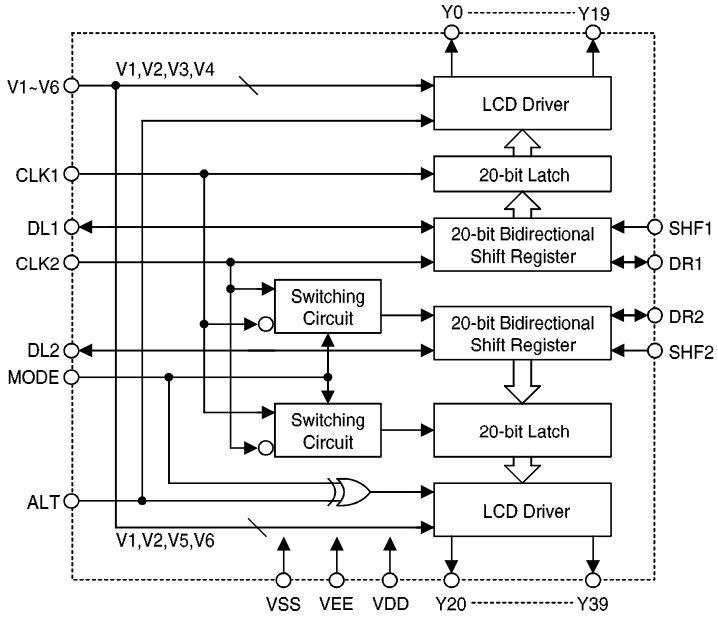
- Electrical dictionaries
- Portable computers
- Remote controllers
- Calculators

General Description

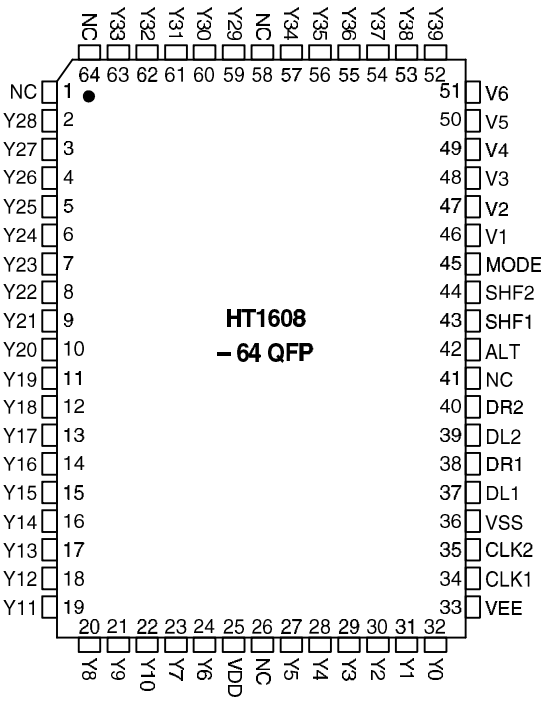
The HT1608 is an LCD driver LSI with 40 output channels using the CMOS technology. It is equipped with two sets of 20-bit bidirectional shift registers, 20-bit data latches, 20-bit LCD drivers, and logic control circuits. The LSI can convert serial data received from an LCD controller into parallel data and supply LCD driving waveforms to the LCD panel.

The HT1608 is designed for general purpose LCD drivers. It can drive both static and dynamic drive LCDs. The LSI can be applied to either a common driver or a segment driver.

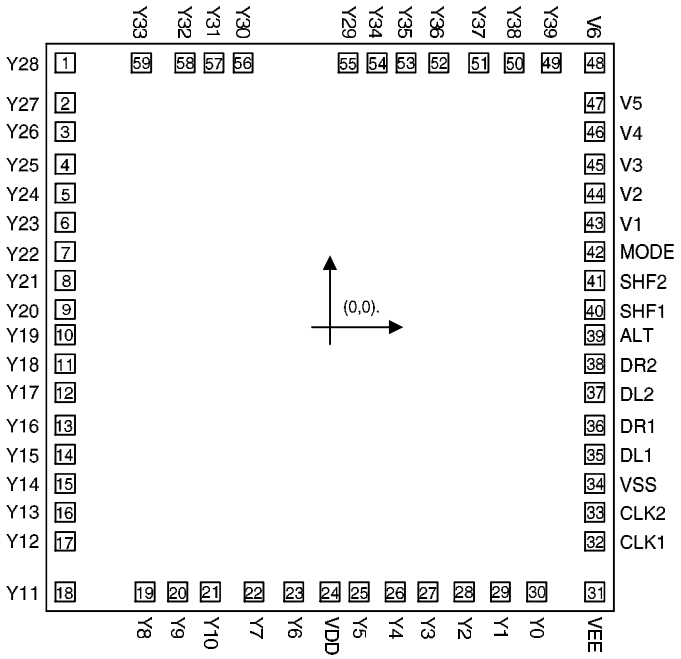
Block Diagram



64 QFP package



Pad Coordinates



Chip size: 160×159 (mil)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Unit: mil

Pad No.	X	Y	Pad No.	X	Y	Pad No.	X	Y
1	−73.80	73.22	21	−33.57	−73.22	41	73.80	13.50
2	−73.80	62.10	22	−21.42	−73.22	42	73.80	21.60
3	−73.80	54.00	23	−10.94	−73.22	43	73.80	29.70
4	−73.80	45.90	24	0.81	−73.22	44	73.80	37.80
5	−73.80	37.80	25	8.19	−73.22	45	73.80	45.90
6	−73.80	29.70	26	18.09	−73.22	46	73.80	54.00
7	−73.80	21.60	27	27.99	−73.22	47	73.80	62.10
8	−73.80	13.50	28	37.89	−73.22	48	73.80	73.22
9	−73.80	5.40	29	47.79	−73.22	49	61.60	73.22
10	−73.80	−2.70	30	57.69	−73.22	50	51.35	73.22
11	−73.80	−10.80	31	73.80	−73.22	51	41.99	73.22
12	−73.80	−18.90	32	73.80	−59.40	52	30.06	73.22
13	−73.80	−27.00	33	73.80	−51.30	53	21.78	73.22
14	−73.80	−35.10	34	73.80	−43.20	54	13.68	73.22
15	−73.80	−43.20	35	73.80	−35.10	55	5.58	73.22
16	−73.80	−51.30	36	73.80	−27.00	56	−24.30	73.22
17	−73.80	−59.40	37	73.80	−18.90	57	−32.40	73.22
18	−73.80	−73.22	38	73.80	−10.80	58	−40.50	73.22
19	−51.03	−73.22	39	73.80	−2.90	59	−52.74	73.22
20	−42.03	−73.22	40	73.80	5.40			

Pad Description

Pad No.	Pad Name	I/O	Note	Description
1~9	Y28~Y20	O		LCD driver outputs for channel 2
10~23	Y19~Y6	O		LCD driver outputs for channel 1
24	VDD			Power supply (positive)
25~30	Y5~Y0	O		LCD driver outputs for channel 1
31	VEE			LCD power supply
32	CLK1	I	Note1	Latch signal for channel 1 on the falling edge CLK1 is used for channel 2 when MODE is set to VSS
33	CLK2	I	Note1	Shift signal for channel 1 on the falling edge and used for channel 2 when MODE is set to VSS
34	VSS			Power supply (ground)
35	DL1	I/O		Data input/output of channel 1 shift register
36	DR1	I/O		Data input/output of channel 1 shift register
37	DL2	I/O		Data input/output of channel 2 shift register
38	DR2	I/O		Data input/output of channel 2 shift register
39	ALT	I		Alternate signal input for LCD driving waveform
40	SHF1	I	Note2	Shift direction selection of channel 1 shift register
41	SHF2	I	Note2	Shift direction selection of channel 2 shift register
42	MODE	I	Note3	Mode select signal of channel 2
43~44	V1,V2	I		LCD bias supply voltage for channels 1 and 2
45~46	V3,V4	I		LCD bias supply voltage for channel 1
47~48	V5,V6	I		LCD bias supply voltage for channel 2
49~59	Y39~Y29	O		LCD driver outputs for channel 2

Note1: Data is processed on the clock falling or rising edge as shown in the following table.

MODE= Lo (VSS)

		Channel 1	Channel 2
CLK1	↑	—	—
	↓	Latch data	Latch data
CLK2	↑	—	—
	↓	Shift data	Shift data

MODE= Hi (VDD)

		Channel 1	Channel 2
CLK1	↑	—	Shift data
	↓	Latch data	—
CLK2	↑	—	Latch data
	↓	Shift data	—

Note2 : Shift direction of channels 1 and 2

Shift Direction of Channel 1 (Channel 2)		
SHF1 (SHF2)	**DL1 (DL2)**	**DR1 (DR2)**
Hi	OUT	IN
Lo	IN	OUT

Note3 :

MODE	Channel 2		ALT Polarity	Purpose
	Latch Data	Shift Data		
Hi	CLK2 ↑	CLK1 ↑	$\overline{ALT}$	for Common drive
Lo	CLK1 ↓	CLK2 ↓	ALT	for Segment drive

The output levels of channels 1 and 2 are decided by the combination of MODE, ALT and latched data. Refer to the following table:

MODE	Latched Data	ALT	Channel 1 (Y0~Y19)	Channel 2 (Y20~Y39)
Hi (VDD)	Hi	Hi	V1	V2
		Lo	V2	V1
	Lo	Hi	V3	V6
		Lo	V4	V5
Lo (VSS)	Hi	Hi	V1	V1
		Lo	V2	V2
	Lo	Hi	V3	V5
		Lo	V4	V6

Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 7V
Storage Temperature..... –50°C to 125°C
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Operating Temperature..... 0°C to 70°C

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

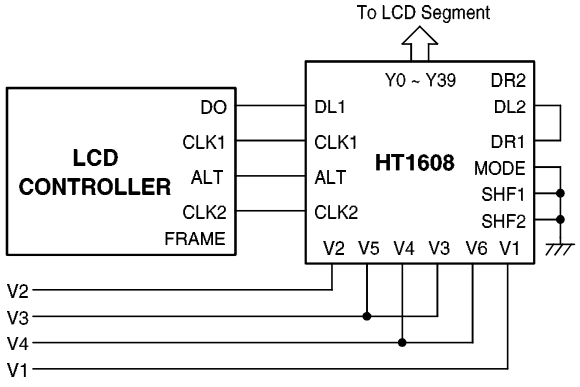
(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	4.5	—	5.5	V
I_{DD}	Operating Current	5V	No load	—	100	300	μA
I_{STB}	Standby Current	5V	—	—	1	5	μA
F_{CLK2}	Data Shift Frequency	5V	—	—	—	400	kHz
tw_{CLK}	Clock Pulse Width	5V	—	800	—	—	ns
V_{IL}	"L" Input Voltage	5V	—	—	—	1	V
V_{IH}	"H" Input Voltage	5V	—	4	—	—	V
V_{OL}	"L" Output Voltage	5V	I_{OL}=+0.4mA	—	—	0.4	V
V_{OH}	"H" Output Voltage	5V	I_{OH}=–0.4mA	4.6	—	—	V
V_{LCD}	LCD Driving Voltage	—	V_{DD}–V_{EE}	5	—	12	V

Functional Description

Both Channels 1 and 2 used as segment drivers (MODE=Lo)

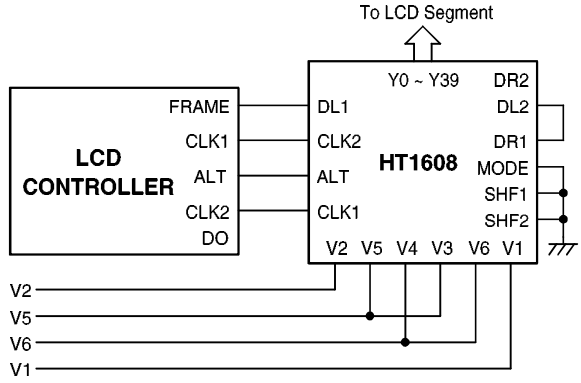
When both channels 1 and 2 of the HT1608 are used as segment drivers, they will shift data on the falling edge of CLK2 and shift latch data on the falling edge of CLK1. V3 &V5 or V4 &V6 are shortened in the application circuit as shown in the following figure.



Note: V1, V2: Selection levels for both segment & common application
V3, V4: Non-selection levels for segment application

Both Channels 1 and 2 used as common drivers (MODE=Lo)

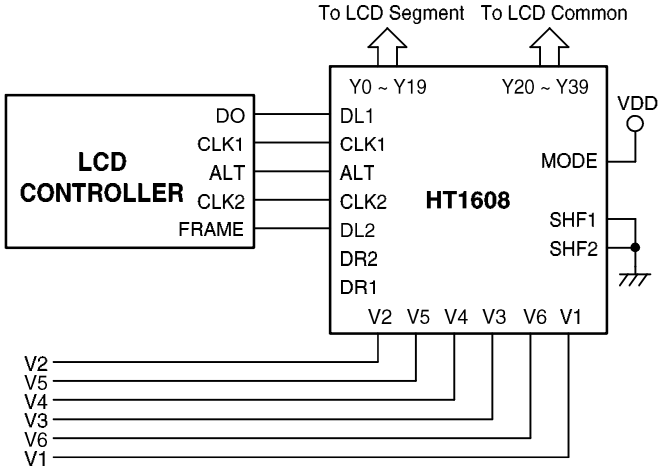
When both channels 1 and 2 of the HT1608 are used as common drivers, the MODE is set low and the signals (CLK1, CLK2, FRAME) from the controller are connected as shown in the following figure.



Note: V1, V2: Selection levels for both segment & common application
V5, V6: Non-selection levels for segment application

Channel 1 used as a segment driver and channel 2 as a common driver (MODE=Hi)

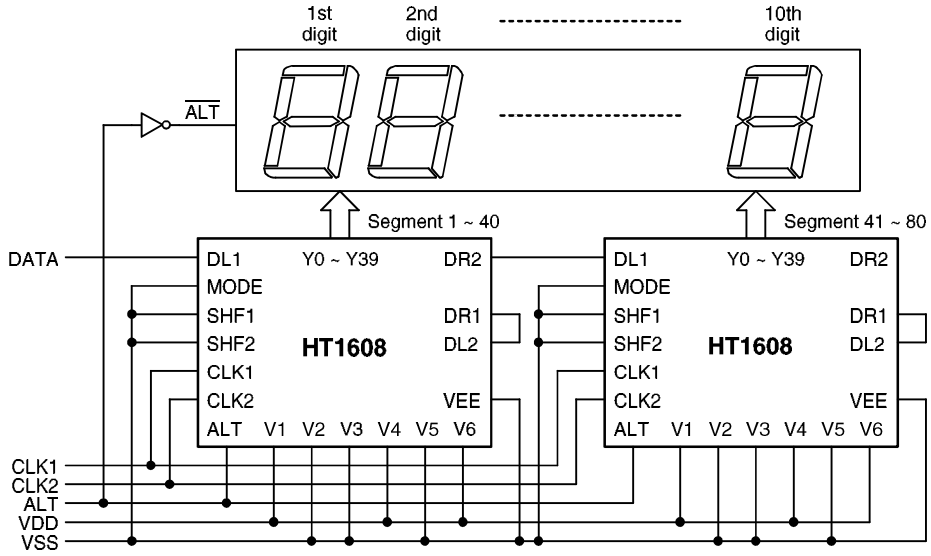
When channel 2 is used as a common driver, MODE is connected to VDD. Channel 2 will shift data on the rising edge of CLK1 and shift latch data on the rising edge of CLK2.



Static Drive

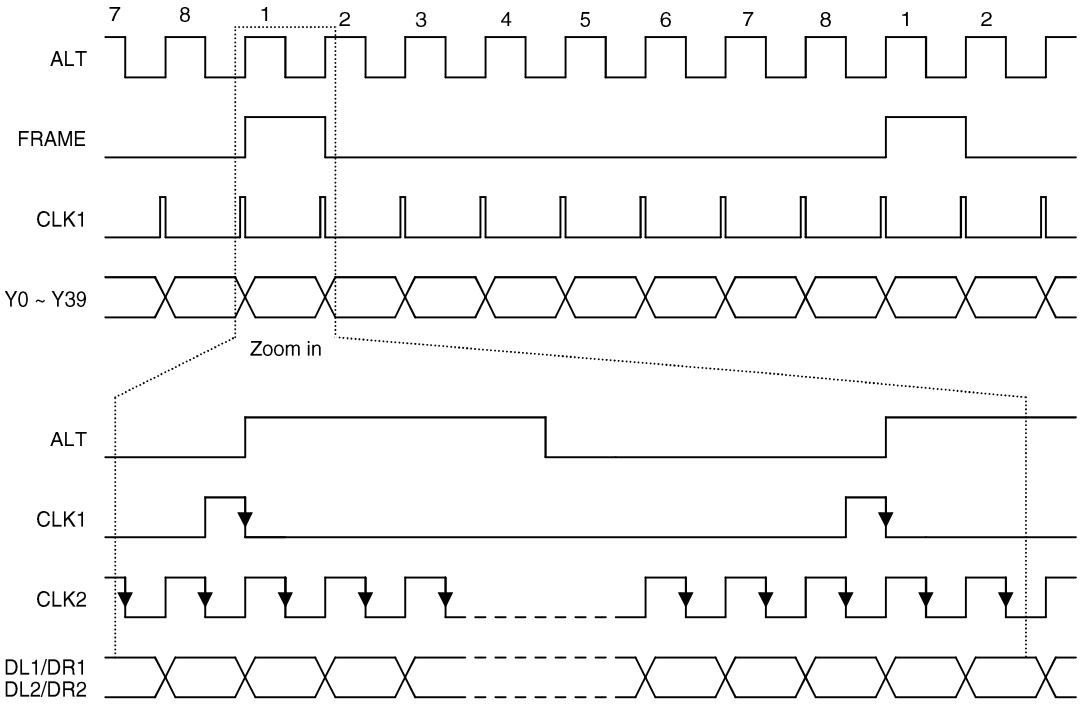
When the HT1608 is used as a static driver, data is transferred on the falling edge of CLK2 and latched on the falling edge of CLK1. The frequency of CLK1 becomes the frame frequency of the LCD driver. The frequency of ALT has to be twice the frequency of CLK1. ALT has to be synchronized on the falling edge of CLK1.

The power supply for the LCD driver is used by shortening V1, V4 and V6 or V2, V3 and V5. One of the LCD output terminals can be used as a common output. The application circuit connections are shown below:

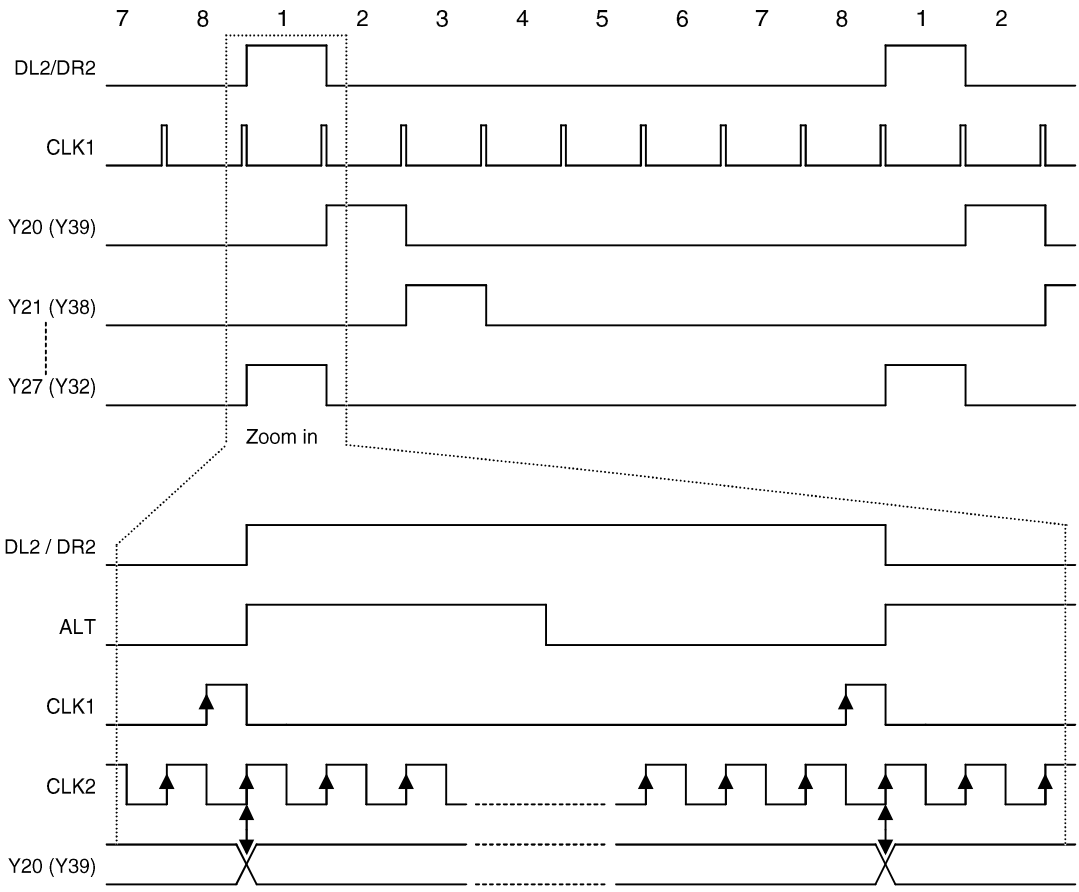


Timing Diagram

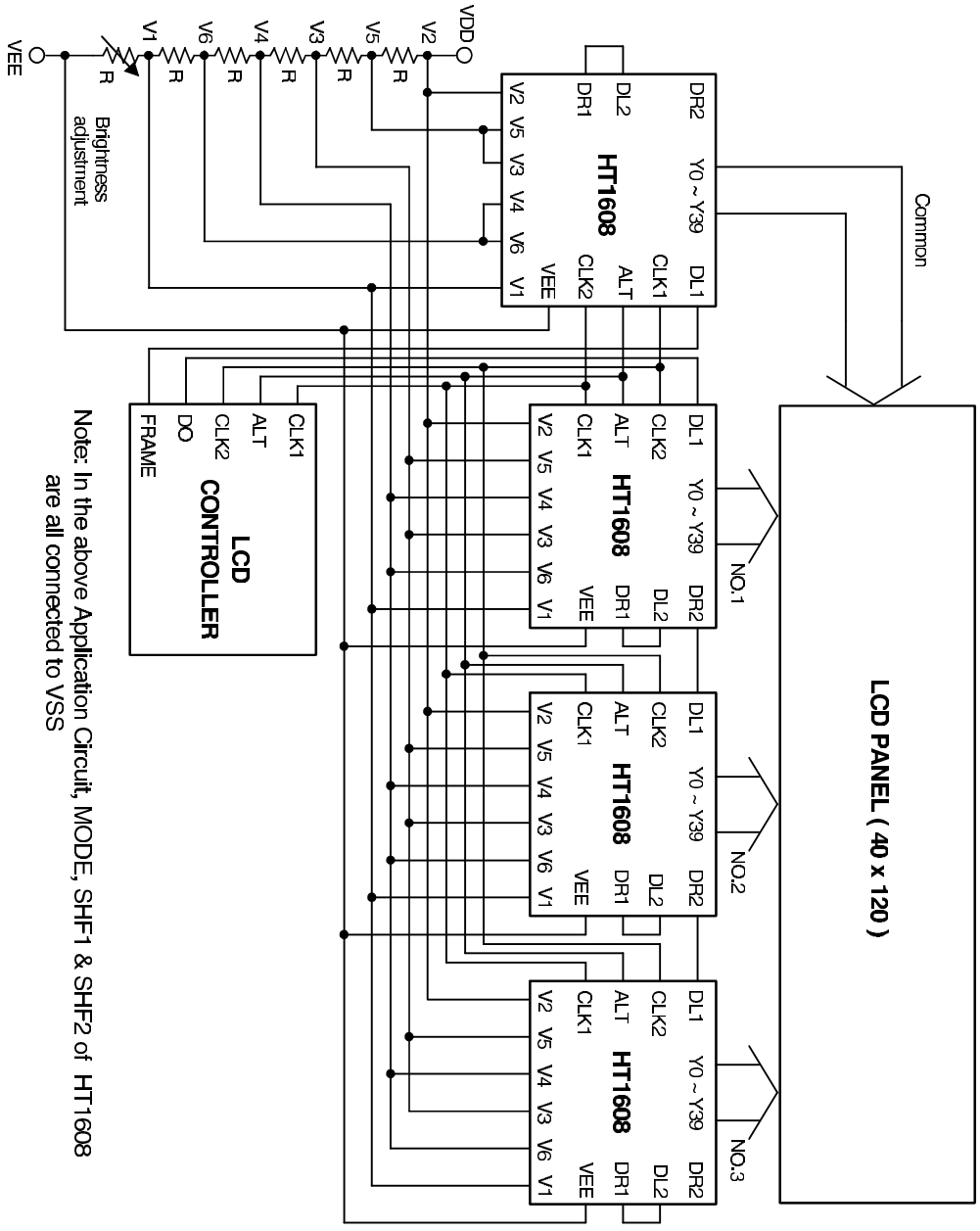
Segment data waveform (1/8 duty)



Common data waveform (A typical waveform of channel 2 as a COMMON driver, 1/8 duty)



Application Circuit



Note: In the above Application Circuit, MODE, SHF1 & SHF2 of HT1608 are all connected to VSS