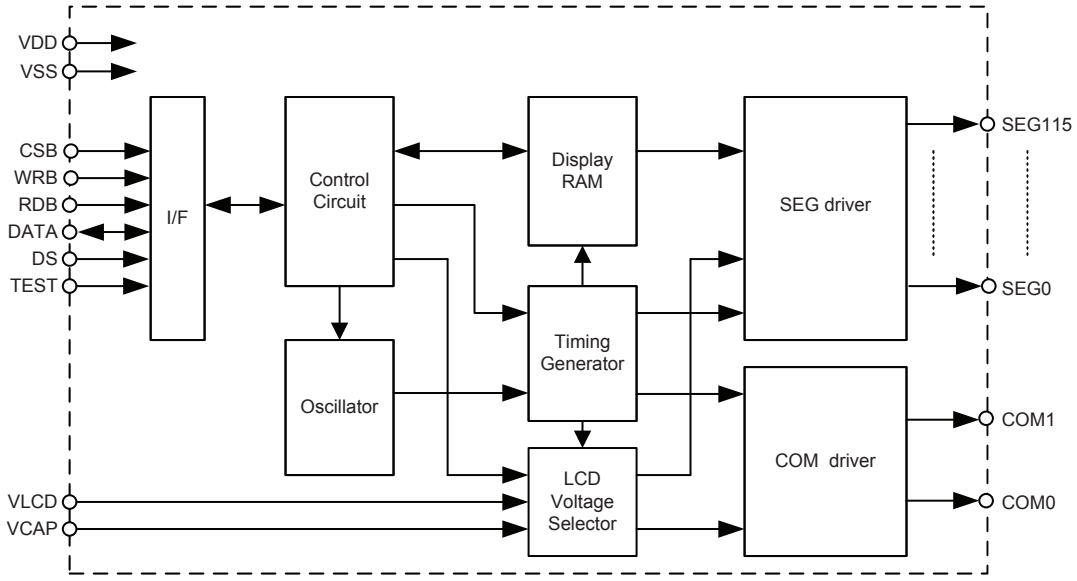
Features

- Logic voltage: 2.4V~5.5V
- LCD operating voltage (V_{LCD}): 2.4V~5.5V
- LCD display: 2 commons, 116 segments
- Support a maximum of 58×4 bit Display RAM
- Duty: Static, 1/2; Bias: 1/1, 1/2
- Internal resistor type bias generator
- Internal RC oscillator
- Software configuration features
- R/W address auto increment
- Data mode and Command mode instructions
- Three data accessing modes
- Power down command reduces power consumption
- 4-wire serial interface
- Package type: 128-pin LQFP and chip

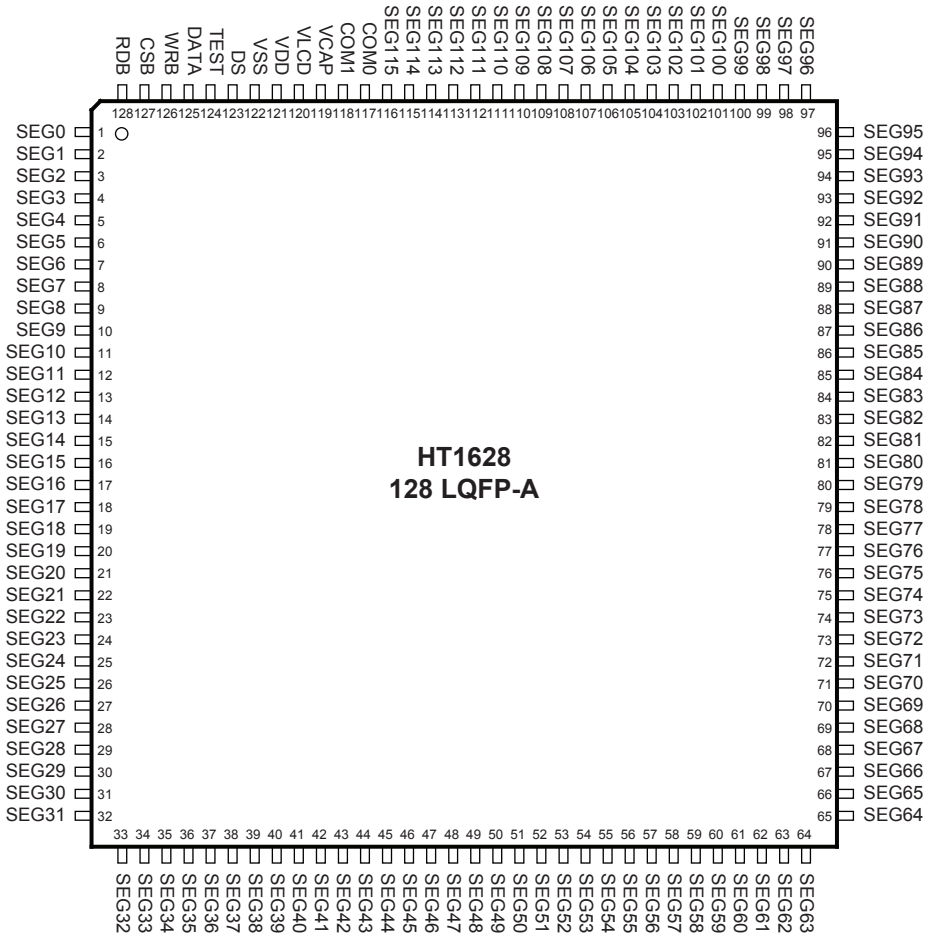
General Description

The HT1628 is a memory mapping and multi-function LCD controller driver which can operate with 1/1 or 1/2 duty. It can display up to 116 patterns with 1/1 duty or 232 patterns with 1/2 duty driver output. The S/W configuration features of the HT1628 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the device.

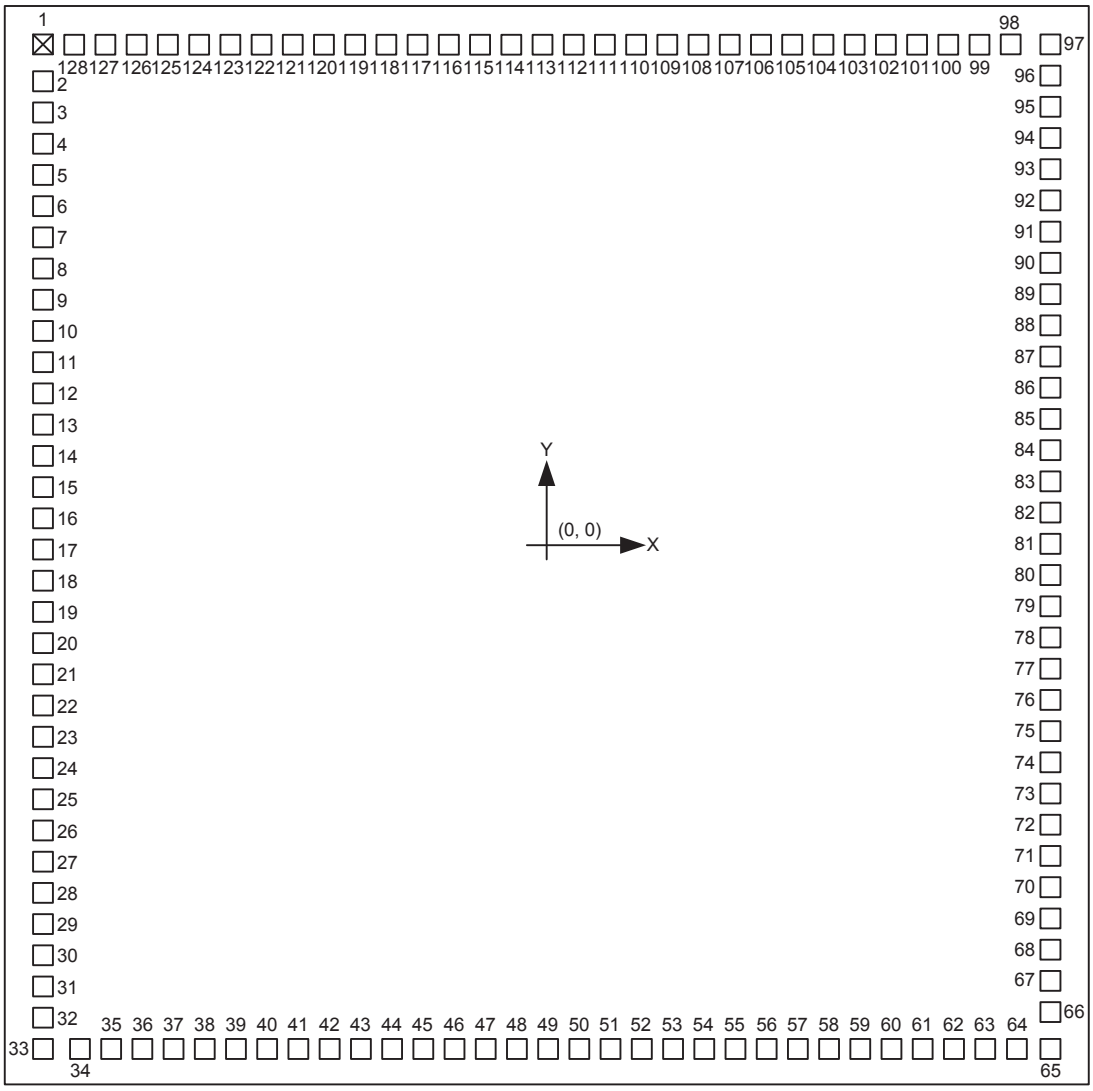
Block Diagram



Pin Assignment



Pad Assignment for COB



Chip size: 2813×2813 (μm)^2

Pad size: 70×70 (μm)^2

Chip thickness: 381 (μm)

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates for COB

Unit: μm

No	Pad Name	X	Y	No	Pad Name	X	Y
1	RDB	-1309.05	1309.05	39	SEG37	-784.95	-1309.05
2	SEG0	-1309.05	1194.95	40	SEG38	-702.95	-1309.05
3	SEG1	-1309.05	1112.95	41	SEG39	-622.95	-1309.05
4	SEG2	-1309.05	1030.95	42	SEG40	-542.95	-1309.05
5	SEG3	-1309.05	948.95	43	SEG41	-462.95	-1309.05
6	SEG4	-1309.05	866.95	44	SEG42	-382.95	-1309.05
7	SEG5	-1309.05	784.95	45	SEG43	-302.95	-1309.05
8	SEG6	-1309.05	702.95	46	SEG44	-222.95	-1309.05
9	SEG7	-1309.05	622.95	47	SEG45	-142.95	-1309.05
10	SEG8	-1309.05	542.95	48	SEG46	-62.95	-1309.05
11	SEG9	-1309.05	462.95	49	SEG47	17.05	-1309.05
12	SEG10	-1309.05	382.95	50	SEG48	97.05	-1309.05
13	SEG11	-1309.05	302.95	51	SEG49	177.05	-1309.05
14	SEG12	-1309.05	222.95	52	SEG50	257.05	-1309.05
15	SEG13	-1309.05	142.95	53	SEG51	337.05	-1309.05
16	SEG14	-1309.05	62.95	54	SEG52	417.05	-1309.05
17	SEG15	-1309.05	-17.05	55	SEG53	497.05	-1309.05
18	SEG16	-1309.05	-97.05	56	SEG54	577.05	-1309.05
19	SEG17	-1309.05	-177.05	57	SEG55	657.05	-1309.05
20	SEG18	-1309.05	-257.05	58	SEG56	737.05	-1309.05
21	SEG19	-1309.05	-337.05	59	SEG57	817.05	-1309.05
22	SEG20	-1309.05	-417.05	60	SEG58	899.05	-1309.05
23	SEG21	-1309.05	-497.05	61	SEG59	981.05	-1309.05
24	SEG22	-1309.05	-577.05	62	SEG60	1063.05	-1309.05
25	SEG23	-1309.05	-657.05	63	SEG61	1145.05	-1309.05
26	SEG24	-1309.05	-737.05	64	SEG62	1227.05	-1309.05
27	SEG25	-1309.05	-817.05	65	SEG63	1309.05	-1309.05
28	SEG26	-1309.05	-899.05	66	SEG64	1309.05	-1194.95
29	SEG27	-1309.05	-981.05	67	SEG65	1309.05	-1112.95
30	SEG28	-1309.05	-1063.05	68	SEG66	1309.05	-1030.95
31	SEG29	-1309.05	-1145.05	69	SEG67	1309.05	-948.95
32	SEG30	-1309.05	-1227.05	70	SEG68	1309.05	-866.95
33	SEG31	-1309.05	-1309.05	71	SEG69	1309.05	-784.95
34	SEG32	-1194.95	-1309.05	72	SEG70	1309.05	-702.95
35	SEG33	-1112.95	-1309.05	73	SEG71	1309.05	-622.95
36	SEG34	-1030.95	-1309.05	74	SEG72	1309.05	-542.95
37	SEG35	-948.95	-1309.05	75	SEG73	1309.05	-462.95
38	SEG36	-866.95	-1309.05	76	SEG74	1309.05	-382.95

No	Pad Name	X	Y	No	Pad Name	X	Y
77	SEG75	1309.05	-302.95	103	SEG101	784.95	1309.05
78	SEG76	1309.05	-222.95	104	SEG102	702.95	1309.05
79	SEG77	1309.05	-142.95	105	SEG103	622.95	1309.05
80	SEG78	1309.05	-62.95	106	SEG104	542.95	1309.05
81	SEG79	1309.05	17.05	107	SEG105	462.95	1309.05
82	SEG80	1309.05	97.05	108	SEG106	382.95	1309.05
83	SEG81	1309.05	177.05	109	SEG107	302.95	1309.05
84	SEG82	1309.05	257.05	110	SEG108	222.95	1309.05
85	SEG83	1309.05	337.05	111	SEG109	142.95	1309.05
86	SEG84	1309.05	417.05	112	SEG110	62.95	1309.05
87	SEG85	1309.05	497.05	113	SEG111	-17.05	1309.05
88	SEG86	1309.05	577.05	114	SEG112	-97.05	1309.05
89	SEG87	1309.05	657.05	115	SEG113	-177.05	1309.05
90	SEG88	1309.05	737.05	116	SEG114	-257.05	1309.05
91	SEG89	1309.05	817.05	117	SEG115	-337.05	1309.05
92	SEG90	1309.05	899.05	118	COM0	-417.05	1309.05
93	SEG91	1309.05	981.05	119	COM1	-497.05	1309.05
94	SEG92	1309.05	1063.05	120	VCAP	-577.05	1309.05
95	SEG93	1309.05	1145.05	121	VLCD	-657.05	1309.05
96	SEG94	1309.05	1227.05	122	VDD	-742.05	1309.05
97	SEG95	1309.05	1309.05	123	VSS	-823.05	1309.05
98	SEG96	1194.95	1309.05	124	DS	-904.05	1309.05
99	SEG97	1112.95	1309.05	125	TEST	-985.05	1309.05
100	SEG98	1030.95	1309.05	126	DATA	-1066.05	1309.05
101	SEG99	948.95	1309.05	127	WRB	-1147.05	1309.05
102	SEG100	866.95	1309.05	128	CSB	-1228.05	1309.05

Pin Description

Pin Name	Type	Description
VDD	—	Positive power supply
VLCD	—	LCD power input
VSS	—	Negative power supply, ground
VCAP	O	1/2 bias voltage output pin, connected to a capacitor
CSB	I	Chip select input with pull-high resistor 1. When high, the data and commands read from or written to the device are disabled. The serial interface circuit is also reset. 2. When low, data and command transmissions between the host controller and the device are all enabled.
RDB	I	READ clock input with pull-high resistor Data in the RAM of the device are clocked out on the falling edge of the RDB signal. The clocked out data will appear on the DATA line. The host controller can use next rising edge to latch the clocked out data.
WRB	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the device on the rising edge of the WRB signal
DATA	I/O	Signal data input/output with pull-high resistor
DS	I	Duty select pin DS="1": Static, COM0 and COM1 are output the same waveform DS="0": 1/2 duty
TEST	I	Test pin with pull-high resister Remains in a floating condition in normal mode
COM0~COM1	O	LCD Common output
SEG0~SEG115	O	LCD Segment output

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.5V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -55°C to 150°C

Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Timing Diagrams

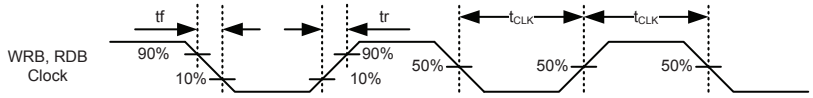


Figure 1

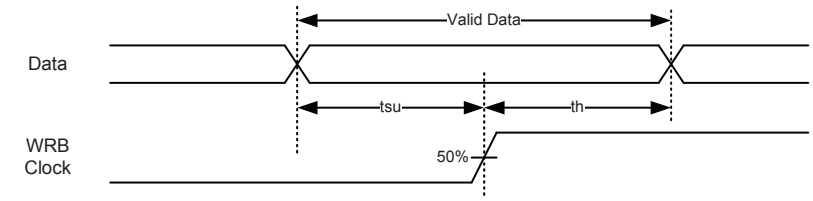


Figure 2

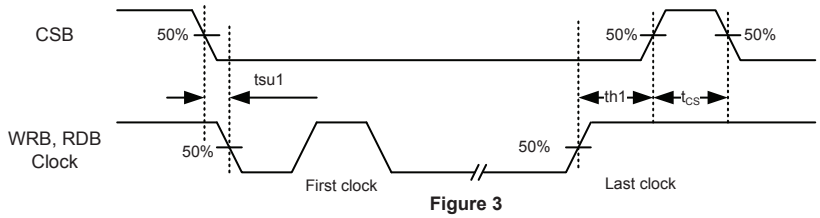


Figure 3

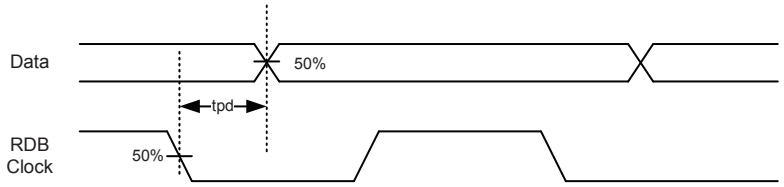


Figure 4

D.C. Characteristics

Ta = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
I_{DD1}	Operating Current	3V	No load, V_{DD}=V_{LCD}, LCD ON	—	60	120	μA
		5V		—	100	200	μA
I_{DD2}	Operating Current	3V	No load , V_{DD}=V_{LCD}, LCD OFF	—	10	20	μA
		5V		—	20	40	μA
I_{STB}	Standby Current	3V	No load, Power Down Mode	—	—	1	μA
		5V		—	—	2	μA
V_{IL}	Input Low Voltage	3V	DATA, CSB, WRB, RDB	0	—	0.6	V
		5V		0	—	1	V
V_{IH}	Input High Voltage	3V	DATA, CSB, WRB, RDB	2.4	—	3	V
		5V		4	—	5	V
I_{OL1}	DATA Sink Current	3V	V_{OL}=0.3V	0.3	0.5	—	mA
		5V	V_{OL}=0.5V	0.5	1	—	mA
I_{OH1}	DATA Source Current	3V	V_{OH}=2.7V	-0.3	-0.5	—	mA
		5V	V_{OH}=4.5V	-0.5	-1	—	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	100	200	—	μA
		5V	V_{OL}=0.5V	190	380	—	μA

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{OH3}	LCD Common Source Current	3V	V_{OH}=2.7V	-100	-200	—	μA
		5V	V_{OH}=4.5V	-190	-380	—	μA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	35	70	—	μA
		5V	V_{OL}=0.5V	65	130	—	μA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	-35	-70	—	μA
		5V	V_{OH}=4.5V	-65	-130	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, CSB, WRB, RDB, TEST	40	100	170	kΩ
		5V		20	50	90	kΩ

A.C. Characteristics

Ta = -40°C to +85°C

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
		V_{DD}	Conditions					
f_{LCD}	LCD Frame Frequency	3V	On-chip RC oscillator		58	90	148	Hz
		5V						
f_{CLK1}	Serial Data Clock (WRB pin)	3V	Duty cycle 50%		—	—	1	MHz
		5V			—	—	2	MHz
f_{CLK2}	Serial Data Clock (RDB pin)	3V	Duty cycle 50%		—	—	0.5	MHz
		5V			—	—	1	MHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	—	CSB		250	300	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode		0.4	—	—	μs
			Read mode		0.8	—	—	
		5V	Write mode		0.2	—	—	μs
			Read mode		0.4	—	—	
tr, tf	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	C_O=15pF		—	50	100	ns
t_{su}	Setup Time for DATA to WRB Clock Width (Figure 2)	—	—		50	100	—	ns
t_h	Hold Time for DATA to WRB Clock Width (Figure 2)	—	—		100	200	—	ns
t_{su1}	Setup Time for CSB to WRB, RDB Clock Width (Figure 3)	—	—		200	300	—	ns
t_{h1}	Hold Time for CSB to WRB, RDB Clock Width (Figure 3)	—	—		100	200	—	ns
t_{PD}	DATA Output Delay Time (RDB-DATA) (Figure 4)	—	C_O=15pF	t_{PD}=50 to 50%	—	100	200	ns
				t_{PD}=50 to 50%				
V_{POR}	V_{DD} Start voltage to ensure Power on reset	—	—		—	—	100	mV
RR_{VDD}	V_{DD} Rise Rate to ensure Power on reset	—	—		0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} to remain at V_{POR} to ensure Power on reset	—	—		10	—	—	ms

Functional Description

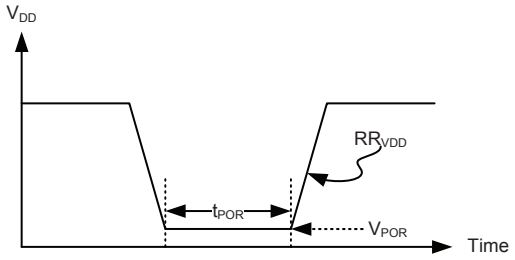
Power-on Reset

When power is turned on, the IC is initialised by an internal power-on reset circuit. The internal circuit status after initialisation is as follows:

- All common outputs are set to V_{LCD}
- All segment outputs are set to V_{LCD}
- The system oscillator and LCD bias generator are both off
- The LCD display is in an off state

Power on Reset timing

The device must be powered up under certain conditions to ensure correct operation as shown in the accompanying diagram.



Note that if the power on reset timing conditions are not satisfied during the power on/off sequence, the internal power on reset (POR) circuit will not operate normally. Also if V_{DD} drops below the operating voltage minimum voltage specification during operation, the power on reset timing conditions must be also satisfied. This means that V_{DD} must fall to 0V and remain at 0V for a minimum time of 20ms before rising to the normal operating voltage.

LCD Driver

The device is a 232 (116 × 2) pattern LCD driver. It can be configured as a 1 or 2 common LCD driver type using the DS pin configuration. This feature makes the device suitable for different kinds of LCD applications. The LCD clock is derived from the system clock.

DS pin	Duty	Bias
0	1/2	1/2
1	1/1	1/1

Note: It is not recommended to change the state of the DS pin input value after the device has been enabled.

System Oscillator

The system clock is used to generate the LCD driving clock. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. Once the system clock stops, the LCD display will become blank.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. At the initial system power on, the device is at the SYS DIS state.

LCD Bias Generator

The full-scale LCD voltage (V_{OP}) is obtained from $V_{LCD} - V_{SS}$.

The LCD voltage may be temperature compensated externally through the Voltage supply to the VLCD pin. Fractional LCD biasing voltages are obtained from an external voltage divider of two series resistors connected between VLCD and VSS. The center resistor can be switched out of the circuit to provide a 1/1bias voltage level configuration or 1/2bias voltage level configuration.

Segment Driver Outputs

The LCD driver section includes segment outputs which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit.

Column Driver Outputs

The LCD drive section includes column outputs which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit.

Address Pointer

The addressing mechanism for the display RAM is realised using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialisation of the address pointer by the Address pointer command.

Display Memory – RAM Structure

The static display RAM is organized into 58×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following shows the mapping from the RAM to the LCD patterns.

1. When the DS pin is set to "1" for 1/1 duty and 1/1 bias (static). The COM1 output waveform is equal to the COM0 output waveform.

D3	D2	D1	D0	Data / Addr
SEG0	SEG1	SEG2	SEG3	00h
SEG4	SEG5	SEG6	SEG7	01h
SEG8	SEG9	SEG10	SEG11	02h
SEG12	SEG13	SEG14	SEG15	03h
SEG16	SEG17	SEG18	SEG19	04h
:	:	:	:	:
SEG108	SEG109	SEG110	SEG111	1Bh
SEG112	SEG113	SEG114	SEG115	1Ch

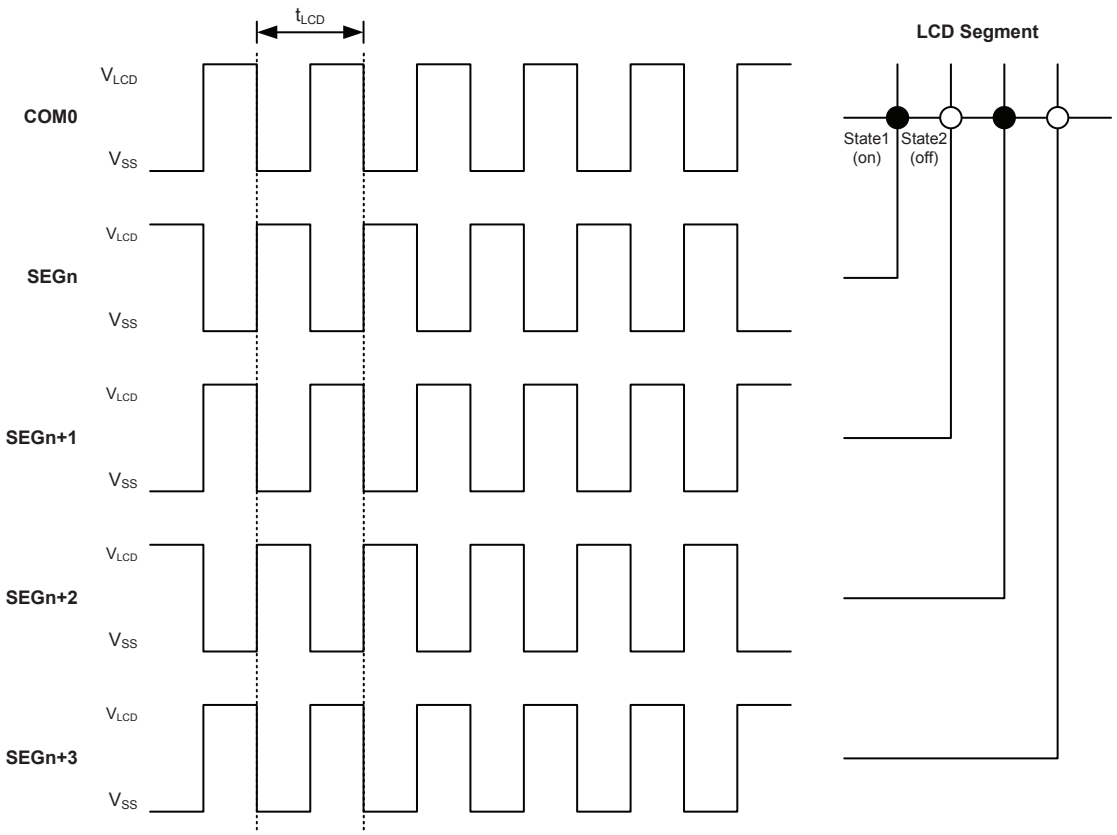
2. When the DS pin is set to "0" for 1/2 duty and 1/2 bias

D3	D2	D1	D0	Data / Addr
SEG0		SEG1		00h
SEG2		SEG3		01h
SEG4		SEG5		02h
SEG6		SEG7		03h
SEG8		SEG9		04h
:		:		:
SEG112		SEG113		38h
SEG114		SEG115		39h
COM1	COM0	COM1	COM0	

Note: It is recommended to initialize the display RAM data by clearing all RAM data before the LCD display function is activated. If the RAM data is not initialized before enabling the LCD display function, it may result in abnormal LCD display effect after executing the LCD ON command.

LCD Drive Mode Waveforms

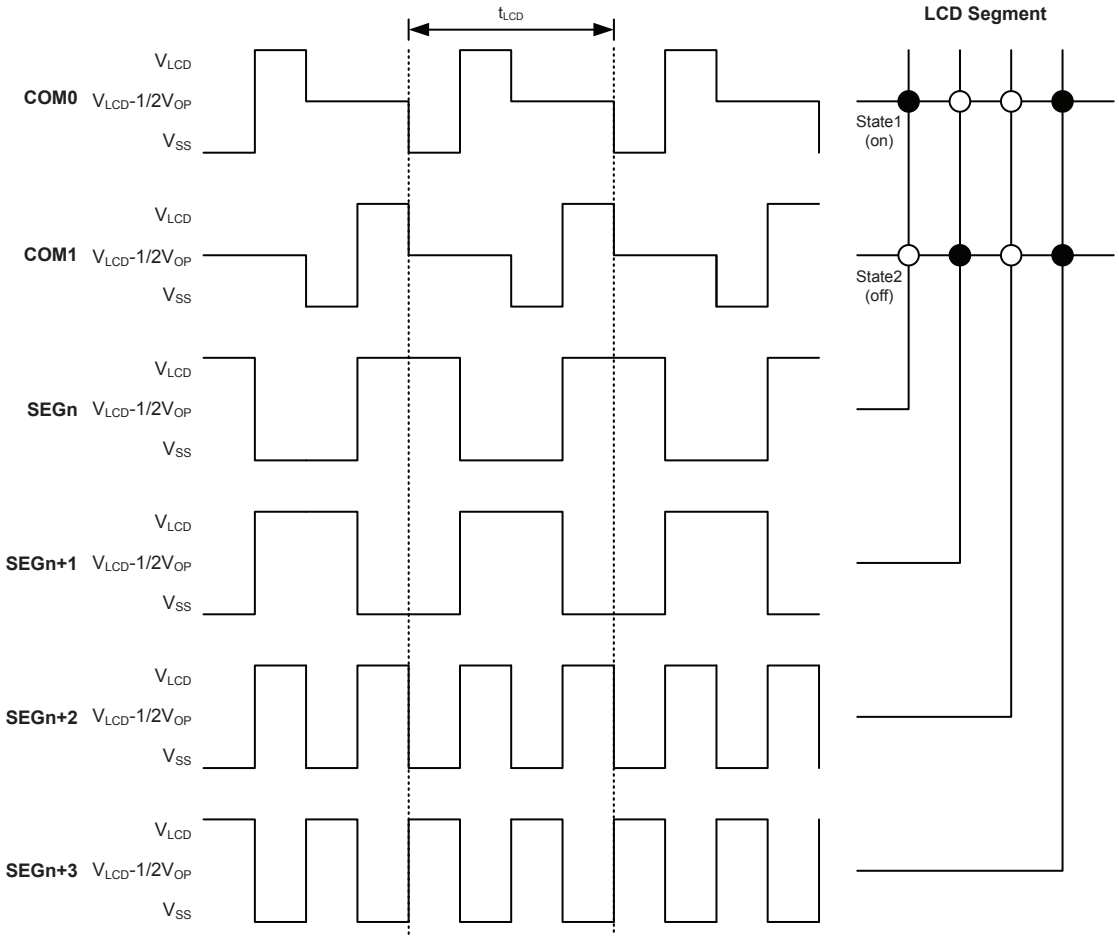
- When the DS pin is set to "1" for 1/1 duty and 1/1 bias (static), the waveform and LCD display is shown as follows:



Waveforms for 1/1 Duty Drive Mode with 1/1 bias

Note: $t_{LCD}=1/f_{LCD}$.

• When the DS pin is set to “0” for 1/2 duty and 1/2 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/2 Duty Drive Mode with 1/2 bias

Note: $t_{LCD}=1/f_{LCD}$.

Program Instruction Description

Instruction Table

The following table shows the full command list for the controller.

Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	—
WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	—
READ-MODIFY-WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Read and Write data to the RAM	—
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	—
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD display	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD display	—

Command Format

The device can be configured by the software setting. There are two mode commands to configure the device resource and to transfer the LCD display data.

The following are the data mode ID and the command mode ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID can be omitted. While the system is operating in a non-successive command or a non-successive address data mode, the CSB pin should be set to "1" and the previous operation mode will be reset also. The CSB pin returns to "0", a new operation ID should be issued first.

Function Set

This command controls the on/off functions for the system oscillator and display.

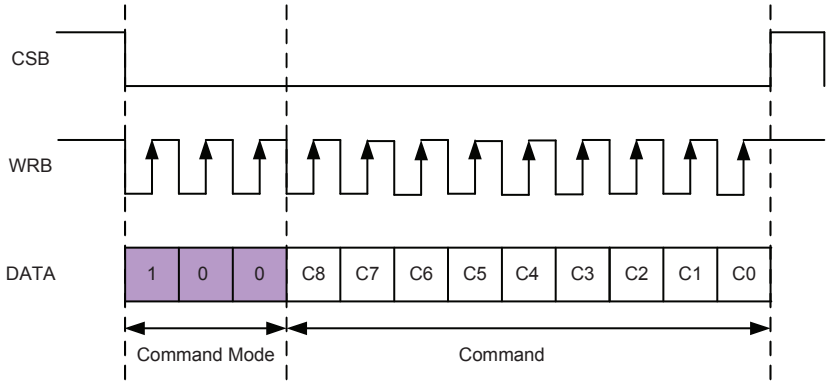
Operation	ID	Command Code									Note
		C8	C7	C6	C5	C4	C3	C2	C1	C0	
SYS DIS	100	0	0	0	0	0	0	0	0	X	system oscillator on/off
SYS EN	100	0	0	0	0	0	0	0	1	X	
LCD OFF	100	0	0	0	0	0	0	1	0	X	display on/off
LCD ON	100	0	0	0	0	0	0	1	1	X	

4-wire Serial Interface

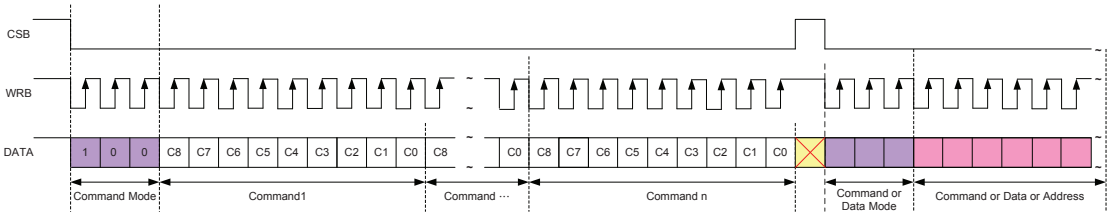
The device includes a 4-wire serial interface which is used for all data and command transfers. The CSB pin is used to indicate when data and command transfers are required. An active low signal on this pin will enable the serial interface allowing data and command transfers to be executed. Data is shifted into the registers on the CLK rising edge with the sequence starting from the CSB signal falling edge. For read operations, the DATA pin will change to an output after the device receives a read clock on the RDB pin.

Write Operations

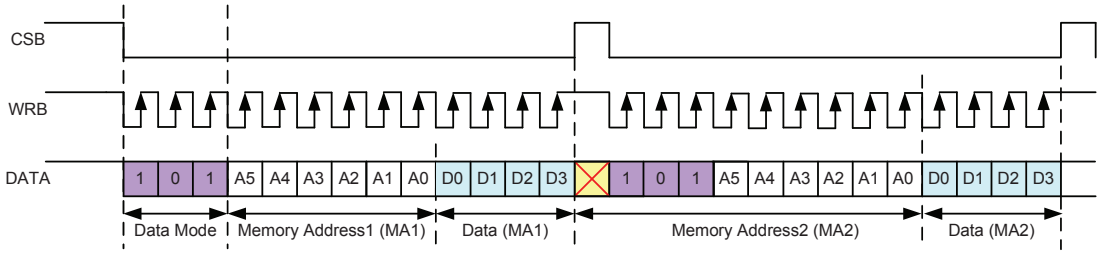
Single Command Byte Operation



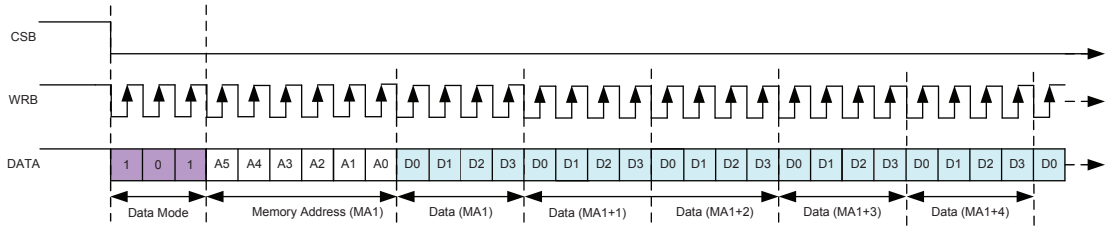
Compound Command Byte Operation



Write Single Display Data Operation



Write Pages Display Data Operation

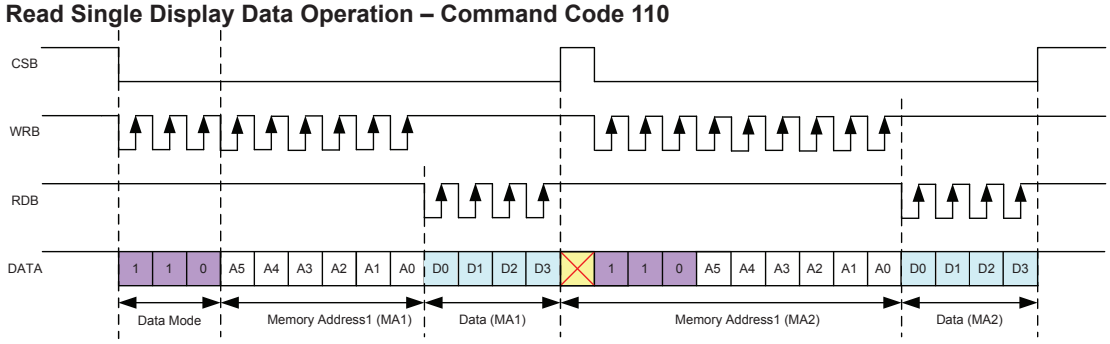


Note: The addresses will increment automatically continuously. The address will be wrapped around to address 0x00H when it exceeds the maximum address. The maximum address is shown as follows:

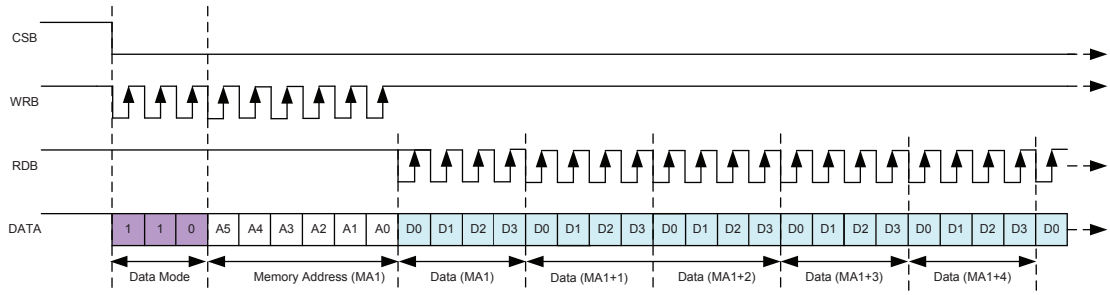
Duty	Maximum Address
1/1	1Ch
1/2	39h

Read Display RAM Data Operations

Read Single Display Data Operation – Command Code 110



Read Pages Display Data Operation – Command Code 110

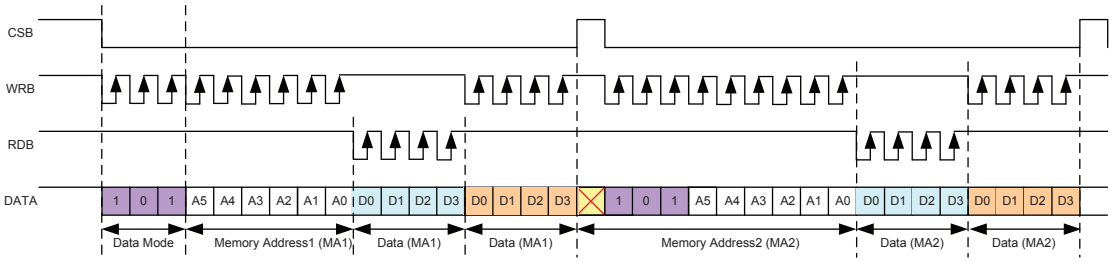


Note: The addresses will increment automatically continuously. The address will be wrapped around to address 0x00H when it exceeds the maximum address. The maximum address is shown as follows:

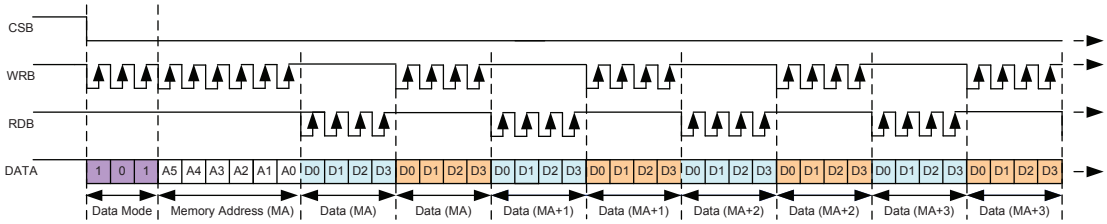
Duty	Maximum Address
1/1	1Ch
1/2	39h

Read Modify Write RAM Data Operation

Read Modify Write Single Display Data Operation – Command Code 101



Read Modify Write Pages Display Data Operation – Command Code 101



Note: The addresses will increment automatically continuously. The address will be wrapped around to address 0x00H when it exceeds the maximum address. The maximum address is shown as follows:

Duty	Maximum Address
1/1	1Ch
1/2	39h

Power Supply Sequence

- If the power is individually supplied on the LCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

Holtek Power Supply Sequence Requirement:

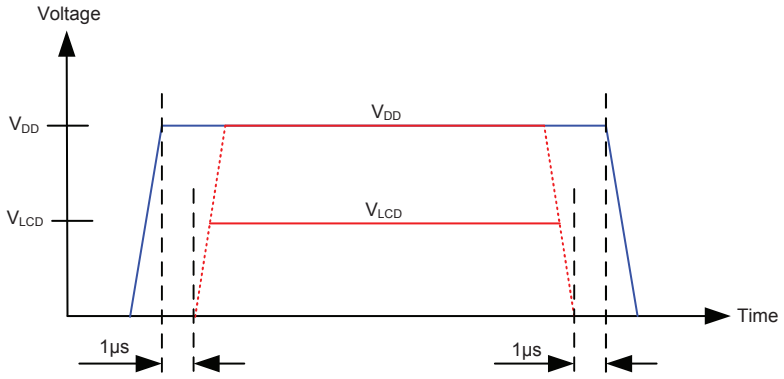
1. Power-on sequence:

   Turn on the logic power supply V_{DD} first and then turn on the LCD driver power supply V_{LCD}.

2. Power-off sequence:

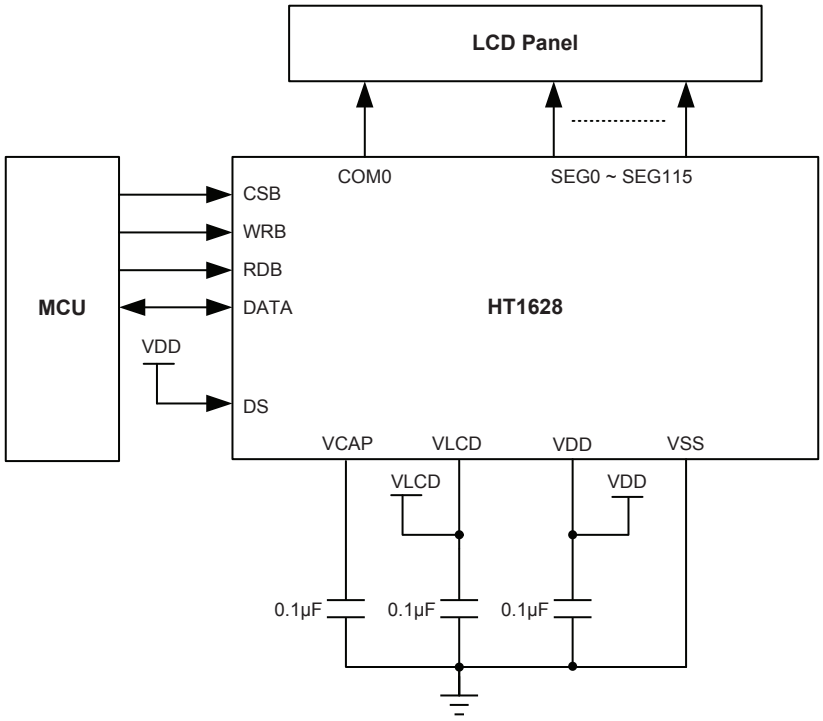
   Turn off the LCD driver power supply V_{LCD}. First and then turn off the logic power supply V_{DD}.

3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the V_{LCD} voltage is higher than the V_{DD} voltage.



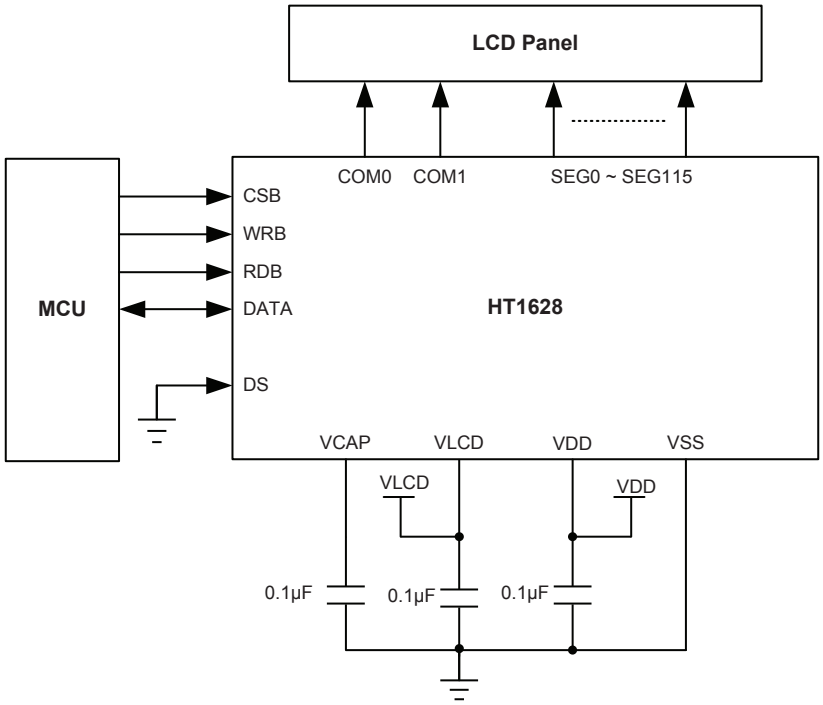
Application Circuits

DS pin is set to “1” for 1/1 duty and 1/1 bias (Static)



Note: The V_{LCD} input voltage must smaller than or equal to V_{DD}.

DS pin set to “0” for 1/2 duty and 1/2 bias



Note: The V_{LCD} input voltage must be smaller than or equal to V_{DD}.

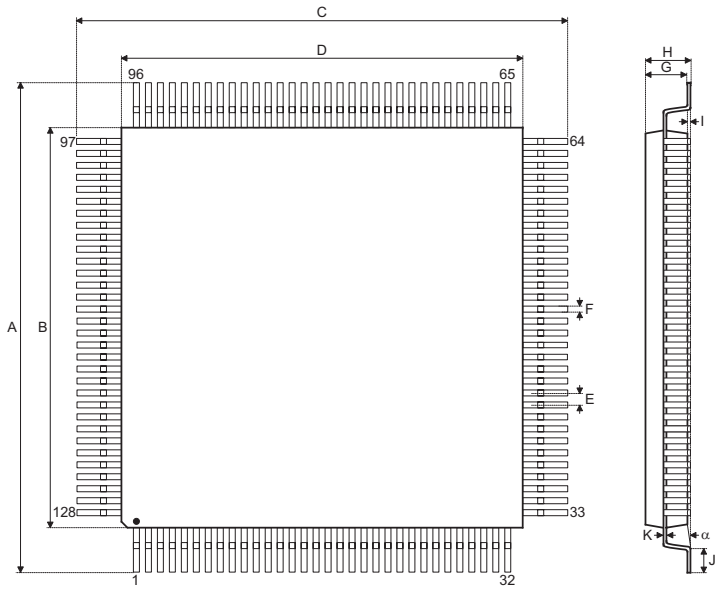
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

128-pin LQFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.630 BSC	—
B	—	0.551 BSC	—
C	—	0.630 BSC	—
D	—	0.551 BSC	—
E	—	0.020 BSC	—
F	0.005	0.006	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	16.00 BSC	—
B	—	14.00 BSC	—
C	—	16.00 BSC	—
D	—	14.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.16	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°