1. General Descriptions

HT1628 is an LED Controller driven on a 1/7to 1/8 duty factor. Eleven segment output lines, six grid output lines, 1 segment/grid output lines, one display memory, control circuit , key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to HT1628 via a four-line serial interface.Housed in a 28-pin SOP Package, HT1628 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.
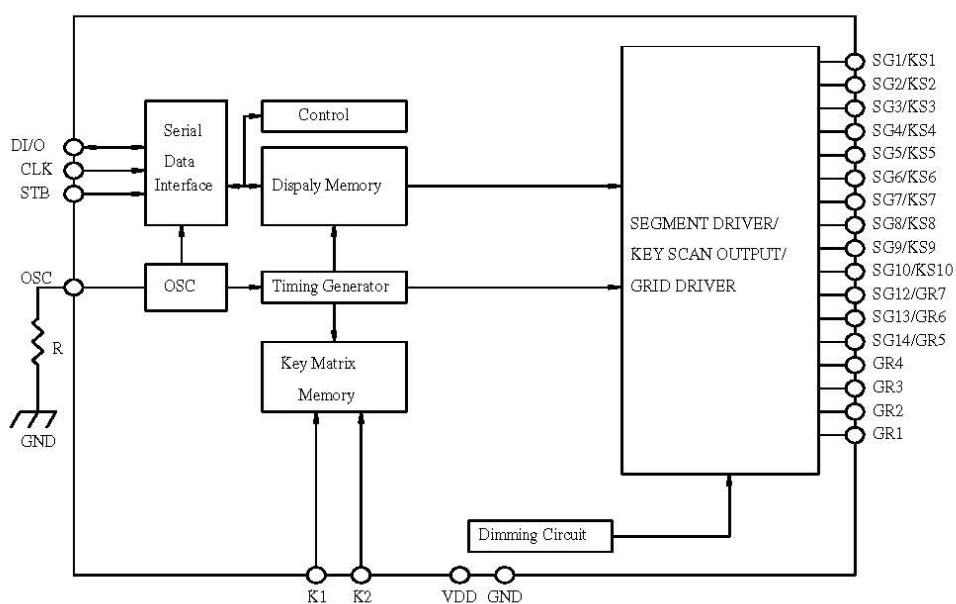
2. Features

- ◆ CMOS Technology
- ◆ Low Power Consumption
- ◆ Multiple Display Modes
- ◆ Key Scanning
- ◆ 8-Step Dimming Circuitry
- ◆ Serial Interface for Clock, Data Input, Data Output, Strobe Pins
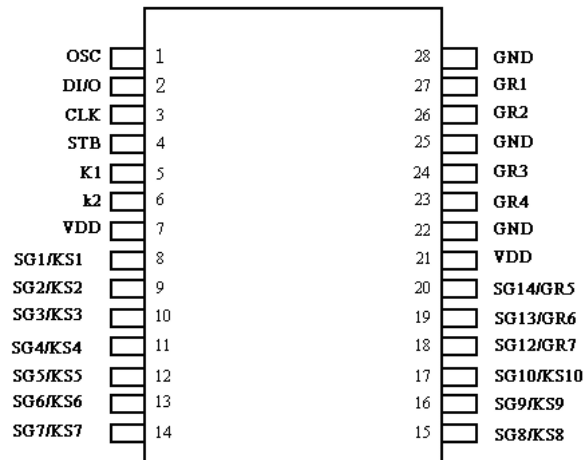- ◆ Available in 28-Pin, SOP Package

Application Features:

- ◆ Micro-computer Peripheral Device
- ◆ VCR set
- ◆ Combi set

3. Function Block Diagram

4. Pin Configuration

OSC	1		28	GND
DI/O	2		27	GR1
CLK	3		26	GR2
STB	4		25	GND
K1	5		24	GR3
k2	6		23	GR4
VDD	7		22	GND
SG1/KS1	8		21	VDD
SG2/KS2	9		20	SG14/GR5
SG3/KS3	10		19	SG13/GR6
SG4/KS4	11		18	SG12/GR7
SG5/KS5	12		17	SG10/KS10
SG6/KS6	13		16	SG9/KS9
SG7/KS7	14		15	SG8/KS8

5. Pin Descriptions

| NO.	Name	I/O	Description
1	OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency
2	DI/O	I/O	Data Output Pin (N-Channel, Open-Drain) or Data Input pin This pin Outputs/Input serial data at the falling(rising) edge of the shift clock.
3	CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.
4	STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command When this pin is "HIGH", CLK is ignored.
5,6	K1 to K2	I	Key Data Input Pins. The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor)
22,25,28	GND	-	Ground Pin
8~17	SG1/KS1 to SG10/KS10	O	Segment Output Pins (p-channel, open drain) Also acts as the Key Source
18~20	SG12/GR7 toSG14/GR5	O	Segment/Grid Output Pins
7,21	VDD	-	Power Supply
23,24,26,27	GR4 to GR1	O	Grid Output Pins

6. *Input/output Configurations*

The schematic diagrams of the input and output circuits of the logic section are shown below.
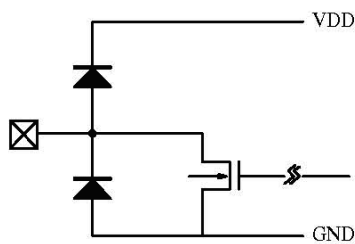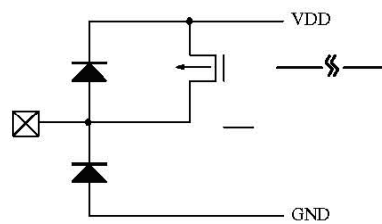
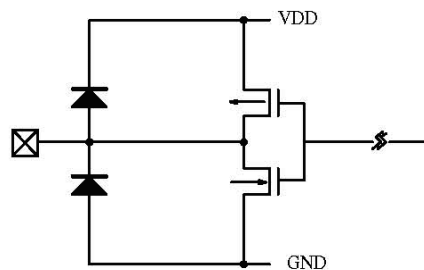### 6.1 *Input Pins: CLK, STB & DIN*
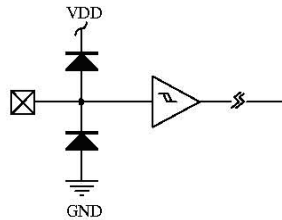
6.2 *Input Pins: K1 to K2*
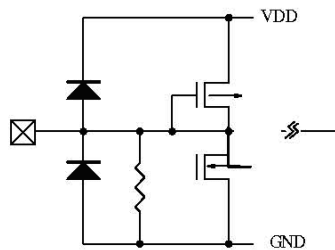
6.3 *Output Pins: DOUT, GR1 to GR4*

6.4 *Output Pins: SG1 to SG10*

6.5 *Output Pins: GR5, GR6 and SG12/GR7*


7. *Function Descriptions*

7.1 Command

A command is the first byte (b0 to b7) inputted to A1628 via the DIN Pin after STB pin has changed from HIGH to LOW Stage. If for some reason the STB Pin is set to HIGH while data or commands are being transmitted, the serial communications is initialized, and the data/commands being transmitted are considered invalid.

7.1.1 Command 1: Display Mode Setting Commands

HT1628 provides 2 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7)transmitted to HT1628 via the DIN Pin when STB is LOW. However, for these commands, the bit 3 to bit 6 (b2 to b5) are ignored, bit 7 & bit 8 (b6 to b7) are given value of 0.

The Display Mode Setting Commands determine the number of segments and grids to be used (12 to 11 segments, 6 to 7 grids). A display command ON must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned ON, the 7-grid, 11-segment modes is selected.
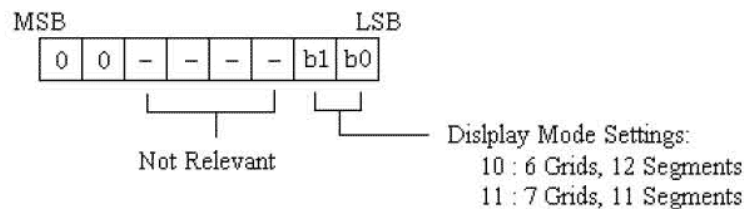
7.1.2 Command 2: Data Setting Commands

The Data Setting Commands executes the Data Write or Data Read Modes for HT1628. The data Setting Command, the bits 5 and 6 (b4,b5) are ignored, bit 7 (b6) is given the value of 1 while bit 8 (b7) is given the value of 0. Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of 0.
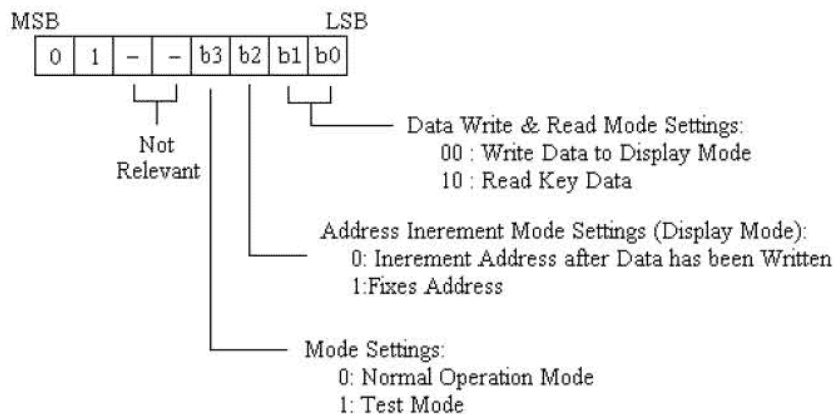
7.1.3. HT1628 Keymatrix & Keyinput Data Storage Ram

HT1628 Key Matrix consists of 10 x 3 array as shown below:
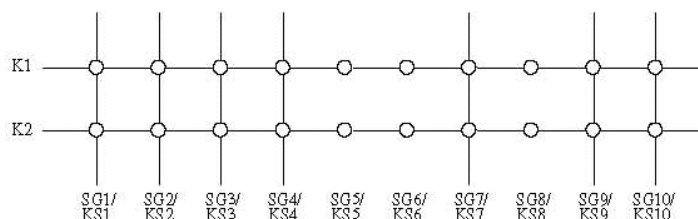
Each data entered by each key is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (b0) has been read, the least significant bit of the next data (b7) is read.

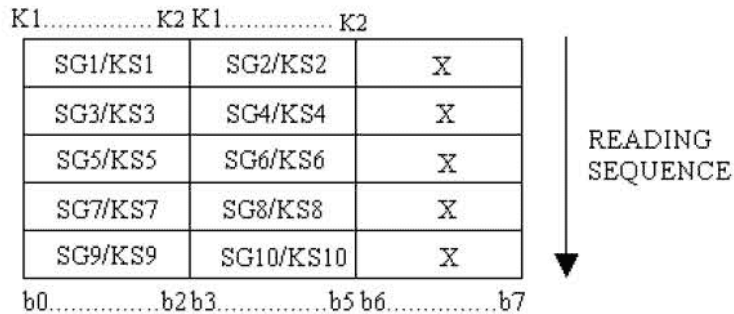| K1 .... K2	K1 .... K2	
SG1/KS1	SG2/KS2	X
SG3/KS3	SG4/KS4	X
SG5/KS5	SG6/KS6	X
SG7/KS7	SG8/KS8	X
SG9/KS9	SG10/KS10	X

b0 .... b2 b3 .... b5 b6 .... b7

READING SEQUENCE

Note: b6 and b7 do not care

7.1.4 Command 3: Address Setting Commands

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of 00H to 0DH. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at at 00H.

Please refer to the diagram below.

MSB .... LSB

| 1 | 1 | – | – | b3 | b2 | b1 | b0 |

Not Relevant   Address: ooH to 0DH
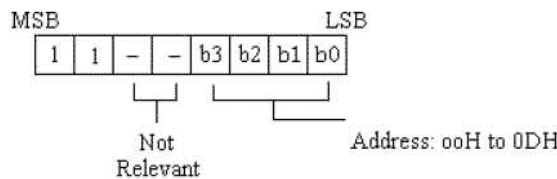
7.1.5 Displaymode And Ramaddress

Data transmitted from an external device to HT1628 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM addresses of HT1628 are given below in 8 bits unit.

SG1 .... SG4	SG5 .... SG8	SG9 .... SG12	
00HL	00Hu	01HL	DIG1
02HL	02Hu	03HL	DIG2
04HL	04Hu	05HL	DIG3
06HL	06Hu	07HL	DIG4
08HL	08Hu	09HL	DIG5
0AHL	0AHu	0BHL	DIG6
0CHL	0CHu	0DHL	DIG7

b0   b3 b4   b7

| xxHL | xxHu |

Lower 4 bits Higher 4 bits
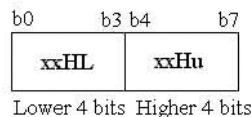
7.1.6 Command 4: Display Control Commands

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 Pulse width is selected and the displayed is turned OFF (the key scanning is started).

MSB — LSB

1 0 – – b3 b2 b1 b0

Not Relevant

Dimming Quantity Settings:
000: Pulse width = 1/16
001: Pulse width = 2/16
010: Pulse width = 4/16
011: Pulse width = 10/16
100: Pulse width = 11/16
101: Pulse width = 12/16
110: Pulse width = 13/16
111: Pulse width = 14/16

Display Settings:
0: Display OFF (Key Scan Continues)
1: Display ON
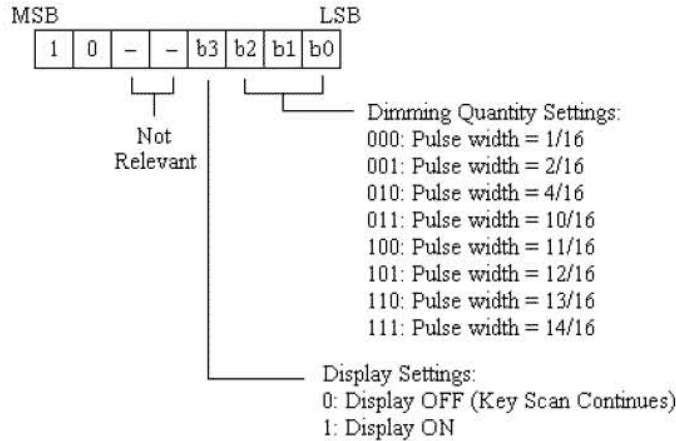
7.2 Scanning And Display Timing

The key Scanning and Display Timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the are 10 x 3 matrix is stored in the RAM.
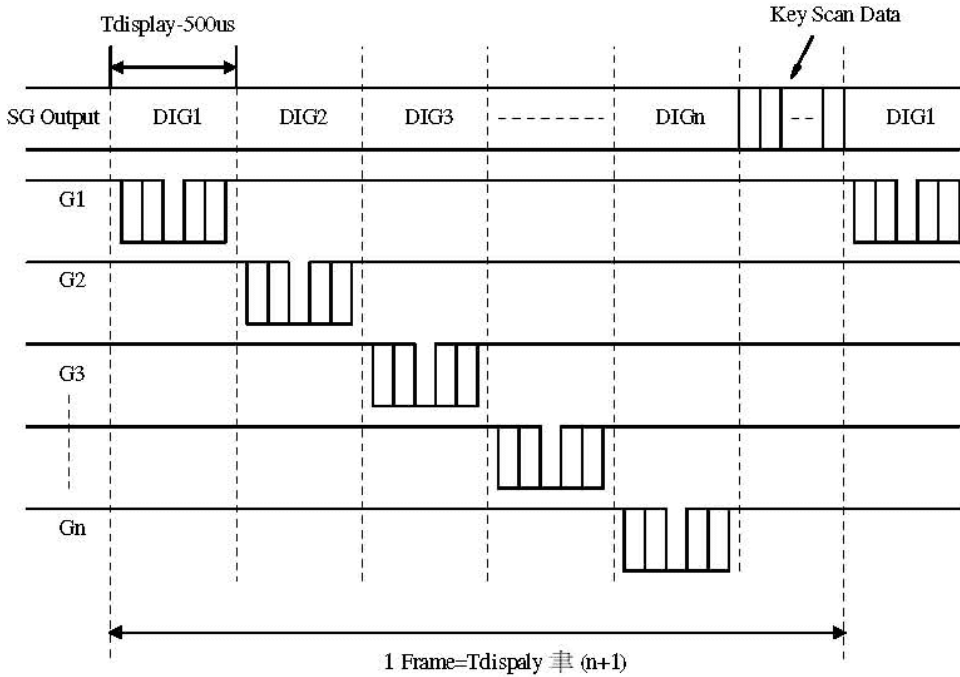
7.3 Serial Communication Format

The following diagram shows the HT1628 serial communication format. The DOUT Pin is an N-channel, open drain output pin; therefore, it is highly recommended that an external pull-up resistor (1 K Ohms to 10 K Ohms) must be connected to DOUT.

7.3.1 Reception (Data/Command Write)
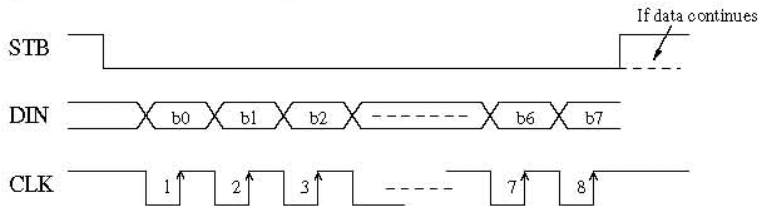
7.3.2 Transmission (Data Read)
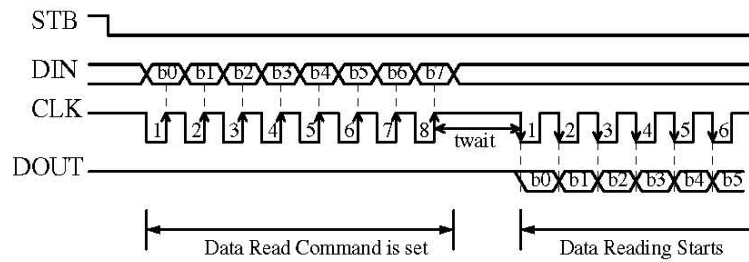
where: t_{wait} (waiting time) $\geqslant 1\mu s$

It must be noted that when the data is read, the waiting time (t_{wait}) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1µs.

7.4 Switching Characteristic Waveform

A1628 Switching Characteristics Waveform is given below.
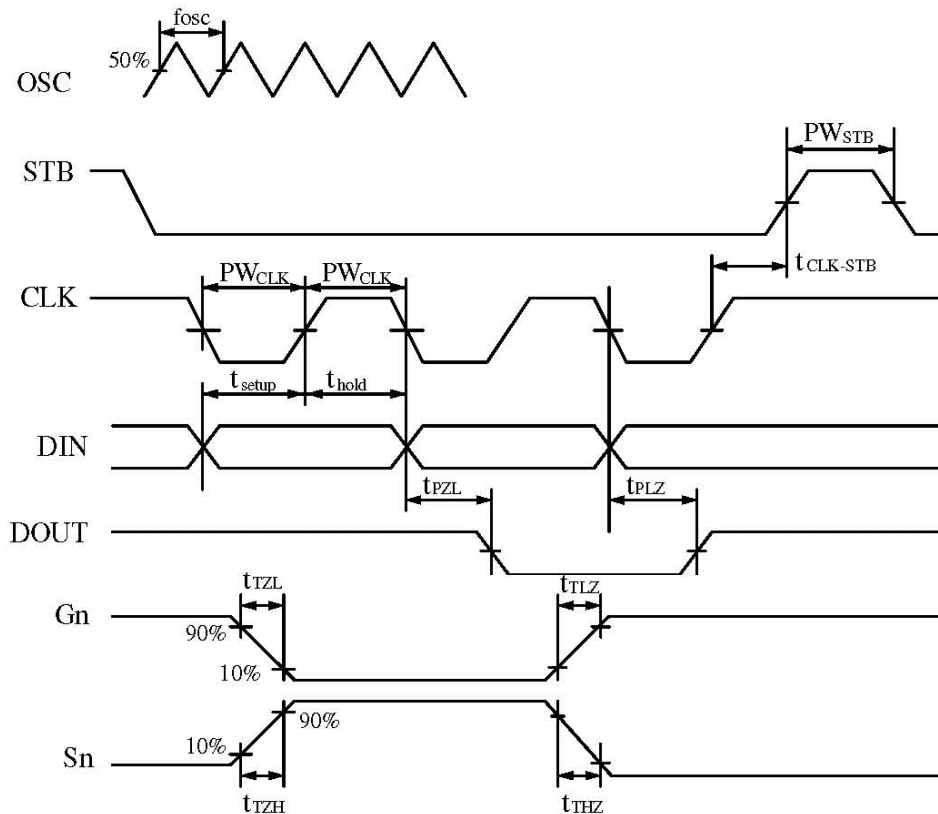
where: PW_{CLK} (Clock Pulse Width) ≥ 400nS PW_{STB} (Strobe Pulse Width) ≥1µs

t_{setup} (Data Setup Time) ≥100nS t_{hold} (Data Hold Time) ≥100nS

t_{CLK}-STB (Clock-Strobe Time) ≥1µs t_{THZ}(Fall Time)≤10µs

t_{TZH}(Rise Time) ≤1µs t_{PZL}(Propagation Delay Time) ≤100nS

f_{osc}=Oscillation Frequency t_{PLZ}(Propagation Delay Time) ≤300uS

t_{TZL}< 1µs t_{TLZ}<10µs

Note: Test condition under

t_{THZ} (Pull low risistor=100k ohms, Loading capacitor =300pf)

t_{TLZ} (Pull high risistor =100k ohms, Loading capacitor=300pf)

7.5 Applications

Display memory is updated by incrementing addresses. Please refer to the following diagram.
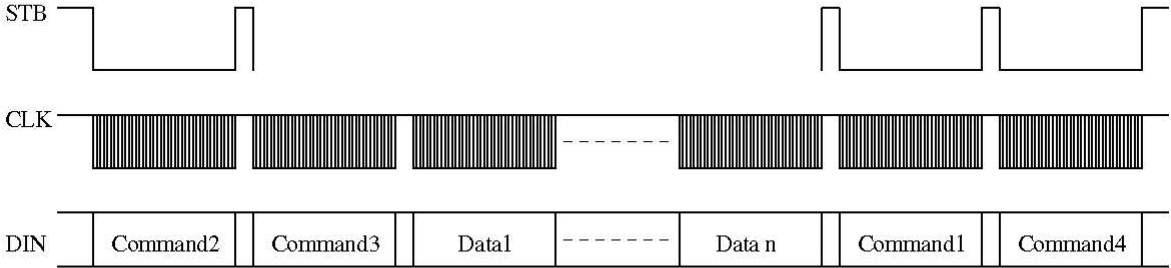
where: Command 1: Display Mode Setting Command

Command 2: Data Setting Command

Command 3: Address Setting Command

Data 1 to n : Transfer Display Data (14 Bytes max.)

Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.
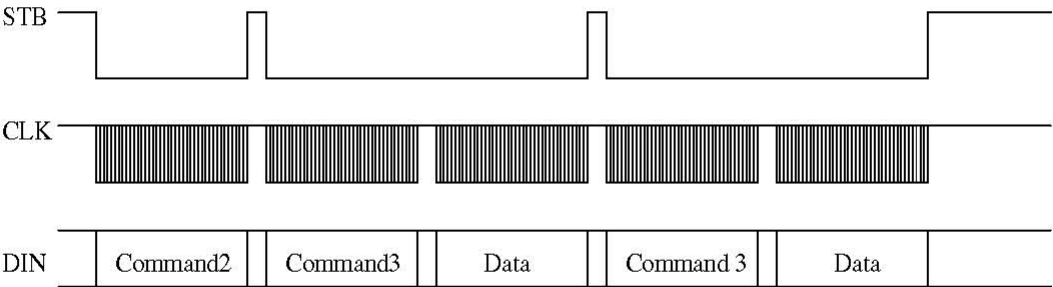
where: Command 2 — Data Setting Command

Command 3 — Address Setting Command

Data — Display Data

8. Recommended Software Programming Flowchart

```
                    ┌─────────────┐
                    │    START    │
                    └──────┬──────┘
                           │
                    ┌──────┴──────┐
                    │ Relay 200ms │
                    └──────┬──────┘
                           │
                    ┌──────┴──────┐
                    │     SET     │────────┐
                    │  COMMAND2   │        │
                    │ (Write Data)│        │
                    └──────┬──────┘        │
                           │               │
                    ┌──────┴──────┐        │
                    │     SET     │        │
                    │  COMMAND3   │        │
                    │Clear Display│    INITIAL
                    │    RAM      │    SETTING
                    │ (See Note 5)│        │
                    └──────┬──────┘        │
                           │               │
                    ┌──────┴──────┐        │
                    │     SET     │        │
                    │  COMMAND1   │        │
                    └──────┬──────┘        │
                           │               │
                    ┌──────┴──────┐        │
                    │     SET     │        │
                    │  COMMAND4   │────────┘
                    │(88H~8FH:    │
                    │ Display ON) │
                    └──────┬──────┘
                           │
                    ┌──────┴──────┐◄───────┐
                    │    MAIN     │        │
                    │  PROGRAM    │        │
                    └──────┬──────┘        │
                           │               │
                    ┌──────┴──────┐        │
                    │     SET     │        │
                    │  COMMAND2   │        │
                    │ (READ KEY & │        │
                    │  WRITEDATA  │        │
                    │  INCLUDED)  │     MAIN
                    └──────┬──────┘     LOOP
                           │               │
                    ┌──────┴──────┐        │
                    │     SET     │        │
                    │  COMMAND3   │        │
                    └──────┬──────┘        │
                           │               │
                    ┌──────┴──────┐        │
                    │     SET     │        │
                    │  COMMAND1   │        │
                    └──────┬──────┘        │
                           │               │
                    ┌──────┴──────┐        │
                    │     SET     │────────┘
                    │  COMMAND4   │
                    └──────┬──────┘
                           │
                    ┌──────┴──────┐
                    │     GND     │
                    └─────────────┘
```
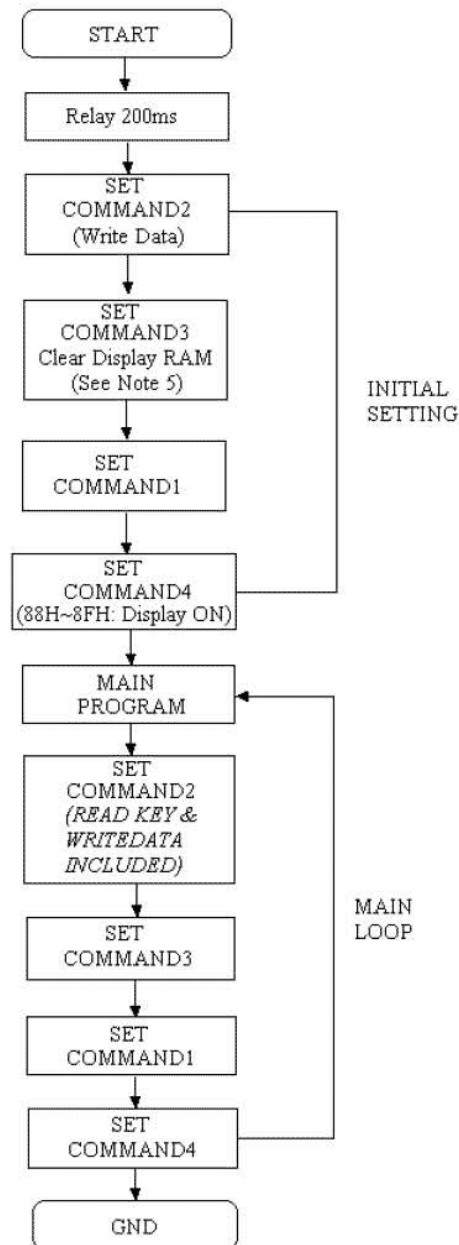
Note: 1. Command 1: Display Mode Commands

2. Command 2: Data Setting Commands

3. Command 3: Address Setting Commands

4. Command 4: Display Control Commands

5. When IC power is applied for the first time, the contents of the Display RAM is not defined; thus, it

is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

9. *Application Circuit*
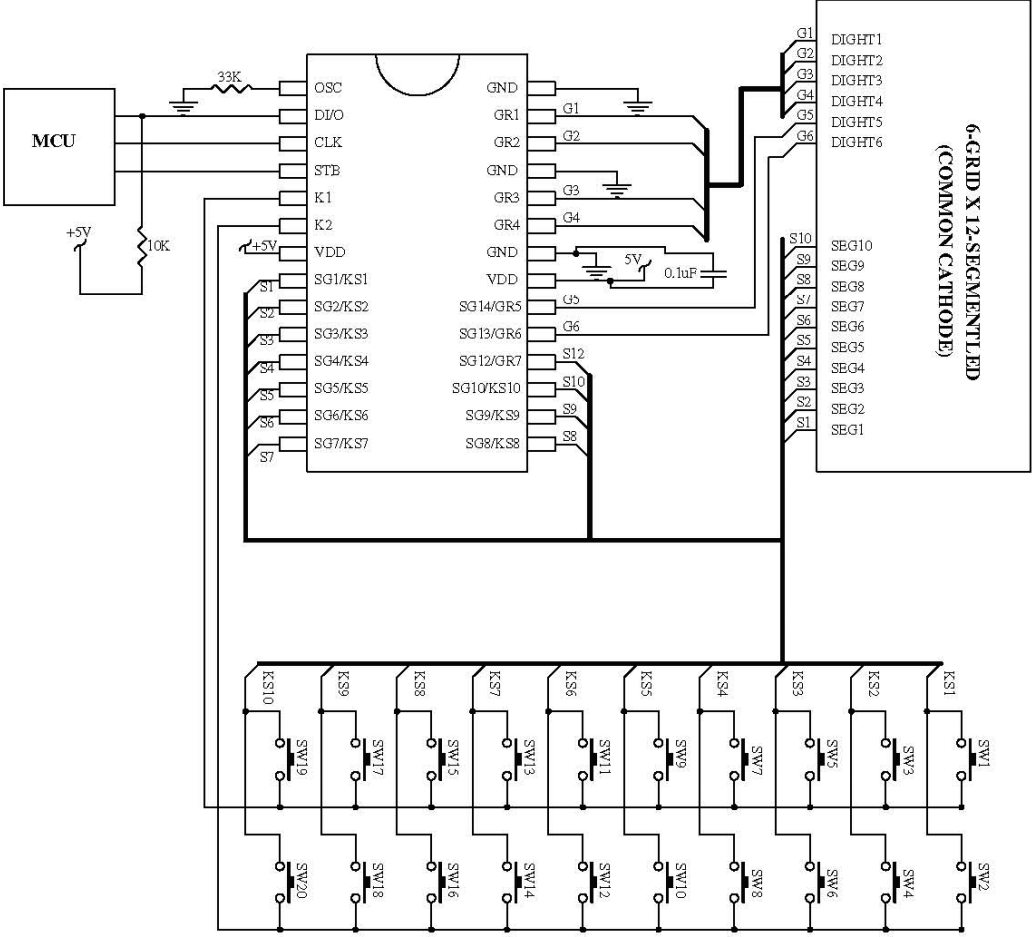
Common Cathode Type LED Panel:
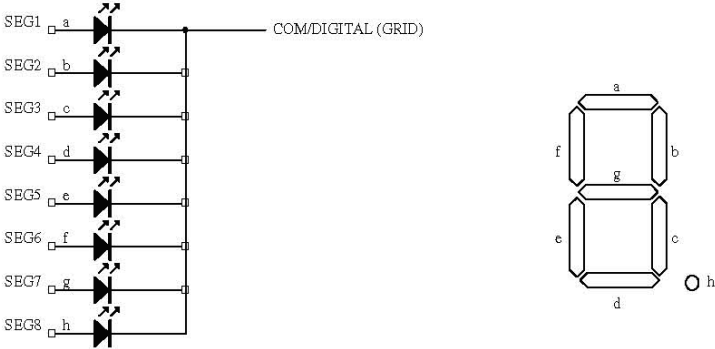
10. PAD Location

NO.	PADNAME	X	Y	NO.	PADNAME	X	Y
1	OSC	205	-446	17	SG8/KS8	-90	468
2	DOUT	332	-446	18	SG9/KS9	-250	468
3	DIN	449	-446	19	SG10/KS10	-360	468
4	CLK	566	-468	20	SG11	-526	468
5	STB	566	-350	21	SG12/GR7	-531	367
6	K1	566	-233	22	GR6	-531	235
7	K2	566	-115	23	GR5	-531	104
8	K3	566	2	24	VDD	-531	-6
9	VDD	566	120	25	GND	-531	-116
10	SG1/KS1	593	237	26	GR4	-531	-226
11	SG2/KS2	593	347	27	GR3	-531	-358
12	SG3/KS3	593	457	28	GND	-531	-468
13	SG4/KS4	451	468	29	GR2	-380	-420
14	SG5/KS5	291	468	30	GR1	-204	-420
15	SG6/KS6	181	468	31	GND	-55	-446
16	SG7/KS7	20	468				
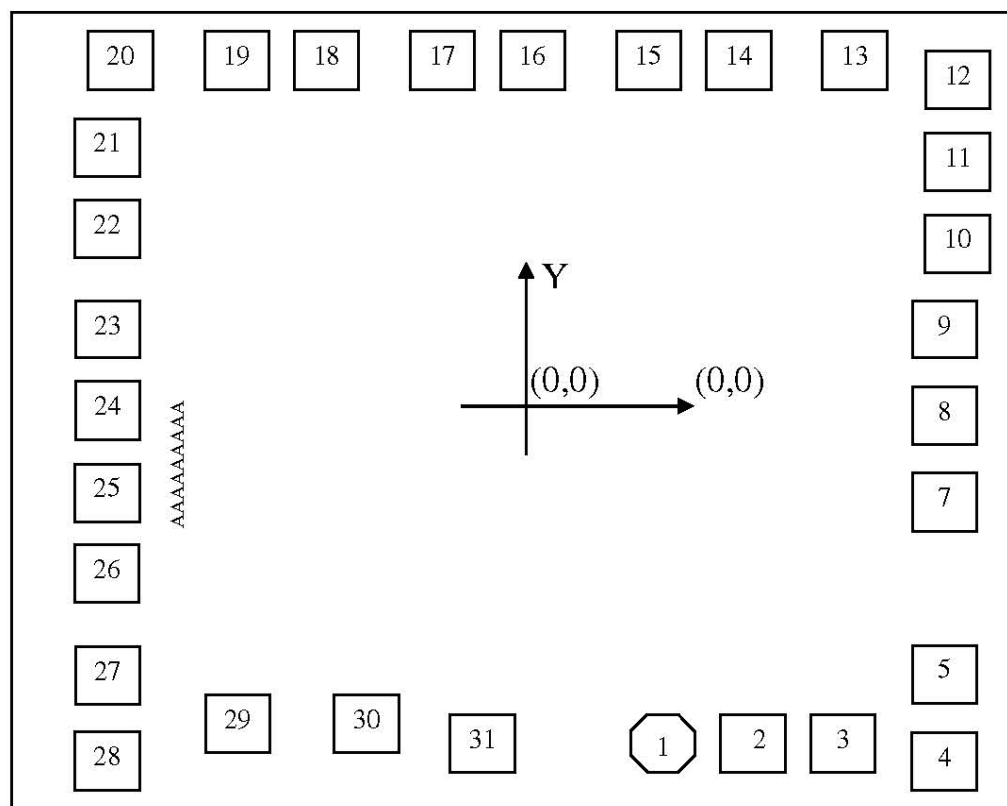
Chip Size: (1520,1280) μ m

Note: The substrate must be connected to GND

11. Absolute Maximum Ratings

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{DD}	-0.5 to +7	V
Logic Input Voltage	V_I	-0.5 to V_{DD} +0.5	V
Driver Output Current	I_{OLGR}	+250	mA
	I_{OHSG}	-50	mA
Maximum Driver Output Current/Total	I_{TOTAL}	400	mA

12. Recommended Operating Range

(Unless otherwise stated, Ta=-20 to +70℃, GND=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}		4.5	5	5.5	V
Dynamic Current (see Note)	I_{DDdyn}		-	-	2.5	mA
High-Level Input Voltage	V_{IH}		$0.8V_{DD}$	-	V_{DD}	V
Low-Level Input Voltage	V_{IL}		0	-	$0.3V_{DD}$	V

Note: Test Condition: Set Display Control Commands = 80H (Display Turn OFF State & under no load)

13. Electrical Characteristics

(Unless otherwise stated, V_{DD}=5V, GND=0V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Current	IOHSG1	Vo=VDD-2V SG1 to SG10, SG12/GR7	-20	-25	-40	mA
	IOHSG2	Vo=VDD-3V SG1 to SG12, SG12/GR7	-25	-30	-50	mA
Low-Level Output Current	IOLGR	Vo=0.3V GR1 to GR6, SG12/GR7	50	65	-	mA
Low-Level Output Current	IOLDOUT	Vo=0.4V	10	-	-	mA
Segment High-Level Output Current Tolerance	ITOLSG	Vo=VDD-3V SG1 to SG10, SG12/GR7	-	-	±5	mA
High-Level Input Voltage	VIH	-	0.8 V_{DD}	-	5	V
Low-Level Input Voltage	VIL	-	0	-	$0.3V_{DD}$	V
Oscillation Frequency	fosc	R=36 KΩ	350	500	650	KHz
K1 to K2 Pull Down Resistor	RKN	K1 to K2 VDD=5V	40	-	100	KΩ

14. **Editions**

Editions	Expression	Date
V1.0	New Editions	2007-01-03

15. **Notices**

1. The information contained herein could be changed without notice owing to product and /or technical improvements. Please make sure before using the product that the information you are referring to is up-to-date.

2. No responsibility is assumed by us for any consequence resulting from any wrong or improper operation, etc.of the product.