HT1670

128×32 LCD Controller for I/O MCU

PATENTED

PAT No. : 099352

Technical Document

- Tools Information
- FAQs
- Application Note

Features

- Operating voltage: 2.7V~5.2V
- Built-in 32kHz RC oscillator
- External 32.768kHz crystal oscillator or 32kHz frequency source input
- Standby current: <1μA at 3V, <2μA at 5V
- Internal resistor type: 1/6 bias or 1/5 bias, 1/32 duty, and 1/16 duty
- Three selectable LCD frame frequencies: 64Hz, 89Hz or 170Hz
- Max. 128×32 patterns, 128 segments and 32 commons
- 144 segments and 16 commons selectable by command method
- Built-in bit-map display RAM: 4096 bits (=128×32 bits)
- Built-in internal resistor type bias generator
- Six-wire interface (four data wires)
- Eight kinds of time base/WDT selection
- Time base or WDT overflow output
- R/W address auto increment
- Built-in buzzer driver (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- Provides VLCD pin to adjust LCD operating voltage and max. VLCD voltage up to 7V
- Provides three kinds of bias current programming
- Control of TN-type and STN-type LCDs
- 208-pin QFP package

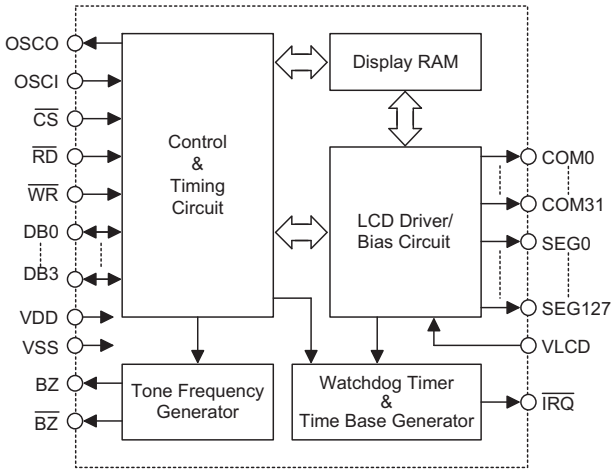
Applications

- Leisure products
- Games
- Personal digital assistant
- Cellular phone
- Global positioning system
- Consumer electronics

General Description

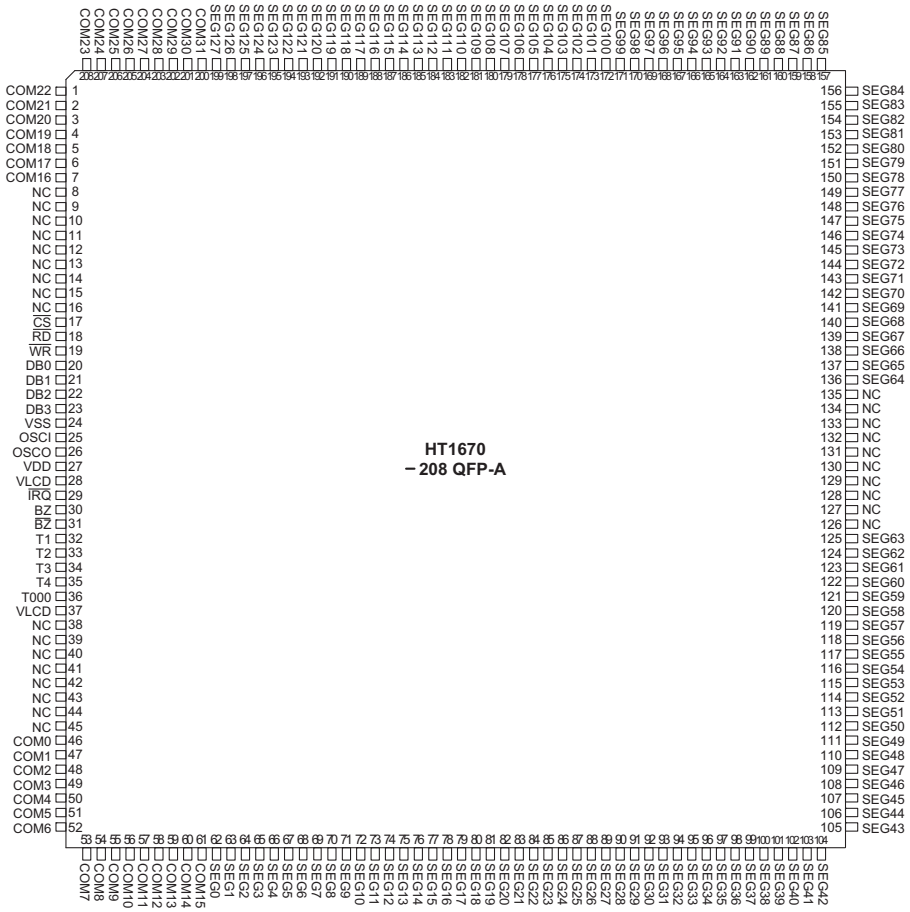
HT1670 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 4096 patterns (128 segments and 32 commons). It also supports four data bits interface, buzzer sound, Watchdog Timer or time base timer functions. The HT1670 is a memory mapping and multi-function LCD controller. Since the HT1670 can control TN-type (Twisted Nematic) or STN-type (Super Twisted Nematic) LCDs. The software configuration feature of the HT1670 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only six lines ($\overline{CS}$, $\overline{WR}$, DB0~DB3) are required for the interface between the host controller and the HT1670.

Block Diagram

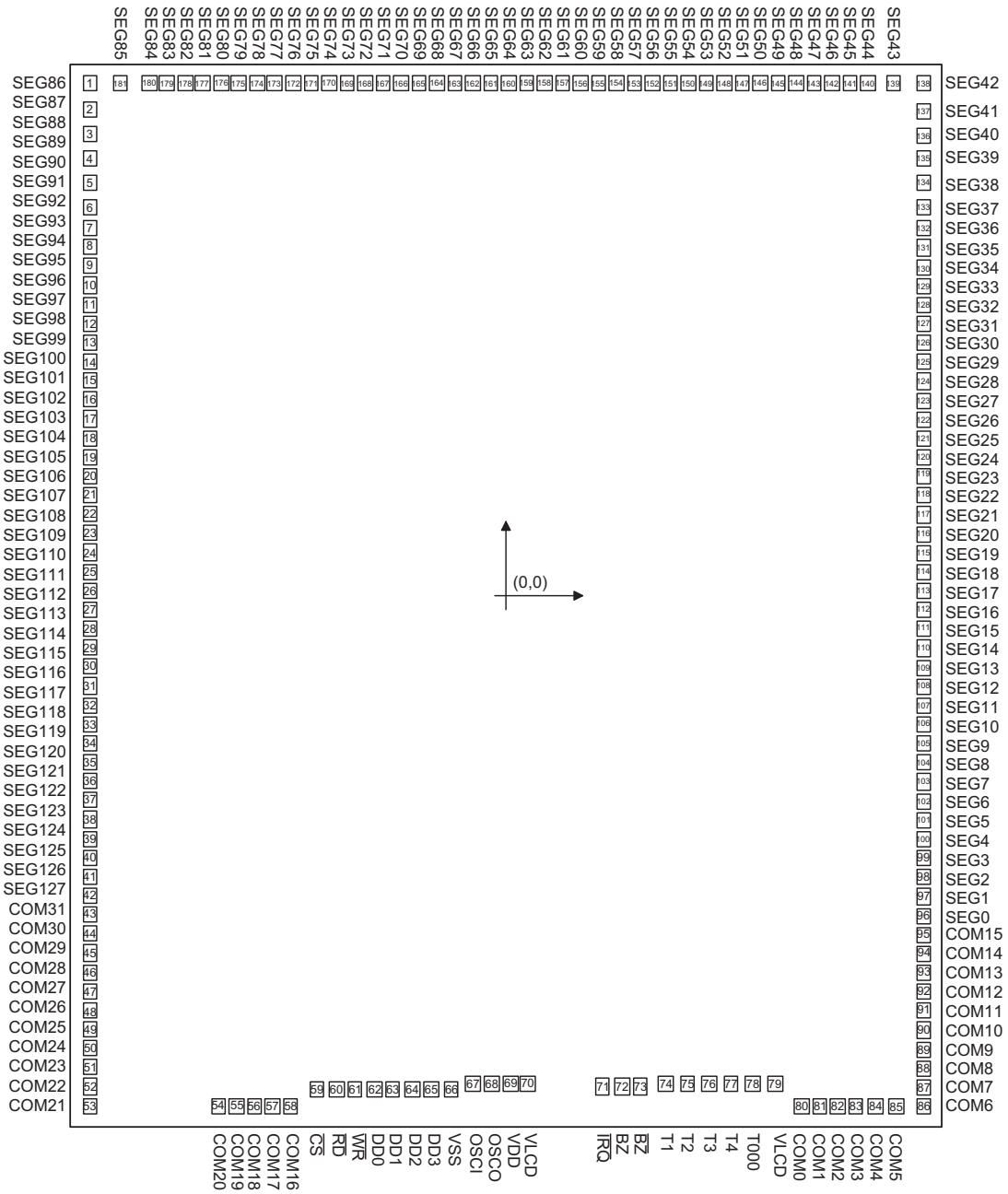


Note: CS: Chip selection
BZ, BZ: Tone outputs
WR, RD: WRITE clock, READ clock
DB0~DB3: Data bus
COM0~COM31, SEG0~SEG127: LCD outputs
IRQ: Time base or WDT overflow output

Pin Assignment



Pad Assignment



Chip size: 4620×5305 $(\mu m)^2$

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y	Pad No.	X	Y
1	–2203.000	2546.300	62	–697.300	–2463.250	123	2203.000	969.550
2	–2203.000	2413.950	63	–602.300	–2463.250	124	2203.000	1064.550
3	–2203.000	2293.950	64	–496.700	–2463.250	125	2203.000	1159.550

Pad No.	X	Y	Pad No.	X	Y	Pad No.	X	Y
4	−2203.000	2173.950	65	−401.700	−2463.250	126	2203.000	1254.550
5	−2203.000	2053.950	66	−292.850	−2463.250	127	2203.000	1349.550
6	−2203.000	1933.950	67	−179.350	−2434.850	128	2203.000	1444.550
7	−2203.000	1827.850	68	−79.050	−2434.850	129	2203.000	1539.550
8	−2203.000	1732.850	69	17.950	−2434.850	130	2203.000	1634.550
9	−2203.000	1637.850	70	113.100	−2434.850	131	2203.000	1729.550
10	−2203.000	1542.850	71	505.400	−2447.250	132	2203.000	1824.550
11	−2203.000	1447.850	72	611.000	−2447.250	133	2203.000	1930.650
12	−2203.000	1352.850	73	706.000	−2447.250	134	2203.000	2050.650
13	−2203.000	1257.850	74	842.450	−2432.500	135	2203.000	2170.650
14	−2203.000	1162.850	75	956.050	−2432.500	136	2203.000	2290.650
15	−2203.000	1067.850	76	1069.650	−2432.500	137	2203.000	2410.650
16	−2203.000	972.850	77	1183.250	−2432.500	138	2203.000	2546.300
17	−2203.000	877.850	78	1296.850	−2432.500	139	2043.000	2546.300
18	−2203.000	782.850	79	1420.400	−2432.500	140	1910.000	2546.300
19	−2203.000	687.850	80	1558.700	−2546.350	141	1815.000	2546.300
20	−2203.000	592.850	81	1653.700	−2546.350	142	1720.000	2546.300
21	−2203.000	497.850	82	1748.700	−2546.350	143	1625.000	2546.300
22	−2203.000	402.850	83	1843.700	−2546.350	144	1530.000	2546.300
23	−2203.000	307.850	84	1950.650	−2546.350	145	1435.000	2546.300
24	−2203.000	212.850	85	2058.700	−2546.350	146	1340.000	2546.300
25	−2203.000	117.850	86	2203.000	−2546.350	147	1245.000	2546.300
26	−2203.000	22.850	87	2203.000	−2451.350	148	1150.000	2546.300
27	−2203.000	−72.150	88	2203.000	−2356.350	149	1055.000	2546.300
28	−2203.000	−167.150	89	2203.000	−2261.350	150	960.000	2546.300
29	−2203.000	−262.150	90	2203.000	−2165.450	151	865.000	2546.300
30	−2203.000	−357.150	91	2203.000	−2070.450	152	770.000	2546.300
31	−2203.000	−452.150	92	2203.000	−1975.450	153	675.000	2546.300
32	−2203.000	−547.150	93	2203.000	−1880.450	154	580.000	2546.300
33	−2203.000	−642.150	94	2203.000	−1785.450	155	485.000	2546.300
34	−2203.000	−737.150	95	2203.000	−1695.450	156	390.000	2546.300
35	−2203.000	−832.150	96	2203.000	−1595.450	157	295.000	2546.300
36	−2203.000	−927.150	97	2203.000	−1500.450	158	200.000	2546.300
37	−2203.000	−1022.150	98	2203.000	−1405.450	159	105.000	2546.300
38	−2203.000	−1117.150	99	2203.000	−1310.450	160	10.000	2546.300
39	−2203.000	−1212.150	100	2203.000	−1215.450	161	−85.000	2546.300
40	−2203.000	−1307.150	101	2203.000	−1120.450	162	−180.000	2546.300
41	−2203.000	−1402.150	102	2203.000	−1025.450	163	−275.000	2546.300
42	−2203.000	−1497.150	103	2203.000	−930.450	164	−370.000	2546.300
43	−2203.000	−1592.150	104	2203.000	−835.450	165	−465.000	2546.300
44	−2203.000	−1687.150	105	2203.000	−740.450	166	−560.000	2546.300
45	−2203.000	−1782.150	106	2203.000	−645.450	167	−655.000	2546.300
46	−2203.000	−1877.150	107	2203.000	−550.450	168	−750.000	2546.300
47	−2203.000	−1972.150	108	2203.000	−455.450	169	−845.000	2546.300
48	−2203.000	−2067.150	109	2203.000	−360.450	170	−940.000	2546.300
49	−2203.000	−2162.150	110	2203.000	−265.450	171	−1035.000	2546.300
50	−2203.000	−2257.150	111	2203.000	−170.450	172	−1130.000	2546.300
51	−2203.000	−2352.150	112	2203.000	−75.450	173	−1225.000	2546.300
52	−2203.000	−2447.150	113	2203.000	19.550	174	−1320.000	2546.300
53	−2203.000	−2542.150	114	2203.000	114.550	175	−1415.000	2546.300
54	−1521.950	−2546.350	115	2203.000	209.550	176	−1510.000	2546.300
55	−1426.950	−2546.350	116	2203.000	304.550	177	−1605.000	2546.300
56	−1331.950	−2546.350	117	2203.000	399.550	178	−1700.000	2546.300
57	−1236.950	−2546.350	118	2203.000	494.550	179	−1795.000	2546.300
58	−1141.950	−2546.350	119	2203.000	589.550	180	−1890.000	2546.300
59	−1003.500	−2463.250	120	2203.000	684.550	181	−2043.000	2546.300
60	−897.900	−2463.250	121	2203.000	779.550			
61	−802.900	−2463.250	122	2203.000	874.550			

Pad Description

Pad No.	Pad Name	I/O	Description
1~42 96~181	SEG86~SEG127 SEG0~SEG85	O	LCD segment outputs
43~58 80~95	COM31~COM16 COM0~COM15	O	LCD common outputs, under 144×16 command mode, COM16~COM31 will share to SEG128~SEG143. COM31/SEG128, COM30/SEG129, COM29/SEG130....., COM18/SEG141, COM17/SEG142, COM16/SEG143
59	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or write to the HT1670 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at a logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1670 are all enabled.
60	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the HT1670 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next rising edge to latch the clocked out data.
61	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1670 on the rising edge of the $\overline{WR}$ signal.
62~65	DB0~DB3	I/O	Parallel data input/output with a pull-high resistor
66	VSS	—	Negative power supply for logic circuit, ground
67 68	OSCI OSCO	I O	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected, the OSCI and OSCO pads can be left open.
69	VDD	—	Positive power supply for logic circuit
70, 79	VLCD	I	Power supply for LCD driver circuit
71	$\overline{IRQ}$	O	Time base or Watchdog Timer overflow flag, NMOS open drain output.
72, 73	BZ, $\overline{BZ}$	O	2kHz or 4kHz frequency output pair (tristate output buffer)
74~78	T1~T4, T000	I	Vary bias current pin It is usually not connected

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+5.5V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... –25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.7	—	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillator	—	150	250	μA
		5V		—	250	370	μA
I_{DD2}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	135	200	μA
		5V		—	200	300	μA
I_{DD11}	Operating Current	3V	No load/LCD OFF On-chip RC oscillator	—	15	30	μA
		5V		—	50	70	μA
I_{DD22}	Operating Current	3V	No load/LCD OFF Crystal oscillator	—	2	10	μA
		5V		—	3	10	μA
I_{STB}	Standby Current	3V	No load, Power down mode	—	—	1	μA
		5V		—	—	2	μA
V_{IL}	Input Low Voltage	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3	V
		5V		4.0	—	5	V
I_{OL1}	BZ, $\overline{BZ}$, $\overline{IRQ}$ Sink Current	3V	V_{OL}=0.3V	1.2	2.5	—	mA
		5V	V_{OL}=0.5V	3	6	—	mA
I_{OH1}	BZ, $\overline{BZ}$ Source Current	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–2	–4	—	mA
I_{OL2}	DB0~DB3 Sink Current	3V	V_{OL}=0.3V	1.2	2.5	—	mA
		5V	V_{OL}=0.5V	3	6	—	mA
I_{OH2}	DB0~DB3 Source Current	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–2	–4	—	mA
I_{OL3}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	160	—	μA
		5V	V_{OL}=0.5V	180	360	—	μA
I_{OH3}	LCD Common Source Current	3V	V_{OH}=2.7V	–40	–80	—	μA
		5V	V_{OH}=4.5V	–90	–180	—	μA
I_{OL4}	LCD Segment Sink Current	3V	V_{OL}=0.3V	50	100	—	μA
		5V	V_{OL}=0.5V	120	240	—	μA
I_{OH4}	LCD Segment Source Current	3V	V_{OH}=2.7V	–30	–60	—	μA
		5V	V_{OH}=4.5V	–70	–140	—	μA
R_{PH}	Pull-high Resistor	3V	DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	150	250	410	kΩ
		5V		60	125	210	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	5V	On-chip RC oscillator	24	32	40	kHz
f_{SYS2}	System Clock	—	Crystal oscillator	—	32768	—	Hz
f_{SYS3}	System Clock	—	External clock source	—	32768	—	Hz
f_{LCD1}	LCD Frame Frequency	5V	On-chip RC oscillator	61/117	89/170	111/213	Hz
f_{LCD2}	LCD Frame Frequency	—	Crystal oscillator	—	64	—	Hz
f_{LCD3}	LCD Frame Frequency	—	External clock source	—	64	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	sec
f_{CLK1}	4-Bit Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	—	—	150	kHz
		5V		—	—	300	kHz
f_{CLK2}	4-Bit Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
t_{CS}	4-Bit Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	150	250	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	—	μs
			Read mode	6.67			
		5V	Write mode	1.67	—	—	μs
			Read mode	3.34			
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	—	—	120	160	ns
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	80	120	—	ns
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	60	120	—	ns
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	50	100	—	ns
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	50	100	—	ns
f_{tone2k}	Tone Frequency	5V	On-chip RC oscillator	1.5	2.0	2.5	kHz
f_{tone4k}	Tone Frequency	5V	On-chip RC oscillato	3.0	4.0	5.0	kHz

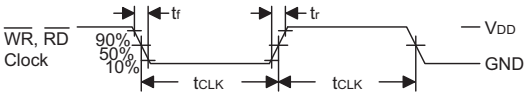


Figure 1

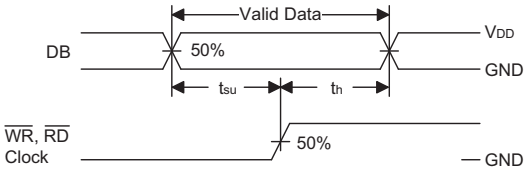


Figure 2

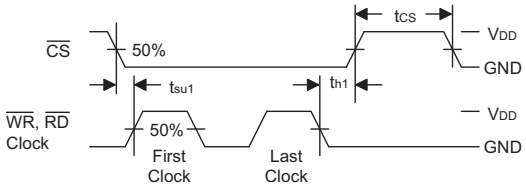


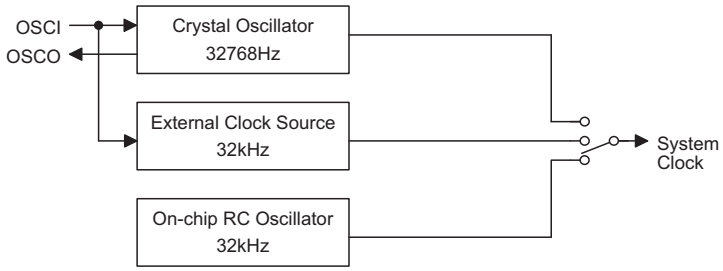
Figure 3

Functional Description

System Oscillator

The HT1670 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The clock source may be from an on-chip RC oscillator (32kHz), a crystal oscillator (32.768kHz), or an external 32kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT loses its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, thus serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 32kHz clock source operation. At the initial system power on, the HT1670 is at the SYS DIS state.



System Oscillator Configuration

Display Memory – RAM Structure

The static display RAM is organized into 1024×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

	00H	08H	10H	18H	20H - - - - - - - - - 3D8H	3E0H	3E8H	3F0H	3F8H
COM0	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM1	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM2	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM3	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	01H	**09H**	**11H**	**19H**	**21H - - - - - - - - - 3D9H**	**3E1H**	**3E9H**	**3F1H**	**3F9H**
COM4	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM5	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM6	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM7	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	02H	**0AH**	**12H**	**1AH**	**22H- - - - - - - - - 3DAH**	**3E2H**	**3EAH**	**3F2H**	**3FAH**
COM8	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM9	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM10	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM11	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	03H	**0BH**	**13H**	**1BH**	**23H- - - - - - - - - 3DBH**	**3E3H**	**3EBH**	**3F3H**	**3FBH**
COM12	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM13	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM14	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM15	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	04H	**0CH**	**14H**	**1CH**	**24H- - - - - - - - - 3DCH**	**3E4H**	**3ECH**	**3F4H**	**3FCH**
COM16	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM17	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM18	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM19	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	05H	**0DH**	**15H**	**1DH**	**25H- - - - - - - - - 3DDH**	**3E5H**	**3EDH**	**3F5H**	**3FDH**
COM20	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM21	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM22	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM23	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	06H	**0EH**	**16H**	**1EH**	**26H- - - - - - - - - 3DEH**	**3E6H**	**3EEH**	**3F6H**	**3FEH**
COM24	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM25	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM26	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM27	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	07H	**0FH**	**17H**	**1FH**	**27H - - - - - - - - - 3DFH**	**3E7H**	**3EFH**	**3F7H**	**3FFH**
COM28	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM29	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM30	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM31	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	SEG0	**SEG1**	**SEG2**	**SEG3**		**SEG124**	**SEG125**	**SEG126**	**SEG127**

128×32 Selection Mode RAM Mapping Table

	00H	04H	08H	0CH	10H - - - - - - - - - 22CH	230H	234H	238H	23CH
COM0	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM1	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM2	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM3	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	01H	**05H**	**09H**	**0DH**	**11H - - - - - - - - - 22DH**	**231H**	**235H**	**239H**	**23DH**
COM4	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM5	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM6	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM7	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	02H	**06H**	**0AH**	**0EH**	**12H - - - - - - - - - 22EH**	**232H**	**236H**	**23AH**	**23EH**
COM8	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM9	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM10	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM11	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	03H	**07H**	**0BH**	**0FH**	**13H - - - - - - - - - 22FH**	**233H**	**237H**	**23BH**	**23FH**
COM12	Bit0	Bit0	Bit0				Bit0	Bit0	Bit0
COM13	Bit1	Bit1	Bit1				Bit1	Bit1	Bit1
COM14	Bit2	Bit2	Bit2				Bit2	Bit2	Bit2
COM15	Bit3	Bit3	Bit3				Bit3	Bit3	Bit3
	SEG0	**SEG1**	**SEG2**	**SEG3**		**SEG140**	**SEG141**	**SEG142**	**SEG143**

144×16 Selection Mode RAM Mapping Table

Name	Command Code	Function
144×16 Mode	X**100**-0001-1111-XXXX	Change segment from 144 to 96 and common from 32 to 16
The default value after power ON reset is 128×32 mode, set "Normal" command will change 144×16 mode to 128×32 mode.		

Frame Frequency

HT1670 provides three kinds of frame frequency option by command code; 64Hz, 89Hz and 170Hz respectively. FRAME 64Hz provides 64Hz frame frequency. FRAME 89Hz provides 89Hz frame frequency. FRAME 170Hz provides 170Hz frame frequency.

Name	Command Code	Function
FRAME 170Hz	X**100**-0001-1000-XXXX	Select 170Hz frame frequency
FRAME 89Hz	X**100**-0001-1101-XXXX	Select 89Hz frame frequency
FRAME 64Hz	X**100**-0001-1110-XXXX	Select 64Hz frame frequency

Frame Frequency Selection Command Code

Time Base and Watchdog Timer – WDT

The time base generator and WDT share the same counter which is divided by 256. The $\overline{IRQ}$ clock can be programmed as 1Hz, 2Hz, ..., 128Hz output. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will remain at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.

If an external clock is selected as the system frequency source, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer Tone Output

A simple tone generator is implemented in the HT1670. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

By executing the TONE 4K and TONE 2K commands there are two tone frequency outputs selectable that can turn on the tone output. The TONE 4K and TONE 2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned off by invoking the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

Command Format

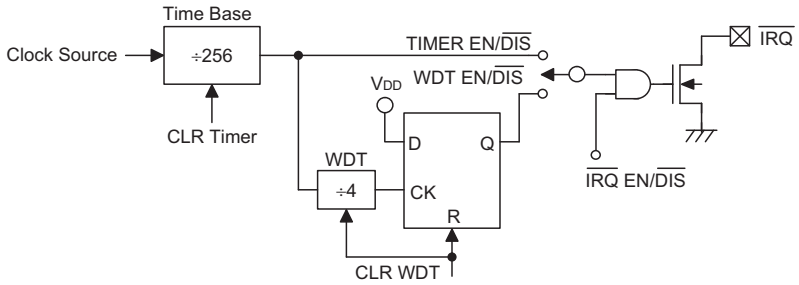
The HT1670 can be configured by software setting. There are two mode commands to configure the HT1670 resource and to transfer the LCD display data.

The configuration mode of the HT1670 is called command mode, and its command mode ID is 100. The command mode consists of a system configuration command, a system frequency selection command, an LCD configuration command, a tone frequency selection command, a bias current selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode ID and the command mode ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will also be reset. The $\overline{CS}$ pin returns to "0", so a new operation mode ID should be issued first.



Time Base and WDT Configurations

Name	Command Code	Function
TONE OFF	**X100**-0000-1000-XXXX	Turn-off tone output
TONE 4K	**X100**-0001-0000-XXXX	Turn-on tone output, tone frequency is 4kHz
TONE 2K	**X100**-0001-0001-XXXX	Turn-on tone output, tone frequency is 2kHz

Buzzer Tone Output Command Code

The following are the data mode ID and the command ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive address data mode, the $\overline{CS}$ pin should be set 1 and the previous operation mode will also be reset. The $\overline{CS}$ pin returns to 0, so a new operation mode ID should be issued first.

Bias Generator

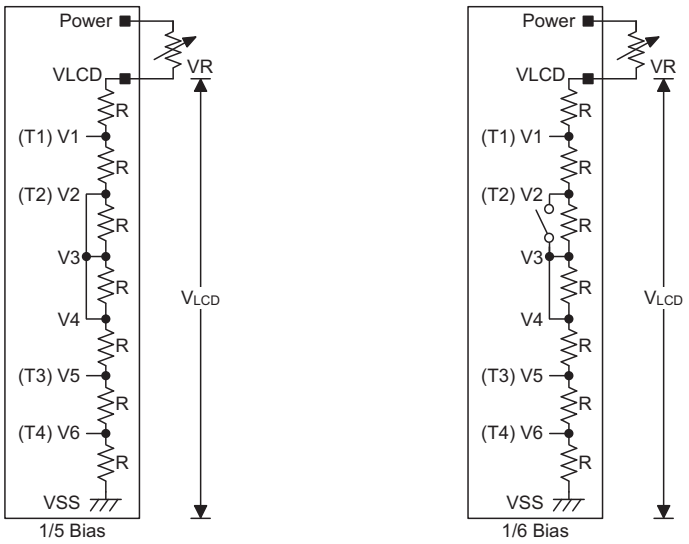
The HT1670 bias voltage belongs to internal resistor type. It provides two kinds of bias option named 1/6 bias and 1/5 bias respectively. It also provides three kinds of bias current option by programming to suitably drive an LCD panel. The three kinds of bias current are large, middle, and small, respectively. Usually, large panel LCD can be excellently displayed by large bias current. Relatively, it consumes large current when LCD ON command is used. Small bias current provides low power consumption during on condition when the LCD is normally displayed. The following are the reference value table.

When the bias current for LCD is more than Large Bias Current setting. It is recommended to add external circuit to increase driving current.

Interfacing

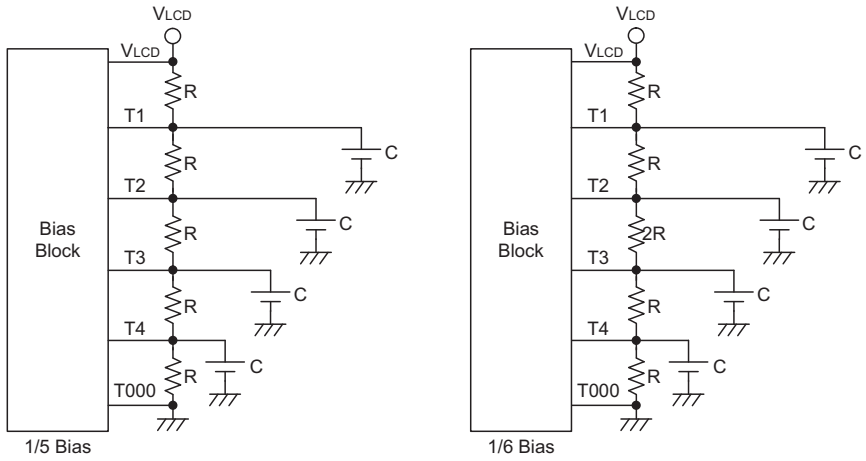
Only six lines are required to interface with the HT1670. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1670. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the HT1670 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1670. The DB0~DB3 are the 4-bit parallel data input/output lines. Data to be read or written or commands to be written have to pass through the DB0~DB3 lines. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DB0~DB3 lines. It is recommended that the host controller read correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DB0~DB3 lines are all clocked into the HT1670 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the HT1670. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by connecting with the $\overline{IRQ}$ pin of the HT1670.

Bias	VLCD	Large Bias Current	Middle Bias Current	Small Bias Current
1/5	3V	165μA	70μA	30μA
	5V	270μA	110μA	50μA
1/6	3V	140μA	55μA	25μA
	5V	225μA	90μA	40μA



Internal Resistor Type Bias Generator Configurations

Note: The voltage applied to V_{LCD} pin must be equal to or lower than 7V.
Adjust VR to fit LCD display.

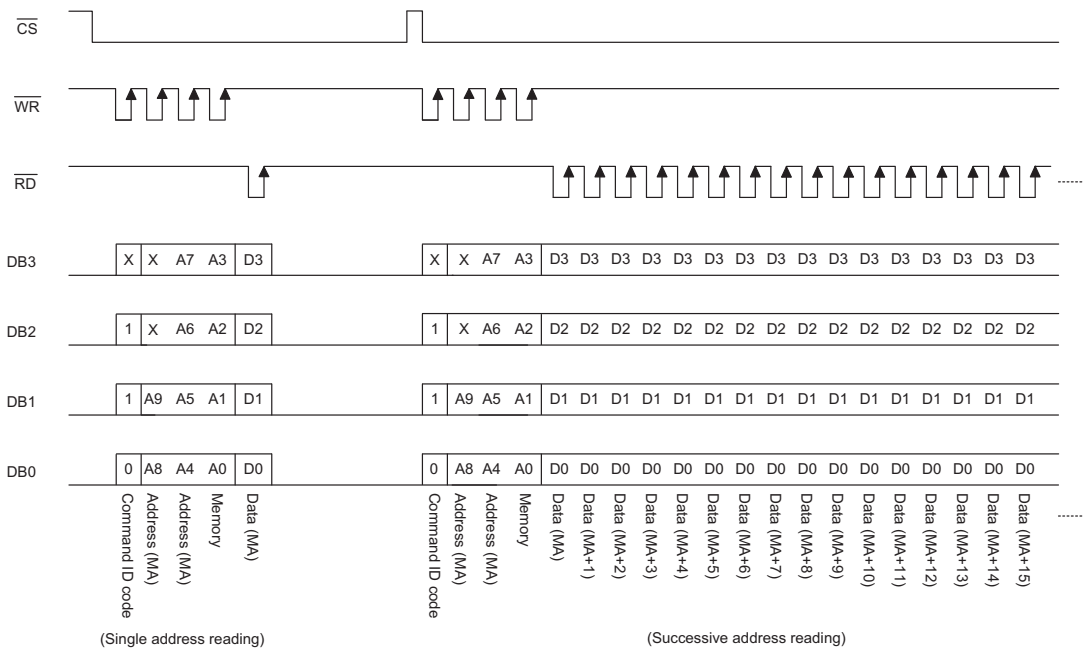


Increase Driver Current Configurations

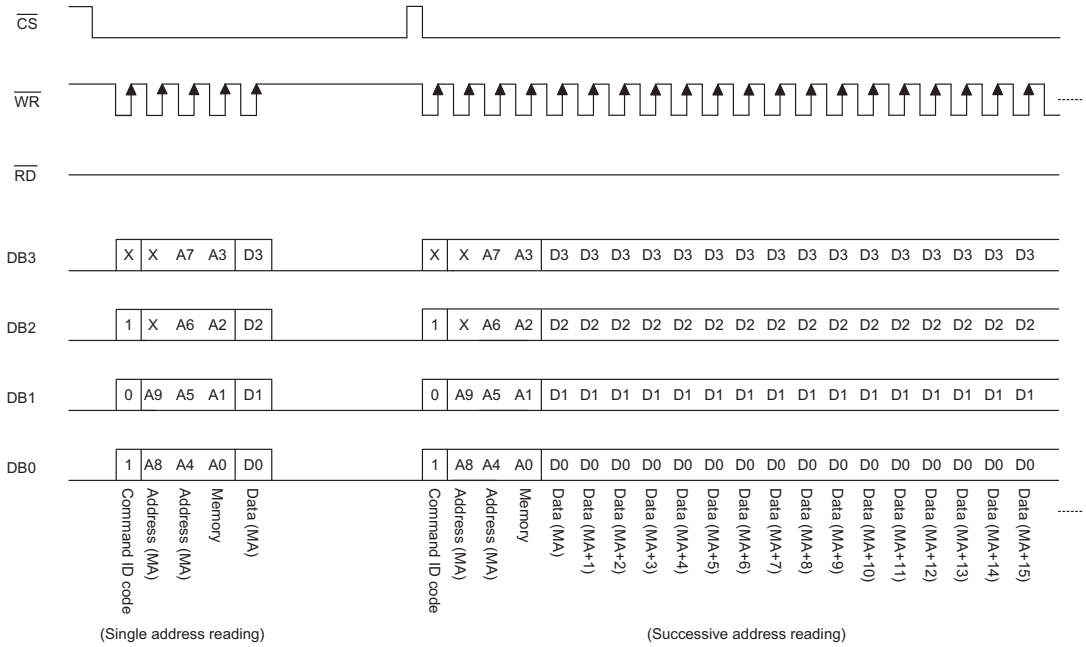
Note: The external resistors are used to increment the driving current.
And the external capacitors are used to keep the bias voltage stable.

Timing Diagrams

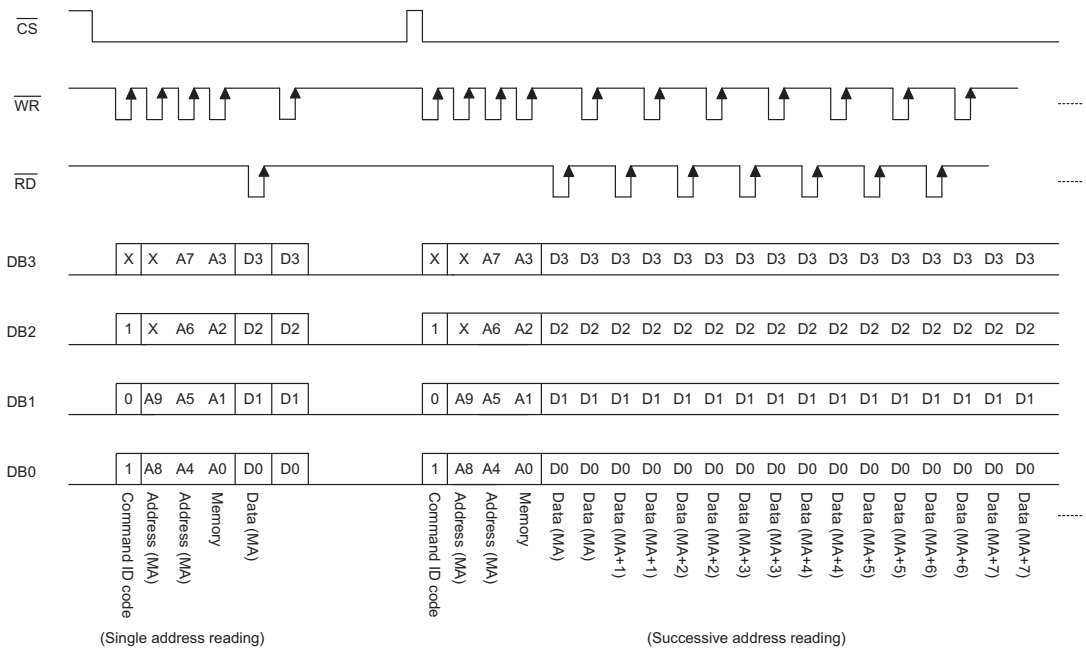
READ Mode (Command ID Code: 1 1 0)



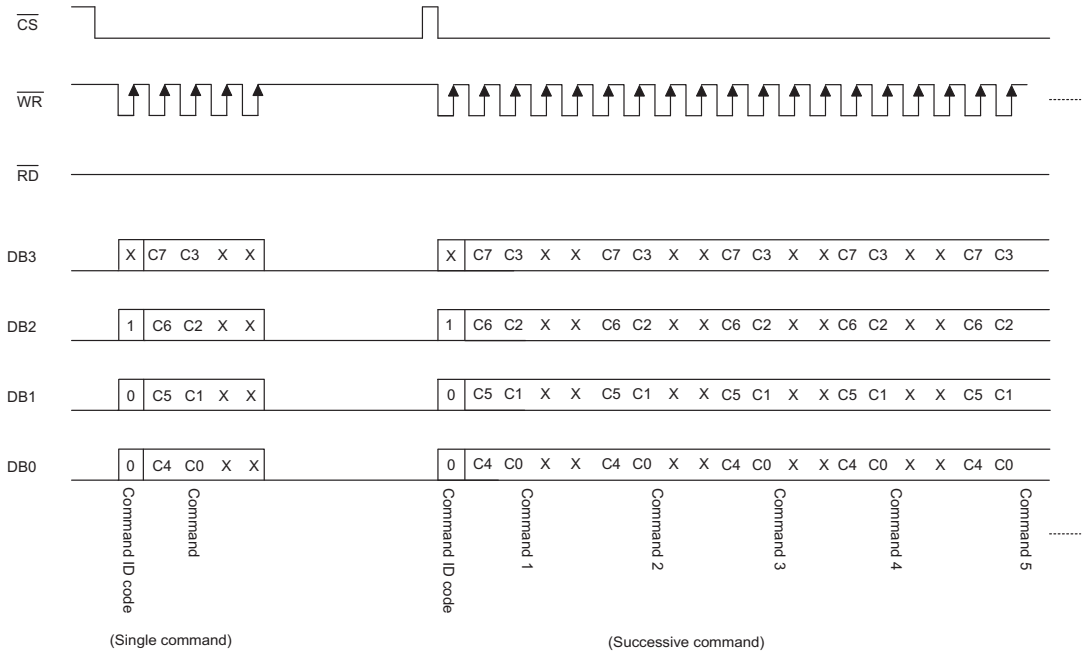
WRITE Mode (Command ID Code: 1 0 1)



READ-MODIFY-WRITE Mode (Command ID Code: 1 0 1)



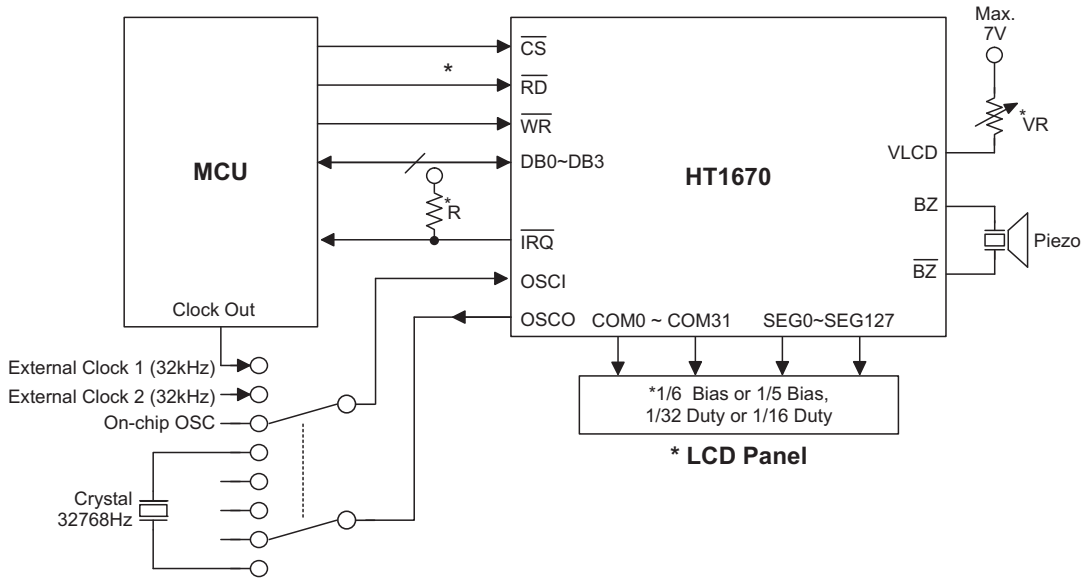
Command Mode (Command ID Code: 1 0 0)



Note: "X" stands for don't care

Application Circuits

Host Controller With an HT1670 Display System



*Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the MCU.

Adjust VR to fit LCD display

Adjust R (external pull-high resistance) to fit user's time base clock.

It is recommended that the internal equivalent capacitance between SEG and COM of LCD panel should be lower than 10pF. (LCR meter test condition: frequency in 1kHz)

Instruction Set Summary

Name	Command Code	D/C	Function	Def.
READ	X110-XXA9A8-A7A6A5A4-A3A2A1A0-D3D2D1D0	D	Read data from the RAM	
WRITE	X101-XXA9A8-A7A6A5A4-A3A2A1A0-D3D2D1D0	D	Write data to the RAM	
READ-MODIFY-WRITE	X101-XXA9A8-A7A6A5A4-A3A2A1A0-D3D2D1D0	D	Read and Write data to the RAM	
SYS DIS	X100-0000-0000-XXXX-XXXX	C	Turn Off both system oscillator and LCD bias generator	Yes
SYS EN	X100-0000-0001-XXXX-XXXX	C	Turn On system oscillator	
LCD OFF	X100-0000-0010-XXXX-XXXX	C	Turn Off LCD display	Yes
LCD ON	X100-0000-0011-XXXX-XXXX	C	Turn On LCD display	
TIMER DIS	X100-0000-0100-XXXX-XXXX	C	Disable time base output	Yes
WDT DIS	X100-0000-0101-XXXX-XXXX	C	Disable WDT time-out flag output	Yes
TIMER EN	X100-0000-0110-XXXX-XXXX	C	Enable time base output	
WDT EN	X100-0000-0111-XXXX-XXXX	C	Enable WDT time-out flag output	
TONE OFF	X100-0000-1000-XXXX-XXXX	C	Turn Off tone outputs	Yes
CLR TIMER	X100-0000-1101-XXXX-XXXX	C	Clear the contents of the time base generator	
CLR WDT	X100-0000-1111-XXXX-XXXX	C	Clear the contents of the WDT stage	
TONE 4K	X100-0001-0000-XXXX-XXXX	C	Turn on tone output, tone frequency output: 4kHz	
TONE 2K	X100-0001-0001-XXXX-XXXX	C	Turn on tone output, tone frequency output: 2kHz	
IRQ DIS	X100-0001-0010-XXXX-XXXX	C	Disable $\overline{\text{IRQ}}$ output	Yes
IRQ EN	X100-0001-0011-XXXX-XXXX	C	Enable $\overline{\text{IRQ}}$ output	
RC 32K	X100-0001-0100-XXXX-XXXX	C	System clock source, on-chip RC oscillator	Yes
EXT (X′TAL)	X100-0001-0101-XXXX-XXXX	C	System clock source, external 32kHz clock source or crystal oscillator 32.768kHz	
LARGE BIAS	X100-0001-0110-XXXX-XXXX	C	Large bias current option	Yes
MIDDLE BIAS	X100-0001-0111-XXXX-XXXX	C	Middle bias current option	
SMALL BIAS	X100-0001-1000-XXXX-XXXX	C	Small bias current option	
BIAS 1/6	X100-0001-1010-XXXX-XXXX	C	LCD 1/6 bias option	Yes
BIAS 1/5	X100-0001-1001-XXXX-XXXX	C	LCD 1/5 bias option	
FRAME 170Hz	X100-0001-1100-XXXX-XXXX	C	Selects 170Hz frame frequency	
FRAME 89Hz	X100-0001-1101-XXXX-XXXX	C	Selects 89Hz frame frequency	
FRAME 64Hz	X100-0001-1110-XXXX-XXXX	C	Selects 64Hz frame frequency	Yes
Select 144×16	X100-0001-1111-XXXX-XXXX	C	This command will change segment from 128 to 144 and common from 32 to 16	
F1	X100-1010-0000-XXXX-XXXX	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	X100-1010-0001-XXXX-XXXX	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	X100-1010-0010-XXXX-XXXX	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	

Name	Command Code	D/C	Function	Def.
F8	X100-1010-0011-XXXX-XXXX	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	X100-1010-0100-XXXX-XXXX	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	X100-1010-0101-XXXX-XXXX	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	X100-1010-0110-XXXX-XXXX	C	Time base clock output: 96Hz The time-out flag after: 1/16s	
F128	X100-1010-0111-XXXX-XXXX	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	X100-1111-1111-XXXX-XXXX	C	Test mode, user don't use.	
NORMAL	X100-1111-1110-XXXX-XXXX	C	Normal mode, 128×32 mode will be set	Yes

Note: "X" stands for don't care

A9~A0: RAM address

D3~D0: RAM data

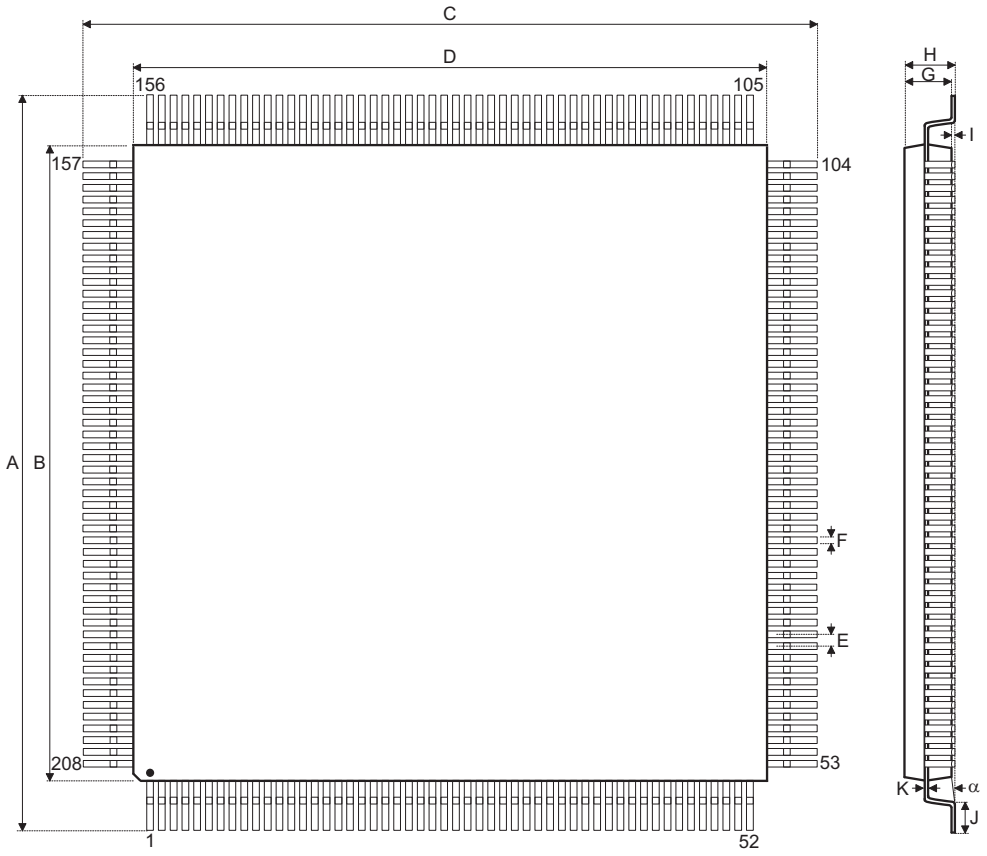
D/C: Data/Command mode

Def.: Power-on reset default

All the bold forms, namely **1 1** 0, **1 0** 1, and **1 0** 0, are mode commands. Of these, **1 0** 0 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The tone frequency source and the time base/WDT clock frequency source can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1670 after power-on reset, otherwise, power on reset may fail, which in turn leads to the malfunctioning of the HT1670.

Package Information

208-pin QFP (28mm×28mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	1.220	—	1.236
B	1.098	—	1.106
C	1.220	—	1.236
D	1.098	—	1.106
E	—	0.020	—
F	—	0.008	—
G	0.098	—	0.122
H	—	—	0.134
I	—	0.004	—
J	0.014	—	0.026
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	31.00	—	31.40
B	27.90	—	28.10
C	31.00	—	31.40
D	27.90	—	28.10
E	—	0.50	—
F	—	0.20	—
G	3.10	—	3.40
H	—	—	3.70
I	—	0.10	—
J	0.35	—	0.65
K	0.10	—	0.20
α	0°	—	7°

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