HT16A102
OLED Driver IC

Features

- Support max. 96 x 64 matrix panel
- Power supply to logic system, 2.4V -3.6V
- Power supply to OLED system, 7.0V-16V
- Segment output maximum current : 315uA
- Common sink maximum current: 40mA
- 6-bits global constant current brightness setting, from 5uA ~ 315uA
- Low current standby mode(<20.0uA)
- Sleep mode current (<5uA, keep RST pin low)
- 16 Gray Scale setting for each output terminal with pulse width modulation.
- Binary/Gray Scale mode selectable
- Flash mode support
- External current reference control by external resistor
- On-Chip Oscillator
- Programmable Frame Rate
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface and 4-wire SPI Interface
- Embedded 96*64*4 bit SRAM display buffer
- Vertical scrolling
- Support Partial display
- Wide range of operating temperatures : -30 to 85 °C
- Current matching accuracy : ±3% intra-die(channel to channel), ±3% inter-die(chip to chip)
- Pre-charge function
- Reverse bias
- Build-in DC-DC function
- Build-in Regulator function control by external resistor

Gernal Description

The HT16A102 OLED Driver IC supports 96*64 OLED panel displays. Larger maximum current capability for per channel let user has flexible choose for OLED panel.

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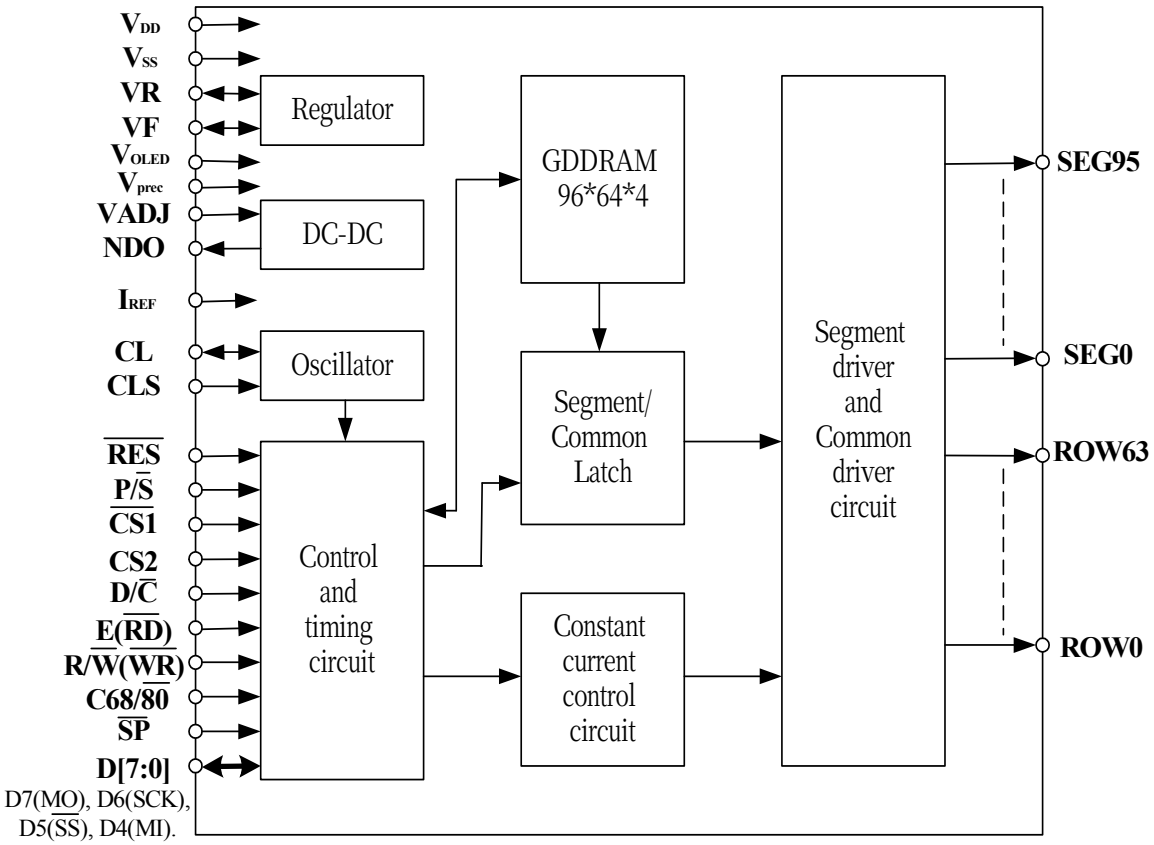
Block Diagram



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Pad Description

M

This pin is the frame signal input/output. In master mode, this pin supplies frame signal to slave devices while in slave mode, this pin receives frame signal from the master device.

CL

This pin is the system clock input/output. In master mode with internal oscillator enabled (CLS pin pulled high), this pin supplies display clock signal to slave devices. In slave mode or when internal oscillator is disabled, this pin receives display clock signal from the master device or external clock source.

$\overline{\text{DOF}}$

This pin is display blanking control between master and slave devices. In master mode, this pin supplies on/off signal to slave devices. In slave mode, this pin receives on/off signal from the master device.

M/$\overline{\text{S}}$

This pin is the master/slave mode selection input. When this pin is pulled high, master mode is selected, CL, M and $\overline{\text{DOF}}$ signals will be output for slave devices. When this pin is pulled low, slave mode is selected, which CL, $\overline{\text{M}}$, DOF are required to be input from master device.

CLS

This pin is internal clock enable. When this pin is pulled high, internal clock is enabled. The internal clock will be disabled when it is pulled low, an external clock source must be connected to CL pin for normal operation.

CS1, CS2

These pins are the chip select inputs. The chip is enabled for MCU communication only when $\overline{\text{CS1}}$ is pulled low and CS2 is pulled high.

$\overline{\text{RES}}$

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

D/$\overline{\text{C}}$

This pin is Data/Command control pin. When the pin is pulled high, the data at D7-D0 is treated as display data. When the pin is pulled low, the data at D7-D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/$\overline{\text{W}}$($\overline{\text{WR}}$)

This pin is MCU interface input. When interfacing to an 6800-series microprocessor, this pin will be used as Read/Write (R/$\overline{\text{W}}$) selection input. Read mode will be carried out when this pin is pulled high and write mode when low. When 8080 interface mode is selected, this pin will be the $\overline{\text{W}}$rite (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected.

E ($\overline{\text{RD}}$)

This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected. When connecting to an 8080-microprocessor this pin receives the $\overline{\text{R}}$ead (RD) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.

D_7-D_0

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D_7 is the serial data output MO and D_6 is the serial clock input SCK, D_5 is the slave select input signal ($\overline{\text{SS}}$) and D_4 is the serial data input MI.

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V_{OLED}
This pin is the reference for OLED driving voltages (high voltage 16V). It could be supplied by internel DC-DC circuit or external high voltage power.

Vprec
This pin is the external precharge voltage for OLED driving voltages. It could be connected to VR pin or supplied by external power source.

V_{DD}
Chip's Power Supply pin (for logic). It must be connected to external source.

V_{SS}
Ground. A reference for the logic pins. It must be connected to external ground.

C68/ $\overline{80}$
This pin is MCU parallel interface selection input. When the pin is pulled high, 6800 series interface is selected and when the pin is pulled low, 8080 series interface is selected.
If Serial Interface is selected (P/ $\overline{S}$ and $\overline{SP}$ pulled low), the setting of this pin is ignored, but must be connected to a known logic (either high or low).

P/ $\overline{S}$
This pin is parallel interface selection input. When this pin is pulled high, parallel interface mode is selected. When this pin and $\overline{SP}$ pins are pulled low, serial interface is selected.
Note: Read data operation is only available in parallel mode and SPI interface in serial mode.

$\overline{SP}$
This input pin cintrol serial interface type. Both P/ $\overline{S}$ and $\overline{SP}$ pulled low, serial mode by data shift method is selected. P/ $\overline{S}$ is low and $\overline{SP}$ is pulled high, then SPI mode is selected.

NDO
This pin is output pin to control external NMOS for voltage charge.

VADJ
This pin is input pin for DC-DC function to adjust the DC-DC output voltage.

VR/VF
There are I/O pin, connect to external component for regulator function.

ROW0-ROW63
These pins provide the Common driving signals to the OLED panel.

SEG0-SEG95
These pins provide the OLED segment driving signals. The output voltage level of these pins is in high impedance stage when display is off.

IREF
This pin is current reference pin. A resistor should be connected between this pin and Vss.

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Function Block Descriptions

Command Decoder and Command Interface
This module determines whether the input data is interpreted as data or command. According to D/C pin, if D/C pin is high, data will be written to Graphic Display Data RAM(GDDRAM). If D/C pin is low, the input D7 ~ D0 will be interpreted as Command and it will be decoded and written to its corresponding command register.

Microprocessor Interface

a. Chip select input
There are CS1 and CS2 pins for chip selection. The HT16A102 can be enabled when CS1 is Low and CS2 is High. When these pins are set to any other combination, D/C, E(RD) and R/W(WR) inputs are disables and D7 to D0 are to be high impedance.

b. Interface

Parallel / Serial interface mode

P/S	Type	CS1	CS2	C68/80	Interface mode
H	Parallel	CS1	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1	CS2	X*	Serial MPU mode

*. X: Don't care

c. Parallel interface (P/S = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68/80 as shown in the following table.
The type of data transfer is determined by signals at D/C, E(RD), and R/W(WR).

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Microprocessor selection for parallel interface

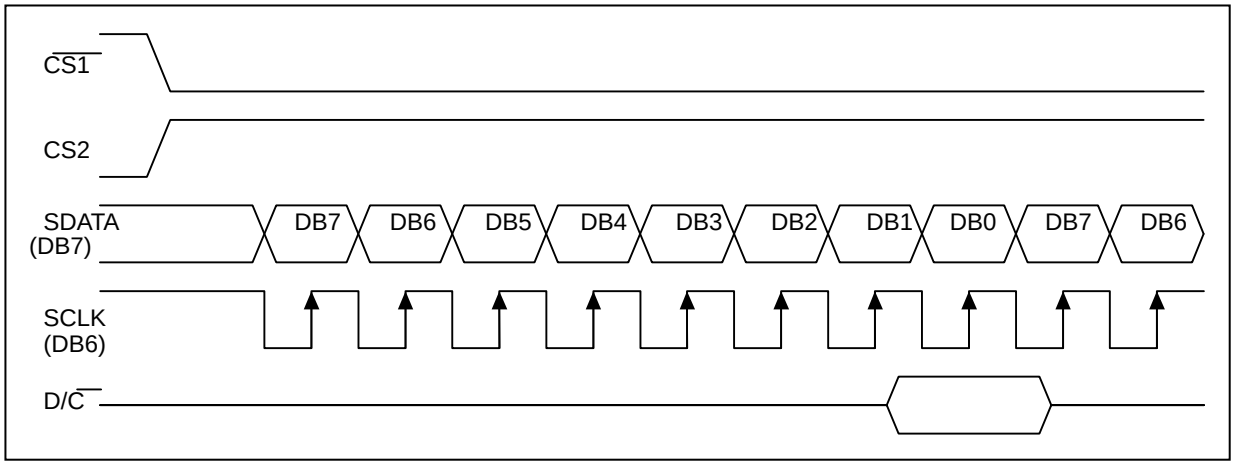
C60/$\overline{80}$	$\overline{CS1}$	CS2	D/$\overline{C}$	E($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)	DB7 to DB0	MPU
H	$\overline{CS1}$	CS2	D/$\overline{C}$	E	R/$\overline{W}$	DB7 to DB0	6800-series
L	$\overline{CS1}$	CS2	D/$\overline{C}$	$\overline{RD}$	$\overline{WR}$	DB7 to DB0	8080-series

Parallel data transfer

Common	6800-series		8080-series		Description
D/$\overline{C}$	E($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)	E($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register command read
L	H	L	H	L	Writes to internal register(command)

d. Serial interface (P/$\overline{S}$ = "L")

Set P/$\overline{S}$ = “0” and $\overline{PS}$ = “0”, the HT16A102 is active and serial interface has been selected, the serial data SDATA (DB7) and the serial clock SCLK (DB6) inputs are enabled.
The serial data can be read on the rising edge of the serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock.
The serial data input is display data when D/$\overline{C}$ is high and control data when D/$\overline{C}$ is low.
Reading is not possible while serial interface mode is activated.



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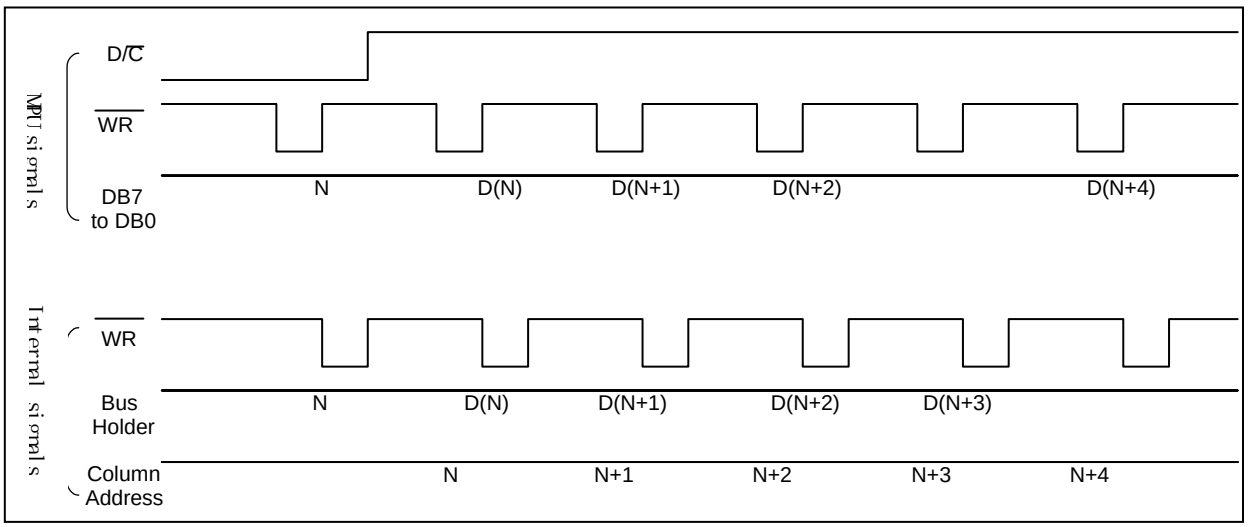
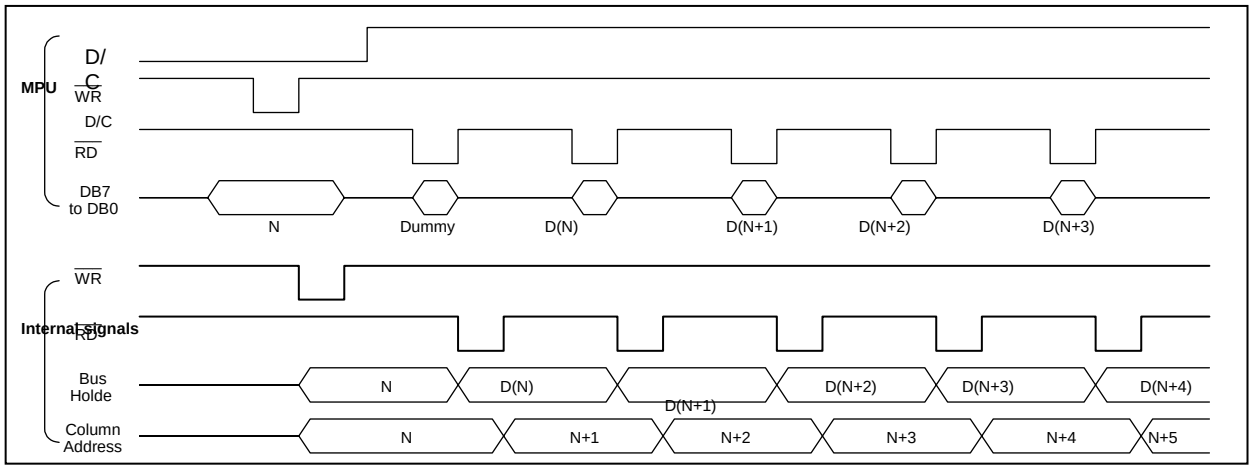
Serial interface timing

e. Data accessing

The HT16A102 uses bus holder and internal data bus for data read and data write with the MPU. When writing data from the MPU to on-chip RAM, the data is automatically transferred from the bus holder to the on-chip RAM as shown in the following figure. When the MPU reads data from on-chip RAM, the first data read cycle stores the data in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle. This means the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data. Therefore, a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed.



Write timing figure



Read timing Figure

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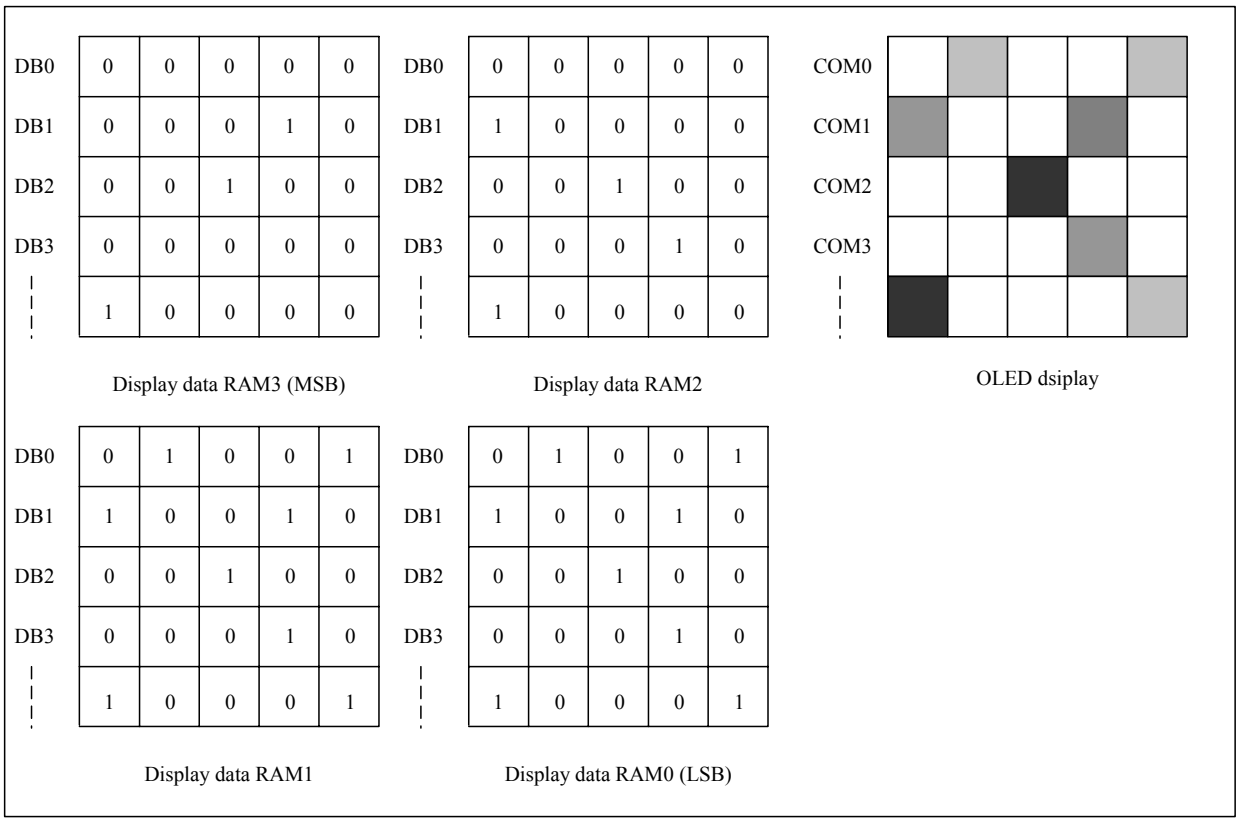
DISPLAY DATA RAM (DDRAM)

The DDRAM stores pixel data for the OLED. It has 64-row (8 page x 8 bit) by 96-column addressable array. Each pixel can be selected by specifying the page and the column address. The 64 rows are divided into 8 pages of 8 lines. Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the MPU correspond to the OLED common direction as shown in the following figure. The MPU can read from and write to DDRAM through the I/O buffer, which is independent operation from signal reading for the OLED driver. This independent operation makes it possible that the MPU writes the data into the DDRAM at the same time as data is being displayed without causing the OLED flicker. HT16A102 OLED driver support 16 step Gray Scale function, user need to write 4 bits data (one pixel) to the corresponding DDRAM (LSB first). For example, user want to write data into page0 and column0 address, first, user need to set page0 command and column0 command, then write 4 byte data (LSB byte first and MSB byte last), {(DB7GS0, DB6GS0, …DB1GS0, DB0GS0), (DB7GS1, DB6GS1, …DB1GS1, DB0GS1), (DB7GS2, DB6GS2, …DB1GS2, DB0GS2), (DB7GS3, DB6GS3, …DB1GS3, DB0GS3)}, GSx data means Gray Scale data setting. HT16A102 will increment write DDRAM address automatically after user write 4 times (one pixel has 4 bits information) under Gary Scale mode setting. Each time user wants to change DDRAM data, it need 4 times data writed as a completely action for one address. HT16A102 will increment write DDRAM address automatically after each write action under Binary mode setting.



RAM-to-OLED data transfer

Gray Scale function is implemented by Pulse Width Modulation method. {0,0,0,0} represent the constant

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current driving timing is zero, and {1,1,1,1} means constant current driving is always on during each display time.
As the mention above, Gray Scale function is executed by PWM method. The ratio of ON/OFF as the below table.

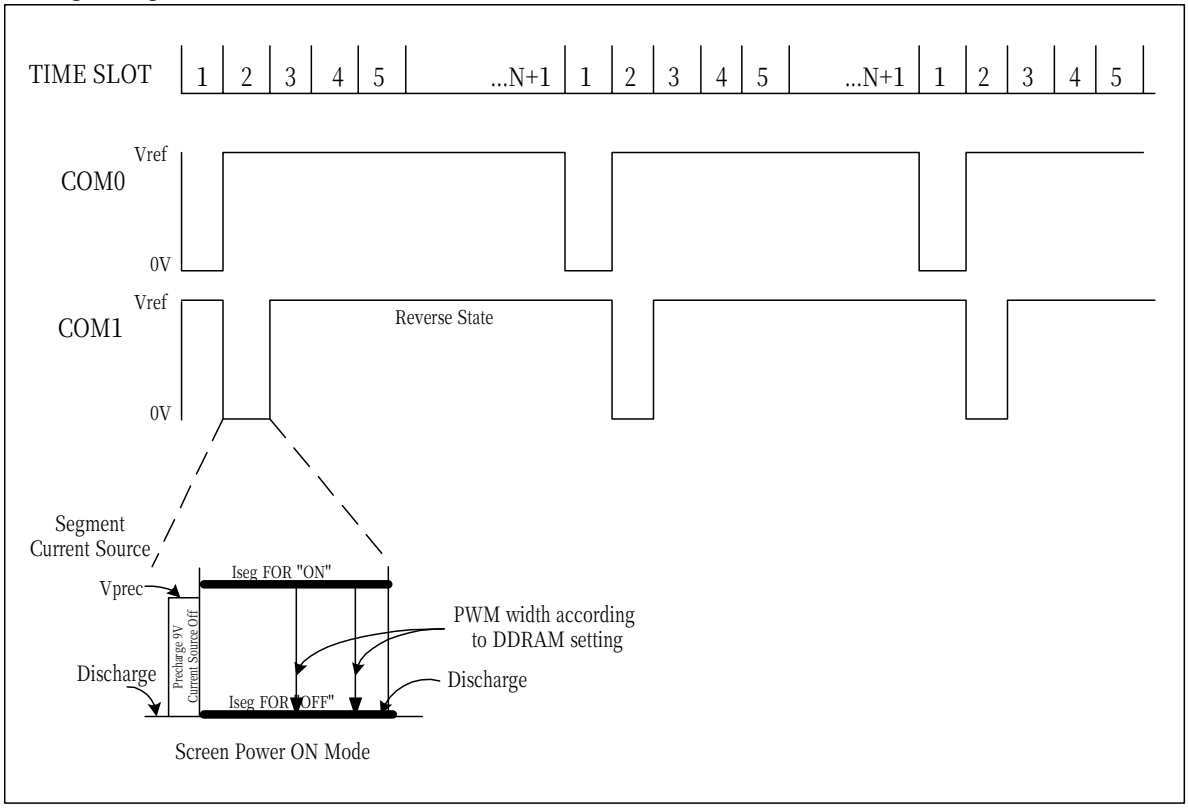
A. 97Hz, The total clock's number during each row scanning time are 24

Gray Scale Setting	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PWM ON Period	3	6	8	9	10	11	12	13	14	15	16	17	18	19	20

B. 110Hz, The total clock's number during each row scanning time are 20

Gray Scale Setting	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
PWM ON Period	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Driving timing Waveform



Precharge voltage value could be modified by external component, so depent on different OLED panel, HT16A102 OLED driver could represent it's best performance.

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DC-DC function

HT16A102 build-in DC-DC function. The application curcuit as the appendix figure. Output pin NDO controls the external NMOS to charge the output voltage. Using R1 and R2 could get the output voltage which we need. The relationship between output voltage and R1/R2 is V_{OLED} = ((R1 + R2)/R2) * Vref $_{Note1}$. The input pin VADJ will inform comparator turn on/off the OSC. If the output voltage is enough, the comparator will turn off the OSC, else the OSC will be turn on and output voltage will be charged.

V_{DD} range is from 2.4V to 3.6V

Note1 : Vref = 1.2V

Absolute Maximum Ratings

Supply Voltage (V_{DD}) …. 3.6V

Supply Voltage (V_{OLED}) …. 16V

Input Voltage (I/Os) …… $V_{SS}-0.3 \sim V_{DD}+0.3V$

Storage Temperature.....….....-50°C to 125°C

Operating Temperature ...…… ..…-30°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

DC characteristics

Symbol	Parameter	Condition (T=25℃)	Min.	Typ.	Max.	Unit
V_{OLED}	High voltage		7	—	16	V
V_{DD}	External positive power		2.4	--	3.6	V
V_{IH}	Input high level voltage	Logic input pin	$0.7V_{DD}$	--	--	V
V_{IL}	Input low level voltage	Logic input pin	--	--	$0.3V_{DD}$	V
V_{OH}	Output high level voltage	I_{OH} = -0.1mA	$0.8V_{DD}$	--	V_{DD}	V
V_{OL}	Output low level voltage	I_{OL} = 0.1mA	--	--	$0.2V_{DD}$	V
I_{SB}	Stand-by current	RC Oscillator on, V_{DD}=3V	--	20	--	uA
I_{SP}	Sleep mode current	RC oscillator disable (Reset low)	--	--	5	uA
I_{SRC1}	Segment source current	V_{OLED} = 12V, V_{DD}=3V	--	-315	--	uA

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I_{SRC3}	Common source current	V_{OLED} = 12V, V_{DS}=2V	-100	--	--	uA
I_{SK3}	Common sink current	V_{OLED} = 12V, V_{DD}=3V	--	--	40	mA
V_{REF}	Reference voltage of I_{REF}	V_{OLED} = 12V, V_{DD}=3V	--	0.9	--	V
II_{REF}	Reference current of I_{REF}	V_{OLED} = 12V, V_{DD}=3V, R=180kΩ	--	5	--	uA
P_{diss}	Power disspation	V_{OLED} = 12V, V_{DD}=3V (DC-DC ON, no load)	--	18	--	mW
VO_{DCDC}	DC-DC output voltage	Load R=200Ω	--	12	16	V
E_{DCDC1}	Efficiency of DC-DC	Vo = 12V; Load R = 200Ω	--	80	--	%
E_{DCDC2}	Efficiency of DC-DC	Vo = 16V; Load R = 300Ω	--	70	--	%

AC Characteristics

Symbol	Parameter	Condition (T=25℃)	Min.	Typ.	Max.	Unit
f_{SYS}	System RC oscillator		—	150	—	kHz

Note. Current matching accuracy(V_{OLED} 12V) : ±3% for intra-die, ±3% for inter-die.

PROGRAM INSTRUCTION DESCRIPTION

Instruction Table *x：Don't care*

Instruction	D/C	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	Busy	ADC	ON / OFF	/RESET	0	0	0	0	Read the internal status
Set page address	0	0	1	0	1	1	0	P2	P1	P0	Set page address Reset State All "0"
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB Reset State All "0"
Set column address MSB	0	0	0	0	0	1	0	Y6	Y5	Y4	Set column address MSB Reset State All "0"
Set global constant current mode	0	0	0	0	1	1	0	0	0	1	Set global constant current mode Control contrast setting
Set global constant current register	0	0	X	X	SV5	SV4	SV3	SV2	SV1	SV0	Set global constant current register Reset State All "0"
Regulator ON/OFF	0	0	1	0	1	1	1	1	0	RLON	Turn ON/OFF for internal regulator (pre-charge voltage) RLON = 0 : internal regulator off RLON = 1 : internal regulator on Reset Status RLON = 0.
DC-DC ON/OFF	0	0	1	0	1	1	1	1	1	DCON	Turn ON/OFF for internal DC-DC DCON = 0 : DC-DC function off DCON = 1 : DC-DC function on Reset Status DCON = 0

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Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON / OFF OLED panel When DON = 0: display OFF When DON=1 : display ON Reset State DON = 0
Binary/Gray Select	0	0	1	1	1	0	0	1	0	BGS	BGS = 1 : Binary mode select BGS = 0 : Gray Scale mode select Reset State 0
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0 Reset State All "0"
Set Segment Re-map	0	0	1	0	1	0	0	0	0	X0	X0 = 0 : column address 00H is mapped to SEG0 (POR) X0 = 1 : column address 5FH is Mapped to SEG0
COMMON Remap select	0	0	1	1	0	0	0	0	0	COM RP	Select COM output direction When COMRP = 0 : normal direction (COM0⇒ COM63) When COMRP = 1 : reverse direction (COM63 ⇒ COM0) Reset State 0
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal / entire display ON When EON = 0 : normal display When EON = 1 : entire display ON Reset State 0
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0 : normal display When REV = 1 : reverse display Reset State 0 ; Note. Binary only
Set Multiplex Ratio	0	0	1	0	1	0	1	0	0	0	Set Multiplex Ratio command
Set Multiplex Ratio	0	0	X	X	X5	X4	X3	X2	X1	X0	To select multiplex ratio N from 2 to the maximum multiplex ratio Max. mux ratio 64 (Reset Status value) $N=X_5X_4X_3X_2X_1X_0 + 1$, Eg. N=001111b + 1 =16
Set FSEL	0	0	1	1	0	0	0	0	1	FSEL	During 64 row all on. FSEL = 0(97Hz) , Reset Status FSEL = 1(110Hz)
Flash mode	0	0	1	1	1	0	0	1	1	FLS	FLS = 1 : Flash display mode ON FLS = 0 : Flash display mode OFF Reset State 0
Flash on time	0	0	1	1	0	1	0	FON2	FON1	FON0	Flash on timer Reset Status FON[2:0] = 0 Flash ON time = 0.4 + 0.3*FON[2:0] seconds
Flash off time	0	0	1	1	0	1	1	FOFF 2	FOFF 1	FOFF 0	Flash off timer Reset Status FOFF[2:0] = 0 Flash OFF time = 0.3 + 0.6*FOFF[2:0] seconds
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Software Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal function
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Reset modify-read mode
NOP	0	0	1	1	1	0	0	0	1	1	Command for no operation
Power save	-	-	-	-	-	-	-	-	-	-	Compound instruction of 1. display

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											OFF and 2. entire display ON
Test instruction	0	0	1	1	1	1	X	X	X	X	***Don't use this instruction.***

Read display data

The 8-bit data from DDRAM specified by the column address and the page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the MPU can continuously read the data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface. Because HT16A102 driver has gray scale function, user need continuous read 4 times DDRAM data to get whole information.

D/$\overline{C}$	**$\overline{RW}$**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
1	1	Read data							

Write display data

8-bit data of display data from the MPU can be written to the RAM location specified by the column address and page address.
The column address is increased by 1 automatically after MPU write DDRAM 4 times, so that the microprocessor can continuously write data to the addressed page.

D/$\overline{C}$	**$\overline{RW}$**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
1	0	Write data							

Read status

Indicates the internal status of the HT16A102.

D/$\overline{C}$	**$\overline{RW}$**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	1	BUSY	ADC	ON/OFF	$\overline{RESET}$	0	0	0	0

Flag	**Description**
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG95 -> SEG0), 1: normal direction (SEG0 -> SEG95)
ON / OFF	Indicates display ON / OFF status. 0: display ON, 1: display OFF

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$\overline{\text{RESET}}$	Indicate the $\overline{\text{RESET}}$.

Display ON/OFF

Turns the display ON or OFF..

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DC-DC ON/OFF

Turns the internal DC-DC function ON or OFF..

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	1	1	DCON

Regulator ON/OFF

Turns the internal regulator ON or OFF..

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	1	0	RLON

Initial Display Line

Set the line address of DDRAM to determine the initial display line. The RAM display data is displayed at the top row (COM0 when COMRP = L, COM63 when COMRP = H) of OLED panel.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	Line address
0	0	0	0	0	0
0	0	0	0	1	1
..	..	..	..	..	..
1	1	1	1	0	62

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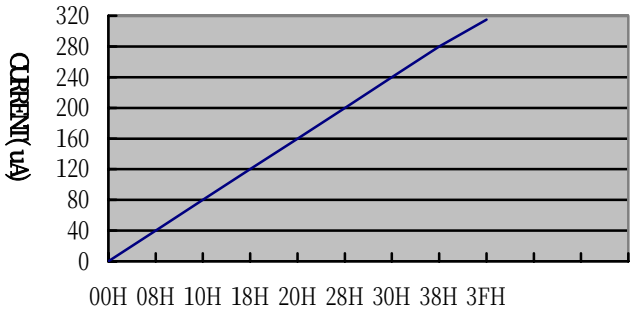
1	1	1	1	1	63

Set global constant current register

Double byte command to control contrast function. When global constant current mode has been set, user can set the SV5 – SV0 register to modify the global current.
The chip has 64 constrast steps from 00 to 3F.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	0	0	1

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	SV5	SV4	SV3	SV2	SV1	SV0



The above figure means the display current could be divided to 63, from 5uA to 315uA.
Condition : @V_{OLED} = 12V. $V_{OLED} - V_{IOUT} > 3V$.

Set page address

Sets the page address of DDRAM from the MPU into the page address register.
Any RAM data bit can be accessed when its page address and column address are specified.
Along with the column address, the page address defines the address of the DDRAM to write or read display data.

Changing the page address doesn't effect to the display status.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	P2	P1	P0

P2	P1	P0	**Line address**
0	0	0	0

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0	0	1	1
..	..	..	..
1	1	1	7

Set column address MSB

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y6	Y5	Y4

Set column address LSB

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
..	..	..	..	..	..	..	..
1	0	1	1	1	1	0	94
1	0	1	1	1	1	1	95

Set Segment Re-mapped

This command changes the mapping between the display data column address and segment driver. It allows flexibility in layout during OLED module assembly. X0 = 0, column address 00H is mapped to SEG0. X0 = 1, column address 5FH is mapped to SEG0

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	X0

Reverse display ON/OFF

Reverses the display status on OLED panel without rewriting the contents of the DDRAM.
Binary mode only.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

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REV	RAM bit data = "1"	RAM bit data = "0"
0(Normal)	OLED pixel is illuminated	OLED pixel is not illuminates
1(Reverse)	OLED pixel is not illuminates	OLED pixel is illuminated

Binary/Gray Scale Select

User could using this instruction to set Black and White or Gray Scale mode. Under Binary mode, HT16A102 will add address by one automatically after one byte data has been written. If Gray Scale mode has been choosen, HT16A102 will add address by one automatically after four byte data have been written.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	BGS

BGS = 0 : Gray Scale mode
BGS = 1 : Black & White mode

Flash mode
HT16A102 support flash function, setting FLS bit to enable flash mode. Flash on timer and flash off timer depend on FON[2:0] and FOFF[2:0] register setting.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	1	FLS

FLS = 0 : normal display
FLS = 1 : flash function ON

Flash ON Timer

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	1	0	FON2	FON1	FON0

Flash OFF Timer

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	1	1	FOFF2	FOFF1	FOFF0

Flash ON time = 0.4 + 0.3*FON[2:0] seconds. Flash OFF time = 0.3 + 0.6*FOFF[2:0] seconds.

Entire display ON/OFF

Forces the whole OLED points to be turned on regardless of the contents of the DDRAM.
At this time, the contents of the DDRAM are held.
This instruction has priority over the reverse display ON/OFF instruction.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0 : normal display

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EON = 1 : entire display ON

Set modify-read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of the MPU when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset modify-read instruction.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset modify-read

This instruction cancels the modify-read mode, and makes the column address return to its initial value just before the set modify-read instruction is started.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

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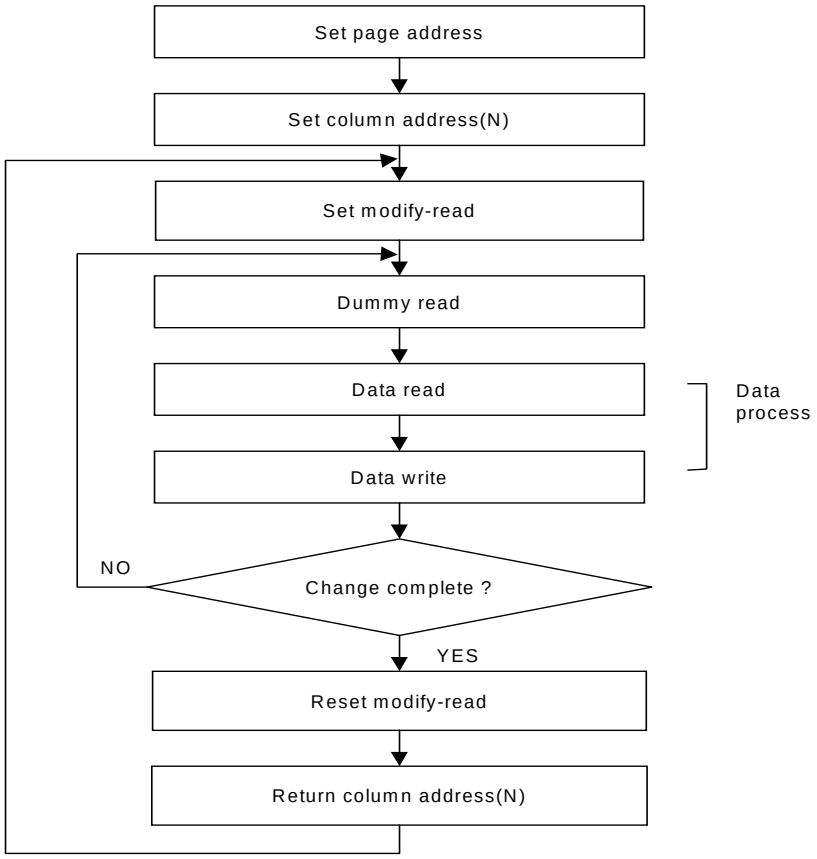

Software Reset

This instruction resets initial display line, column address, page address, and common output status select to their status, but does not affects the contents of DDRAM.
This instruction can not initialize the OLED power supply which is initialized by the $\overline{\text{RESET}}$ pin.
This command also causes some of the internal status of the chip to be initialized:

1. Initial display line register are set to 0
2. Column address counter is set to 0
3. Page address is set to 0
4. Multi-ratio reset as 64
5. Flash ON and flash OFF time reset as 0
6. Global brightness reset as 0

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

NOP

No Operation Command

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COMRP select

COM output scanning direction is selected by this instruction which determines the OLED driver output status.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	0	0	COMRP

COMRP = 0 : normal direction (COM0 => COM63)
COMRP = 1 : reverse direction (COM63 => COM0)

Power save (Compound instruction)

To enter Standby Mode, it should be done by using a double byte command composed of "Set Display ON/OFF" and "Set Entire Display ON/OFF" commands. First, set "Display OFF command" then set "Entire Display ON" command, the Standby Mode will be entered.
For Standby Mode:
1. Internal OLED power supply circuits are stopped.
2. Segment and Common drivers output high impedance level
3. The display data and operation mode before sleep are held.
4. Internal display RAM can still be accessed.
5. Sleep Mode can be exited by the issue of a new software command or by pulling Low at hardware pin $\overline{RESET}$.

Set Multiplex Ratio

This command switched default 64 multiplex mode to any multiplex mode from 2 to 64. The output pads ROW0 ~ ROW63 will be switched to corresponding COM signal.

Die Pad Name	64 Mux Com Signal Output	54 Mux Com Signal Output	53 Mux Com Signal Output	49 Mux Com Signal Output	48 Mux Com Signal Output	33 Mux Com Signal Output	32 Mux Com Signal Output	16 Mux Com Signal Output
ROW0	COM0	COM 0	COM 0	COM 0	COM 0	COM 0	COM 0	COM 0
ROW1	COM 1	COM 1	COM 1	COM 1	COM 1	COM 1	COM 1	COM 1
ROW2	COM 2	COM 2	COM 2	COM 2	COM 2	COM 2	COM 2	COM 2
ROW3	COM 3	COM 3	COM 3	COM 3	COM 3	COM 3	COM 3	COM 3
ROW4	COM 4	COM 4	COM 4	COM 4	COM 4	COM 4	COM 4	COM 4
ROW5	COM 5	COM 5	COM 5	COM 5	COM 5	COM 5	COM 5	COM 5
ROW6	COM 6	COM 6	COM 6	COM 6	COM 6	COM 6	COM 6	COM 6
ROW7	COM 7	COM 7	COM 7	COM 7	COM 7	COM 7	COM 7	COM 7
ROW8	COM 8	COM 8	COM 8	COM 8	COM 8	COM 8	COM 8	COM 8
ROW9	COM 9	COM 9	COM 9	COM 9	COM 9	COM 9	COM 9	COM 9
ROW10	COM 10	COM 10	COM 10	COM 10	COM 10	COM 10	COM 10	COM 10
ROW11	COM 11	COM 11	COM 11	COM 11	COM 11	COM 11	COM 11	COM 11
ROW12	COM 12	COM 12	COM 12	COM 12	COM 12	COM 12	COM 12	COM 12
ROW13	COM 13	COM 13	COM 13	COM 13	COM 13	COM 13	COM 13	COM 13
ROW14	COM 14	COM 14	COM 14	COM 14	COM 14	COM 14	COM 14	COM 14
ROW15	COM 15	COM 15	COM 15	COM 15	COM 15	COM 15	COM 15	COM 15
ROW16	COM 16	COM 16	COM 16	COM 16	COM 16	COM 16	COM 16	NON-SELECT
ROW17	COM 17	COM 17	COM 17	COM 17	COM 17	COM 17	COM 17	NON-SELECT
ROW18	COM 18	COM 18	COM 18	COM 18	COM 18	COM 18	COM 18	NON-SELECT
ROW19	COM 19	COM 19	COM 19	COM 19	COM 19	COM 19	COM 19	NON-SELECT
ROW20	COM 20	COM 20	COM 20	COM 20	COM 20	COM 20	COM 20	NON-SELECT
ROW21	COM 21	COM 21	COM 21	COM 21	COM 21	COM 21	COM 21	NON-SELECT
ROW22	COM 22	COM 22	COM 22	COM 22	COM 22	COM 22	COM 22	NON-SELECT
ROW23	COM 23	COM 23	COM 23	COM 23	COM 23	COM 23	COM 23	NON-SELECT
ROW24	COM 24	COM 24	COM 24	COM 24	COM 24	COM 24	COM 24	NON-SELECT
ROW25	COM 25	COM 25	COM 25	COM 25	COM 25	COM 25	COM 25	NON-SELECT
ROW26	COM 26	COM 26	COM 26	COM 26	COM 26	COM 26	COM 26	NON-SELECT
ROW27	COM 27	COM 27	COM 27	COM 27	COM 27	COM 27	COM 27	NON-SELECT
ROW28	COM 28	COM 28	COM 28	COM 28	COM 28	COM 28	COM 28	NON-SELECT

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ROW29	COM 29	COM 29	COM 29	COM 29	COM 29	COM 29	COM 29	NON-SELECT
ROW30	COM 30	COM 30	COM 30	COM 30	COM 30	COM 30	COM 30	NON-SELECT
ROW31	COM 31	COM 31	COM 31	COM 31	COM 31	COM 31	COM 31	NON-SELECT
ROW32	COM 32	COM 32	COM 32	COM 32	COM 32	COM 32	NON-SELECT	NON-SELECT
ROW33	COM 33	COM 33	COM 33	COM 33	COM 33	NON-SELECT	NON-SELECT	NON-SELECT
ROW34	COM 34	COM 34	COM 34	COM 34	COM 34	NON-SELECT	NON-SELECT	NON-SELECT
ROW35	COM 35	COM 35	COM 35	COM 35	COM 35	NON-SELECT	NON-SELECT	NON-SELECT
ROW36	COM 36	COM 36	COM 36	COM 36	COM 36	NON-SELECT	NON-SELECT	NON-SELECT
ROW37	COM 37	COM 37	COM 37	COM 37	COM 37	NON-SELECT	NON-SELECT	NON-SELECT
ROW38	COM 38	COM 38	COM 38	COM 38	COM 38	NON-SELECT	NON-SELECT	NON-SELECT
ROW39	COM 39	COM 39	COM 39	COM 39	COM 39	NON-SELECT	NON-SELECT	NON-SELECT
ROW40	COM 40	COM 40	COM 40	COM 40	COM 40	NON-SELECT	NON-SELECT	NON-SELECT
ROW41	COM 41	COM 41	COM 41	COM 41	COM 41	NON-SELECT	NON-SELECT	NON-SELECT
ROW42	COM 42	COM 42	COM 42	COM 42	COM 42	NON-SELECT	NON-SELECT	NON-SELECT
ROW43	COM 43	COM 43	COM 43	COM 43	COM 43	NON-SELECT	NON-SELECT	NON-SELECT
ROW44	COM 44	COM 44	COM 44	COM 44	COM 44	NON-SELECT	NON-SELECT	NON-SELECT
ROW45	COM 45	COM 45	COM 45	COM 45	COM 45	NON-SELECT	NON-SELECT	NON-SELECT
ROW46	COM 46	COM 46	COM 46	COM 46	COM 46	NON-SELECT	NON-SELECT	NON-SELECT
ROW47	COM 47	COM 47	COM 47	COM 47	COM 47	NON-SELECT	NON-SELECT	NON-SELECT
ROW48	COM 48	COM 48	COM 48	COM 48	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW49	COM 49	COM 49	COM 49	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW50	COM 50	COM 50	COM 50	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW51	COM 51	COM 51	COM 51	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW52	COM 52	COM 52	COM 52	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW53	COM 53	COM 53	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW54	COM 54	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW55	COM 55	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW56	COM 56	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW57	COM 57	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW58	COM 58	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW59	COM 59	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW60	COM 60	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW61	COM 61	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW62	COM 62	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT
ROW63	COM 63	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT

ROW pins assignment for COM signals in Programable Multiplex Ratio

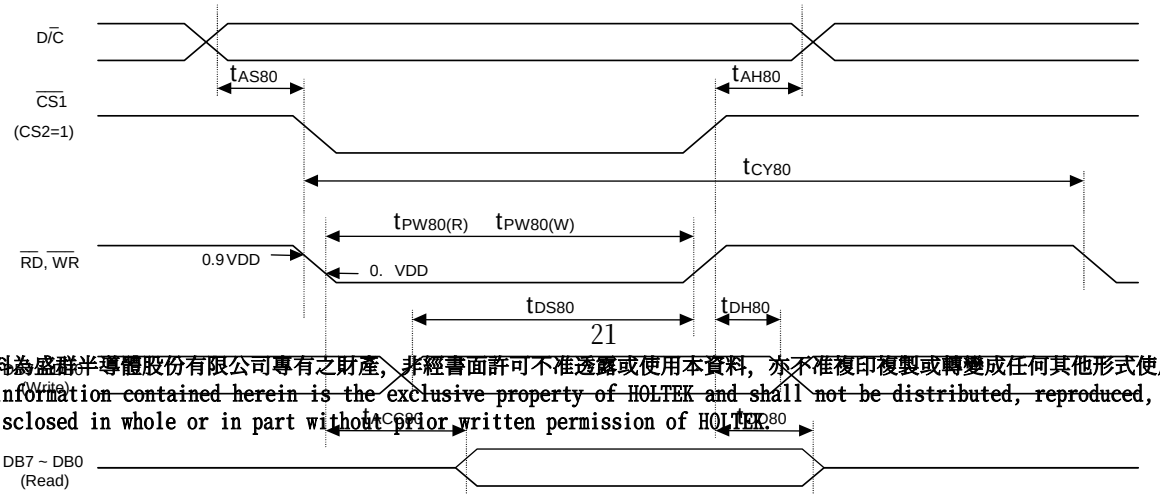
Set FSEL

MPU could use this command to set display frequency, FSEL = 0 for 97Hz(Reset Status), "1" for 110Hz. (The frequency is under all row(64) has been set. If MCU choose Multiplex Ratio mode, the frequency will be change.

D/$\overline{C}$	$\overline{RW}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	0	1	FSEL

Timing diagram

Read / write characteristics (8080-series MPU)



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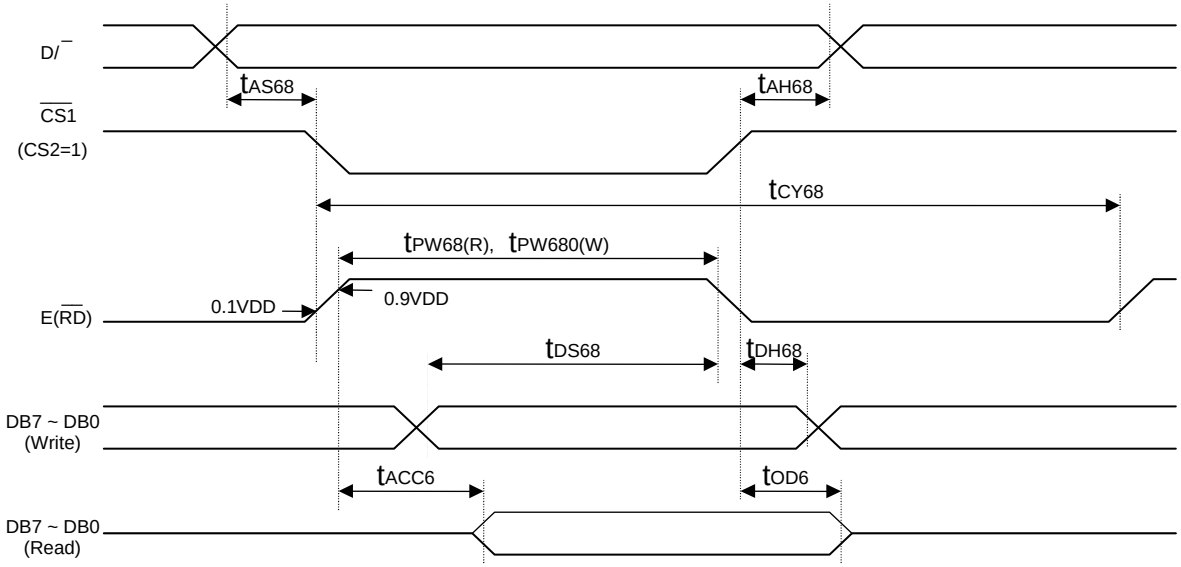
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	13 17	-	-	ns	
System cycle time	RS	t_{CY80}	400	-	-	ns	
Pulse width(/WR)	RW-/WR	t_{PW80} (W)	55	-	-	ns	
Pulse width(/RD)	E-/RD	t_{PW80} (R)	125	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	35 13	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	- 10	-	125 90	ns	CL = 100pF

Read/Write characteristics (6800-series MPU)



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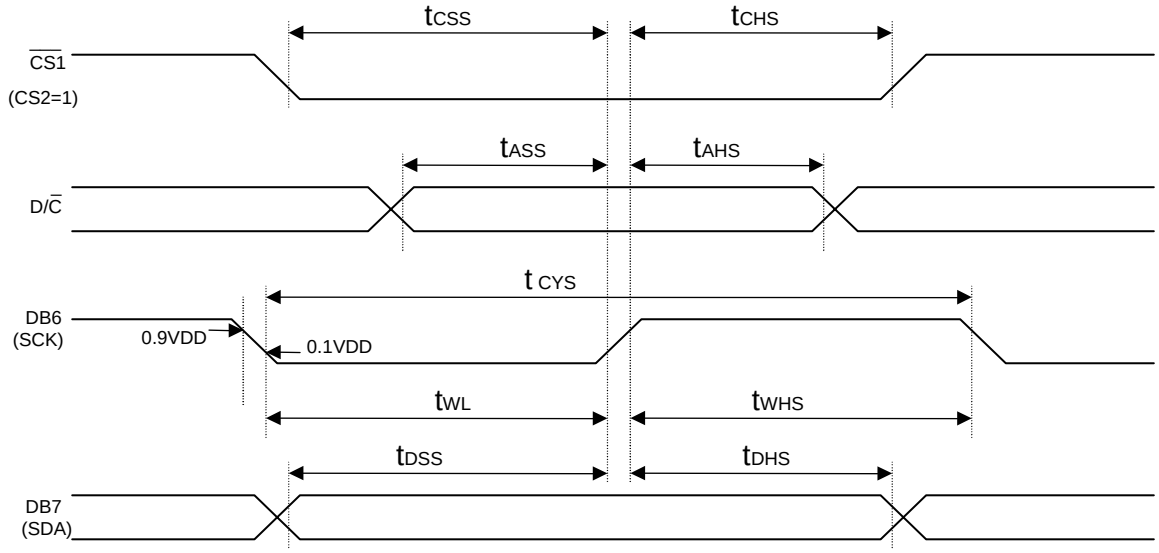
Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	13 17	-	-	ns	
System cycle time		RS	t_{CY68}	400	-	-	ns	
Enable pulse width	Read Write	E-/RD	t_{PW68} (R) t_{PW68} (W)	125 55	-	-	ns	
Data setup time Data hold time		DB7 to DB0	t_{DS68} t_{DH68}	35 13	-	-	ns	
Access time Output disable time			T_{ACC68} t_{OD68}	- 10	-	125 90	ns	CL = 100pF

Serial interface characteristics



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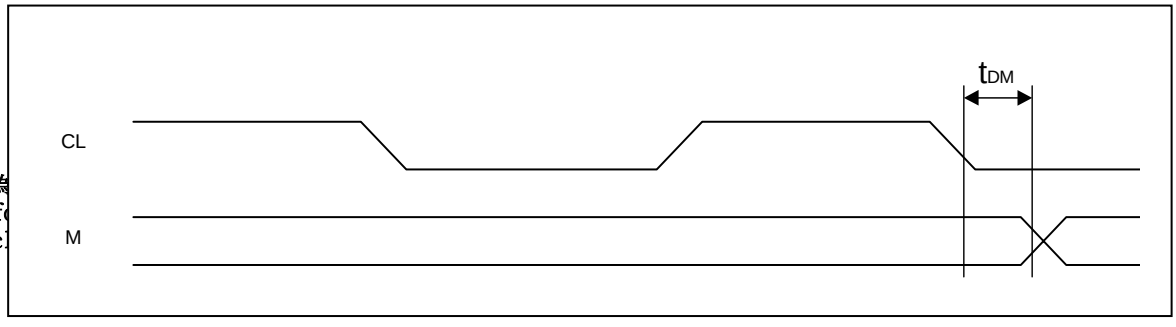
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYC} t_{WHS} t_{WLS}	450 180 135	-	-	ns	
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	90 360	-	-	ns	
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	90 90	-	-	ns	
$\overline{CS1}$ set up time $\overline{CS1}$ hold time	$\overline{CS1}$	t_{CSS} t_{CHS}	55 180	-	-	ns	

Reset input timing

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	$\overline{RESET}$	t_{RW}	5	-	-	us	

Display control output timing



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Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
M delay time	M	t_{DM}	-	13	70	ns	

SPI TIMING DIAGRAM AND PIN CONNECTION

When input pin $\overline{SP}$ is high and input pin P/$\overline{S}$ is low, the SPI interface mode is selected.

MPU SPI Interface

The SPI communication interface consists of a Slave Select ($\overline{SS}$) , SPI Write data signal to Slave(MI) and SPI Read data signal from Slave (SO) and SPI serial clock signal (SCK). There are also five input pin (/RES, /CS1, P/S, CS2, /SP) which is used for the initialization of device.

1. Slaves Select
   HT16A102 have to recognize the slave address before transmitting or receiving any information by the SPI-bus. The device will responds by the slave select signal and the ID (R/W data or command).
   ID = **100X-XXXX** : Command Write mode; **ID** = **101X-XXXX** : Data Write mode; **ID** = **110X-XXXX** : Data Read mode
2. MI signal
   Microprocessor write data by the MI pin
3 MO signal
   Microprocessor read data from the MO pin.
3. SPI-bus serial clock signal
   We suggest Microprocessor change data at falling edge SCK under write mode and latch data at rising edge at rising edge SCK.

Command Decoder

If the **ID** code is **100**, the input signal is interpreted as a Command write instruction. It will be decoded and

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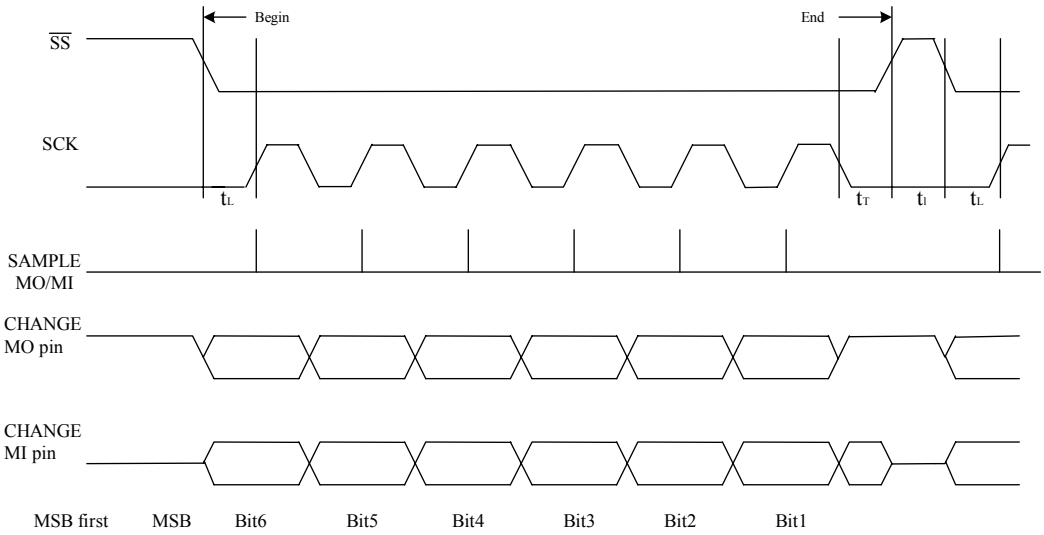
written input value to the corresponding command regester.

SPI-bus Write command/data and read data

The SPI-bus interface gives access to write data and command into the device. The data formate as the following figure.

SPI INTERFACE TIMING



Minimum 1/2 SCK for t_T, t_I, t_L

t_L : Minimum leading time before first SCK edge
t_T : Minimum trailing time after the last SCK edge
t_I : Minimum idling time between transfers(minimum SS high time)
t_L, tT and tl are guaranteed for the master mode and required for the slave mode.

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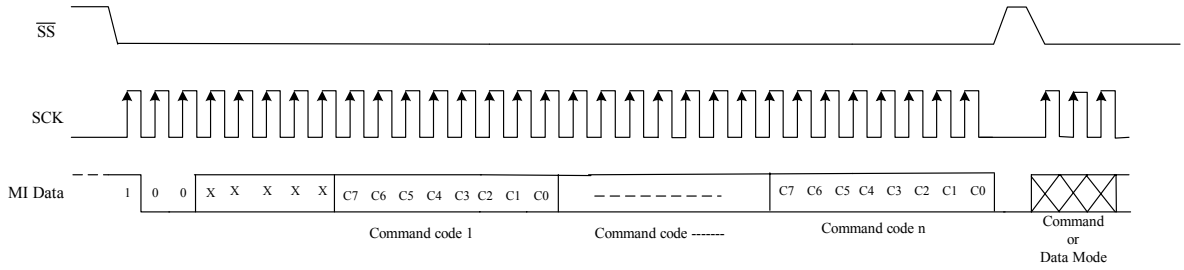
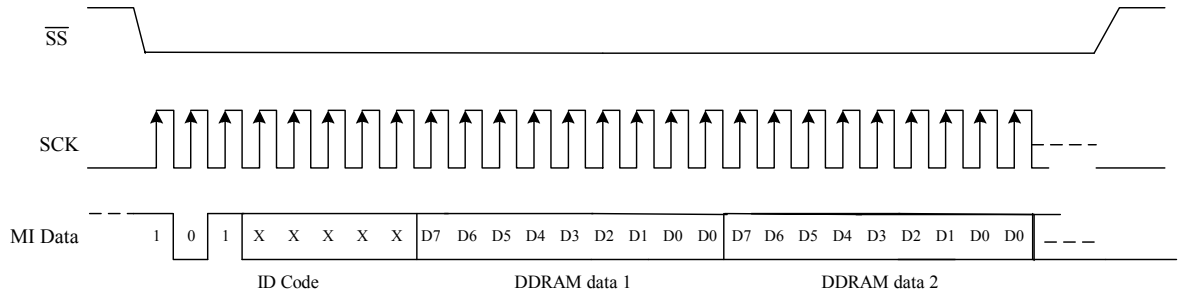
Write Command Mode (ID : 1 0 0 X-XXXX)



User could write only command or continuous command to the device. Pull $\overline{SS}$ signal high to stop the command transfer.

Write DDRAM data mode (ID 1 0 1 X-XXXX)



Read DDRAM data mode (ID : 1 1 0 X-XXXX)

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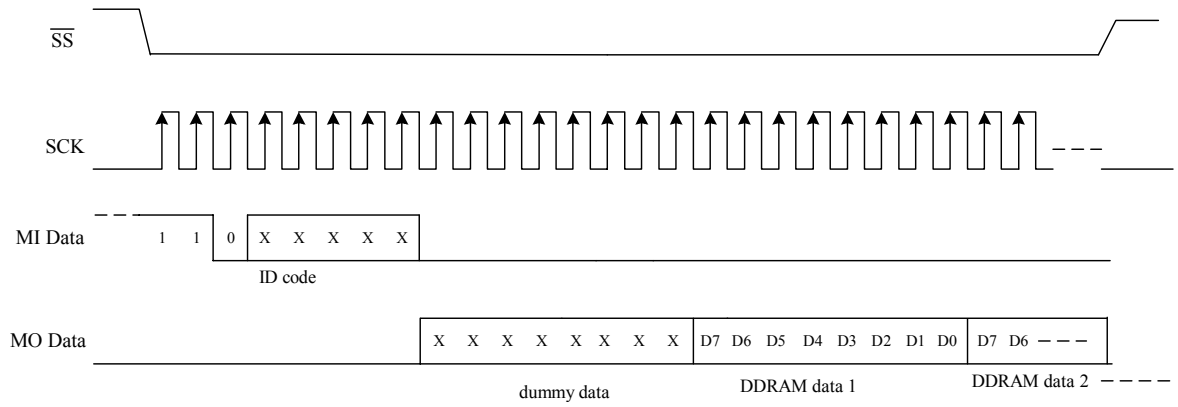

Note : It is recommended that the host controller should read in the data from SO line between the rising edge of the SCK line and the falling edge of the next SCK line

Appendix

DC-DC application diagram

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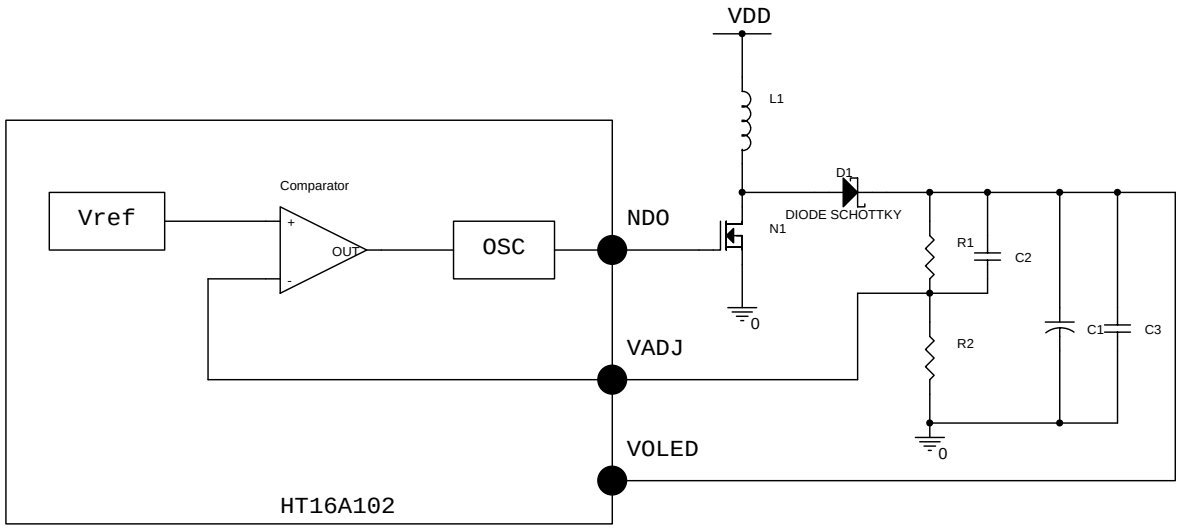

Note:

1. R1=470kΩ, R2=51kΩ, V_{OLED} = 12V
2. C2 = 10pF, C1 = 100uF(Low ESR) and C3 = 0.1uF
3. D1 : SS12 (General Semiconductor)
4. NMOS : Si968A (VISHAY)
5. 33uH : (R_{DC} = 0.7Ω. Rated current = 0.6A : Test frequency at 100kHz, Ta = 20° C)
6. The DC-DC PCB layout trace should be short and the width should be large enough (60mil width will be safe). The critical path VDD -> L1 -> N1 -> VSS, VDD -> L1 -> D1 -> R1/C2 -> C1/C3.

HT16A102 COF PACKAGE DIMENSION

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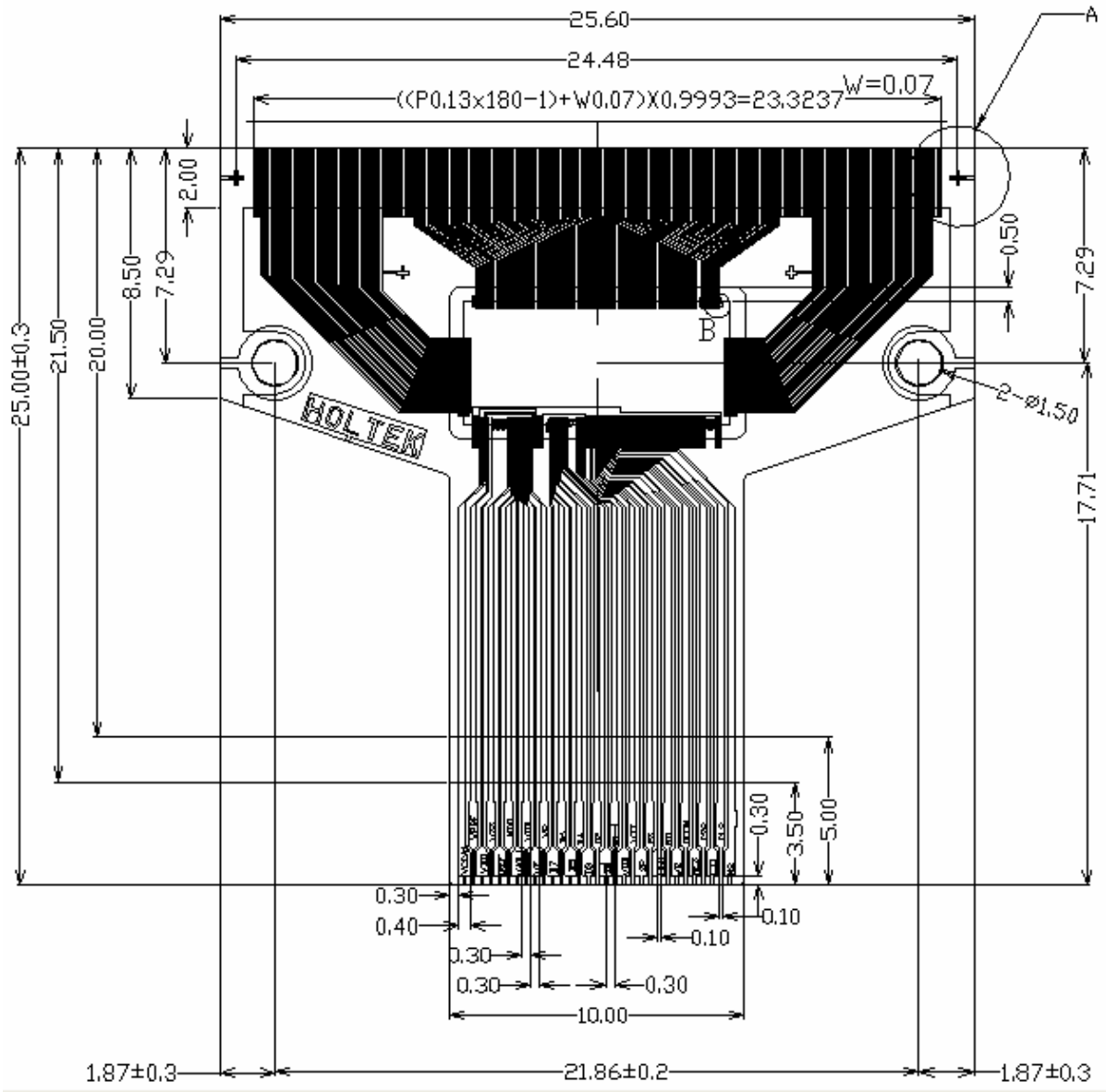

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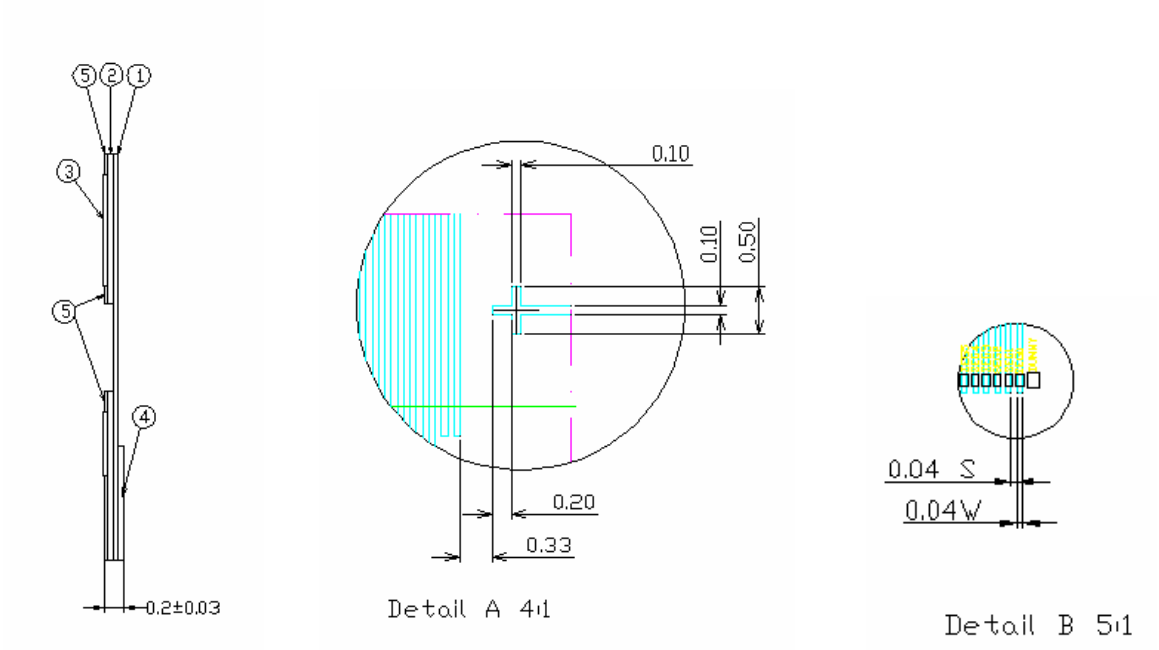

No.	material	Remark
1	Base Film	PI 25um ± 10%
2	Cupper	CU 12um ± 6um
3	Solder resist	Epoxy 10um+20/-5um
4	Stiffener with ADH	Polyester : 150um (100+50)
5	Plating	Ni : 0.5um+/-0.25, Au : 0.4um+/-0.15um

Note:
1. This drawing shows the view from the copper side.
2. Where not specified, dimensional tolerance is ± 0.2mm.
3. Solder resist misregistration tolerance is ± 0.3mm.
4. Stiffener bonding tolerance is ± 0.5mm.
5. Material, thickness, etc, shall be in accordance with the component list.
6. The edge width of input connector modify from 0.3mm to 0.1mm.

Software initial steps

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1. Reset HT16A102 more then 5us
2. Send 0BDH command -> Regulator ON
3. Send 0BFH command -> Turn ON DC-DC
4. Send 0A4H command for Normal pixel ON (User could send 0A5H for all pixel on testing)
5. Send 031H command then send 0XXH for global current setting
6. Send 0AFH command to turn ON OLED panel

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