

Feature

- Logic Operating Voltage: 2.4V ~ 3.6V
- Analog Power Supply Voltage: 2.4V ~ 3.6V
- Output channel with three level voltage switching
 - ♦ 120 segments × 1 COM × 1 BG
 - ♦ 4 common/background combo pins can be set as common or background
- Output voltage setting: 0V, V_{DL}, V_{DH}
- Integrated LUT
- Integrated Charge pump controller
- Integrated Temperature sensor
- Data comparison function
- Device cascading function
- Integrated 3-wire SPI serial interface
- Package Type: COG

Applications

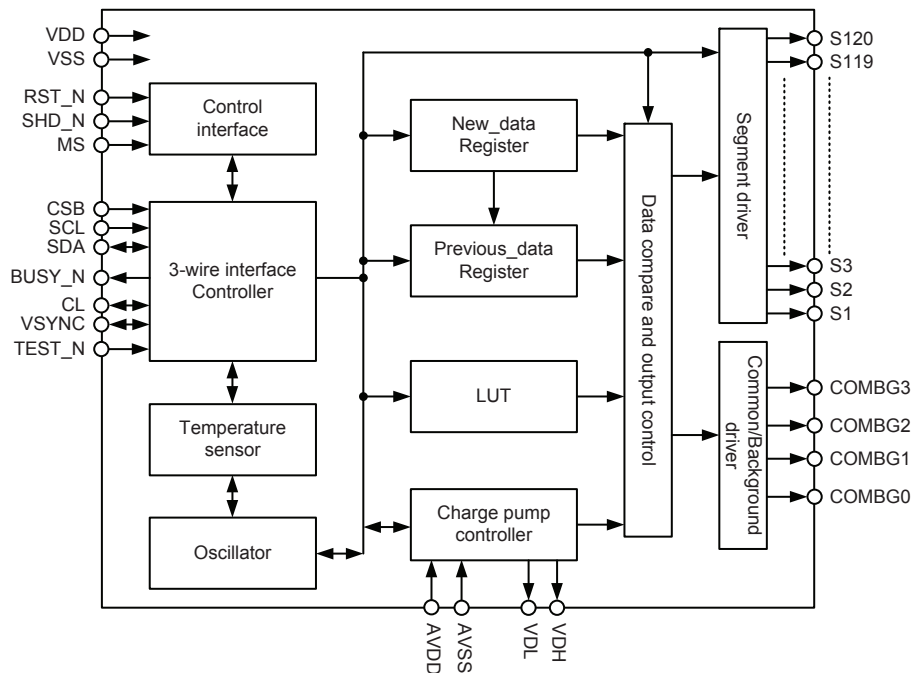
- Smart cards
- Industrial gauges
- Electronic shelf labels
- Consumer electronics

General Description

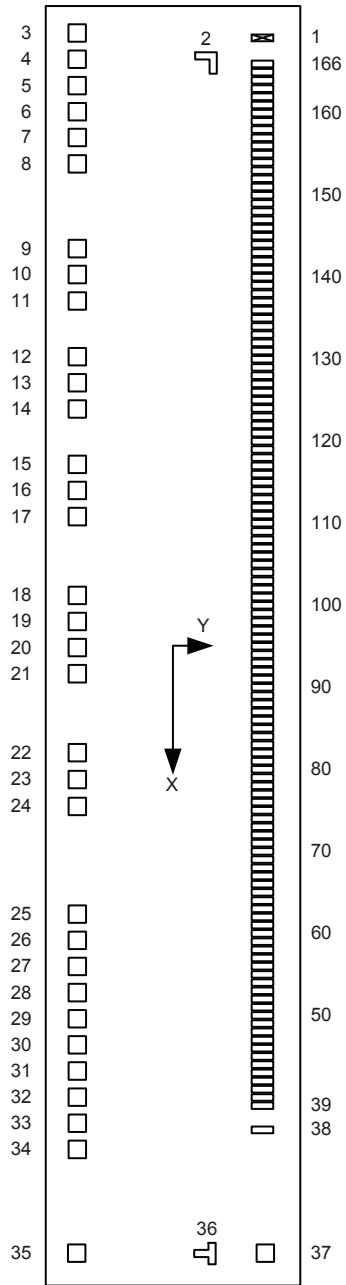
The HT16E07 is an electronic paper display (EPD) driver IC. It consists of 120 segments and 4 background or common selectable outputs. The output drivers have a three level driving voltage to match the EPD characteristic. The driving voltage is generated by a charge pump circuit.

The HT16E07 device communicates with external microcontrollers using its internal 3-wire SPI serial interface.

Block Diagram



Pad Assignment



Pad Dimensions

| Item | Pad Number | Size | | Unit |
|----------------|-------------|----------|-----|------|
| | | X | Y | |
| Chip size | — | 4228 | 850 | μm |
| Chip thickness | — | 508 ± 38 | | μm |
| Pad pitch | 1, 38 ~ 166 | 27 | | μm |
| | 3 ~ 35, 37 | > 86 | | μm |
| Bump size | 1, 38 ~ 166 | 15 | 126 | μm |
| | 3 ~ 35, 37 | 68 | 68 | μm |
| Bump height | All pad | 18 ± 3 | | μm |

Alignment Mark Dimensions

| Item | Number | Size | Unit |
|---------|--------|------|------|
| ALIGN_A | 2 | | μm |
| ALIGN_B | 36 | | μm |

Pad Coordinates

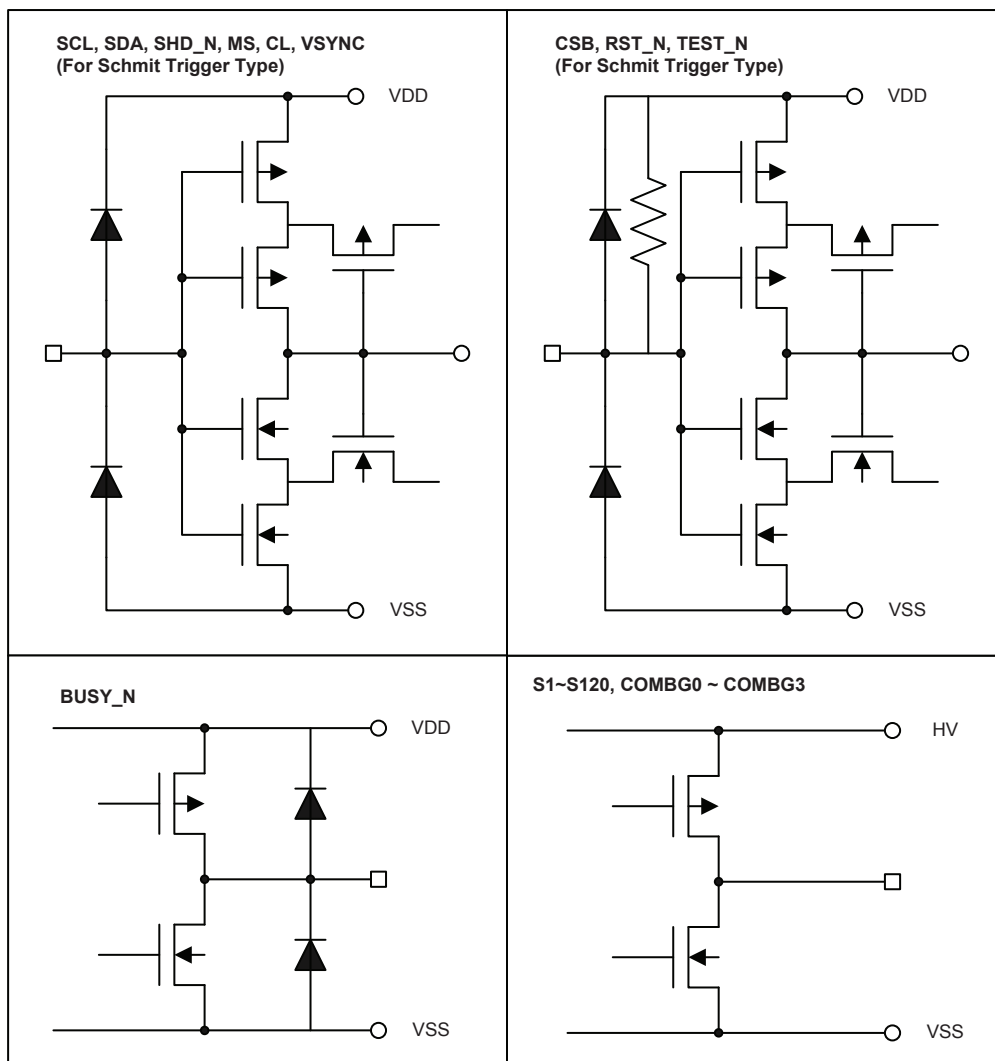
| No. | Name | X | Y | No. | Name | X | Y | No. | Name | X | Y |
|-----|---------|-----------|----------|-----|--------|----------|---------|-----|------|-----------|---------|
| 1 | DUMMY | -1999.870 | 296.000 | 57 | S17 | 1029.120 | 296.000 | 113 | S69 | -482.880 | 296.000 |
| 2 | ALIGN_A | -1926.500 | 113.280 | 58 | S18 | 1002.120 | 296.000 | 114 | S70 | -509.880 | 296.000 |
| 3 | VDH | -2015.000 | -315.615 | 59 | S19 | 975.120 | 296.000 | 115 | S71 | -536.880 | 296.000 |
| 4 | VDH | -1929.000 | -315.615 | 60 | S20 | 948.120 | 296.000 | 116 | S72 | -563.880 | 296.000 |
| 5 | VDH | -1843.000 | -315.615 | 61 | S21 | 921.120 | 296.000 | 117 | S73 | -590.880 | 296.000 |
| 6 | VDL | -1757.000 | -315.615 | 62 | S22 | 894.120 | 296.000 | 118 | S74 | -617.880 | 296.000 |
| 7 | VDL | -1671.000 | -315.615 | 63 | S23 | 867.120 | 296.000 | 119 | S75 | -644.880 | 296.000 |
| 8 | VDL | -1585.000 | -315.615 | 64 | S24 | 840.120 | 296.000 | 120 | S76 | -671.880 | 296.000 |
| 9 | AVSS | -1305.285 | -315.615 | 65 | S25 | 813.120 | 296.000 | 121 | S77 | -698.880 | 296.000 |
| 10 | AVSS | -1219.285 | -315.615 | 66 | S26 | 786.120 | 296.000 | 122 | S78 | -725.880 | 296.000 |
| 11 | AVSS | -1133.285 | -315.615 | 67 | S27 | 759.120 | 296.000 | 123 | S79 | -752.880 | 296.000 |
| 12 | AVSS | -950.285 | -315.615 | 68 | S28 | 732.120 | 296.000 | 124 | S80 | -779.880 | 296.000 |
| 13 | VSS | -864.285 | -315.615 | 69 | S29 | 705.120 | 296.000 | 125 | S81 | -806.880 | 296.000 |
| 14 | VSS | -778.285 | -315.615 | 70 | S30 | 678.120 | 296.000 | 126 | S82 | -833.880 | 296.000 |
| 15 | AVDD | -595.285 | -315.615 | 71 | S31 | 651.120 | 296.000 | 127 | S83 | -860.880 | 296.000 |
| 16 | AVDD | -509.285 | -315.615 | 72 | S32 | 624.120 | 296.000 | 128 | S84 | -887.880 | 296.000 |
| 17 | AVDD | -423.285 | -315.615 | 73 | S33 | 597.120 | 296.000 | 129 | S85 | -914.880 | 296.000 |
| 18 | VDD | -164.285 | -315.615 | 74 | S34 | 570.120 | 296.000 | 130 | S86 | -941.880 | 296.000 |
| 19 | VDD | -78.285 | -315.615 | 75 | S35 | 543.120 | 296.000 | 131 | S87 | -968.880 | 296.000 |
| 20 | VDD | 7.715 | -315.615 | 76 | S36 | 516.120 | 296.000 | 132 | S88 | -995.880 | 296.000 |
| 21 | NC | 93.715 | -315.615 | 77 | S37 | 489.120 | 296.000 | 133 | S89 | -1022.880 | 296.000 |
| 22 | NC | 353.355 | -315.615 | 78 | S38 | 462.120 | 296.000 | 134 | S90 | -1049.880 | 296.000 |
| 23 | NC | 444.715 | -315.615 | 79 | S39 | 435.120 | 296.000 | 135 | S91 | -1076.880 | 296.000 |
| 24 | NC | 530.715 | -315.615 | 80 | S40 | 408.120 | 296.000 | 136 | S92 | -1103.880 | 296.000 |
| 25 | SHD_N | 885.715 | -315.615 | 81 | S41 | 381.120 | 296.000 | 137 | S93 | -1130.880 | 296.000 |
| 26 | RST_N | 971.715 | -315.615 | 82 | S42 | 354.120 | 296.000 | 138 | S94 | -1157.880 | 296.000 |
| 27 | SDA | 1057.715 | -315.615 | 83 | S43 | 327.120 | 296.000 | 139 | S95 | -1184.880 | 296.000 |
| 28 | SCL | 1143.715 | -315.615 | 84 | S44 | 300.120 | 296.000 | 140 | S96 | -1211.880 | 296.000 |
| 29 | CSB | 1229.715 | -315.615 | 85 | S45 | 273.120 | 296.000 | 141 | S97 | -1238.880 | 296.000 |
| 30 | BUSY_N | 1315.715 | -315.615 | 86 | S46 | 246.120 | 296.000 | 142 | S98 | -1265.880 | 296.000 |
| 31 | MS | 1401.715 | -315.615 | 87 | S47 | 219.120 | 296.000 | 143 | S99 | -1292.880 | 296.000 |
| 32 | CL | 1487.715 | -315.615 | 88 | S48 | 192.120 | 296.000 | 144 | S100 | -1319.880 | 296.000 |
| 33 | TEST_N | 1573.715 | -315.615 | 89 | S49 | 165.120 | 296.000 | 145 | S101 | -1346.880 | 296.000 |
| 34 | VSYN | 1659.715 | -315.615 | 90 | S50 | 138.120 | 296.000 | 146 | S102 | -1373.880 | 296.000 |
| 35 | DUMMY | 2000.800 | -315.615 | 91 | S51 | 111.120 | 296.000 | 147 | S103 | -1400.880 | 296.000 |
| 36 | ALIGN_B | 2002.000 | 113.280 | 92 | S52 | 84.120 | 296.000 | 148 | S104 | -1427.880 | 296.000 |
| 37 | DUMMY | 2000.800 | 305.300 | 93 | S53 | 57.120 | 296.000 | 149 | S105 | -1454.880 | 296.000 |
| 38 | DUMMY | 1595.870 | 296.000 | 94 | S54 | 30.120 | 296.000 | 150 | S106 | -1481.880 | 296.000 |
| 39 | COMBG0 | 1515.120 | 296.000 | 95 | S55 | 3.120 | 296.000 | 151 | S107 | -1508.880 | 296.000 |
| 40 | COMBG0 | 1488.120 | 296.000 | 96 | S56 | -23.880 | 296.000 | 152 | S108 | -1535.880 | 296.000 |
| 41 | S1 | 1461.120 | 296.000 | 97 | S57 | -50.880 | 296.000 | 153 | S109 | -1562.880 | 296.000 |
| 42 | S2 | 1434.120 | 296.000 | 98 | S58 | -77.880 | 296.000 | 154 | S110 | -1589.880 | 296.000 |
| 43 | S3 | 1407.120 | 296.000 | 99 | S59 | -104.880 | 296.000 | 155 | S111 | -1616.880 | 296.000 |
| 44 | S4 | 1380.120 | 296.000 | 100 | S60 | -131.880 | 296.000 | 156 | S112 | -1643.880 | 296.000 |
| 45 | S5 | 1353.120 | 296.000 | 101 | COMBG1 | -158.880 | 296.000 | 157 | S113 | -1670.880 | 296.000 |
| 46 | S6 | 1326.120 | 296.000 | 102 | COMBG1 | -185.880 | 296.000 | 158 | S114 | -1697.880 | 296.000 |
| 47 | S7 | 1299.120 | 296.000 | 103 | COMBG2 | -212.880 | 296.000 | 159 | S115 | -1724.880 | 296.000 |
| 48 | S8 | 1272.120 | 296.000 | 104 | COMBG2 | -239.880 | 296.000 | 160 | S116 | -1751.880 | 296.000 |
| 49 | S9 | 1245.120 | 296.000 | 105 | S61 | -266.880 | 296.000 | 161 | S117 | -1778.880 | 296.000 |

| No. | Name | X | Y | No. | Name | X | Y | No. | Name | X | Y |
|-----|------|----------|---------|-----|------|----------|---------|-----|--------|-----------|---------|
| 50 | S10 | 1218.120 | 296.000 | 106 | S62 | -293.880 | 296.000 | 162 | S118 | -1805.880 | 296.000 |
| 51 | S11 | 1191.120 | 296.000 | 107 | S63 | -320.880 | 296.000 | 163 | S119 | -1832.880 | 296.000 |
| 52 | S12 | 1164.120 | 296.000 | 108 | S64 | -347.880 | 296.000 | 164 | S120 | -1859.880 | 296.000 |
| 53 | S13 | 1137.120 | 296.000 | 109 | S65 | -374.880 | 296.000 | 165 | COMBG3 | -1886.880 | 296.000 |
| 54 | S14 | 1110.120 | 296.000 | 110 | S66 | -401.880 | 296.000 | 166 | COMBG3 | -1913.880 | 296.000 |
| 55 | S15 | 1083.120 | 296.000 | 111 | S67 | -428.880 | 296.000 | | | | |
| 56 | S16 | 1056.120 | 296.000 | 112 | S68 | -455.880 | 296.000 | | | | |

Pad Description

| Pad Name | Type | Description |
|--|------|--|
| Power Supply Pins | | |
| VDD | — | Logic power supply |
| GND | — | Logic ground |
| AVDD | — | Analog power supply |
| AGND | — | Analog ground |
| Charge Pump Controller Pins | | |
| VDL | O | Driver low supply voltage – bypass to GND with 1μF capacitor |
| VDH | O | Driver high supply voltage – bypass to GND with 1μF capacitor |
| Serial Communication Interface Pins | | |
| CSB | I | Chip select CSB="0" – device is active |
| SDA | I/O | Serial data input/output pin |
| SCL | I | Serial clock input pin |
| Control Interface Pins | | |
| RST_N | I | Reset pin – active low |
| SHD_N | I | Charge pump enable pin – low shutdown |
| BUSY_N | O | Busy flag output pin BUSY_N="0" – driver is busy, driver is refreshing the display BUSY_N="1" – driver is idle, host can send command/data to driver |
| MS | I | Master or slave IC select pin MS="1" – device set as master MS="0" – device set as slave |
| CL | I/O | System clock pin In the cascade mode, the master IC generates a clock signal for the slave IC via the CL pin when the cascade setting command is executed. In the single chip mode, this pin remains at a high level and is not used. |
| VSYNC | I/O | Frame synchronization signal pin In the cascade mode, the master IC generates a vsync signal for the slave IC through the VSYNC pin when the cascade setting command is executed. In the single chip mode, this pin remains at a high level and is not used. |
| TEST_N | I | Test pin, remains floating in normal mode |
| Driver Output Pins | | |
| S1~S120 | O | Segment driver output pins |
| COMBG0~COMBG3 | O | Common or Background driver output pin These pins can be set as COM or BG pin separately by a CBS command |

Approximate Internal Connections



Absolute Maximum Ratings

Logic Supply Voltage..... $V_{SS}-0.3V$ to $V_{SS}+6.5V$
 Driver Supply Voltage..... $V_{SS}-0.3V$ to $V_{SS}+13.2V$
 Input Voltage..... $V_{SS}-0.3V$ to $V_{DD}+0.3V$

Storage Temperature $-55^{\circ}C$ to $150^{\circ}C$
 Operating Temperature $0^{\circ}C$ to $70^{\circ}C$

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics
 $V_{SS}=0V$; $V_{DD}=2.4V\sim 3.6V$; $T_a=0^{\circ}C\sim 70^{\circ}C$

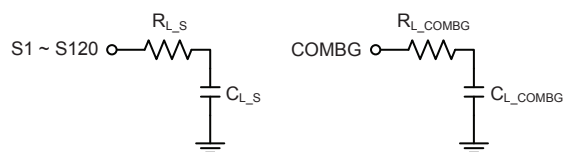
| Symbol | Parameter | Test condition | | Min. | Typ. | Max. | Unit |
|------------|-----------------------------|----------------|---|---------------------|------|---------------------|------------|
| | | V_{DD} | Condition | | | | |
| V_{DD} | Logic Power Supply Voltage | — | — | 2.4 | — | 3.6 | V |
| AV_{DD} | Analog Power Supply Voltage | — | — | 2.4 | — | 3.6 | V |
| V_{DH} | EPD High Driving Voltage | — | $V_{DH_LV}[5:0]=010100b$ | 5.75 | 6 | 6.25 | V |
| V_{DL} | EPD Low Driving Voltage | — | $V_{DL_LV}[5:0]=010100b$ | 2.75 | 3 | 3.25 | V |
| V_{IH} | Input High Voltage | — | All input pins | $0.7 \times V_{DD}$ | — | V_{DD} | V |
| V_{IL} | Input Low Voltage | — | All input pins | 0 | — | $0.3 \times V_{DD}$ | V |
| I_{IL} | Input leakage Current | — | $V_{IN}=V_{DD}, V_{SS}$. All input pins except CSB, RST_N | -1 | — | 1 | μA |
| I_{OH} | High Level Output Current | 3.3V | $V_{OH}=0.9 \times V_{DD}$, SDA, BUSY_N, CL, VSYNC | -6 | — | — | mA |
| I_{OL} | Low Level Output Current | 3.3V | $V_{OL}=0.1 \times V_{DD}$, SDA, BUSY_N, CL, VSYNC | 6 | — | — | mA |
| I_{STB} | Logic Standby Current | 3.3V | No load, charge pump Off status | — | — | 1 | μA |
| I_{STB1} | Analog Standby Current | 3.3V | | — | — | 1 | μA |
| I_{DD} | Logic Operating Current | 3.3V | No load, charge pump On status | — | 80 | 120 | μA |
| I_{DD1} | Analog Operating Current | 3.3V | | — | 80 | 120 | μA |
| I_{OL1} | COMBG Sink Current | 3.3V | $V_o=12V, V_{OL}=1.2V$ | 3.0 | 6.0 | — | mA |
| I_{OH1} | COMBG Source Current | 3.3V | $V_o=12V, V_{OH}=10.8V$ | -2.2 | -4.5 | — | mA |
| I_{OL2} | Segment Sink Current | 3.3V | $V_o=12V, V_{OL}=1.2V$ | 1.0 | 2.0 | — | mA |
| I_{OH2} | Segment Source Current | 3.3V | $V_o=12V, V_{OH}=10.8V$ | -0.7 | -1.5 | — | mA |
| R_{PH} | Pull-high Resistance | 3.3V | CSB, RST_N, TEST_N | — | 50 | 100 | k Ω |

A.C. Characteristics

 $V_{SS}=0V; V_{DD}=2.4V\sim 3.6V; T_a=0^{\circ}C\sim 70^{\circ}C$

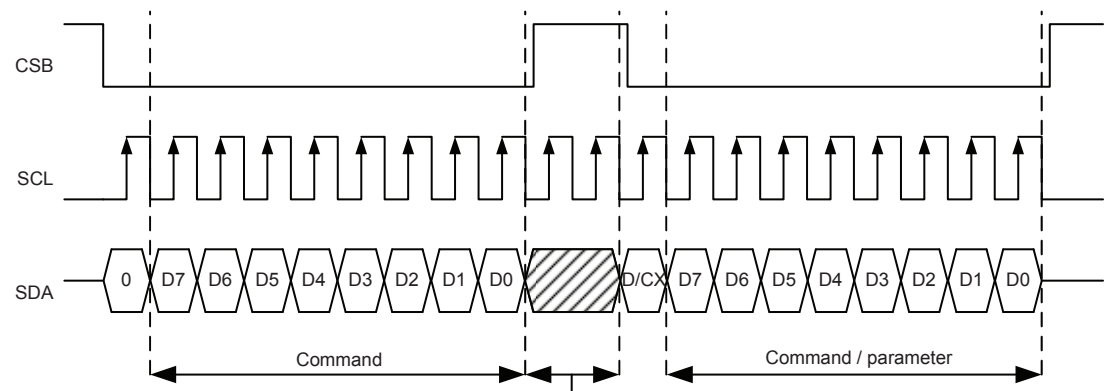
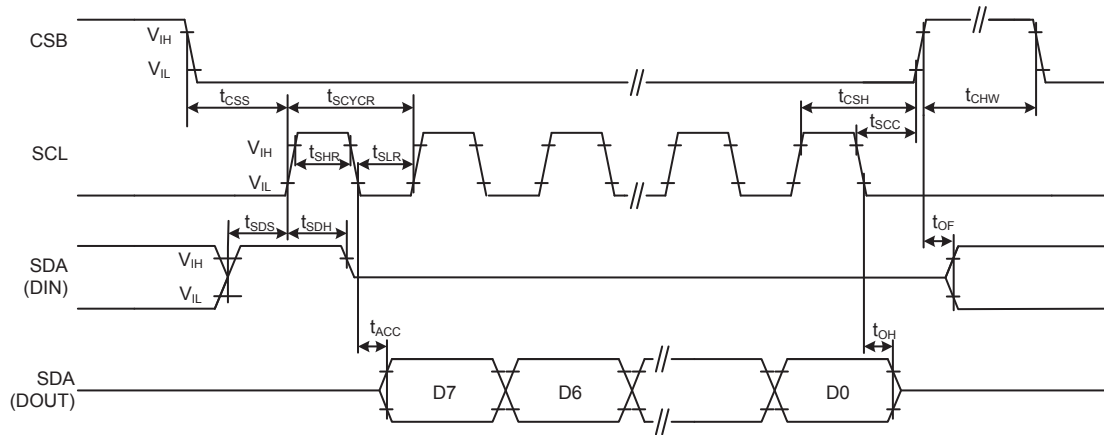
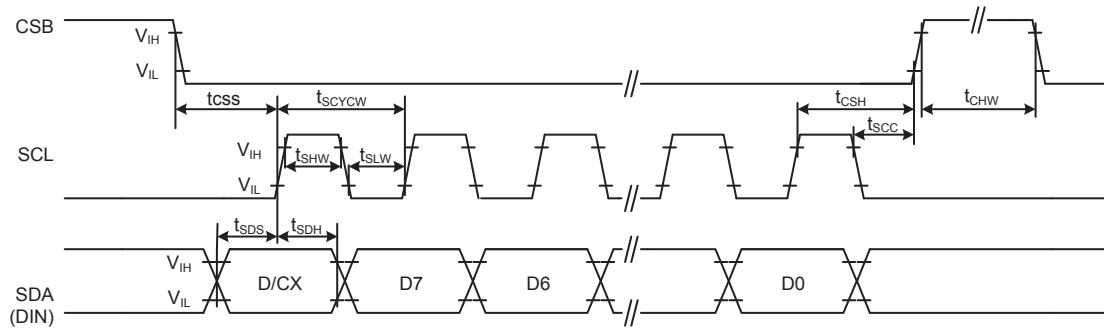
| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------------|--|--|------|------|------|---------|
| t_{CSS} | Chip Select Setup Time | — | 60 | — | — | ns |
| t_{CSH} | Chip Select Hold Time | — | 100 | — | — | ns |
| t_{SCC} | Chip Select Hold Time in Read Mode | — | 60 | — | — | ns |
| t_{CHW} | Chip Select Pulse Width | — | 60 | — | — | ns |
| t_{SCYCW} | SCL Clock Cycle Time in Write Mode | — | 100 | — | — | ns |
| t_{SHW} | SCL High Pulse Width in Write Mode | — | 35 | — | — | ns |
| t_{SLW} | SCL Low Pulse Width in Write Mode | — | 35 | — | — | ns |
| t_{SCYCR} | SCL Clock Cycle Time in Read Mode | — | 150 | — | — | ns |
| t_{SHR} | SCL High Pulse Width in Read Mode | — | 60 | — | — | ns |
| t_{SLR} | SCL Low Pulse Width in Read Mode | — | 60 | — | — | ns |
| t_{SDS} | Data Setup Time | — | 50 | — | — | ns |
| t_{SDH} | Data Hold Time | — | 50 | — | — | ns |
| t_{ACC} | Access Time | — | — | 25 | 35 | ns |
| t_{OH} | Output Disable Time | — | — | 25 | 35 | ns |
| t_{OF} | Output Floating Time | — | 50 | — | — | ns |
| t_{RSEG} | Segment Driver Rise Time | 99% final value, $C_{L_S}=30pF$, $R_{L_S}=10k\Omega^*$ | — | 1.0 | 1.5 | μs |
| t_{FSEG} | Segment Driver Fall Time | 1% final value, $C_{L_S}=30pF$, $R_{L_S}=10k\Omega^*$ | — | 0.8 | 1.2 | μs |
| t_{RCOMBG} | COMBG Driver Rise Time | 99% final value, $C_{L_COMBG}=2nF$, $R_{L_COMBG}=1k\Omega^*$ | — | 8 | 12 | μs |
| t_{FCOMBG} | COMBG Driver Fall Time | 1% final value, $C_{L_COMBG}=2nF$, $R_{L_COMBG}=1k\Omega^*$ | — | 6 | 9 | μs |
| V_{POR} | VDD Start Voltage to Ensure Power-on Reset | — | — | — | 100 | mV |
| RR_{VDD} | VDD Rise Rate to Ensure Power-on Reset | — | 0.05 | — | — | V/ms |
| t_{POR} | Minimum Time for VDD to Remain at V_{POR} to Ensure Power-on Reset | — | 10 | — | — | ms |

Note: * driver output RC loading.

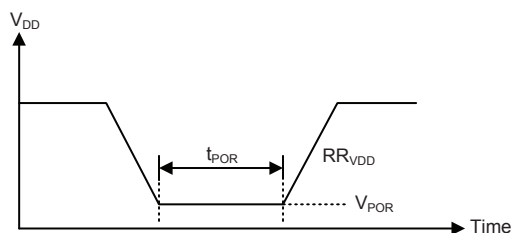


Timing Diagrams

SPI 3-Wire Interface Timing



1. CSB can be set to "1" between command and command/parameter
2. SCL and SDA is invalid when CSB = "1"

Power on Reset Timing


Note: 1. If the conditions of Reset timing are not satisfied during the power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.

2. Data transfers on the serial bus should at least be delayed for 1ms after the power-on sequence to ensure that the reset operation is complete.

Command Table

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|-----|------|--------------|--------------|-------------|------|---------|------|--------|---------|---------|
| Panel Setting (PSR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h |
| | 0 | 1 | BWR | — | — | — | VDLH_EN | DDX | SHD_N | RST_N | 8Fh |
| Power Setting (PWR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h |
| | 0 | 1 | — | — | VDH_LV[5:0] | | | | | | 1Eh |
| | 0 | 1 | — | — | VDL_LV[5:0] | | | | | | 1Eh |
| Charge Pump OFF (CPOF) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02h |
| | 0 | 1 | — | — | — | — | — | — | SGM_FL | VCOM_FL | 03h |
| Charge Pump ON (CPON) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04h |
| COMBG Set (CBS) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05h |
| | 0 | 1 | — | — | — | — | CBS3 | CBS2 | CBS1 | CBS0 | 0Bh |
| Data Start Transmission (DTM) (17-byte command) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10h |
| | 0 | 1 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | 00h |
| | 0 | 1 | S9 | S10 | S11 | S12 | S13 | S14 | S15 | S16 | 00h |
| | 0 | 1 | S17 | S18 | S19 | S20 | S21 | S22 | S23 | S24 | 00h |
| | 0 | 1 | ... | ... | ... | ... | ... | ... | ... | ... | 00h |
| | 0 | 1 | S113 | S114 | S115 | S116 | S117 | S118 | S119 | S120 | 00h |
| | 0 | 1 | BG | — | — | — | — | — | — | — | 00h |
| Data Stop (DSP) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11h |
| | 1 | 1 | data_flag | — | — | — | — | — | — | — | — |
| Display Refresh (DRF) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12h |
| V _{COM} LUT (LUTV) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| | 0 | 1 | LVL_V1[1:0] | FRM_V1[5:0] | | | | | | 00h | |
| | 0 | 1 | LVL_V2[1:0] | FRM_V2[5:0] | | | | | | 00h | |
| | 0 | 1 | PHS_V[7:0] | | | | | | | | |
| BlackBlack LUT (LUT_KK) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21h |
| | 0 | 1 | LVL_KK1[1:0] | FRM_KK1[5:0] | | | | | | 00h | |
| | 0 | 1 | LVL_KK2[1:0] | FRM_KK2[5:0] | | | | | | 00h | |
| | 0 | 1 | PHS_KK[7:0] | | | | | | | | |
| BlackWhite LUT (LUT_KW) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22h |
| | 0 | 1 | LVL_KW1[1:0] | FRM_KW1[5:0] | | | | | | 00h | |
| | 0 | 1 | LVL_KW2[1:0] | FRM_KW2[5:0] | | | | | | 00h | |
| | 0 | 1 | PHS_KW[7:0] | | | | | | | | |
| WhiteBlack LUT (LUT_WK) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23h |
| | 0 | 1 | LVL_WK1[1:0] | FRM_WK1[5:0] | | | | | | 00h | |
| | 0 | 1 | LVL_WK2[1:0] | FRM_WK2[5:0] | | | | | | 00h | |
| | 0 | 1 | PHS_WK[7:0] | | | | | | | | |

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|-----|------|--------------|-------|--------------|-------|-----------|-----|-----|--------|---------|
| WhiteWhite LUT (LUT_WW) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24h |
| | 0 | 1 | LVL_WW1[1:0] | | FRM_WW1[5:0] | | | | | | 00h |
| | 0 | 1 | LVL_WW2[1:0] | | FRM_WW2[5:0] | | | | | | 00h |
| | 0 | 1 | PHS_WW[7:0] | | | | | | | | |
| Frame Rate Control (FRC) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30h |
| | 0 | 1 | SF[1] | SF[0] | NF[1] | NF[0] | — | P2 | P1 | P0 | 83h |
| Temperature Sensor (TSC) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40h |
| | 1 | 1 | Busy_N | — | — | — | TS3 | TS2 | TS1 | TS0 | — |
| Revision (REV) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70h |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h |
| Get Status (FLG) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71h |
| | 1 | 1 | 0 | 0 | 0 | TS_ON | data_flag | PON | POF | Busy_N | 02h |
| Cascade Setting | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0h |
| | 0 | 1 | — | — | — | — | — | — | — | CAS_EN | 00h |
| Test mode | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FEh |

Command Description

Panel Setting (PSR) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|------------------------|-----|------|-----|----|----|----|---------|-----|-------|-------|---------|
| Panel Setting (PSR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h |
| | 0 | 1 | BWR | — | — | — | VDLH_EN | DDX | SHD_N | RST_N | 8Fh |

“—”: Don't care

The command descriptions are as follows:

BWR: Black/white or red color select

0: Select red. V_{DH} and V_{DL} are set by PWR command

1: Select black/white (default). V_{DH} is fixed to 12V and V_{DL} is set by the PWR command

VDLH_EN: V_{DL}/V_{DH} source select

0: External V_{DL}/V_{DH} power from V_{DL}/V_{DH} pin

1: Generate V_{DL}/V_{DH} using internal charge pump (default)

DDX: Data index control

0: “0: white, 1: black/red”

1: “0: black/red, 1: white” (default)

SHD_N: Charge pump control

0: Charge pump OFF

1: Charge pump ON (default)

When SHD_N is set to “0”, the charge pump will be switched OFF, and when VDLH_EN=“1” the driver output will be tied to VSS

RST_N: Reset control

0: Reset all registers to their default value

1: Normal operation (default)

When RST_N is set to “0”, the driver will be reset and all register will be reset to their default value.

Power Setting (PWR) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---------------------|-----|------|----|----|-------------|----|----|----|----|----|---------|
| Power Setting (PWR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h |
| | 0 | 1 | — | — | VDH_LV[5:0] | | | | | | 1Eh |
| | 0 | 1 | — | — | VDL_LV[5:0] | | | | | | 1Eh |

“—”: Don't care

The command descriptions are as follows:

VDH_LV[5:0]: The default value is 011110b, $V_{DH}=7.00V$

| VDH_LV[5:0] | V_{DH} | VDH_LV[5:0] | V_{DH} | VDH_LV[5:0] | V_{DH} |
|-------------|----------|-------------|----------|-------------|----------|
| 000000 | 4.00 | 010000 | 5.60 | 100000 | 7.20 |
| 000001 | 4.10 | 010001 | 5.70 | 100001 | 7.30 |
| 000010 | 4.20 | 010010 | 5.80 | 100010 | 7.40 |
| 000011 | 4.30 | 010011 | 5.90 | 100011 | 7.50 |
| 000100 | 4.40 | 010100 | 6.00 | 100100 | 7.60 |
| 000101 | 4.50 | 010101 | 6.10 | 100101 | 7.70 |
| 000110 | 4.60 | 010110 | 6.20 | 100110 | 7.80 |
| 000111 | 4.70 | 010111 | 6.30 | 100111 | 7.90 |
| 001000 | 4.80 | 011000 | 6.40 | 101000 | 8.00 |
| 001001 | 4.90 | 011001 | 6.50 | Others | 8.00 |
| 001010 | 5.00 | 011010 | 6.60 | | |
| 001011 | 5.10 | 011011 | 6.70 | | |
| 001100 | 5.20 | 011100 | 6.80 | | |
| 001101 | 5.30 | 011101 | 6.90 | | |
| 001110 | 5.40 | 011110 | 7.00 | ←-default | |
| 001111 | 5.50 | 011111 | 7.10 | | |

VDL_LV[5:0]: The default value is 011110b, $V_{DL}=3.50V$

| VDL_LV[5:0] | V_{DL} | VDL_LV[5:0] | V_{DL} | VDL_LV[5:0] | V_{DL} |
|-------------|----------|-------------|----------|-------------|----------|
| 000000 | 2.00 | 010000 | 2.80 | 100000 | 3.60 |
| 000001 | 2.05 | 010001 | 2.85 | 100001 | 3.65 |
| 000010 | 2.10 | 010010 | 2.90 | 100010 | 3.70 |
| 000011 | 2.15 | 010011 | 2.95 | 100011 | 3.75 |
| 000100 | 2.20 | 010100 | 3.00 | 100100 | 3.80 |
| 000101 | 2.25 | 010101 | 3.05 | 100101 | 3.85 |
| 000110 | 2.30 | 010110 | 3.10 | 100110 | 3.90 |
| 000111 | 2.35 | 010111 | 3.15 | 100111 | 3.95 |
| 001000 | 2.40 | 011000 | 3.20 | 101000 | 4.00 |
| 001001 | 2.45 | 011001 | 3.25 | Others | 4.00 |
| 001010 | 2.50 | 011010 | 3.30 | | |
| 001011 | 2.55 | 011011 | 3.35 | | |
| 001100 | 2.60 | 011100 | 3.40 | | |
| 001101 | 2.65 | 011101 | 3.45 | | |
| 001110 | 2.70 | 011110 | 3.50 | ←-default | |
| 001111 | 2.75 | 011111 | 3.55 | | |

Charge Pump OFF (CPOF) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|------------------------|-----|------|----|----|----|----|----|----|--------|---------|---------|
| Charge Pump OFF (CPOF) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02h |
| | 0 | 1 | — | — | — | — | — | — | SGM_FL | VCOM_FL | 03h |

“—”: Don't care

After executing a charge pump OFF command, BUSY_N will be set to “0”. This command will turn off the charge pump, driver output and temperature sensor but the register data will be kept until VDD OFF. The charge pump OFF sequence is shown below.

The command descriptions are as follows:

SGM_FL: Segment and BG level selection when charge pump OFF

0: Segment and BG – floating when charge pump OFF

1: Segment and BG – ground when charge pump OFF (default)

VCOM_FL: COM level selection when charge pump OFF

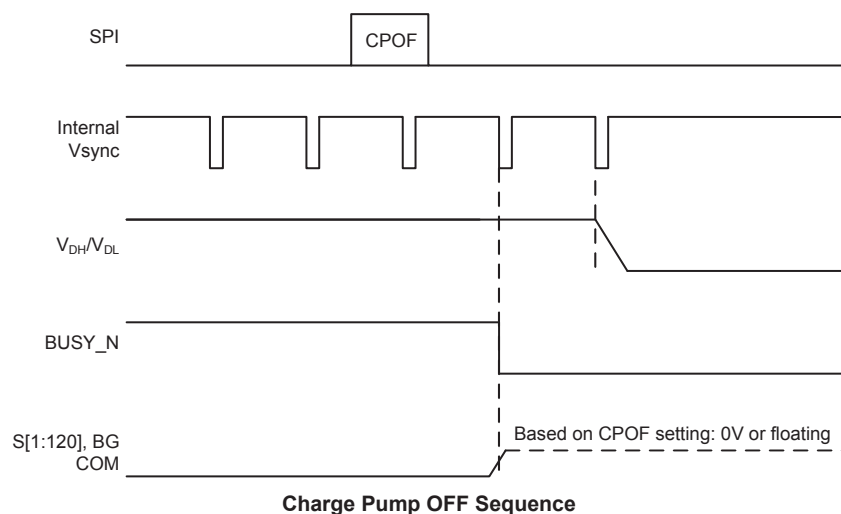
0: COM – floating when charge pump OFF

1: COM – ground when charge pump OFF (default)

Note that this action could not change the data_flag status.

This command is only active when BUSY_N = “1”.

After finishing a power-on reset, the driver is in the charge pump OFF stage.



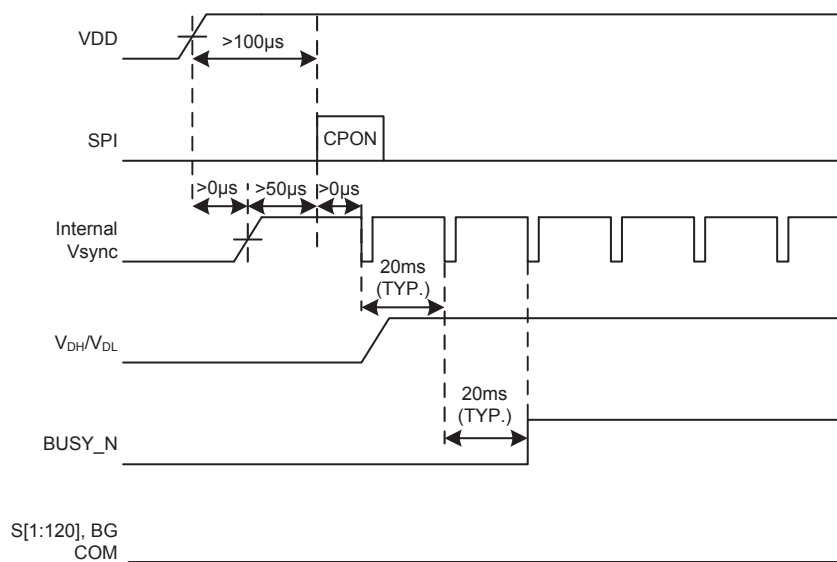
Charge Pump ON (CPON) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----------------------|-----|------|----|----|----|----|----|----|----|----|---------|
| Charge Pump ON (CPON) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04h |

After executing the charge pump ON command, the charge pump will be active. The charge pump ON sequence is shown below.

After the charge pump ON command and all power sequences are ready, BUSY_N will be set to “1”.

The user must execute a charge pump ON command before accessing the driver IC.



Charge Pump ON Sequence

COMBG Set (CBS) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----------------|-----|------|----|----|----|----|------|------|------|------|---------|
| COMBG Set (CBS) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05h |
| | 0 | 1 | — | — | — | — | CBS3 | CBS2 | CBS1 | CBS0 | 0Bh |

The command descriptions are as follows.

CBS3:

- 0: COMBG3 pin is set as COM pin
- 1: COMBG3 pin is set as BG pin

CBS2:

- 0: COMBG2 pin is set as COM pin
- 1: COMBG2 pin is set as BG pin

CBS1:

- 0: COMBG1 pin is set as COM pin
- 1: COMBG1 pin is set as BG pin

CBS0:

- 0: COMBG0 pin is set as COM pin
- 1: COMBG0 pin is set as BG pin

This command is used to set the COMBG0~COMBG3 pins as COM or BG pins separately for various applications.

When CBS[3:0]=Bh, the COMBG3~COMBG0 pins are set as shown in the table.

| | | | | | | | | | | | | | | | | | | |
|----------|----------------|----------------|------|------|------|-----|-----|-----------------|-----------------|----------------|----------------|-----|-----|------|----|----|----------------|----------------|
| Pin Name | BG (COMBG3) | BG (COMBG3) | S120 | S119 | | S62 | S61 | COM (COMBG2) | COM (COMBG2) | BG (COMBG1) | BG (COMBG1) | S60 | S59 | | S2 | S1 | BG (COMBG0) | BG (COMBG0) |
|----------|----------------|----------------|------|------|------|-----|-----|-----------------|-----------------|----------------|----------------|-----|-----|------|----|----|----------------|----------------|

Data Start Transmission (DTM) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|-----|------|------|------|------|------|------|------|------|------|---------|
| Data Start Transmission (DTM) (17-byte command) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10h |
| | 0 | 1 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | 00h |
| | 0 | 1 | S9 | S10 | S11 | S12 | S13 | S14 | S15 | S16 | 00h |
| | 0 | 1 | S17 | S18 | S19 | S20 | S21 | S22 | S23 | S24 | 00h |
| | 0 | 1 | S25 | S26 | S27 | S28 | S29 | S30 | S31 | S32 | 00h |
| | 0 | 1 | S33 | S34 | S35 | S36 | S37 | S38 | S39 | S40 | 00h |
| | 0 | 1 | S41 | S42 | S43 | S44 | S45 | S46 | S47 | S48 | 00h |
| | 0 | 1 | S49 | S50 | S51 | S52 | S53 | S54 | S55 | S56 | 00h |
| | 0 | 1 | S57 | S58 | S59 | S60 | S61 | S62 | S63 | S64 | 00h |
| | 0 | 1 | S65 | S66 | S67 | S68 | S69 | S70 | S71 | S72 | 00h |
| | 0 | 1 | S73 | S74 | S75 | S76 | S77 | S78 | S79 | S80 | 00h |
| | 0 | 1 | S81 | S82 | S83 | S84 | S85 | S86 | S87 | S88 | 00h |
| | 0 | 1 | S89 | S90 | S91 | S92 | S93 | S94 | S95 | S96 | 00h |
| | 0 | 1 | S97 | S98 | S99 | S100 | S101 | S102 | S103 | S104 | 00h |
| | 0 | 1 | S105 | S106 | S107 | S108 | S109 | S110 | S111 | S112 | 00h |
| | 0 | 1 | S113 | S114 | S115 | S116 | S117 | S118 | S119 | S120 | 00h |
| | 0 | 1 | BG | — | — | — | — | — | — | — | — |

“—”: Don't care

The command starts to transmit data and write to the new_data register. The original data will be moved to the previous_data register at the same time for the data comparison function.

Note that users must send the full 17-byte command at once. If less than a 17-byte command is sent, the contents of the previous_data register will be incorrect. In this case the outcome will be that the result of the data comparison between the new_data register and the previous_data register will be incorrect.

After transmitting all data completely (17-bytes command), the data_flag will be set to “1”.

This command is only active when BUSY_N = “1”.

Data Stop (DSP) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----------------|-----|------|-----------|----|----|----|----|----|----|----|---------|
| Data Stop (DSP) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11h |
| | 1 | 1 | data_flag | — | — | — | — | — | — | — | — |

“—”: Don't care

The command descriptions are as follows.

Data_flag:

- 0: The driver IC did not receive all the data
- 1: The driver IC has received all the data completely

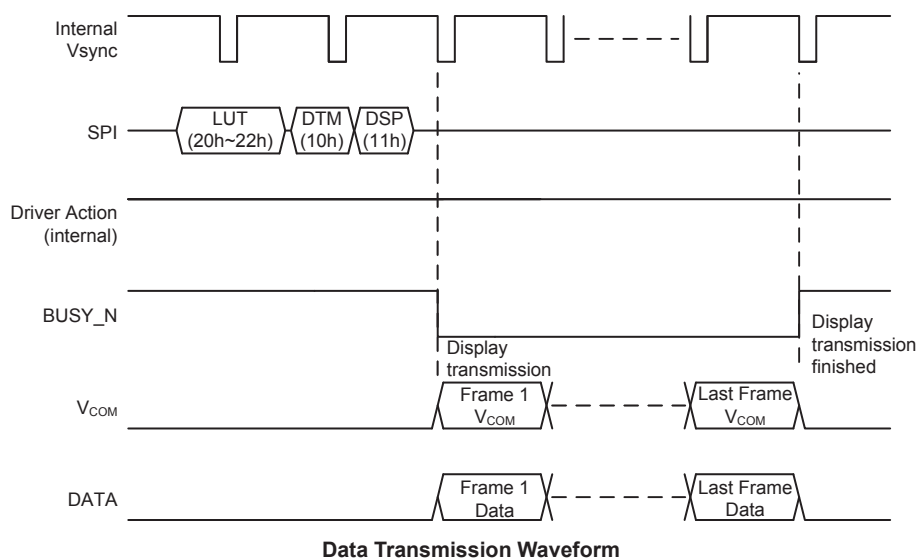
This command is used to read the data transmission status. When the driver IC has received all the 16 bytes data through the DTM command, the data_flag will be set to “1”.

When this command is executed and the data_flag is “1”, the IC will refresh the display according to the new_data register, previous_data register and LUT.

After executing a DTM command and a DSP command, BUSY_N will be set to “0”.

After finishing a display refresh, BUSY_N will be set to “1” and the data_flag will be set to “0”.

The data transmission waveform is shown below:



Display Refresh (DRF) Command

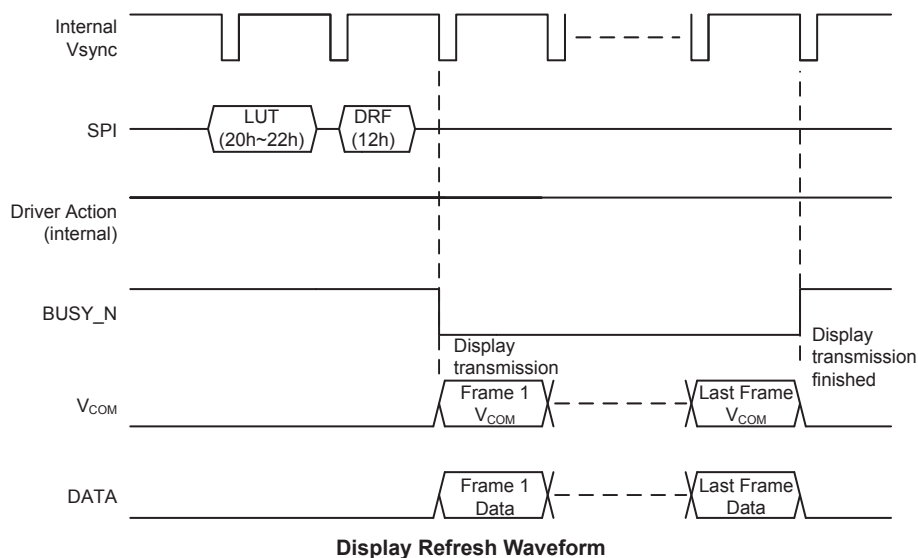
| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----------------------|-----|------|----|----|----|----|----|----|----|----|---------|
| Display Refresh (DRF) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12h |

After executing a DRF command, BUSY_N will be set to “0”. Then the driver IC will refresh the display according to the new_data register, the previous_data register and LUT.

After finishing display fresh, BUSY_N will be set to “1” automatically.

This command only active when BUSY_N = “1”.

The display refresh waveform is shown below:



V_{COM} LUT (LUTV) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|-----|------|-------------|----|-------------|----|----|----|----|----|---------|
| V _{COM} LUT (LUTV) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| | 0 | 1 | LVL_V1[1:0] | | FRM_V1[5:0] | | | | | | 00h |
| | 0 | 1 | LVL_V2[1:0] | | FRM_V2[5:0] | | | | | | 00h |
| | 0 | 1 | PHS_V[7:0] | | | | | | | | |

The command descriptions are as follows:

LVL_V1[1:0]: (bytes 2, 5, 8, 11, 14): Level selection (1)

LVL_V2[1:0]: (bytes 3, 6, 9, 12, 15): Level selection (2)

| LVL_Vx[1:0] | Level(x) |
|-------------|-----------------|
| 00 | V _{DL} |
| 01 | V _{DH} |
| 10 | 0V |
| 11 | Floating |

FRM_V1[5:0]: (bytes 2, 5, 8, 11, 14): Number of Frames (1)

FRM_V2[5:0]: (bytes 3, 6, 9, 12, 15): Number of Frames (2)

| FRM_Vx[5:0] | Number of Frames(x) |
|-------------|---------------------|
| 000000 | 0 |
| 000001 | 1 |
| 000010 | 2 |
| 000011 | 3 |
| : | : |
| 111111 | 63 |

The frame rate is set by the FRC command.

PHS_V[7:0]: (bytes 4, 7, 10, 13, 16): Number of Phases to repeat

| PHS_V[7:0] | Number of Phase |
|------------|-----------------|
| 00000000 | 0 |
| 00000001 | 1 |
| 00000010 | 2 |
| 00000011 | 3 |
| : | : |
| 11111111 | 255 |

This command stores V_{COM} LUT using 5 groups of data with each group containing information for one phase and being stored with 3 bytes.

This command is only active when $BUSY_N = "1"$.

BlackBlack LUT (LUT_KK) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|-----|------|--------------|----|--------------|----|----|----|----|-----|---------|
| BlackBlack LUT (LUT_KK) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21h |
| | 0 | 1 | LVL_KK1[1:0] | | FRM_KK1[5:0] | | | | | 00h | |
| | 0 | 1 | LVL_KK2[1:0] | | FRM_KK2[5:0] | | | | | 00h | |
| | 0 | 1 | PHS_KK[7:0] | | | | | | | | 00h |

The command descriptions are as follows:

LVL_KK1[1:0]: (bytes 2, 5, 8, 11, 14): Level selection (1)

LVL_KK2[1:0]: (bytes 3, 6, 9, 12, 15): Level selection (2)

| LVL_KKx[1:0] | Level(x) |
|--------------|----------|
| 00 | V_{DL} |
| 01 | V_{DH} |
| 10 | 0V |
| 11 | Floating |

FRM_KK1[5:0]: (bytes 2, 5, 8, 11, 14): Number of Frames (1)

FRM_KK2[5:0]: (bytes 3, 6, 9, 12, 15): Number of Frames (2)

| FRM_KKx[5:0] | Number of Frames(x) |
|--------------|---------------------|
| 000000 | 0 |
| 000001 | 1 |
| 000010 | 2 |
| 000011 | 3 |
| : | : |
| 111111 | 63 |

The frame rate is set by the FRC command.

PHS_KK[7:0]: (bytes 4, 7, 10, 13, 16): Number of Phases to repeat

| PHS_KK[7:0] | Number of Phase |
|-------------|-----------------|
| 00000000 | 0 |
| 00000001 | 1 |
| 00000010 | 2 |
| 00000011 | 3 |
| : | : |
| 11111111 | 255 |

This command stores BlackBlack LUT using 5 groups of data with each group containing information for one phase and being stored with 3 bytes.

BlackBlack means that the previous color is black and the new color is black.

This command is only active when **BUSY_N** = “1”.

BlackWhite LUT (LUT_KW) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|-----|------|--------------|----|--------------|----|----|----|----|-----|---------|
| BlackWhite LUT (LUT_KW) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22h |
| | 0 | 1 | LVL_KW1[1:0] | | FRM_KW1[5:0] | | | | | 00h | |
| | 0 | 1 | LVL_KW2[1:0] | | FRM_KW2[5:0] | | | | | 00h | |
| | 0 | 1 | PHS_KW[7:0] | | | | | | | | 00h |

The command descriptions are as follows:

LVL_KW1[1:0]: (bytes 2, 5, 8, 11, 14): Level selection (1)

LVL_KW2[1:0]: (bytes 3, 6, 9, 12, 15): Level selection (2)

| LVL_KWx[1:0] | Level(x) |
|--------------|-----------------|
| 00 | V _{DL} |
| 01 | V _{DH} |
| 10 | 0V |
| 11 | Floating |

FRM_KW1[5:0]: (bytes 2, 5, 8, 11, 14): Number of Frames (1)

FRM_KW2[5:0]: (bytes 3, 6, 9, 12, 15): Number of Frames (2)

| FRM_KWx[5:0] | Number of Frames(x) |
|--------------|---------------------|
| 000000 | 0 |
| 000001 | 1 |
| 000010 | 2 |
| 000011 | 3 |
| : | : |
| 111111 | 63 |

The frame rate is set by the FRC command.

PHS_KW[7:0]: (bytes 4, 7, 10, 13, 16): Number of Phases to repeat

| PHS_KW[7:0] | Number of Phases |
|-------------|------------------|
| 00000000 | 0 |
| 00000001 | 1 |
| 00000010 | 2 |
| 00000011 | 3 |
| : | : |
| 11111111 | 255 |

This command stores BlackWhite LUT using 5 groups of data with each group containing information for one phase and being stored with 3 bytes.

BlackWhite means that the previous color is black and the new color is white.

This command only active when **BUSY_N** = "1".

WhiteBlack LUT (LUT_WK) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|-----|------|--------------|----|--------------|----|----|-----|----|-----|---------|
| WhiteBlack LUT (LUT_WK) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23h |
| | 0 | 1 | LVL_WK1[1:0] | | FRM_WK1[5:0] | | | | | 00h | |
| | 0 | 1 | LVL_WK2[1:0] | | FRM_WK2[5:0] | | | | | 00h | |
| | 0 | 1 | PHS_WK[7:0] | | | | | 00h | | | |
| | 0 | 1 | PHS_WK[7:0] | | | | | 00h | | | |

The command descriptions are as follows:

LVL_WK1[1:0]: (bytes 2, 5, 8, 11, 14): Level selection (1)

LVL_WK2[1:0]: (bytes 3, 6, 9, 12, 15): Level selection (2)

| LVL_WKx[1:0] | Level(x) |
|--------------|-----------------|
| 00 | V _{DL} |
| 01 | V _{DH} |
| 10 | 0V |
| 11 | Floating |

FRM_WK1[5:0]: (bytes 2, 5, 8, 11, 14): Number of Frames (1)

FRM_WK2[5:0]: (bytes 3, 6, 9, 12, 15): Number of Frames (2)

| FRM_WKx[5:0] | Number of Frames(x) |
|--------------|---------------------|
| 000000 | 0 |
| 000001 | 1 |
| 000010 | 2 |
| 000011 | 3 |
| : | : |
| 111111 | 63 |

The frame rate is set by the FRC command.

PHS_WK[7:0]: (bytes 4, 7, 10, 13, 16): Number of Phases to repeat

| PHS_WK[7:0] | Number of Phase |
|-------------|-----------------|
| 00000000 | 0 |
| 00000001 | 1 |
| 00000010 | 2 |
| 00000011 | 3 |
| : | : |
| 11111111 | 255 |

This command stores WhiteBlack LUT using 5 groups of data with each group containing information for one phase and being stored with 3 bytes.

WhiteBlack means that the previous color is white and the new color is black.

This command only active when **BUSY_N** = "1".

WhiteWhite LUT (LUT_WW) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | |
|---|-----|------|--------------|----|--------------|----|----|----|----|----|---------|-----|
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24h | |
| WhiteWhite LUT (LUT_WW) (16-byte command, bytes 2~4 repeated 5 times) | 0 | 1 | LVL_WW1[1:0] | | FRM_WW1[5:0] | | | | | | 00h | |
| | 0 | 1 | LVL_WW2[1:0] | | FRM_WW2[5:0] | | | | | | 00h | |
| | 0 | 1 | PHS_WW[7:0] | | | | | | | | | 00h |
| | 0 | 1 | | | | | | | | | | |

The command descriptions are as follows:

LVL_WW1[1:0]: (bytes 2, 5, 8, 11, 14): Level selection (1)

LVL_WW2[1:0]: (bytes 3, 6, 9, 12, 15): Level selection (2)

| LVL_WWx[1:0] | Level(x) |
|--------------|----------|
| 00 | V_{DL} |
| 01 | V_{DH} |
| 10 | 0V |
| 11 | Floating |

FRM_WW1[5:0]: (bytes 2, 5, 8, 11, 14): Number of Frames (1)

FRM_WW2[5:0]: (bytes 3, 6, 9, 12, 15): Number of Frames (2)

| FRM_WWx[5:0] | Number of Frames(x) |
|--------------|---------------------|
| 000000 | 0 |
| 000001 | 1 |
| 000010 | 2 |
| 000011 | 3 |
| : | : |
| 111111 | 63 |

The frame rate is set by the FRC command.

PHS_WW[7:0]: (bytes 4, 7, 10, 13, 16): Number of Phases to repeat

| PHS_WW[7:0] | Number of Phase |
|-------------|-----------------|
| 00000000 | 0 |
| 00000001 | 1 |
| 00000010 | 2 |
| 00000011 | 3 |
| : | : |
| 11111111 | 255 |

This command stores WhiteWhite LUT using 5 groups of data with each group containing information for one phase and being stored with 3 bytes.

WhiteWhite means that the previous color is white and the new color is white.

This command only active when BUSY_N = "1".

Frame Rate Control (FRC) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|--------------------------|-----|------|-------|-------|-------|-------|----|----|----|----|---------|
| Frame Rate Control (FRC) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30h |
| | 0 | 1 | SF[1] | SF[0] | NF[1] | NF[0] | — | P2 | P1 | P0 | 83h |

“—”: Don't care

The command descriptions are as follows:

SF[1:0]: Switching frequency control during the charge-pump start-up stage.

| SF[1] | SF[0] | Frequency |
|-------|-------|----------------|
| 0 | 0 | 2MHz |
| 0 | 1 | 4MHz |
| 1 | 0 | 8MHz (default) |
| 1 | 1 | 12MHz |

NF[1:0]: Switching frequency control during the charge-pump normal stage.

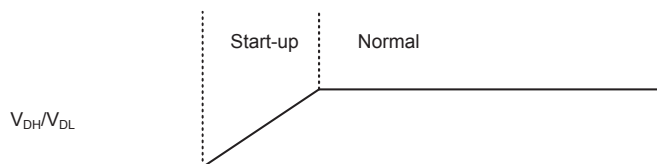
| NF[1] | NF[0] | Frequency |
|-------|-------|----------------|
| 0 | 0 | 2MHz (default) |
| 0 | 1 | 4MHz |
| 1 | 0 | 8MHz |
| 1 | 1 | 12MHz |

P[2:0]: The frame rate control.

| P[2:0] | Frame rate | P[2:0] | Frame rate |
|--------|---------------|--------|------------|
| 000 | 10Hz | 100 | 57Hz |
| 001 | 20Hz | 101 | 67Hz |
| 010 | 40Hz | 110 | 80Hz |
| 011 | 50Hz(default) | 111 | 100Hz |

SF[1:0] and NF[1:0] are used to control the charge pump switching frequency. During the start-up stage, the default frequency is set to 8MHz and the rise time is about 40ms at $V_{DD}=3V$. In the normal stage, the default frequency is set to 2MHz to reduce power consumption.

The user can control the switching frequency for different applications to reduce the power consumption, noise, cost and capacitor value.



Note: The V_{DH}/V_{DL} charge stage definition.

Temperature sensor (TSC) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|--------------------------|-----|------|--------|----|----|----|-----|-----|-----|-----|---------|
| Temperature Sensor (TSC) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40h |
| | 1 | 1 | Busy_N | — | — | — | TS3 | TS2 | TS1 | TS0 | — |

“—”: Don't care

The command descriptions are as follows:

Busy_N:

When the TSC command is executed, the Busy_N flag will be active and the temperature sensor will also be active. It will then sense and convert the temperature.

After finishing conversion, the Busy_N flag will be idle.

The user can poll the Busy_N status to detect the temperature sensor status.

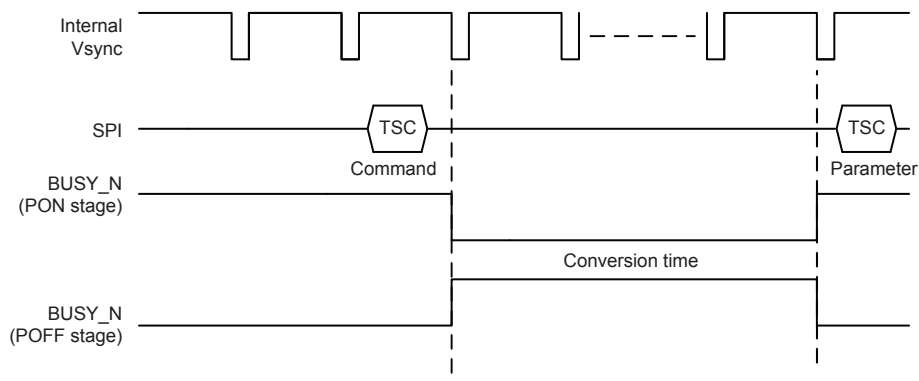
Busy_N flag definition:

| Busy_N Status | CPON Stage | CPOF Stage |
|---------------|------------|------------|
| Active | 0 | 1 |
| Idle | 1 | 0 |

TS[3:0]: Temperature values.

| TS[3:0] | Temperature | TS[3:0] | Temperature |
|---------|-------------|---------|-------------|
| 0000 | <-10°C | 1000 | 25°C |
| 0001 | <-10°C | 1001 | 30°C |
| 0010 | -5°C | 1010 | 35°C |
| 0011 | 0°C | 1011 | 40°C |
| 0100 | 5°C | 1100 | 45°C |
| 0101 | 10°C | 1101 | 50°C |
| 0110 | 15°C | 1110 | 55°C |
| 0111 | 20°C | 1111 | >60°C |

After the TSC command has been sent, BUSY_N will active and the temperature sensor will be active. It will then sense and convert the temperature. After finishing conversion, the BUSY_N flag will be idle. The host can then read the temperature value.



Revision Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|----------------|-----|------|----|----|----|----|----|----|----|----|---------|
| Revision (REV) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70h |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h |

The command is used to read the IC revision. The default value is 00h.

Get status (FLG) Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|------------------|-----|------|----|----|----|-------|-----------|-----|-----|--------|---------|
| Get Status (FLG) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71h |
| | 1 | 1 | 0 | 0 | 0 | TS_ON | Data_Flag | PON | POF | Busy_N | 02h |

The command descriptions are as follows:

TS_ON:

- 0: Temperature Sensor OFF (default)
- 1: Temperature Sensor ON

Data_Flag:

- 0: All data has not been received
- 1: All data completely received

PON:

- 0: —
- 1: Power is ON

POFF:

- 0: —
- 1: Power is OFF

BUSY_N:

- 0: Busy
- 1: Idle

Cascade Setting Command

| Command | R/W | D/CX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----------------|-----|------|----|----|----|----|----|----|----|--------|---------|
| Cascade Setting | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0h |
| | 0 | 1 | — | — | — | — | — | — | — | CAS_EN | 00h |

“—”: Don't care

The command descriptions are as follows:

CAS_EN: Cascade function control

- 0: Cascade function disabled – CL and VSYNC set to “1” (default)
- 1: Cascade function enabled – CL and VSYNC output clock and VSYNC signal connected to the slave IC

This command is valid when the MS pin is set to “1”. To enable the cascade function the user has to set the MS pin for the master IC and slave IC selection.

In the slave mode the charge pump and oscillator are disabled and V_{DH} and V_{DL} are supplied from the master IC. It is not allowed to change the VDLH_EN and SHD_N status in the PSR command.

This command is only active when BUSY_N = “1”.

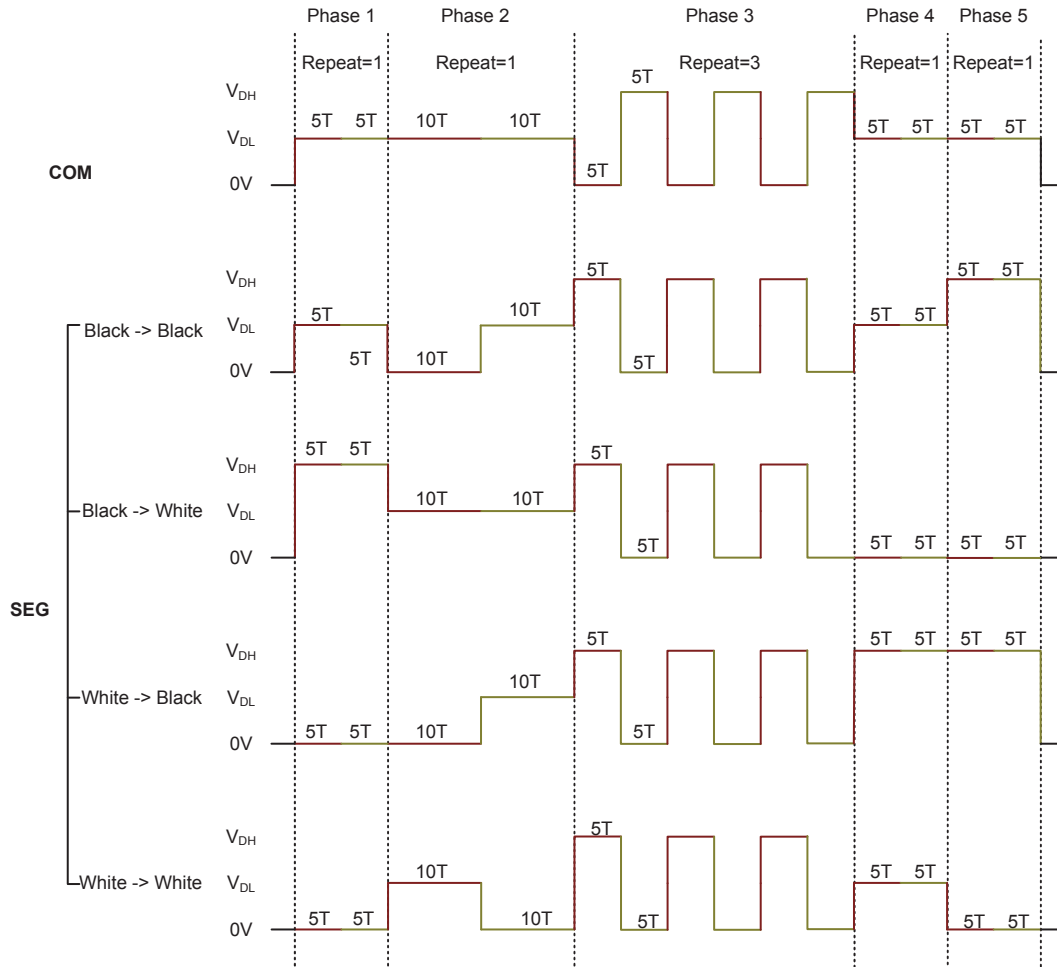
Example for LUT setting and output waveform

The LUT register structure is shown below.

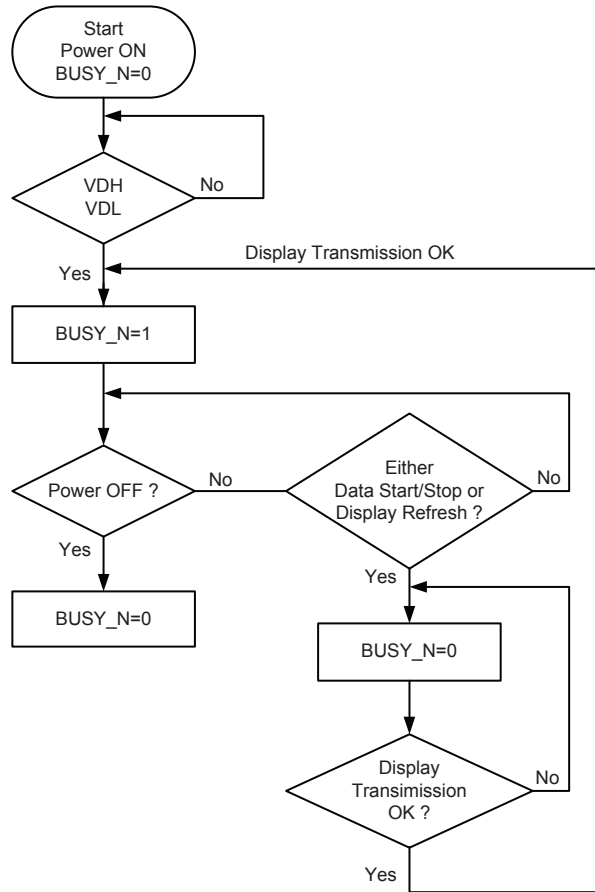
| LUT Registers | Phase 1 | | | Phase 2 | | | Phase 3 | | | Phase 4 | | | Phase 5 | | | |
|---------------|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|-----|
| LUTV | 20h | 05h | 05h | 01h | 0Ah | 0Ah | 01h | 85h | 45h | 03h | 05h | 05h | 01h | 05h | 05h | 01h |
| LUT_KK | 21h | 05h | 05h | 01h | 8Ah | 0Ah | 01h | 45h | 85h | 03h | 45h | 45h | 01h | 05h | 05h | 01h |
| LUT_KW | 22h | 45h | 45h | 01h | 0Ah | 0Ah | 01h | 45h | 85h | 03h | 05h | 05h | 01h | 05h | 05h | 01h |
| LUT_WK | 23h | 85h | 85h | 01h | 8Ah | 0Ah | 01h | 45h | 85h | 03h | 45h | 45h | 01h | 45h | 45h | 01h |
| LUT_WW | 24h | 85h | 85h | 01h | 0Ah | 8Ah | 01h | 45h | 85h | 03h | 45h | 45h | 01h | 85h | 85h | 01h |

According to the LUT register setup the output waveforms are shown below.

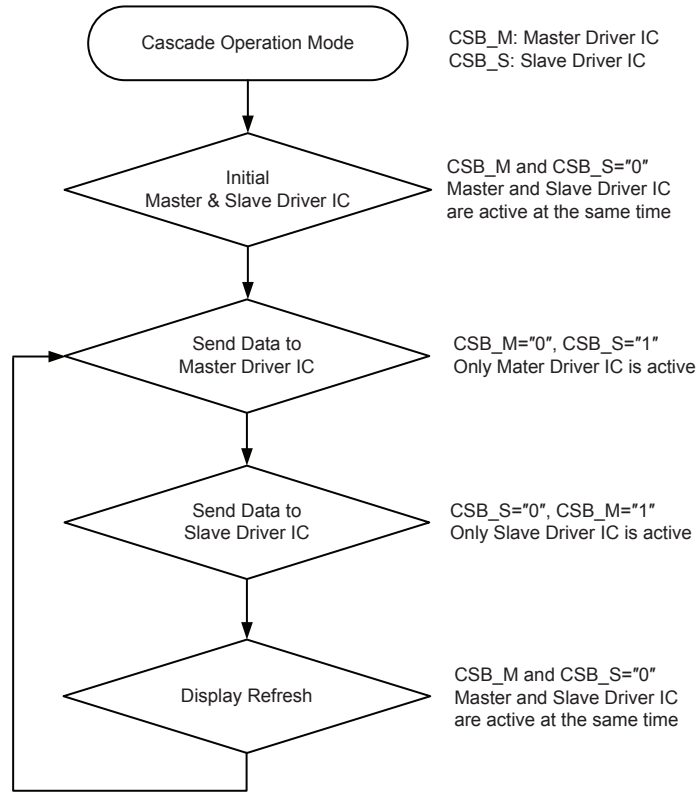
Note: $T=1/f$, the parameter is setup using the FRC command.



BUSY_N Signal Flow Chart



Cascade Operation Flow Chart



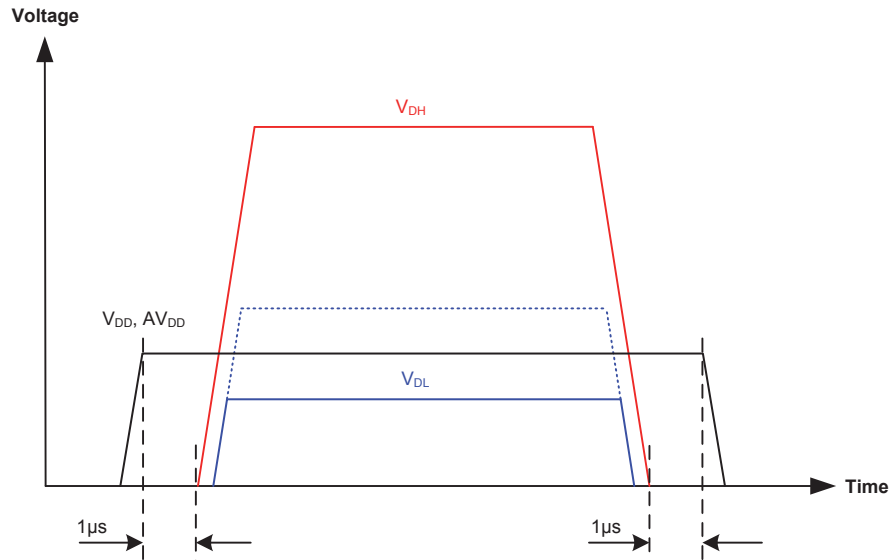
Power Supply Sequence

If the V_{DH} and V_{DL} power is supplied from external power, it is strongly recommended to follow the Holtek power supply sequence requirement.

If the power supply sequence requirement is not followed, it may result in malfunction.

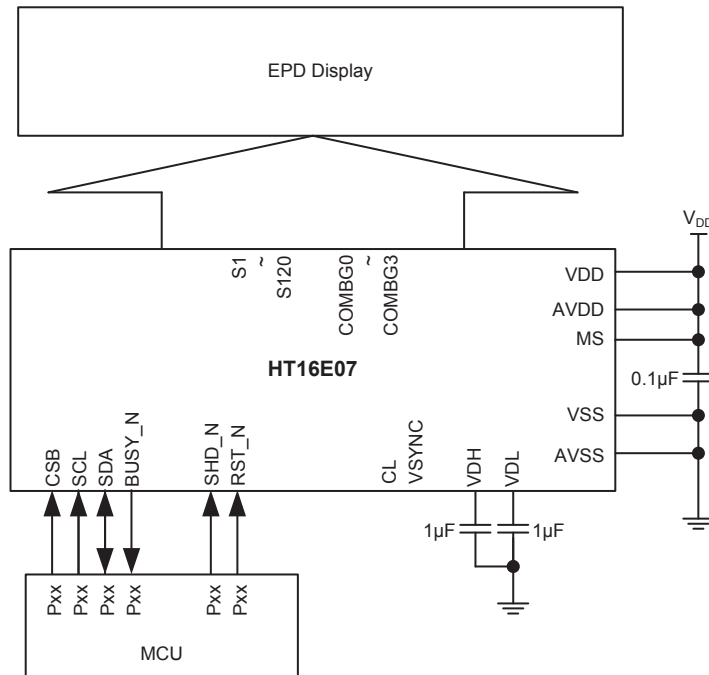
Holtek Power Supply Sequence Requirement:

- Power-on sequence
Turn on the power of V_{DD} and AV_{DD} first and then turn on the power of V_{DH} and V_{DL} .
- Power-off sequence
Turn off the power of V_{DH} and V_{DL} first and then turn off the power of V_{DD} and AV_{DD} .

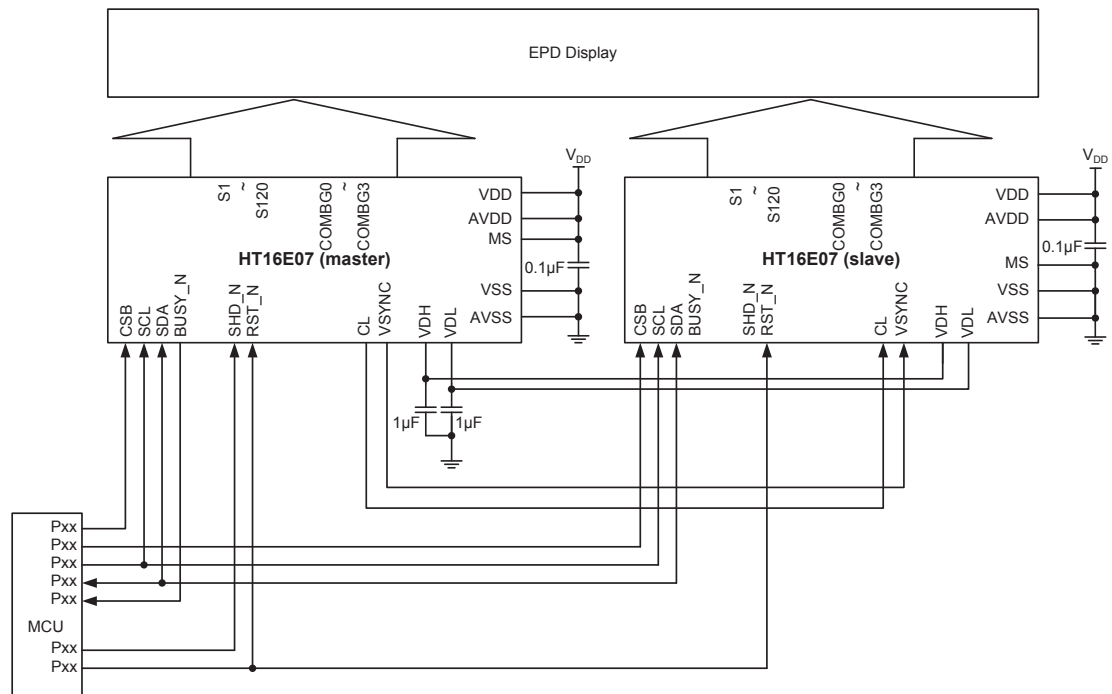


Application Circuits

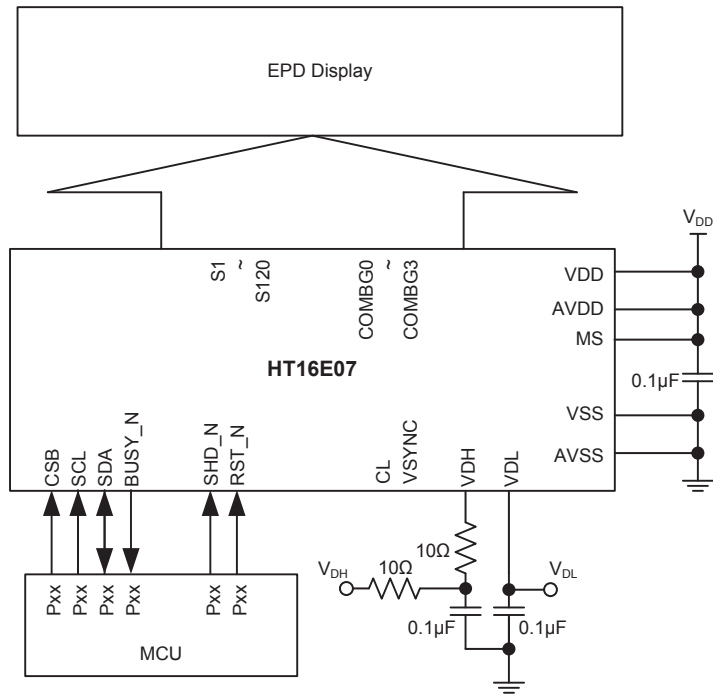
Single Chip Application



Cascade Mode Application



V_{DH} and V_{DL} are Supplied from External Power



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