HT16K23
RAM Mapping 20*4/16*8 LCD Controller Driver with keyscan

Feature

- Logic voltage: 2.4~5.5V
- Integrated RC oscillator
- Various display modes
  – Max. 20*4 patterns, 20 segments, 4 commons, 1/3 bias, 1/4 duty
  – Max. 16*8 patterns, 16 segments, 8 commons, 1/4 bias, 1/8 duty
- I^2C-bus interface
- Key scan function
  – Max. 20*1 matrix key scanning in 20*4 display mode
  – Max. 16*1 matrix key scanning in 16*8 display mode
- 16*8 bits RAM for display data storage
- Selectable hardware interrupt
- R/W address auto increment
- Manufactured in silicon gate COMS process
- 28-pin SOP package

Applications

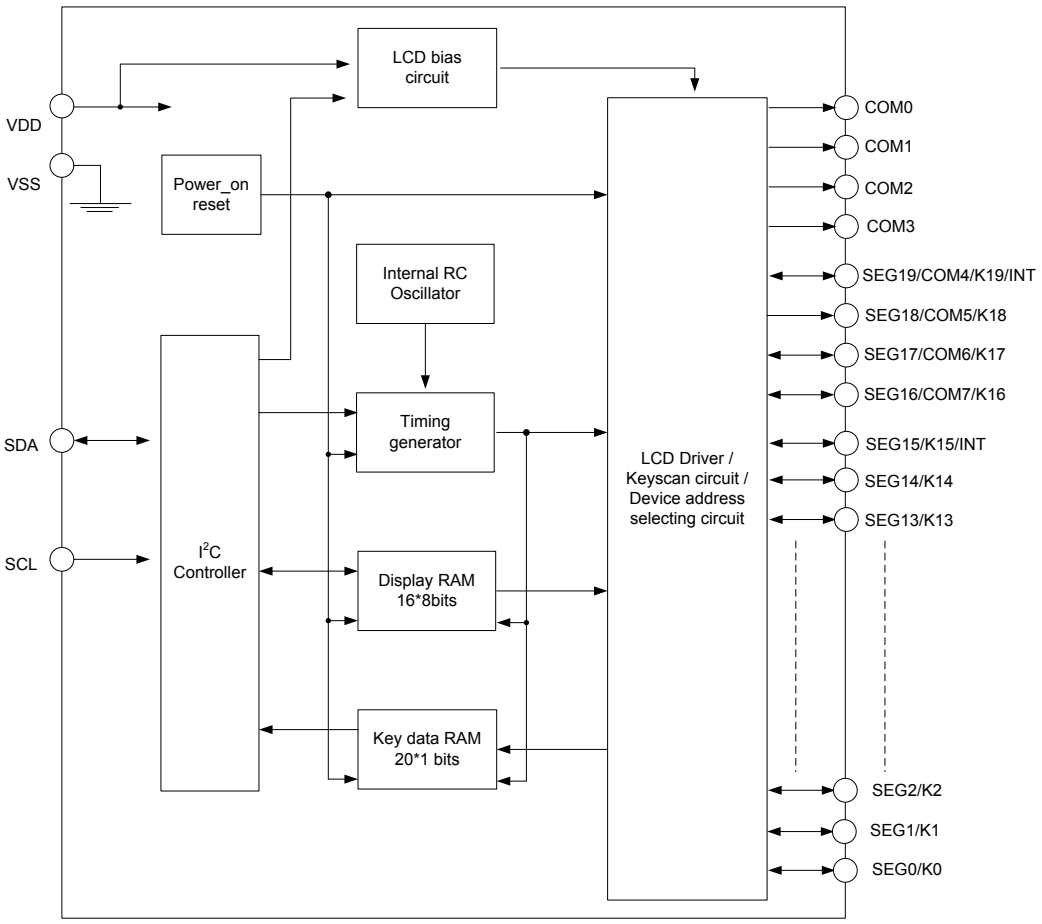
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Combo set.
- VCR set
- Instrumentation readouts
- Other consumer application
- LCD displays

General Description

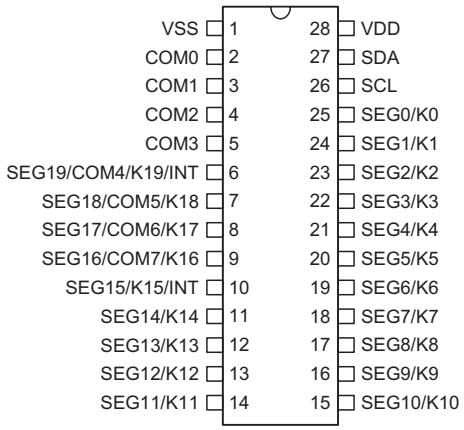
The HT16K23 is a memory mapping and multi-function LCD controller driver. The Max. display segment numbers in the device are 80 patterns (20 segments and 4 commons) or 128 patterns (16 segments and 8 commons). The Max. key scan circuits are 20*1 matrix or 16*1 matrix. The software configuration feature of the HT16K23 makes it suitable for multiple LCD applications including LCD modules and display subsystems. The HT16K23 supports a hardware interrupt using register setting.

The HT16K23 is compatible with most microcontrollers and communicates via a two-line bidirectional I^2C-bus.

Block Diagram



Pin Assignment



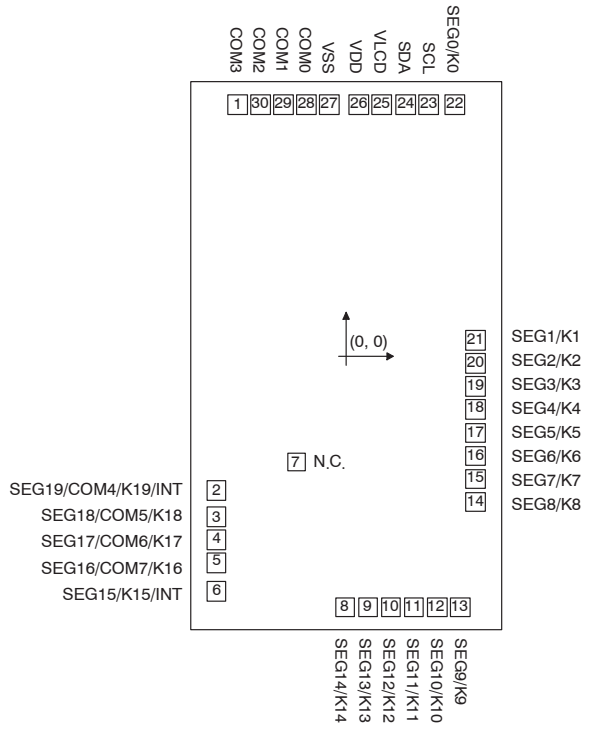
HT16K23
28 SOP-A

Pad Coordinates

unit: μm²

No	Pad Name	X	Y	No	Pad Name	X	Y
1	COM3	-400.967	924.900	16	SEG6/K6	479.400	-368.200
2	SEG19/COM4/K19/INT	-479.400	-496.281	17	SEG5/K5	479.400	-283.200
3	SEG18/COM5/K18	-479.400	-592.981	18	SEG4/K4	479.400	-198.200
4	SEG17/COM6/K17	-479.400	-677.981	19	SEG3/K3	479.400	-113.200
5	SEG16/COM7/K16	-479.400	-762.981	20	SEG2/K2	479.400	-28.200
6	SEG15/K15/INT	-479.400	-868.000	21	SEG1/K1	479.400	56.800
7	N.C.	-182.270	-392.291	22	SEG0/K0	400.967	924.900
8	SEG14/K14	-3.500	-924.900	23	SCL	305.917	924.900
9	SEG13/K13	81.500	-924.900	24	SDA	220.917	924.900
10	SEG12/K12	166.500	-924.900	25	VLCD	132.317	924.900
11	SEG11/K11	251.500	-924.900	26	VDD	47.317	924.950
12	SEG10/K10	336.500	-924.900	27	VSS	-60.967	924.950
13	SEG9/K9	421.500	-924.900	28	COM0	-145.967	924.900
14	SEG8/K8	479.400	-538.200	29	COM1	-230.967	924.900
15	SEG7/K7	479.400	-453.200	30	COM2	-315.967	924.900

Pad Assignment



Chip size: 1167× 2058μm²

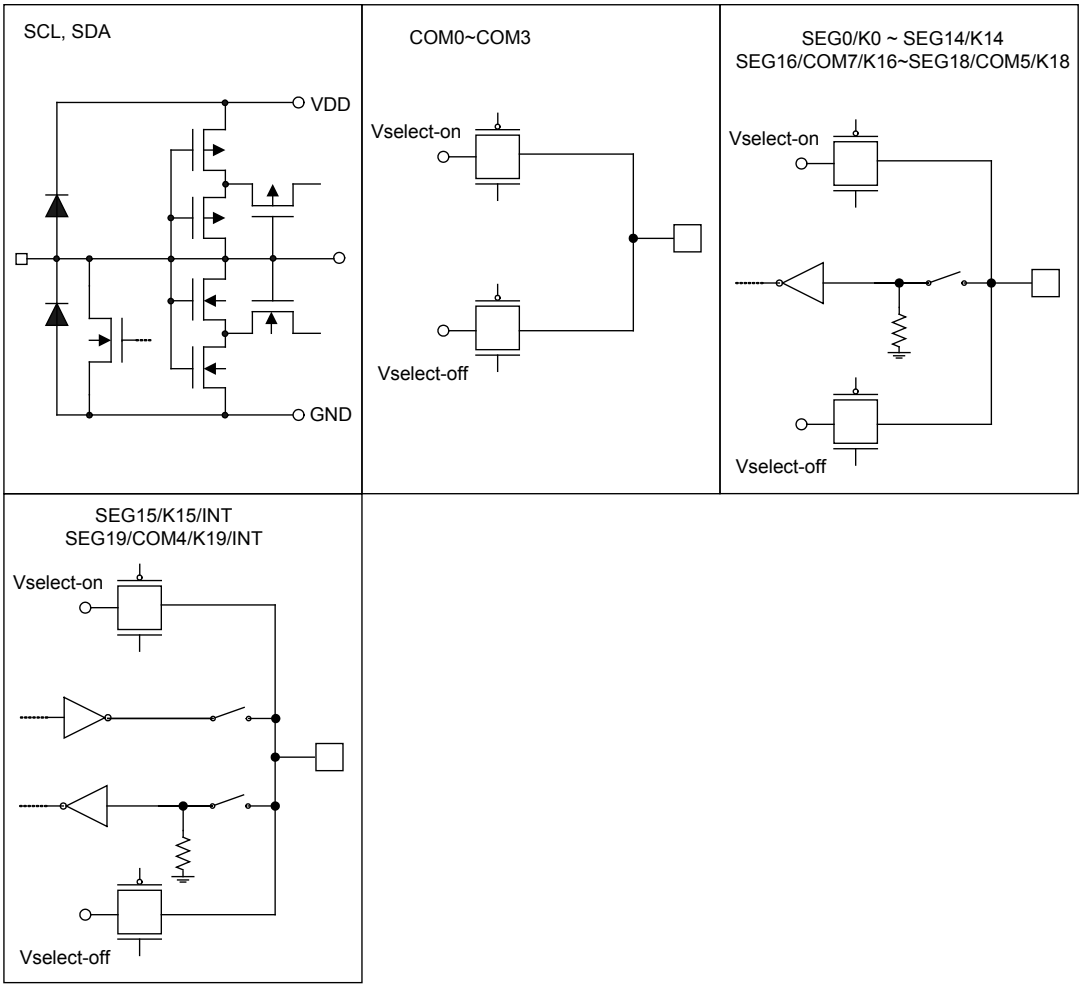
The IC substrate should be connected to VSS in the PCB layout artwork.

The VLCD and VDD should be bonded together.

Pin Description

Pin Name	Type	Description
SDA	I/O	Serial Data Input/Output for I^2C interface.
SCL	I	Serial Clock Input for I^2C.
V_{DD}	—	Positive power supply for logic circuits.
V_{SS}	—	Negative power supply for logic circuits, ground.
COM0 ~ COM3	O	LCD Common output.
SEG0/K0 ~ SEG14/K14	I/O	● LCD Segment output. ● Key data input, internal pull-low during key scan.
SEG15/K15/INT	I/O	● When the “M” bit of the mode set command is set to “1”, and the “INT/ROW” bit of the mode set command is set to “0”, this pin becomes an LCD Segment output and key data input with internal pull-low during key scan. ● When the “M” bit of the mode set command is set to “1”, and the “INT/ROW” bit of the mode set command is set to “1”, this pin becomes an INT pin, interrupt signal out. INT is output active-low when the “ACT” bit of mode set command is set to “0”, The INT output is active-high when the “ACT” bit of the mode set command is set to “1”
SEG16/COM7/K16 ~ SEG18/COM5/K18	I/O	● When the “M” bit of the mode set command is set to “0”, this pin becomes an LCD Segment output and a key data input with internal pull-low during a key scan. ● When the “M” bit of the mode set command is set to “1”, this pin becomes an LCD Common output.
SEG19/COM4/K19/INT	I/O	● When the “M” bit of the mode set command is set to “0”, and the “INT/ROW” bit of the mode set command is set to “0”, this pin becomes a LCD Segment output and a key data input with internal pull-low during key scan. ● When the “M” bit of the mode set command is set to “0”, and the “INT/ROW” bit of the mode set command is set to “1”, this pin becomes an INT pin, interrupt signal out. The INT output is active-low when the “ACT” bit of the mode set command is set to “0”, The INT output active-high when the “ACT” bit of the mode set command is set to “1” ● When the “M” bit of the mode set command is set to “1”, this pin becomes an LCD Common output.

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.5V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -55°C to 150°C

Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{DD} =2.4~5.5V; Ta=25°C (Unless otherwise specified)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
I_{DD1}	Operating Current	3V	No load, LCD ON , 20*4 display mode	—	155	310	μA
		5V		—	260	420	μA
I_{DD2}	Operating Current	3V	No load, LCD OFF , 20*4 display mode	—	8	30	μA
		5V		—	20	60	μA
I_{STB}	Standby Current	3V	No load, standby mode	—	1	3	μA
		5V		—	2	5	μA
V_{IL}	Input Low Voltage	—	SDA, SCL	0	—	$0.3V_{DD}$	V
V_{IH}	Input High Voltage	—	SDA, SCL	$0.7V_{DD}$	—	V_{DD}	V
I_{IL}	Input leakage current	—	V_{IN} = V_{SS} or V_{DD}	-1	—	1	μA
I_{OL}	Low level output current	3V	V_{OL}=0.4V, SDA	3	—	—	mA
		5V		6	—	—	mA
I_{OL1}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	160	—	μA
		5V	V_{OL}=0.5V	180	360	—	μA
I_{OH1}	LCD Common Source Current	3V	V_{OH}=2.7V	-80	-120	—	μA
		5V	V_{OH}=4.5V	-120	-200	—	μA
I_{OL2}	LCD Segment Sink Current	3V	V_{OL}=0.3V	60	120	—	μA
		5V	V_{OL}=0.5V	120	200	—	μA
I_{OH2}	LCD Segment Source Current	3V	V_{OH}=2.7V	-40	-70	—	μA
		5V	V_{OH}=4.5V	-70	-140	—	μA
I_{OL3}	INT Sink Current	3V	V_{OL}=0.3V	1	—	—	mA
		5V	V_{OL}=0.5V	2	—	—	mA
I_{OH3}	INT Source Current	3V	V_{OH}=2.7V	-1	—	—	mA
		5V	V_{OH}=4.5V	-2	—	—	mA
R_{PL}	Input pull-low Resistance	3V	SEG0/K0~SEG19/K19, during keyscan period	220	400	600	KΩ
		5V		220	400	600	

A.C. Characteristics

V_{DD} =2.4~5.5V; Ta=25°C (Unless otherwise specified)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{LCD}	LCD Frame Frequency	3V	20*4 display mode 16*8 display mode	58	72	90	Hz
		5V					
t_{OFF}	V_{DD} OFF Times	—	V_{DD} drop down to 0V	20	—	—	Ms
t_{SR}	V_{DD} Slew Rate	—	—	0.05	—	—	V/ms

Note: 1. If the Power on Reset timing conditions are not satisfied in the power ON/OFF sequence, the internal Power on Reset circuit will not operate normally.

2. If VDD drops below the minimum voltage of the operating voltage spec. during operating, the Power on Reset timing conditions must also be satisfied. That is, VDD must drop to 0V and remain at 0V for 20ms (min.) before rising to the normal operating voltage.

A.C. Characteristics

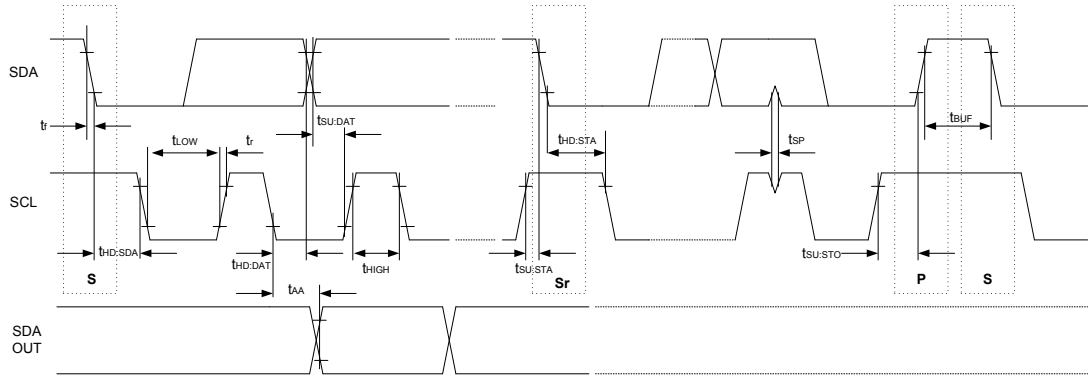
I^2C-Bus Ta=25°C (Unless otherwise specified)

Symbol	Parameter	Test condition	V_{DD}=2.4V to 5.5V		V_{DD}=3.0V to 5.5V		Unit
		Condition	Min.	Max.	Min.	Max.	
f_{SCL}	Clock frequency	—	—	100	—	400	kHZ
t_{BUF}	Bus free time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD;\ STA}$	Start condition hold time	After this period, the first clock pulse is generated	4	—	0.6	—	μs
t_{LOW}	SCL Low time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High time	—	4	—	0.6	—	μs
$t_{SU;\ STA}$	Start condition set-up time	Only relevant for repeated START condition.	4.7	—	0.6	—	μs
$t_{HD;\ DAT}$	Data hold time	—	0	—	0	—	μs
$t_{SU;\ DAT}$	Data set-up time	—	250	—	100	—	ns
t_r	Rise time	Note	—	1	—	0.3	μs
t_f	Fall time	Note	—	0.3	—	0.3	μs
$t_{SU;\ STO}$	Stop condition set-up time	—	4	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns

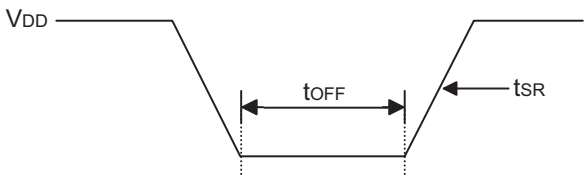
Note: These parameters are periodically sampled but not 100% tested.

Timing Diagrams

- **I²C Timing**



- **Power-on Reset Timing**



Functional Description

Power-on Reset

When power is turned on, the IC is initialised by the internal power-on reset circuit. The status of the internal circuit after initialization is as follows:

- Display mode is 20*4, 20 segments and 4 commons.
- System oscillator is off.
- LCD Display is off.
- Key scan stopped.
- All common pins are set to VSS.
- All segment pins are in an input state.
- SEG19/COM4/INT pin is set to segment driver.
- The control registers, key data RAM and display data RAM are set to a default value.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset procedure.

Standby Mode

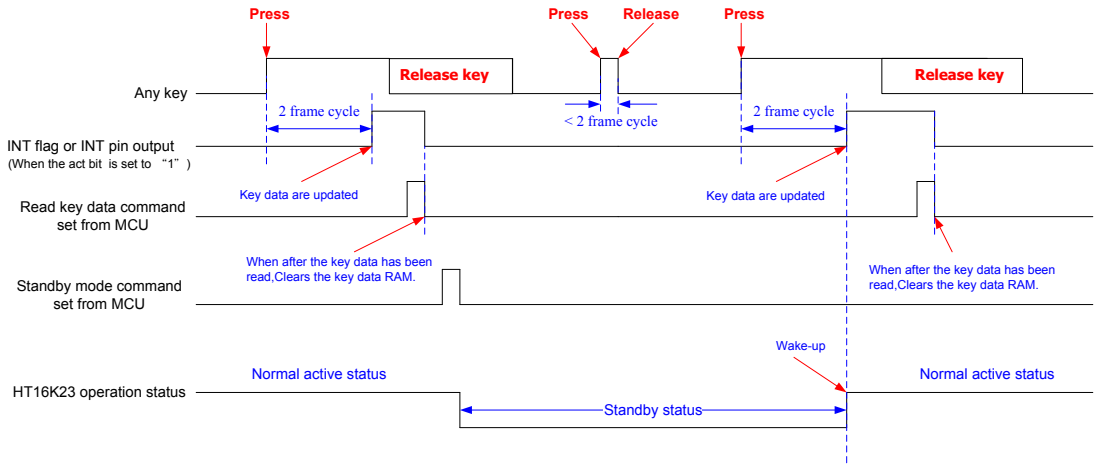
In the standby mode, the HT16K23 cannot accept any input command or write data to the display RAM except for the system set command.

If standby mode is selected with the "S" bit of system set command is set to "0", the status of the standby mode is as follows:

- System Oscillator is off.
- LCD display is off.
- Key scan stopped.
- All key data and INT flags are cleared, until the standby mode is cancelled.
- The key matrix is pushed by any key or if the "S" bit of the system set command is set to "1", this standby mode will be cancelled and the device will wake-up.
- All common pins are set to VSS.
- If the "INT/ROW" bit of mode set command is set to "0", all segment pins are changed to input pins.
- If the "INT/ROW" bit of mode set command is set to "1": all segment pins are changed to input pins except for the INT pin (output).
- The INT pin output keeps a high level when the "ACT" bit of the mode set command is set to "0",.The INT pin output keeps to a low level when the "ACT" bit of the mode set command is set to "1", if the "INT/ROW" bit of mode set command is set to "1".

Wake-up

- Wake-up is implemented by a key press by any key or if the "S" bit of the system set command is set to "1". Then a key scan is performed.
- System Oscillator restarts for normal operation.
- The previous output will be displayed until updated by each mode command set.
- The relationship between Wake-up and any key press delay timeless and INT output and INT flag status is as follows:



System Set Command

This command is used to set the follow functions.

- The HT16K23 operates in normal mode or standby mode. Before the standby mode command is sent, it is strongly recommended to read key data first.
- LCD display on/off

Name	Command								Option	Description	Def.
	D7	D6	D5	D4	D3	D2	D1	D0			
System set	1	0	0	0	0	0	D	S	S	Standby mode selecting ● {0}: standby mode ● {1}: normal mode	80H
									D	LCD display on/off ● {0}: LCD display off ● {1}: LCD display on	

Mode Set Command

This command is used to set the follow functions.

- Display mode selecting, 20*4 display mode or 16*8 display mode.
- Set the HT16K23 SEG/INT port to be a segment output or an INT output.
- INT output is active-low or active-high.

Name	Command								Option	Description	Def.
	D7	D6	D5	D4	D3	D2	D1	D0			
Mode set	1	0	1	0	0	ACT	INT/ ROW	M	M	LCD display mode selecting ● {0}: 20*4 display mode ● {1}:16*8 display mode	A0H
									INT/ ROW	Segment or INT pin selecting ● {0}: Segment output SEG19/COM4/K19/INT is segment output in 20*4 display mode. SEG15/K15/INT is segment output in 16*8 display mode. ● {1}: INT output SEG19/COM4/K19/INT is INT output in 20*4 display mode. SEG15/K15/INT is INT output in 16*8 display mode.	
									ACT	INT output level selection, ● {0}: INT output is active-low. ● {1}: INT output is active-high.	

System Oscillator

The internal logic and the LCD driver signals of the HT16K23 are timed by the integrated RC oscillator.

The System Clock frequency (f_{SYS}) determines the LCD frame frequency. A clock signal must always be supplied to the device as removing the clock may freeze the standby mode command is executed. At initial system power on, the System Oscillator is in the stop state.

LCD Bias Generator

The full-scale LCD voltage (Vop) is obtained from $V_{DD} - V_{SS}$.

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{LCD} and V_{SS}. The centre resistor can be switched out of the circuit to provide a 1/3 bias voltage level for the 1/4 duty configuration or 1/4 bias voltage level for the 1/8 duty configuration.

Segment Driver Outputs

The LCD driver section includes segment outputs which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit.

Common Driver Outputs

The LCD driver section includes column outputs which should be connected directly to the LCD panel. The common output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit.

Display Memory – RAM Structure

The display RAM is a static 16 x 8-bit RAM where the LCD data is stored. A logic "1" in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly a logic 0 indicates the "off" state.

There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the column outputs. The following tables show the mapping from the RAM to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	address
SEG1	—	—	—	—	SEG0	—	—	—	—	00H
SEG3	—	—	—	—	SEG2	—	—	—	—	01H
SEG5	—	—	—	—	SEG4	—	—	—	—	02H
SEG7	—	—	—	—	SEG6	—	—	—	—	03H
SEG9	—	—	—	—	SEG8	—	—	—	—	04H
SEG11	—	—	—	—	SEG10	—	—	—	—	05H
SEG13	—	—	—	—	SEG12	—	—	—	—	06H
SEG15	—	—	—	—	SEG14	—	—	—	—	07H
SEG17	—	—	—	—	SEG16	—	—	—	—	08H
SEG19	—	—	—	—	SEG18	—	—	—	—	09H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

RAM mapping of 20*4 display mode

Output	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	address
SEG0	—	—	—	—	—	—	—	—	00H
SEG1	—	—	—	—	—	—	—	—	01H
SEG2	—	—	—	—	—	—	—	—	02H
SEG3	—	—	—	—	—	—	—	—	03H
SEG4	—	—	—	—	—	—	—	—	04H
SEG5	—	—	—	—	—	—	—	—	05H
SEG6	—	—	—	—	—	—	—	—	06H
SEG7	—	—	—	—	—	—	—	—	07H
SEG8	—	—	—	—	—	—	—	—	08H
SEG9	—	—	—	—	—	—	—	—	09H
SEG10	—	—	—	—	—	—	—	—	0AH
SEG11	—	—	—	—	—	—	—	—	0BH
SEG12	—	—	—	—	—	—	—	—	0CH
SEG13	—	—	—	—	—	—	—	—	0DH
SEG14	—	—	—	—	—	—	—	—	0EH
SEG15	—	—	—	—	—	—	—	—	0FH
	D7	D6	D5	D4	D3	D2	D1	D0	Data

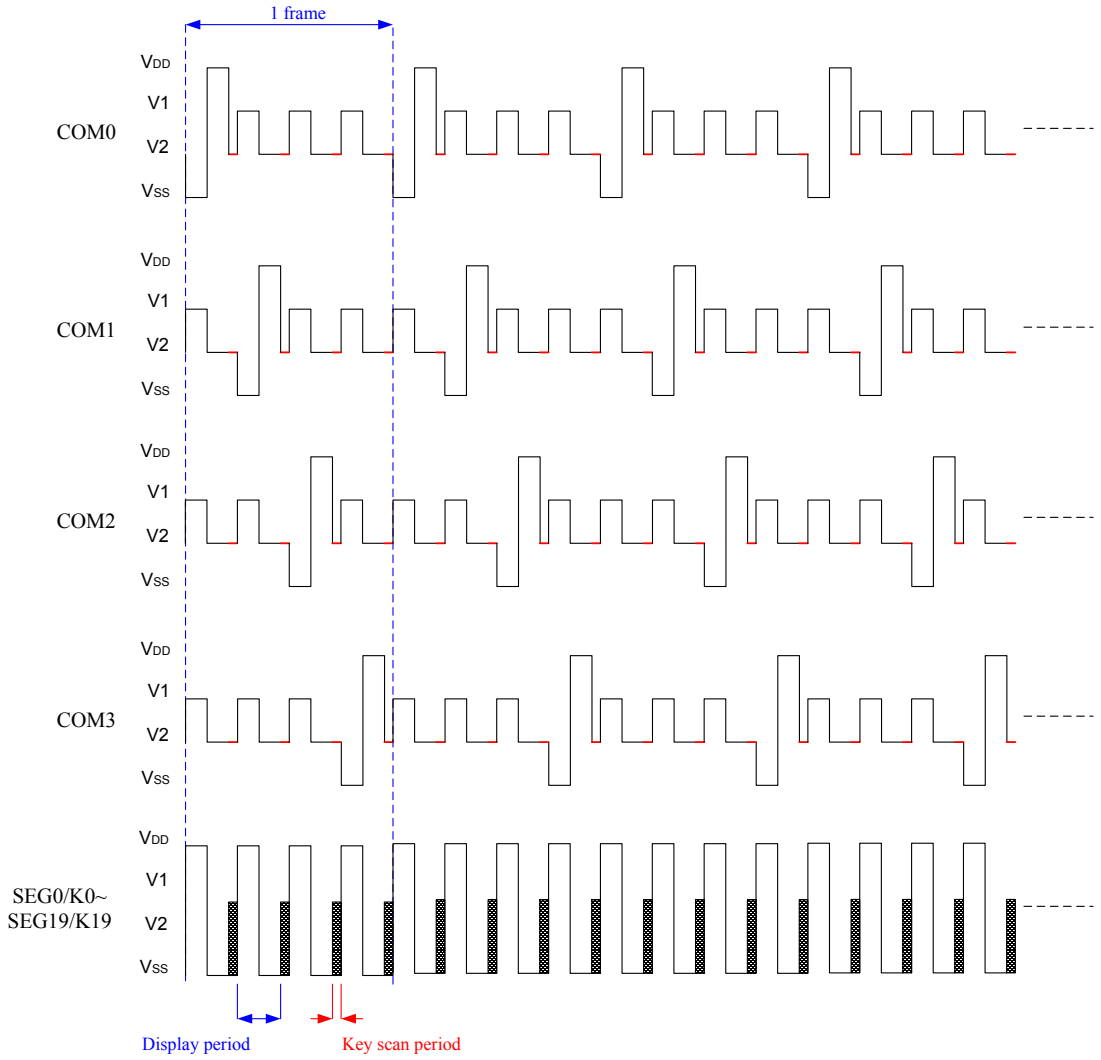
RAM mapping of 16*8 display mode

MSB LSB

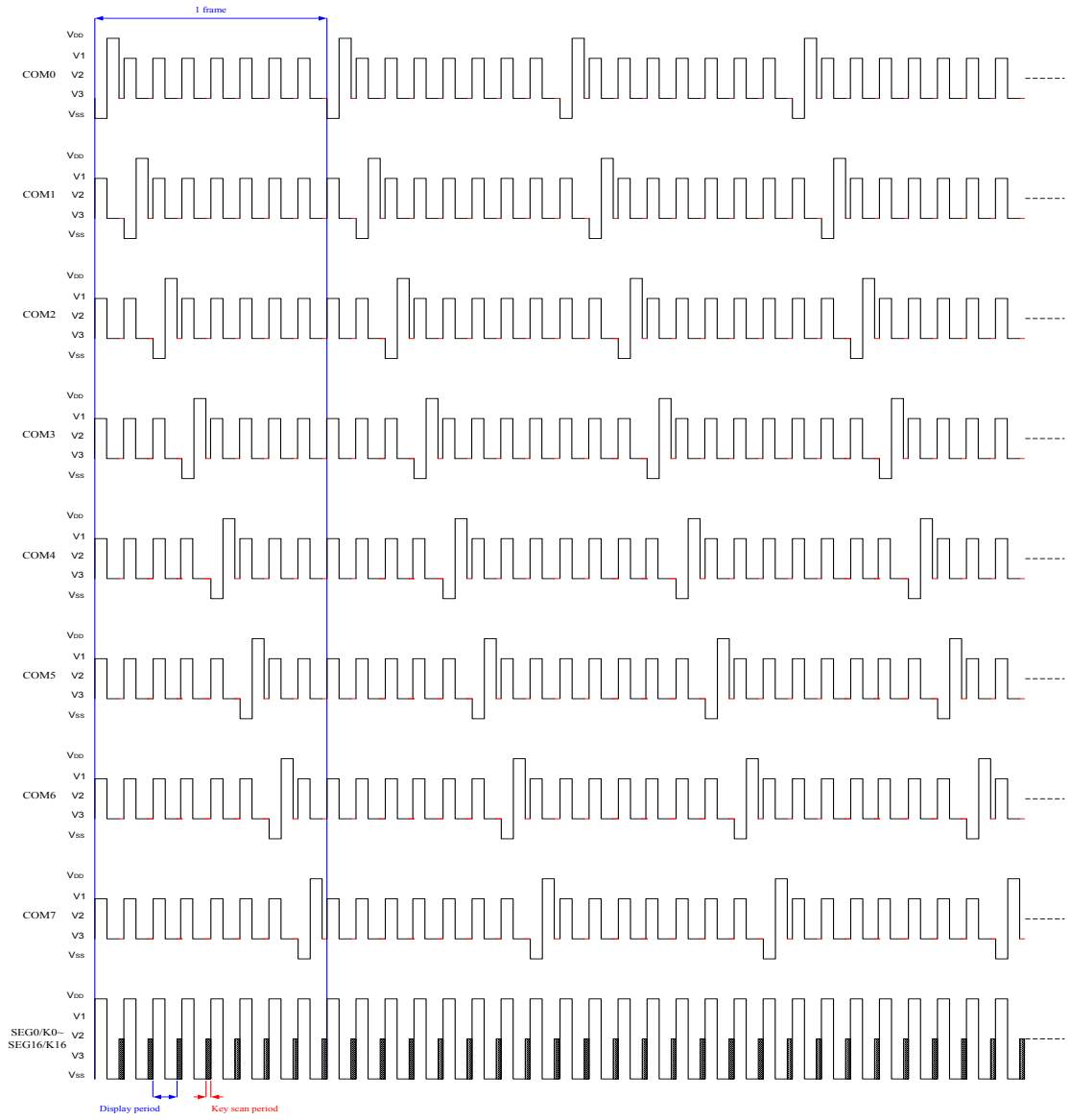
D7	D6	D5	D4	D3	D2	D1	D0

LCD Drive Mode Waveforms

- **20*4 display mode, 1/4 duty , 1/3 bias**



- **16*8 display mode, 1/8 duty , 1/4 bias**



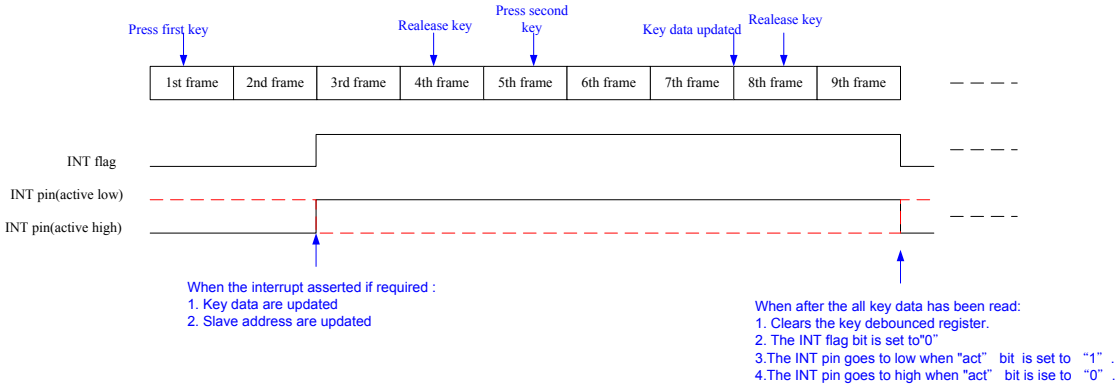
Keyscan

- The HT16K23 supports a 20*1 matrix key scan in the 20*4 display mode and a 16*1 matrix key scan in the 16*8 display mode.
- The hardware interrupt function is optional, allowing SEG19/COM4/K19/INT in the 20*4 display mode or SEG15/K15/INT to be used as an INT output or as a segment driver. The interrupt flag can be read (polled) through the serial interface instead.
- The key scan input pins are shared with segment output pins.
- The keyscan cycle loops continuously with time, with all keys experiencing a full keyscan debounce of over 20ms. A key press is debounced and an interrupt issued if at least one key that was not pressed in a previous cycle is found pressed during both sampling periods.
- INT output is active-low when the “act” bit of the mode set command is set to “0”,
- INT output is active-high when the “act” bit of the mode set command is set to “1”

Keyscan and INT Timing

- The key data is updated and the INT function is changed if the key has been pressed for 2 key-cycles.
- The INT function is changed when the first key has been pressed.
- After the key data has been read, the key data registers are cleared to “0” and the INT flag bit is set to “0”. The INT pin goes low when the “ACT” bit of the mode set command is set to “1”.
- After the key data has been read, the key data registers are cleared to “0” and the INT flag bit is set to “1”, and the INT pin goes low when the “ACT” bit of the mode set command is set to “0”.
- The INT flag register is shown below. To clear the INT flag status, the key data register must be read from 0x20H~0x22H in one operation.

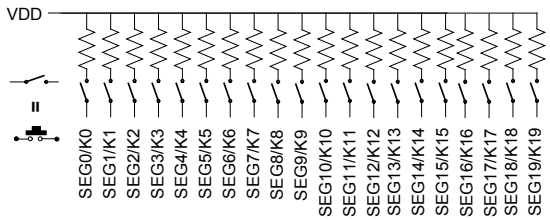
INT flag register	Address code	R/W	Register Data								
			D7	D6	D5	D4	D3	D2	D1	D0	Def.
INT flag register	0X30H	R	0	0	0	0	0	0	0	INT flag	00H



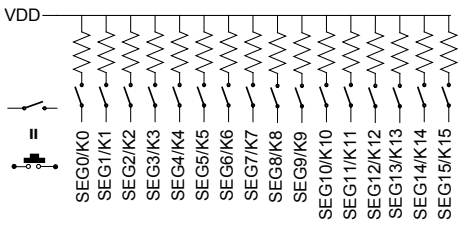
Key Matrix Configuration

There is a key scan circuit integral to the HT16K23 which can detect a key press. It includes twenty inputs (K0 to K19, shared with SEG0 to SEG19) in the 20*4 display mode or sixteen inputs (K0 to K15, shared with SEG0 to SEG15) in the 16*8 display mode.

The key matrix has a 20*1 matrix in the 20*4 display mode or a 16*1 matrix in the 16*8 display configuration as shown below:



20*1 matrix in 20*4 display mode



16*1 matrix in 16*8 display mode

Key Data Register

After the key data registers have been read, the key data registers are cleared to "0". To enable future key presses to be identified, if the key data register is not read, the key data accumulates. There is no FIFO register in the HT16K23. Key-press order, or whether a key has been pressed more than once, cannot be determined unless the all of the key data RAM is read after each interrupt and before completion of the next keyscan cycle.

After the key data registers have been read, the INT output and INT flag status are cleared. If a key is pressed and held down, the key is reported as being debounced (and an INT is issued) only once. The key must be detected as released by the keyscan circuit before it is debounced again.

It is strongly recommended to read the key data registers from the address 0x20H only. The key data registers of addresses from 0X20H to 0X22H should be read continuously and completed in one operation.

There is a one-to-one correspondence between the key data register addresses and the key data outputs and between the individual bits of a key data register word and the key data outputs. The following shows the mapping from the RAM to the key data output:

The key data registers are read only. The key data register format is shown below:

Key data register	Address code	R/W	Register Data								
			D7	D6	D5	D4	D3	D2	D1	D0	Def.
Key data register address point	0X20H	R	K7	K6	K5	K4	K3	K2	K1	K0	00H
	0X21H	R	K15	K14	K13	K12	K11	K10	K9	K8	00H
	0X22H	R	0	0	0	0	K19	K18	K17	K16	00H

Key scan period setting Command

- HT16K23 can adjust the key scan period through this command. The setting is show as below.
- The default value of key scan period is 2 clock cycle time in 20*4 display mode, 1 clock cycle time in 16*8 display mode.
- In generally, user does not need to use this command, when key data can be read correctly.
- Due to various LCD characteristic, it will have different RC time constant in key scan period. If the equivalent capacitance is larger in the LCD, it can not be charged or discharged fully in key scan period. The key can not be read correctly. To avoid read key error, user can adjust the key scan period through this command. If key scan period is too longer, it may affect the LCD visual quality.

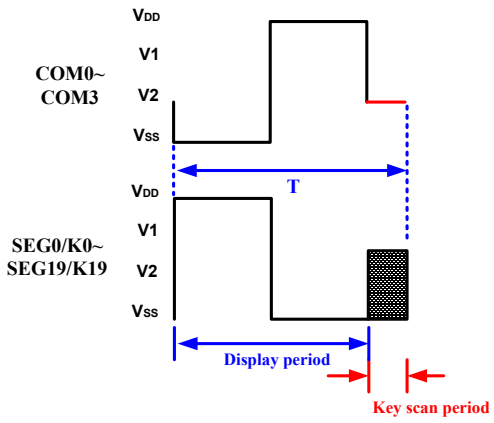
Name	Command								Option	Description	Def.
	D7	D6	D5	D4	D3	D2	D1	D0			
Key scan period setting	1	1	1	1	1	P2	P1	P0	[P2:P0]	To adjust key scan period	F8H

The setting of key scan period

[P2:P0]	20*4 display mode	16*8 display mode
000	2 clock cycle time	1 clock cycle time
001	4 clock cycle time	3 clock cycle time
010	6 clock cycle time	5 clock cycle time
011	8 clock cycle time	7 clock cycle time
100	10 clock cycle time	9 clock cycle time
101	12 clock cycle time	11 clock cycle time
110	14 clock cycle time	13 clock cycle time
111	16 clock cycle time	15 clock cycle time

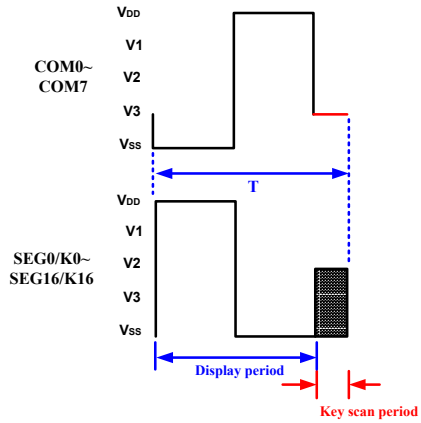
The relationship of display period and key scan period

20*4 display mode



T= Display period + Key scan period
= 110 clock cycle time (fixed)

16*8 display mode



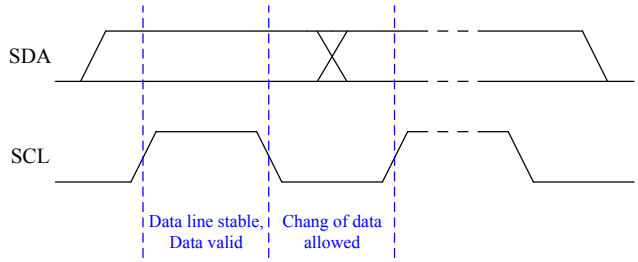
T= Display period + Key scan period
= 55 clock cycle time (fixed)

I²C Serial Interface

The device includes a I²C serial interface. The I²C bus is used for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines are connected to a positive supply via a pull-up resistor. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector output type to implement the required wired and function. Data transfer is initiated only when the bus is not busy.

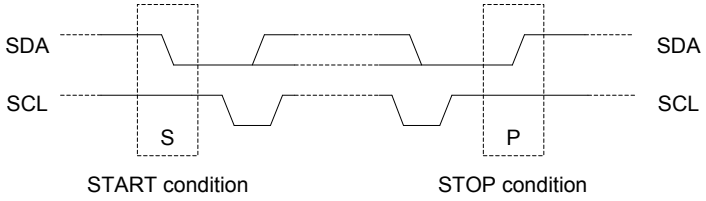
Data Validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is Low (see as below).



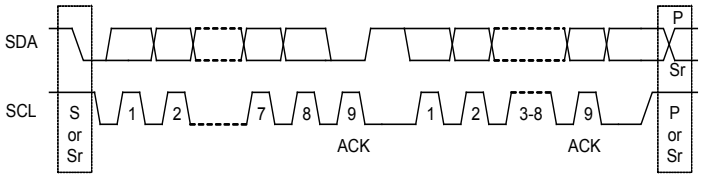
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START(S) and repeated START (Sr) conditions are functionally identical.



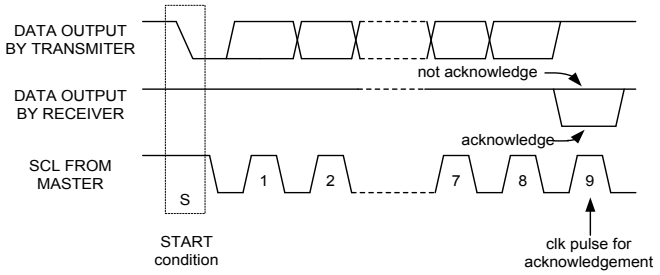
Byte Format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



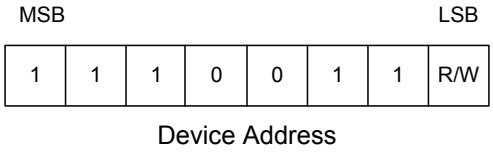
Acknowledge

- Each byte of eight bits is followed by a single acknowledge bit. This acknowledge bit is a low level which is placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge (ACK) after the reception of each byte.
- The acknowledging device must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data status to the slave by generating a not-acknowledge (NACK) bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Device Addressing

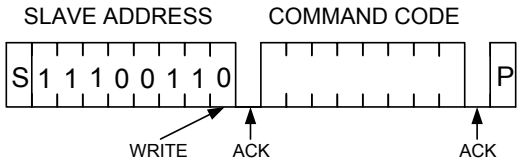
- The slave address byte is the first byte received following a START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When this R/$\overline{W}$ bit is "1", then a read operation is selected. A "0" selects a write operation.
- The HT16K23 address bit format is shown below. When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an acknowledge on the SDA line.



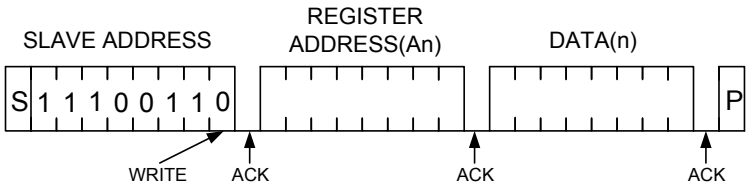
Write Operation

Byte Write Operation

A byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a valid Register Address, Data and a STOP condition. After each of the three bytes have been transmitted, the device responds with an ACK.



Command Byte Received

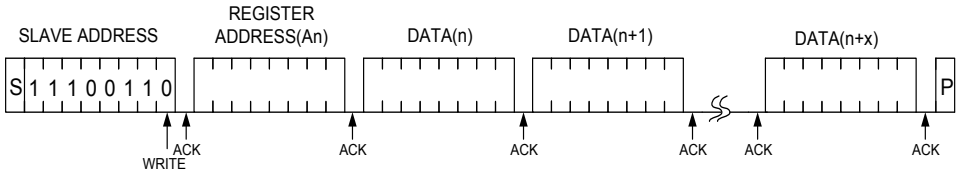


Single Data Byte Received

Note: If the byte following slave address is a command code, the byte following the command code will be ignored.

Page Write Operation

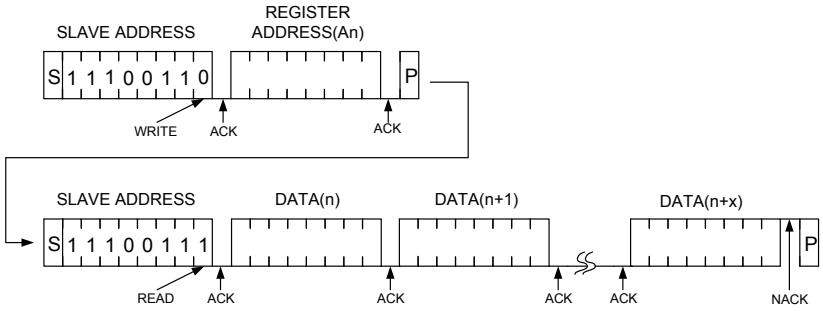
A START condition and a slave address with a R/$\overline{W}$ bit placed on the bus indicates to the addressed device that a Register Address will follow and is to be written to the address pointer. The data to be written to the memory is next and the internal address pointer will be incremented to the next address location on the reception of an acknowledge clock. After reaching the memory location 0X8Ah in the 20*4 display mode or 0X8Fh in the 16*8 display mode, the pointer will be reset to 0X80h.



N Data Bytes Received

Read Operation

- In this mode, the master reads the HT16K23 data after setting the slave address. Following a R/$\overline{W}$ bit (="0") and an acknowledge bit, the register address (An) is written to the address pointer. Next a START condition and a slave address are repeated followed by a R/$\overline{W}$ bit ("1"). The data which was addressed is then transmitted. The address pointer is only incremented on reception of an acknowledge clock. The HT16K23 will place the data at address An+1 on the bus. The master reads and acknowledges the new byte and the address pointer is incremented to "An+2". If the register address (An) is 0X00H ~ 0X0FH, after reaching the memory location 0X0FH, the pointer will reset to 0X00H. If the register address (An) is 0X20H ~ 0X22H, after reaching the memory location 0X22H, the pointer will reset to 0X20H.
- This cycle of reading consecutive addresses will continue until the master sends a STOP condition.



Command Summary

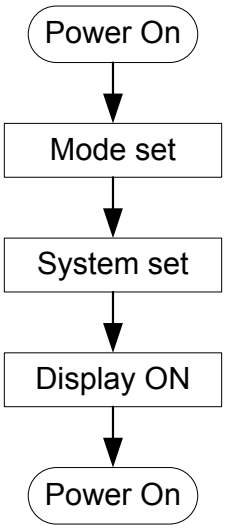
Name	Command / Address								Option	Description	Def.
	D7	D6	D5	D4	D3	D2	D1	D0			
Display data Address pointer	0	0	0	0	A3	A2	A1	A0	[A3:A0] (R/W)	Four bits of immediate data, bits A0 to A4, are transferred to the data pointer to define display RAM addresses.	00H
Key data Address pointer	0	0	1	0	0	0	K1	K0	{K0~K1} (R)	It is strongly recommended that the key data registers with addresses from 0x20H to 0x22H should be read continuously and in one operation. Therefore the key data RAM addresses should be started form 0x20H only.	20H
INT flag Address pointer	0	0	1	1	0	0	0	0	(R)	INT flag address for reading INT flag status.	30H
System set command	1	0	0	0	0	0	D	S	S	Standby mode selecting ● {0}: standby mode ● {1}: normal mode	80H
									D	LCD display on/off ● {0}: LCD display off ● {1}: LCD display on	
Mode set command	1	0	1	0	0	ACT	INT/ ROW	M	M	LCD display mode selecting ● {0}: 20*4 display mode ● {1}:16*8 display mode	A0H
									INT/ROW	Segment or INT pin selecting ● {0}: Segment output SEG19/COM4/K19/INT is segment output in 20*4 display mode. SEG15/K15/INT is segment output in 16*8 display mode. ● {1}: INT output SEG19/COM4/K19/INT is INT output in 20*4 display mode. SEG15/K15/INT is INT output in 16*8 display mode.	
									ACT	INT output level selection, ● {0}: INT output is active-low. ● {1}: INT output is active-high.	
Key scan period setting	1	1	1	1	1	P2	P1	P0	[P2:P0]	To adjust key scan period	F8H

Note: If the programmed command data is not defined, the function will not be affected.

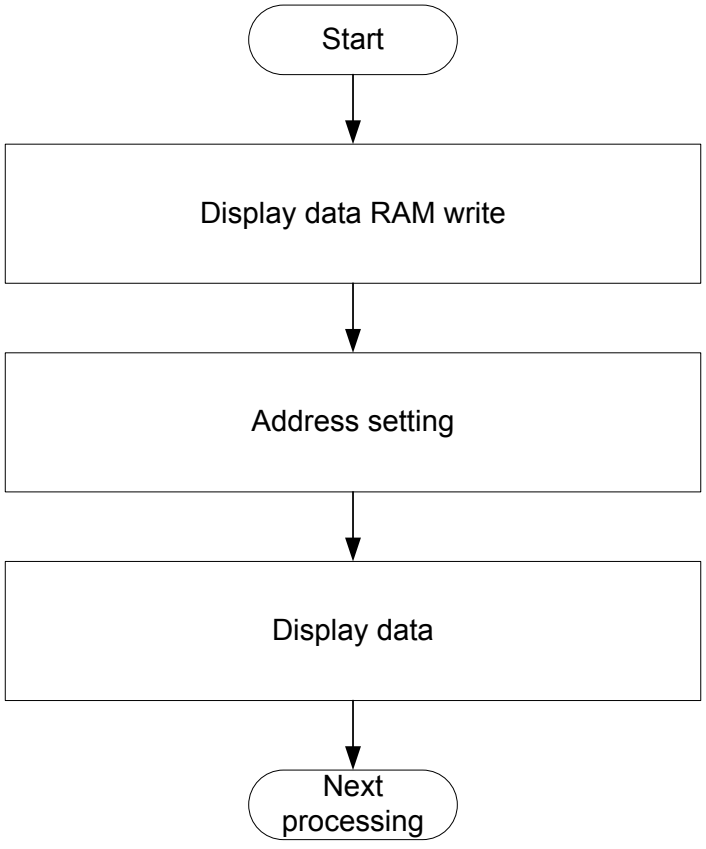
HT16K23 Operation Flow Chart

The access procedure is illustrated using the following flowcharts.

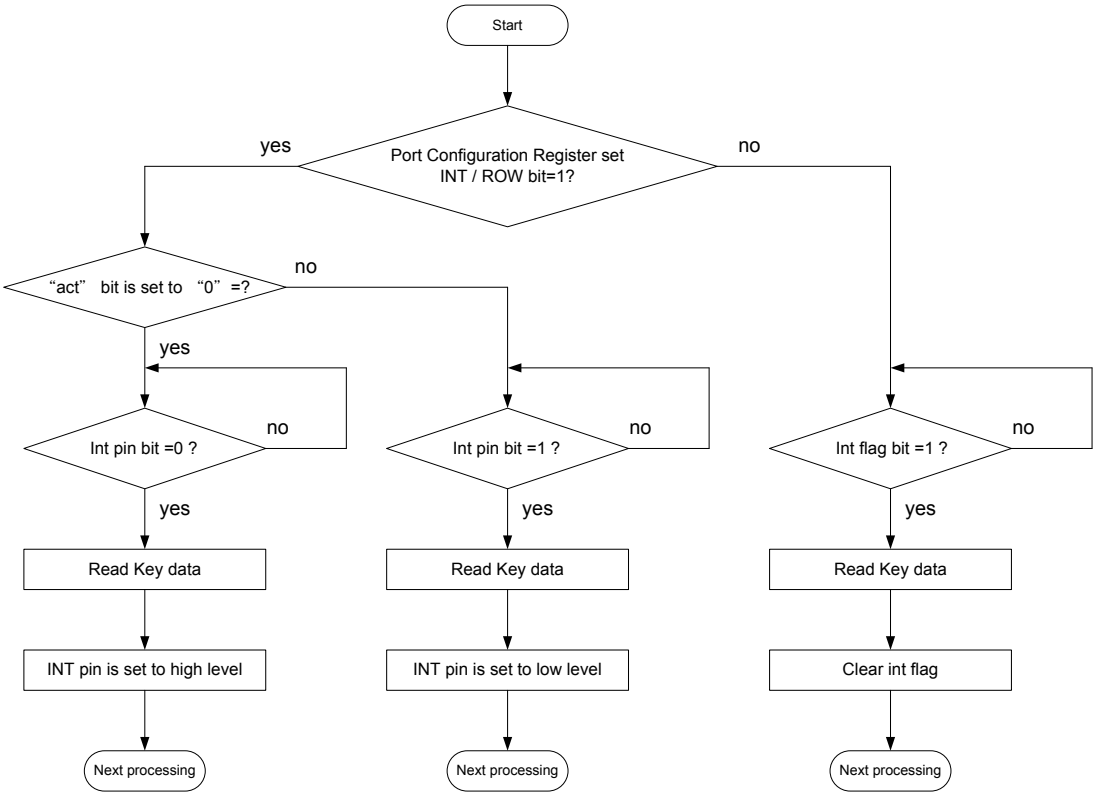
- **Initialisation**



- **Display Data Rewrite – Address Setting**

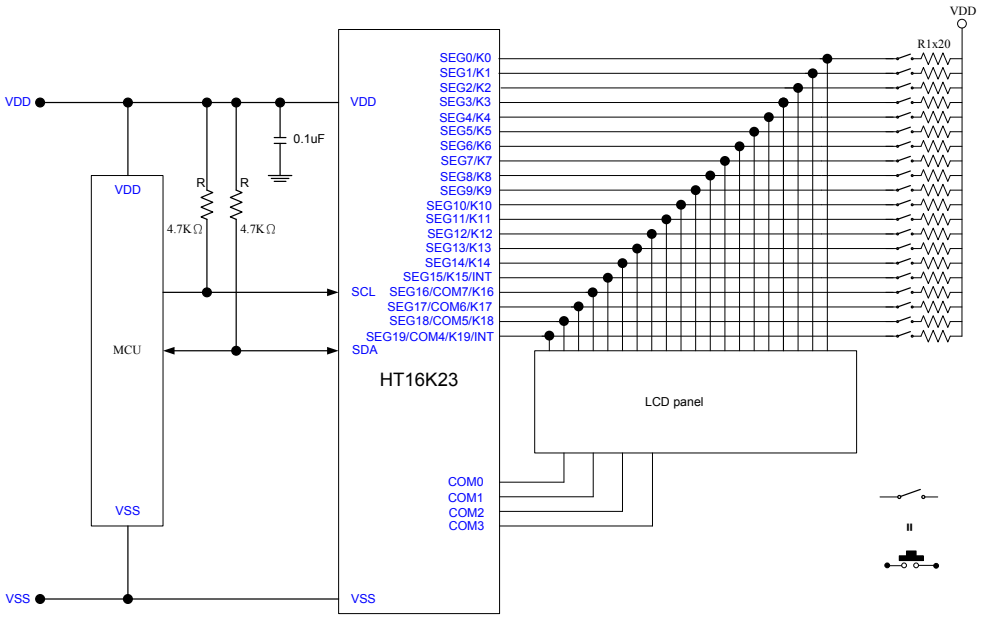


- **Key Data Read**

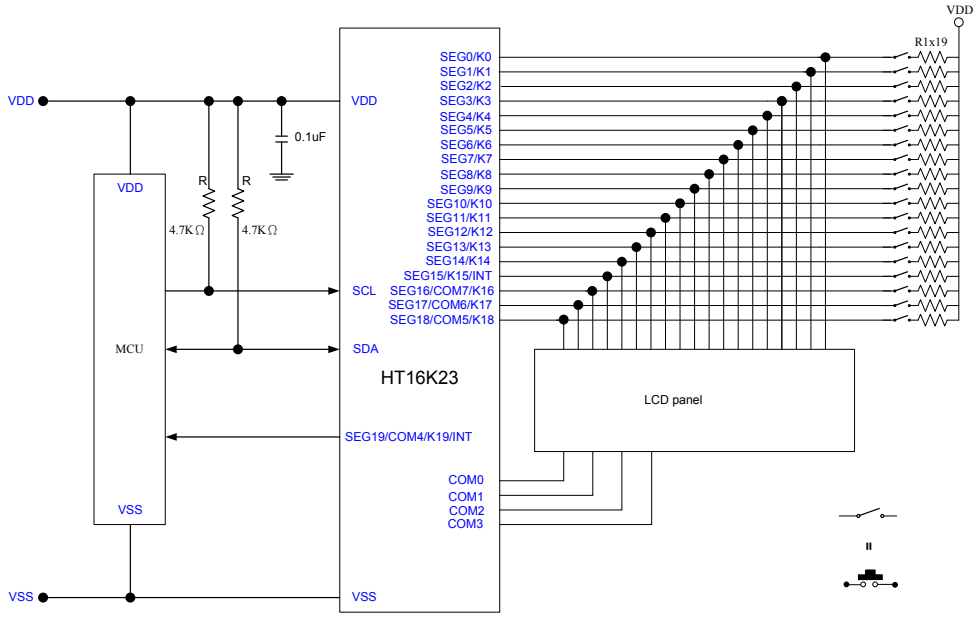


Application Circuit

- **20*4 display mode without INT**

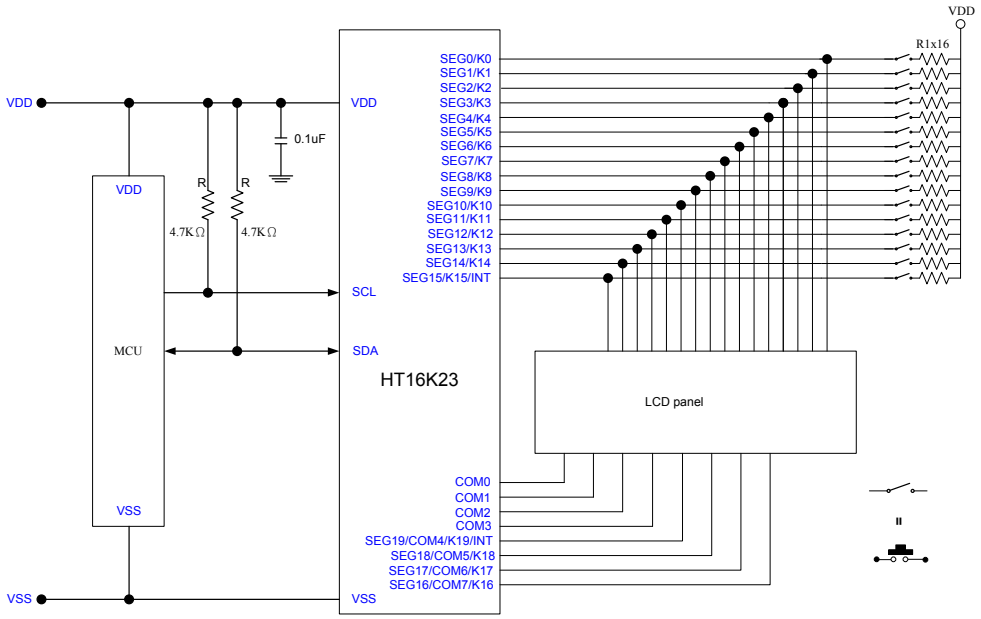


- **19*4 display mode with INT**

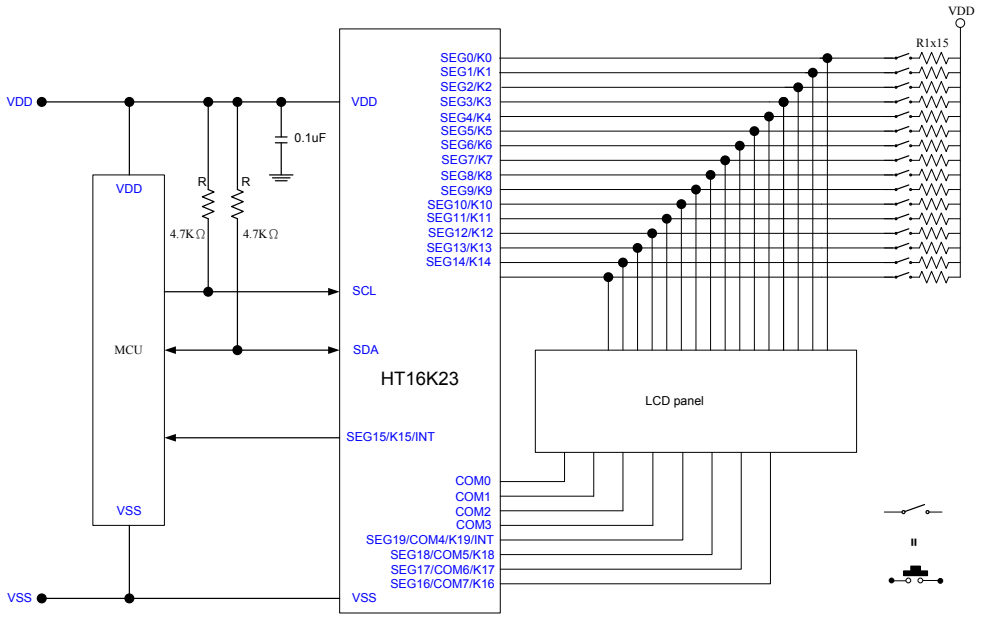


Note: R1=180KΩ ~ 220KΩ, adjust R1 to fit the LCD visual quality.

- **16*8 display mode without INT**



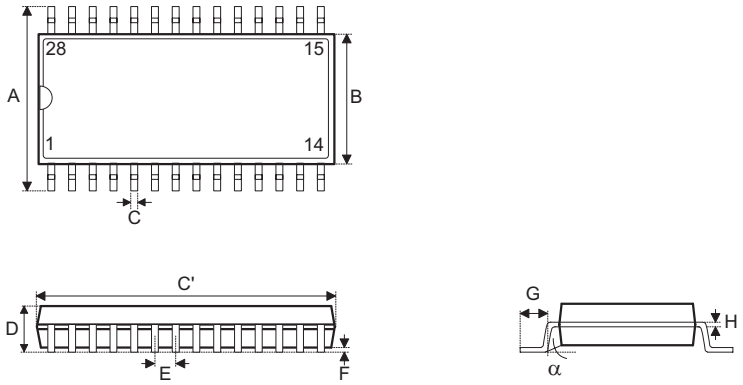
- **15*8 display mode with INT**



Note: R1=180KΩ ~ 220KΩ, adjust R1 to fit the LCD visual quality.

Package Information

28-pin SOP (300mil) Outline Dimensions

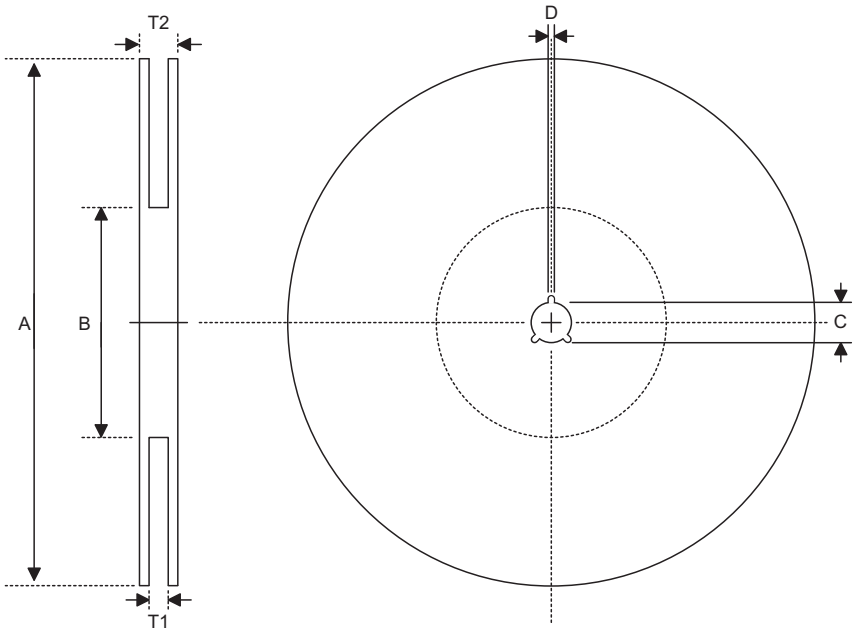


MS-013

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.393	—	0.419
B	0.256	—	0.300
C	0.012	—	0.020
C’	0.697	—	0.713
D	—	—	0.104
E	—	0.050	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.98	—	10.64
B	6.50	—	7.62
C	0.30	—	0.51
C’	17.70	—	18.11
D	—	—	2.64
E	—	1.27	—
F	0.10	—	0.30
G	0.41	—	1.27
H	0.20	—	0.33
α	0°	—	8°

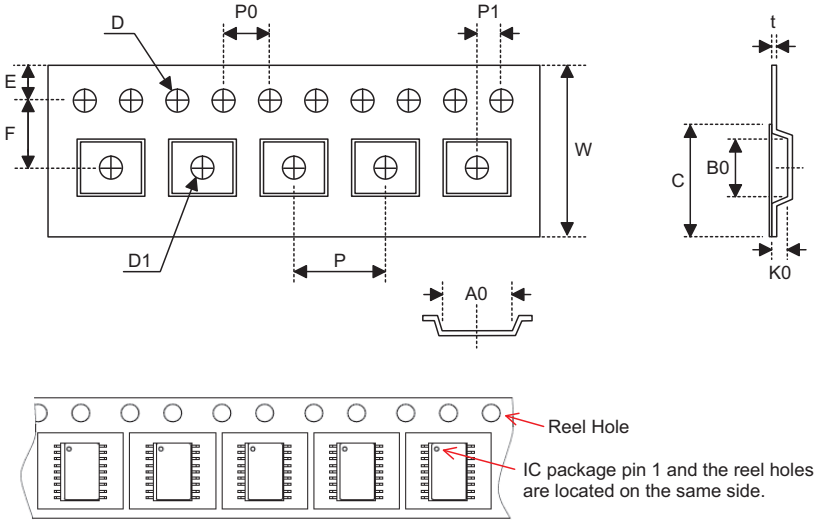
Reel Dimensions



SOP 28W (300mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	24.8 $^{+0.3/-0.2}$
T2	Reel Thickness	30.2±0.2

Carrier Tape Dimensions



SOP 28W (300mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.50^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.85±0.10
B0	Cavity Width	18.34±0.10
K0	Cavity Depth	2.97±0.10
t	Carrier Tape Thickness	0.35±0.01
C	Cover Tape Width	21.3±0.1

Holtek Semiconductor Inc. (Headquarters)
No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189
http://www.holtek.com.tw

Holtek Semiconductor Inc. (Taipei Sales Office)
4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan
Tel: 886-2-2655-7070
Fax: 886-2-2655-7373
Fax: 886-2-2655-7383 (International sales hotline)

Holtek Semiconductor Inc. (Shenzhen Sales Office)
5F, Unit A, Productivity Building, No.5 Gaoxin M 2nd Road, Nanshan District, Shenzhen, China 518057
Tel: 86-755-8616-9908, 86-755-8616-9308
Fax: 86-755-8616-9722

Holtek Semiconductor (USA), Inc. (North America Sales Office)
46729 Fremont Blvd., Fremont, CA 94538, USA
Tel: 1-510-252-9880
Fax: 1-510-252-9885
http://www.holtek.com