HT16LK24
RAM Mapping 67×4/63×8 LCD Driver with Key Scan

Feature

- Logic Operating Voltage:1.8V ~ 5.5V
- LCD Operating Voltage (V_{LCD}):2.4V ~ 6.0V
- Internal 32kHz RC oscillator
- Duty:1/1 (static), 1/2, 1/3, 1/4 or 1/8;
  Bias: 1/1 (static), 1/2, 1/3 or 1/4
- Internal LCD bias generation with voltage-follower buffers
- External V_{LCD} pin to supply LCD operating voltage
- Integrated regulator to adjust LCD operating voltage: 3.0V, 3.2V, 3.3V, 3.4V, 4.4V, 4.5V, 4.6V, 5.0V
- Four Selectable LCD frame frequencies: 64Hz, 85.3Hz, 128Hz or 170.6Hz
- Integrated LED driver up to 12 channels
- Support key scan function with up to 4×12 key matrix
- Support up to 128 levels PWM luminance control
- Support I^2C-bus or SPI 3-wire serial interface
- Up to 63×8 bits RAM for display data storage
- Display patterns:
  – 1/1 duty: up to 67×1 patterns
  – 1/2 duty: up to 67×2 patterns
  – 1/3 duty: up to 67×3 patterns
  – 1/4 duty: up to 67×4 patterns
  – 1/8 duty: up to 63×8 patterns
- Support three driver output modes: Segment/COM, LED or Key Scan
- Versatile blinking modes: off, 0.5Hz, 1Hz, 2Hz
- R/W address auto increment
- Support Power Save Mode for low power consumption
- Manufactured in silicon gate CMOS process
- Package Type: 64LQFP and 80LQFP packages

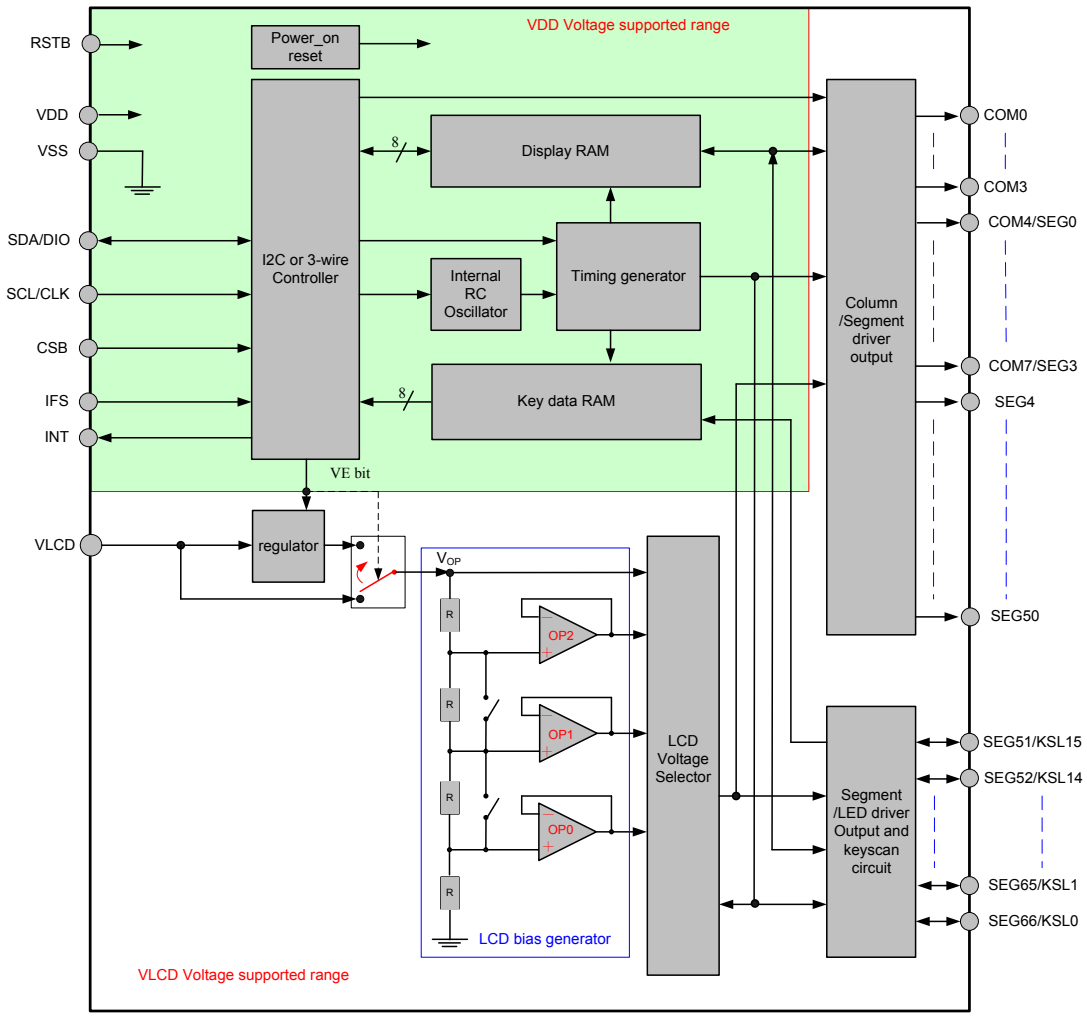
Applications

- Leisure products
- Games
- Telephone display
- Audio Combo display
- Video Player display
- Kitchen Appliance display
- Measurement equipment display
- Household appliance
- Consumer electronics

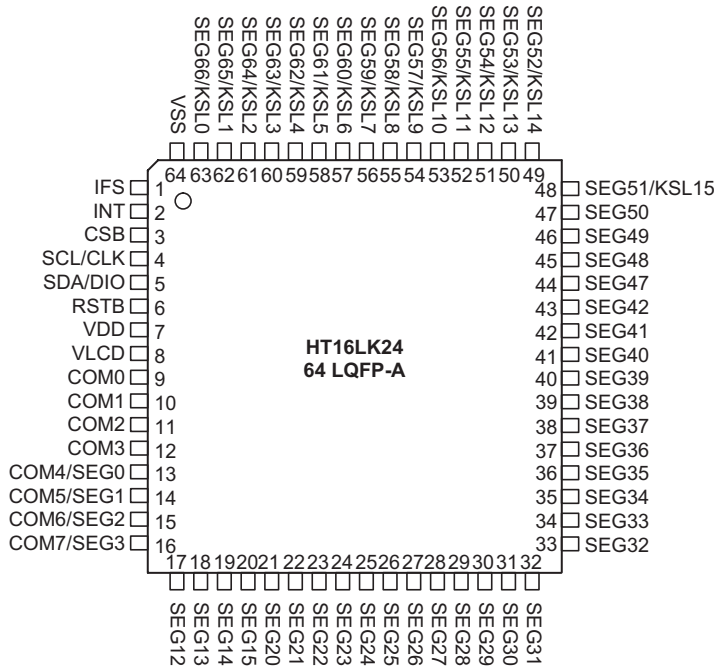
General Description

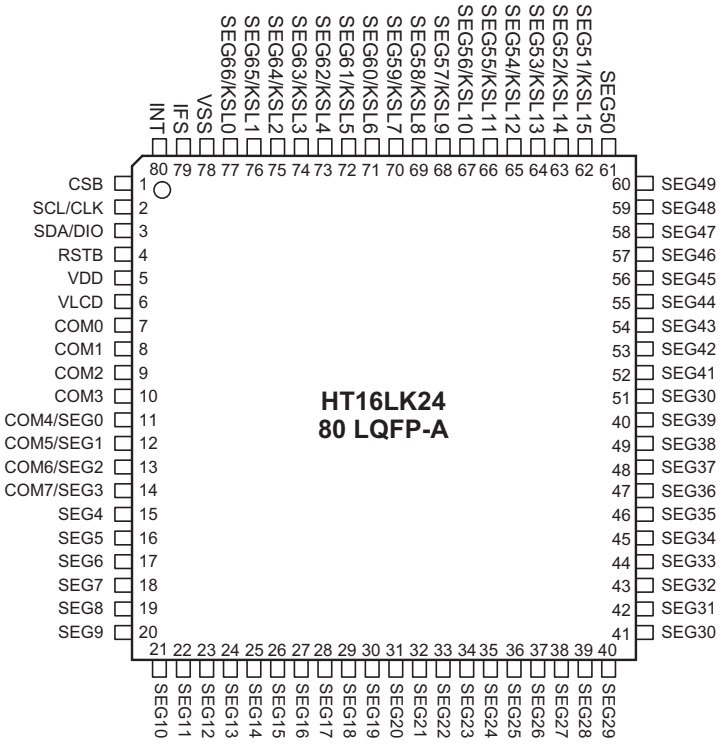
The HT16LK24 device is a memory mapping and multi-function LCD controller driver. The Display segments of the device may be 67 patterns for 1/1 duty display, 134 patterns for 1/2 duty display, 201 patterns for 1/3 duty display, 268 patterns for 1/4 duty display or 504 patterns for 1/8 duty display. It can also support LED drive outputs on certain Segment pins with up to 128 levels luminance PWM control. The key scan circuitry which can be organized into a 4×12 matrix is also integrated in this device. The software configuration feature of the HT16LK24 device makes it suitable for multiple LCD applications including LCD modules and display subsystems. The HT16LK24 device communicates with most microprocessors/ microcontrollers via a two-wire bidirectional I^2C-bus or a three-wire SPI interface.

Block Diagram



Pin Assignment



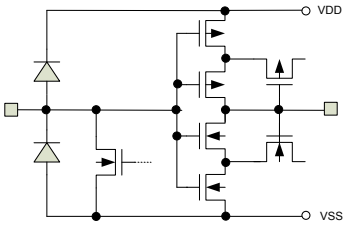


Pin Description

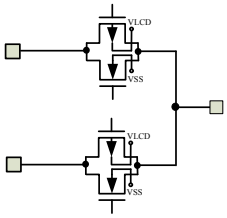
Pin Name	Type	Description
SDA/DIO	I/O	Serial Data Input/Output pin Serial Data (SDA) Input/Output for 2-wire I^2C interface is an NMOS open drain structure. Serial Data (DIO) Input/Output for 3-wire SPI interface is a CMOS input/output structure.
SCL/CLK	I	Serial Clock Input pin Serial Clock (SCL) for 2-wire I^2C interface. Serial Clock (CLK) for 3-wire SPI interface
CSB	I	SPI Chip Select pin This pin is active low and only available for 3-wire SPI interface. When the I^2C interface is used, this pin is not used and must be connected to VDD.
IFS	I	Communication interface select pin This pin is used to select the communication interface. When this pin is connected to VDD, the device communicates with MCU or microprocessors via a 2-wire I^2C interface. When this pin is connected to VSS, the device communicates with MCU or microprocessors using a 3-wire SPI interface.
INT	O	Interrupt signal output pin After a power-on or reset condition occurs, the INT pin is in a high level. The INT output polarity can be changed by configuring the POL bit in the key scan control command via the I^2C or SPI interface.
COM0~COM3	O	LCD Common outputs.
COM4/SEG0~ COM7/SEG3	O	LCD Common/Segment multiplexed driver outputs
SEG4~SEG50	O	LCD Segment outputs.
SEG51/KSL15~ SEG66/KSL0	O	LCD Segment / Key input / Key Scan output / LED output pins These pins are LCD segment pins after a power on or reset condition. When the KSLn pins are configured as other shared functional pins except segment outputs, the LED outputs has higher priority than the Key Scan outputs followed by the Key inputs. After the KSLn pin-shared functions are determined by configuring the corresponding L, KX and KY fields in the shared-pin configuration command, the rest pins then are used as the LCD segment outputs.
RSTB	I	Reset input pin This pin is active low and used to initialize all the internal registers and the commands pin.
VDD	—	Positive power supply.
VSS	—	Negative power supply, ground.
VLCD	—	LCD power supply pin

Approximate Internal Connections

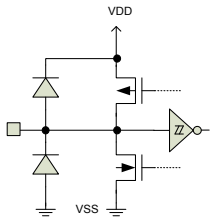
SCL, SDA (for Schmitt trigger type)



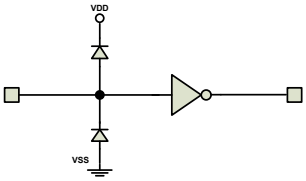
COM0~COM7; SEG0~SEG50



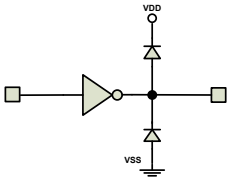
DIO (for Schmitt trigger type)



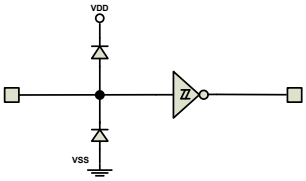
IFS, RSTB



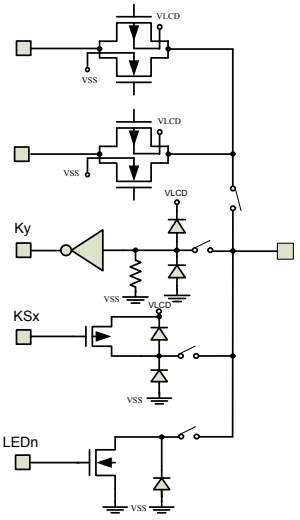
INT



CSB, CLK (for Schmitt trigger type)



SEG51_KSL15~SEG66_KSL0



Ky: Key input
KSx: Key Scan output

Absolute Maximum Ratings

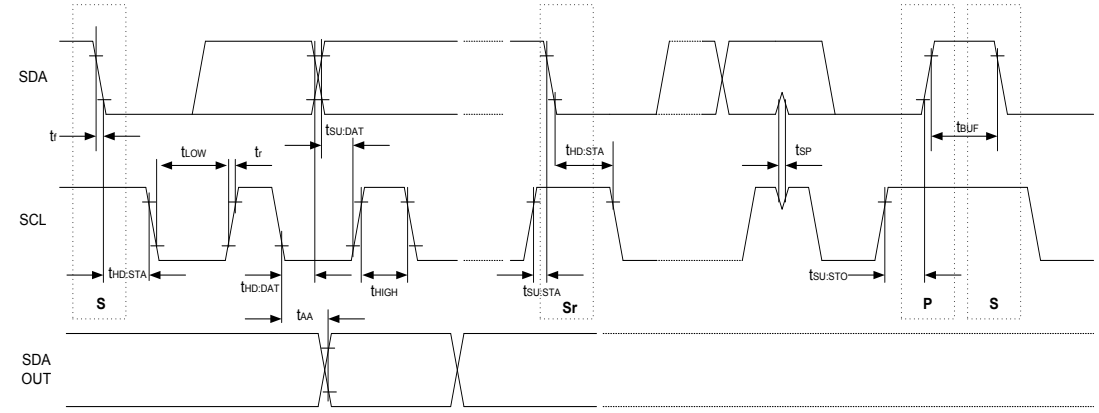
Supply Voltage .... V_{SS}-0.3V to V_{SS}+6.6V
Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V
Total LED Driver Output Current (Ta=25°C)....132mA

Storage Temperature ..... -55°C to 150°C
Operating Temperature ..... -40°C to 85°C

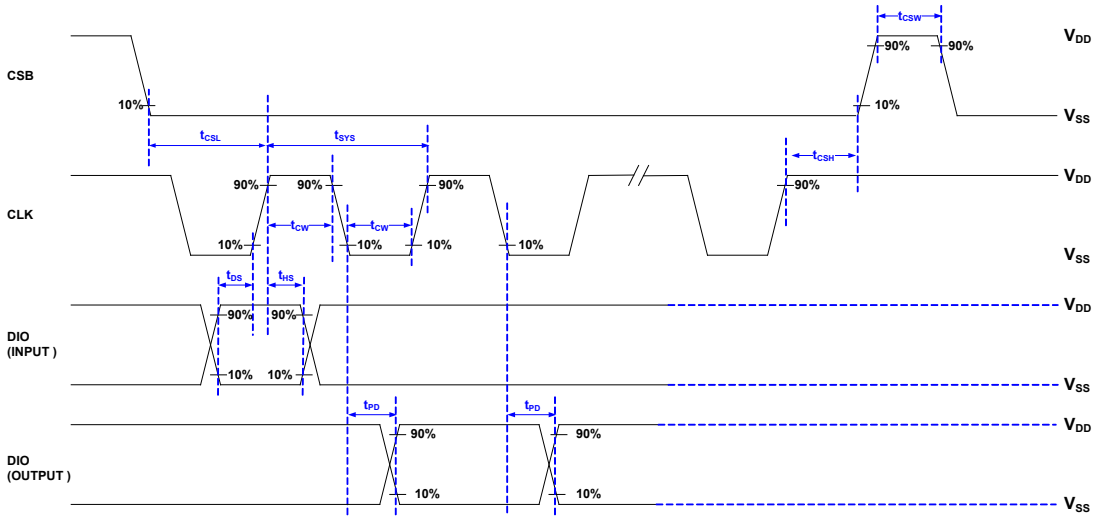
Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Timing Diagrams

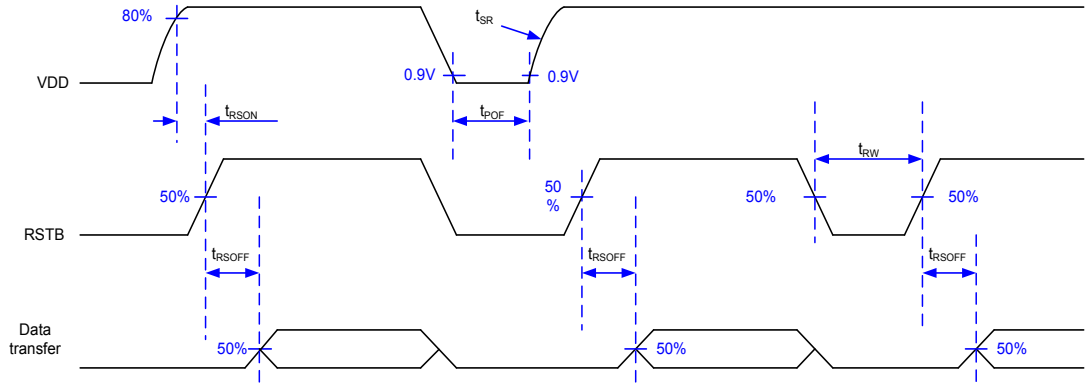
I²C Interface Timing



SPI Timing



Reset Timing



Note: 1. If the conditions of Reset timing are not satisfied in power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.

2. If the V_{DD} drops lower than the minimum operating voltage during operating, the conditions of Power on Reset timing must also be satisfied. That is the V_{DD} drop to 0.9V and keep at 0.9V for 10ms (min.) before rising to the normal operating voltage.

3. Data transfers on the I^2C-bus or SPI 3-wire serial bus should at least be delayed for 1ms after the power-on sequence to ensure that the reset operation is complete.

D.C. Characteristics

V_{SS}= 0V, V_{DD}= 1.8V to 5.5V, Ta= -40°C to +85°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	1.8	—	5.5	V
V_{LCD}	LCD Operating Voltage	—	—	2.4	—	6	V
V_{IH}	Input High Voltage	—	CSB, CLK, DIO, RSTB	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input Low Voltage	—	CSB, CLK, DIO, RSTB	0	—	0.3V_{DD}	V
I_{IL}	Input Leakage Current	—	V_{IN}=V_{SS} or V_{DD}	-1	—	1	μA
I_{OH}	High Level Output Current	2.0V	V_{OH}=0.9V_{DD} for DIO pin	-2	—	—	mA
		3.3V		-6	—	—	mA
		5.0V		-12	—	—	mA
I_{OL}	Low Level Output Current	2.0V	V_{OL}=0.4V for SDA/DIO pin	3	—	—	mA
		3.3V		6	—	—	mA
		5.0V		9	—	—	mA
I_{DD}	Operating Current	2.0V	No load, f_{LCD}=64Hz, 1/3bias, LCD display on, Internal system oscillator on, VLCD pin input voltage =5V, Disable integrated regulator, LED and Key scan	—	1	3	μA
		3.3V		—	2	6	μA
		5.0V		—	4	12	μA
I_{LCD1}	Operating Current	—	No load, f_{LCD}=64Hz, 1/3bias, LCD display on, Internal system oscillator on, current mode is set to low current 2, VLCD pin input voltage =5V. Disable integrated regulator, LED and Key scan	—	10	20	μA

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
I_{LCD2}	Operating Current	—	No load, f_{LCD}=64Hz, 1/3bias, LCD display on, Internal system oscillator on, current mode is set to low current 2, VLCD pin input voltage =5.5V, Regulator output is set to 5V, disable keyscan and LED	—	25	40	μA
I_{STB1}	Standby Current for VDD	3.3V	No load, 1/3bias, LCD display off, Internal system oscillator off, VLCD pin input voltage =5V, Disable integrated regulator, LED and Key scan	—	—	1	μA
		5.0V		—	—	2	μA
I_{STB2}	Standby Current for VLCD	3.3V	No load, 1/3bias, LCD display off, Internal system oscillator off, VLCD pin input voltage =5V, Disable integrated regulator, LED and Key scan	—	—	1	μA
		5.0V		—	—	2	μA
V_{reg}	Regulator Output	—	VLCD pin input voltage =5.5V, Regulator output is set to 4.5V, Ta =-40~85°C	4.35	4.5	4.65	V
			VLCD pin input voltage =5.5V, Regulator output is set to 4.5V, Ta =25°C	4.42	4.5	4.58	V
I_{OL1}	LCD Common Sink Current	—	V_{LCD}=3.3V, V_{OL}=0.33V, Disable integrated regulator	250	400	—	μA
			V_{LCD}=5V, V_{OL}=0.5V Disable integrated regulator	500	800	—	μA
I_{OH1}	LCD Common Source Current	—	V_{LCD}=3.3V, V_{OH}=2.97V, Disable integrated regulator	-140	-230	—	μA
			V_{LCD}=5V, V_{OH}=4.5V, Disable integrated regulator	-300	-500	—	μA
I_{OL2}	LCD Segment Sink Current	—	V_{LCD}=3.3V, V_{OL}=0.33V, Disable integrated regulator	250	400	—	μA
			V_{LCD}=5V, V_{OL}=0.5V, Disable integrated regulator	500	800	—	μA
I_{OH2}	LCD Segment Source Current	—	V_{LCD}=3.3V, V_{OH}=2.97V, Disable integrated regulator	-140	-230	—	μA
			V_{LCD}=5V, V_{OH}=4.5V, Disable integrated regulator	-300	-500	—	μA
I_{OL3}	LED Sink Current	—	V_{LCD}=3.3V, V_{OL}= 1V,	10	—	—	mA
			V_{LCD}=5.0V, V_{OL}= 2V,	20	—	—	mA
I_{OH3}	Key Scan Output Source Current	—	V_{LCD}=3.3V, V_{OL}= 1V,	-2.5	—	—	mA
			V_{LCD}=5.0V, V_{OL}= 2V,	-5	—	—	mA
R_{PL}	Input Pull-low Resistor	—	Key0~Key15 are pressed, Disable regulator	220	—	—	KΩ

Note: 1. Please use the integrated regulator when the Regulator output voltage is less than (V_{LCD} – 0.5V).

2. If the 12 LED outputs are all turned on at the same time, the total current consumption of the LED drivers can not be greater than 120mA.

A.C. Characteristics

Ta= -40°C to +85°C

Symbol	Parameter	Test Condition			Min.	Typ.	Max.	Unit
		V_{DD}	Condition					
f_{LCD1}	LCD Frame Frequency (1/3 duty)	3.3V	Ta=25°C	Frame frequency = 68.3Hz	61	68.3	75.1	Hz
				Frame frequency = 91Hz	81.5	91	100.2	
				Frame frequency = 136.5Hz	122.5	136.5	150.2	
				Frame frequency = 182Hz	164	182	200.3	
f_{LCD2}	LCD Frame Frequency (1/3 duty)	2.5V~5.5V	Ta=-40°C ~ 85°C	Frame frequency = 68.3Hz	54.5	68.3	88.6	Hz
				Frame frequency = 91Hz	72.0	91	118.5	
				Frame frequency = 136.5Hz	109.2	136.5	177.1	
				Frame frequency = 182Hz	145	182	237	
f_{LCD3}	LCD Frame Frequency (1/3 duty)	1.8V~2.5V	Ta=-40°C ~ 85°C	Frame frequency = 68.3Hz	48	—	68.3	Hz
				Frame frequency = 91Hz	62.5	—	91	
				Frame frequency = 136.5Hz	95.5	—	136.5	
				Frame frequency = 182Hz	125.5	—	182	
f_{LCD4}	LCD Frame Frequency (1/4 duty)	3.3V	Ta=25°C	Frame frequency = 64Hz	57.6	64	70.4	Hz
				Frame frequency = 85.3Hz	76	85.3	94	
				Frame frequency = 128Hz	115.2	128	140.8	
				Frame frequency = 170.6Hz	152	170.6	188	
f_{LCD5}	LCD Frame Frequency (1/4 duty)	2.5V~5.5V	Ta=-40°C ~ 85°C	Frame frequency = 64Hz	51.2	64	83	Hz
				Frame frequency = 85.3Hz	68	85.3	111	
				Frame frequency = 128Hz	102.4	128	166	
				Frame frequency = 170.6Hz	136	170.6	222	
f_{LCD6}	LCD Frame Frequency (1/4 duty)	1.8V~2.5V	Ta=-40°C ~ 85°C	Frame frequency = 64Hz	45	—	64	Hz
				Frame frequency = 85.3Hz	59	—	85.3	
				Frame frequency = 128Hz	90	—	128	
				Frame frequency = 170.6Hz	118	—	170.6	
f_{PWM1}	LED Output PWM Frequency (1/4 duty)	3.3V	Ta=25°C	PWM frequency = 85.3Hz	76	85.3	94	Hz
				PWM frequency = 128Hz	115.2	128	140.8	
				PWM frequency = 170.6Hz	152	170.6	188	
				PWM frequency = 256Hz	230.4	256	281.6	
f_{PWM2}	LED Output PWM Frequency (1/4 duty)	2.5V~5.5V	Ta=-40°C ~ 85°C	PWM frequency = 85.3Hz	68	85.3	111	Hz
				PWM frequency = 128Hz	102.4	128	166	
				PWM frequency = 170.6Hz	136	170.6	222	
				PWM frequency = 256Hz	204.8	256	332	
f_{PWM3}	LED Output PWM Frequency (1/4 duty)	1.8V~2.5V	Ta=-40°C ~ 85°C	PWM frequency = 85.3Hz	59	—	85.3	Hz
				PWM frequency = 128Hz	90	—	128	
				PWM frequency = 170.6Hz	118	—	170.6	
				PWM frequency = 256Hz	180	—	256	
t_{KCT}	Key Scan Cycle Time	3.3V	Ta=25°C, Key scan pulse width = 2ms		6.8	8	9.2	ms
		2.5V~5.5V	Ta=-40°C~85°C, Key scan pulse width = 2ms		5.6	8	10.4	
		1.8V~2.5V	Ta=-40°C~85°C, Key scan pulse width = 2ms		7.2	—	12	

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
t_{KPW}	Key Scan Pulse Width	3.3V	Ta=25°C, Key scan pulse width = 2ms	1.7	2	2.3	ms
		2.5V~5.5V	Ta=-40°C~85°C, Key scan pulse width = 2ms	1.4	2	2.6	
		1.8V~2.5V	Ta=-40°C~85°C, Key scan pulse width = 2ms	1.8	—	3.0	
t_{SR}	V_{DD} Slew Rate	—	—	0.05	—	—	V/ms
t_{POF}	V_{DD} OFF Times	—	V_{DD} drop down to 0.9V	10	—	—	ms
t_{RSON}	RSTB Input Time	—	When RSTB signal is externally input from a microcontroller, etc.	250	—	—	ns
			R=100KΩ and C=0.1μF (see application circuit)	—	100	—	ms
t_{RW}	RSTB Pulse Width	—	When RSTB signal is externally input from a microcontroller etc.	400	—	—	ns
t_{RSOFF}	Wait Time for Data Transfers	—	2-wire I^2C-bus or 3-wire SPI bus	1	—	—	ms

I^2C Interface Characteristics

Unless otherwise specified, V_{SS}=0 V, V_{DD}=1.8V to 5.5V, Ta= -40°C to +85°C

Symbol	Parameter	Condition	V_{DD}=1.8V to 5.5V		V_{DD}=3.0V to 5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock Frequency	—	—	100	—	400	kHz
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD: STA}$	Start Condition Hold Time	After this period, the first clock pulse is generated	4	—	0.6	—	μs
t_{LOW}	SCL Low Time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High Time	—	4	—	0.6	—	μs
$t_{SU: STA}$	Start Condition Setup Time	Only relevant for repeated START condition.	4.7	—	0.6	—	μs
$t_{HD: DAT}$	Data Hold Time	—	0	—	0	—	ns
$t_{SU: DAT}$	Data Setup Time	—	250	—	100	—	ns
t_R	SDA and SCL Rise Time	Note	—	1	—	0.3	μs
t_F	SDA and SCL Fall Time	Note	—	0.3	—	0.3	μs
$t_{SU: STO}$	Stop Condition Set-up Time	—	4	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	20	—	20	ns

Note: These parameters are periodically sampled but not 100% tested.

A.C. Characteristics – SPI Interface

Unless otherwise specified, V_{SS}=0V, V_{DD}=1.8V to 5.5V, Ta= -40°C to +85°C

Symbol	Parameter	Test Condition			Min.	Typ.	Max.	Unit
		V_{DD}	Condition					
t_{SYS}	Clock cycle time	—	For write data		250	—	—	ns
			For read data		1000	—	—	ns
t_{CW}	Clock Pulse Width	—	For write data		50	—	—	ns
			For read data		400	—	—	ns
t_{DS}	Data Setup Time	—	For write data		50	—	—	ns
t_{DH}	Data Hold Time	—	For write data		50	—	—	ns
t_{CSW}	"H" CSB Pulse Width	—	—		50	—	—	ns
t_{CSL}	CSB Setup Time (CSB↓ — CLK↑)	—	For write data		50	—	—	ns
			For read data		400	—	—	ns
t_{CSH}	CS Hold Time (CLK↑ — CSB↑)	—	—		2	—	—	μs
t_{PD}	DATA Output Delay Time (CLK — DIO)	—	C_O=15pF	t_{PD}=10% to 90%	—	—	350	ns
				t_{PD}=90% to 10%				

Note: $f_{LCD}= 1/t_{LCD}$

Functional Description

Power-On Reset

When the power is applied, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common outputs are set to V_{LCD}.
- All segment outputs are set to V_{LCD}.
- The drive mode 1/4 duty output and 1/3 bias is selected.
- The System Oscillator and the LCD bias generator are off state.
- LCD Display is off state.
- Integrated regulator is disabled.
- Key scan pulse width is set to 2 ms and INT output is set to a high level.
- The Segment/Key scan/LED shared pin is set as the Segment pin.
- The LCD driving mode is set to the normal current mode.
- Frame Frequency is set to 64Hz.
- Blinking function is switched off.

Reset Function

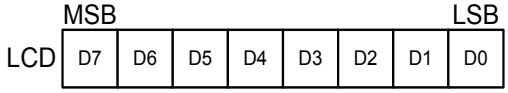
When the RSTB pin is pulled to a low level, a reset operation is executed and it will initialize all functions. The status of the internal circuits after initialization is as follows:

- All common outputs are set to V_{LCD}.
- All segment outputs are set to V_{LCD}.
- The drive mode 1/4 duty output and 1/3 bias is selected.
- The System Oscillator and the LCD bias generator are off state.
- LCD Display is off state.
- Integrated regulator is disabled.
- The Segment/Key scan/LED shared pin is set as the Segment pin.
- The LCD driving mode is set to the normal current mode.
- Frame Frequency is set to 64Hz.
- Blinking function is switched off

Display Memory – RAM Structure

The display RAM is static 63 x 8-bits RAM which stores the LCD data. Logic "1" in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly, logic 0 indicates the ‘off’ state.

The contents of the RAM data are directly mapped to the LCD data. The first RAM column corresponds to the segments operated with respect to COM0. In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with COM1, COM2 and COM3 respectively. The LCD display duty can be 1/4 or 1/8 determined by a Duty bit contained in the Drive Mode Command. The following diagram is a data transfer format for I^2C or SPI interface.



LCD Display data transfer format for I^2C or SPI bus

Display Mode

- **1/1, 1/2, 1/3, 1/4 duty**
  When the Duty2 bit is set to 0, the drive mode can be selected as 1/1, 1/2, 1/3 or 1/4 duty using the Duty1 and Duty0 bits and the LCD RAM map is implemented as the following table shown. This default display mode is 1/4 duty after a reset.

- **1/8 duty**
  When the Duty2 bit is set to 1, the drive mode is selected as 63 segments by 8 commons and the LCD RAM map is implemented as the following table shown.

System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator. The System Clock frequency (f_{SYS}) determines the LCD frame frequency. During initial system power on the System Oscillator will be in the stop state.

LCD Bias Generator

The LCD supply power can come from the external VLCD pin or the internal regulator output voltage determined using the Internal Voltage Adjustment (IVA) setting command. The device provides an external VLCD pin and also integrates an internal regulator. The LCD voltage may be temperature compensated externally through the Voltage supply to the V_{LCD} pin. The internal regulator can also provide the LCD operating voltage. Therefore, the full-scale LCD voltage (V_{OP}) is obtained from ($V_{LCD} - V_{SS}$) or ($V_{reg} - V_{SS}$).

Fractional LCD biasing voltages, known as 1/1, 1/2, 1/3 or 1/4 bias voltage, are obtained from an internal voltage divider of four series resistors connected between V_{OP} and V_{SS}. The resistors can be switched out of circuits to provide a 1/2, 1/3 or 1/4 bias voltage level configuration.

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
SEG65					SEG64					20H
					SEG66					21H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

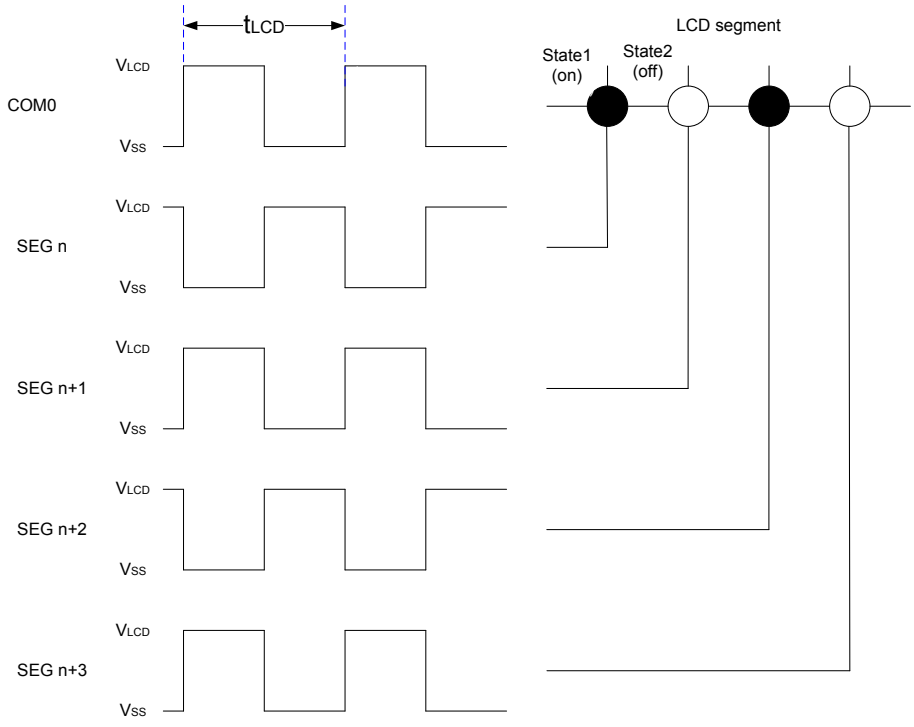
RAM mapping of 67x4 display mode – 1/1, 1/2, 1/3 and 1/4 duty

Output	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	Address
SEG4									00H
SEG5									01H
SEG6									02H
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
SEG66									3EH
	D7	D6	D5	D4	D3	D2	D1	D0	Data

RAM mapping of 63x8 display mode – 1/8 duty

LCD Drive Mode Waveforms

- When the LCD drive mode is selected as 1/1 duty and 1/1 bias (static), the waveform and LCD display is shown as follows:

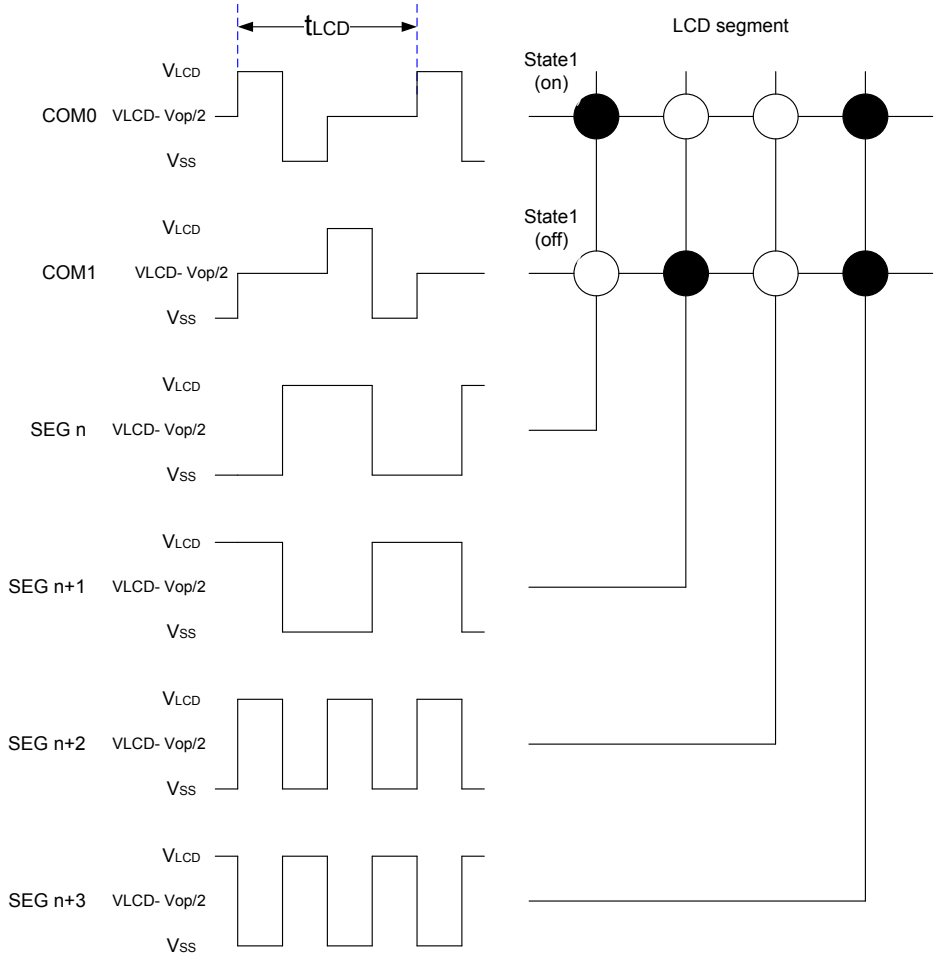


Waveforms for 1/1 duty drive mode with 1/1 bias (V_{OP}=V_{LCD}-V_{SS})

Note: 1. t_{LCD}=1/ f_{LCD}

2. The unused COM1~3 outputs must be left open-circuit and the outputs are pulled to a high level (V_{LCD}).

- When the LCD drive mode is selected as 1/2 duty and 1/2 bias, the waveform and LCD display is shown as follows:

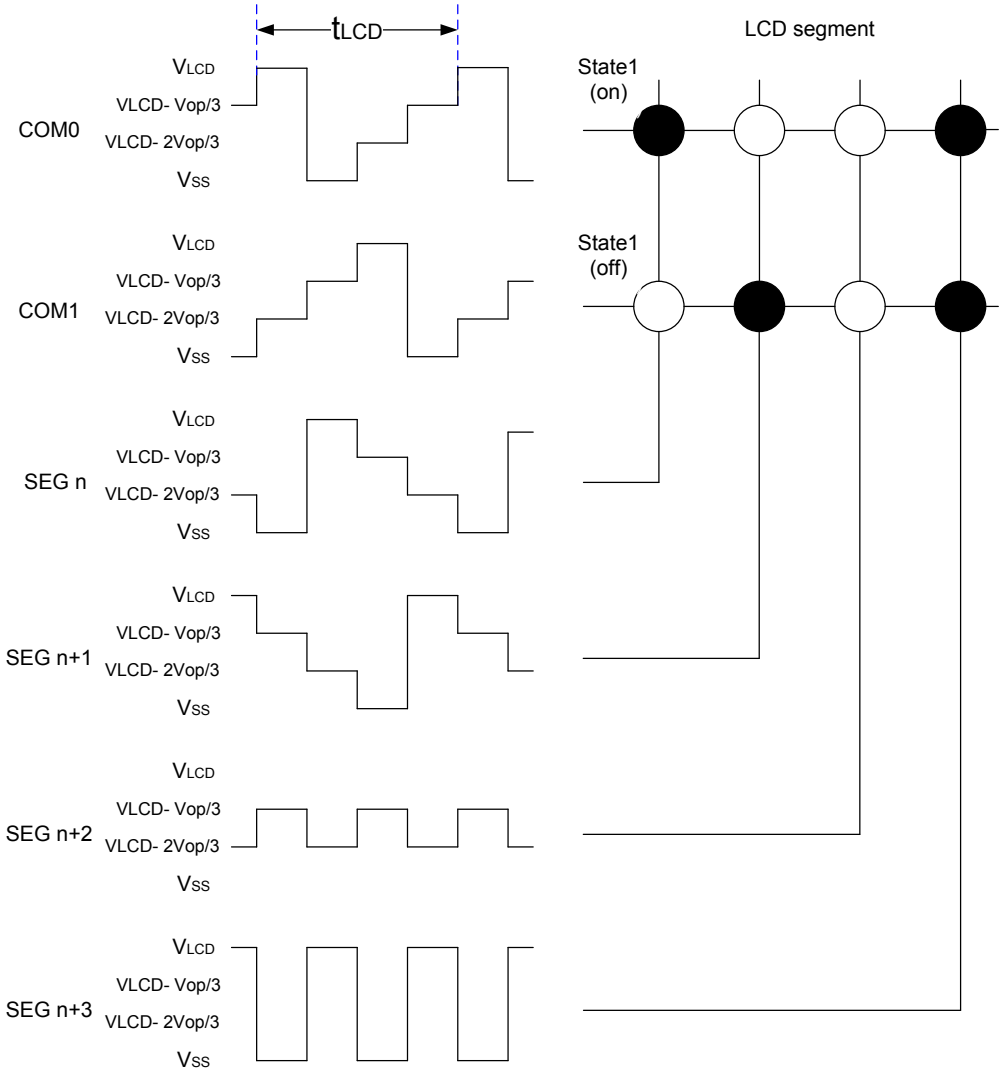


Waveforms for 1/2 duty drive mode with 1/2 bias ($V_{OP}=V_{LCD}-V_{SS}$)

Note: 1. $t_{LCD}=1/f_{LCD}$

2.The unused COM2~3 outputs must be left open-circuit and the outputs are pulled to a high level (V_{LCD}).

- When the LCD drive mode is selected as 1/2 duty and 1/3 bias, the waveform and LCD display is shown as follows:

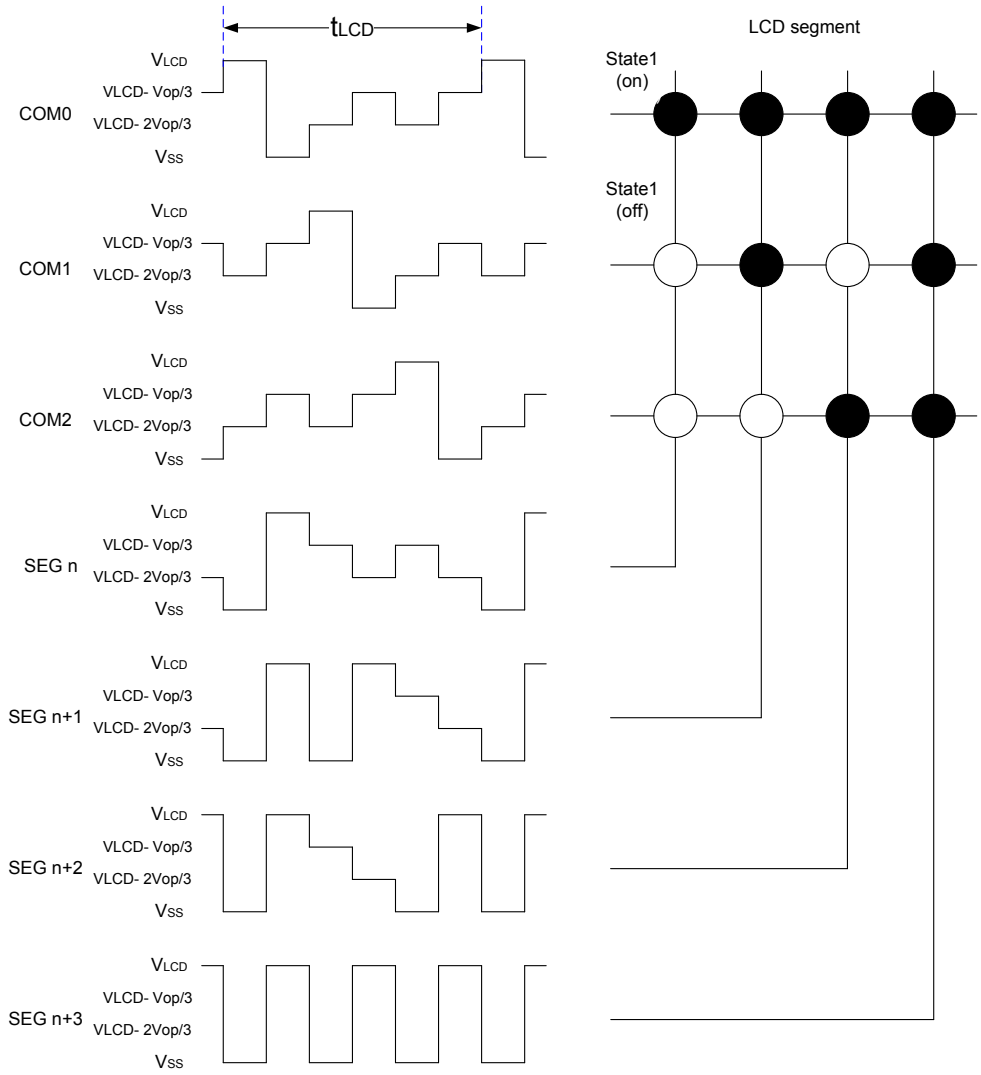


Waveforms for 1/2 duty drive mode with 1/3 bias (V_{OP}=V_{LCD}-V_{SS})

Note: 1. t_{LCD}=1/ f_{LCD}

2. The unused COM2~3 outputs must be left open-circuit and the outputs are pulled to a high level (V_{LCD}).

- When the LCD drive mode is selected as 1/3 duty and 1/3 bias, the waveform and LCD display is shown as follows:

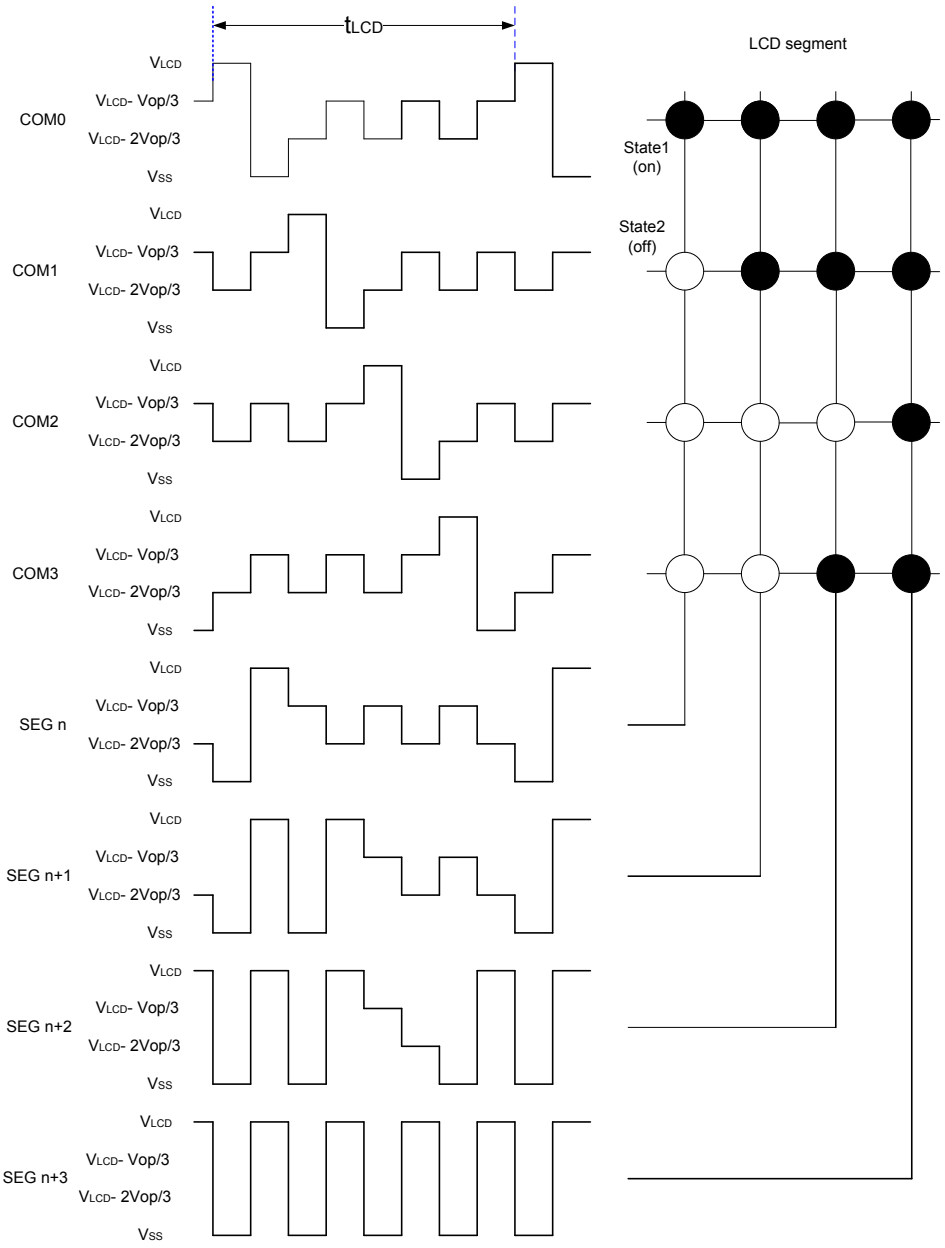


Waveforms for 1/3 duty drive mode with 1/3 bias ($V_{OP}=V_{LCD}-V_{SS}$)

Note: 1. $t_{LCD}=1/f_{LCD}$

2. The unused COM3 output must be left open-circuit and the output is pulled to a high level (V_{LCD}).

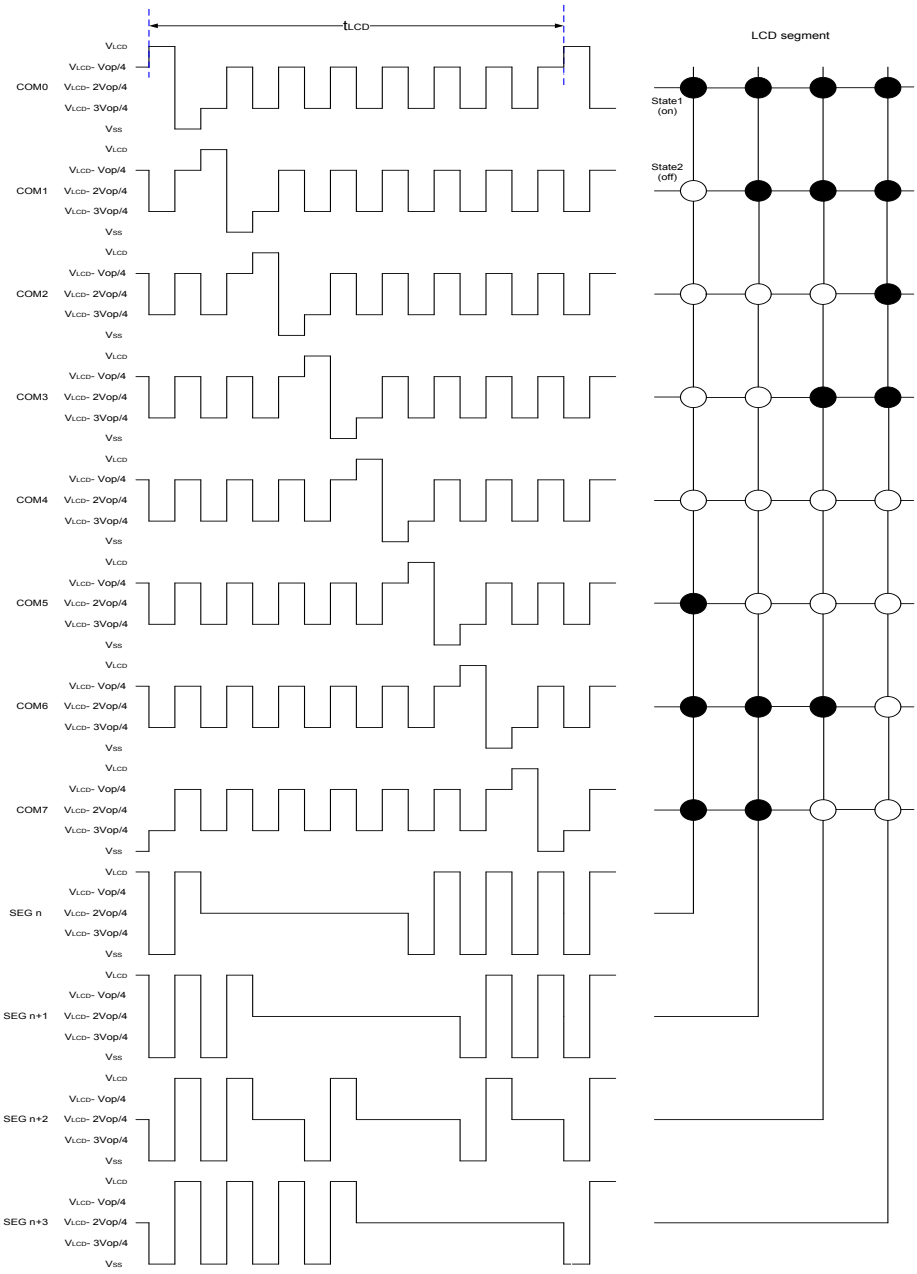
- When the LCD drive mode is selected as 1/4 duty and 1/3 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/4 duty drive mode with 1/3 bias (V_{OP}=V_{LCD}-V_{SS})

Note: t_{LCD}=1/ f_{LCD}

- When the LCD drive mode is selected as 1/8 duty and 1/4 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/8 duty drive mode with 1/4 bias ($V_{OP}=V_{LCD}-V_{SS}$)

Note: $t_{LCD}=1/ f_{LCD}$

Segment Driver Outputs

The LCD drive section includes up to 67 segment outputs which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit.

Column Driver Outputs

The LCD drive section includes 4 column outputs COM0~COM3 or 8 column outputs COM0~COM7 which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit if less than 4 or 8 column outputs are required.

Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the Display Data Input command.

Blinking Function

The device contains versatile blinking capabilities. The whole display can be blinked at frequencies selected by the Blinking Frequency command. The blinking frequency is a subdivided ratio of the system frequency. The ratio between the system oscillator and blinking frequencies depends on the blinking mode in which the device is operating, as shown in the following table:

Blinking Mode	Blinking frequency (Hz)
0	Blink off
1	2
2	1
3	0.5

Frame Frequency

The HT16LK24 device provides four frame frequencies selected with Frame Frequency command known as 64Hz, 85.3Hz, 128Hz and 170.6Hz respectively.

LED Function

The device provides up to 12 LED output driving pins with 128-level PWM luminance control. The LED pins are NMOS-structured output pins. The Data for the LED output is contained in the LED output control command, starting from the most significant bit. When a written data bit for a LED pin is set to 1, the corresponding driving LED lights up while the LED is switched off when the written data bit is 0. The LED data is transferred from the MSB first via I^2C or SPI interface.

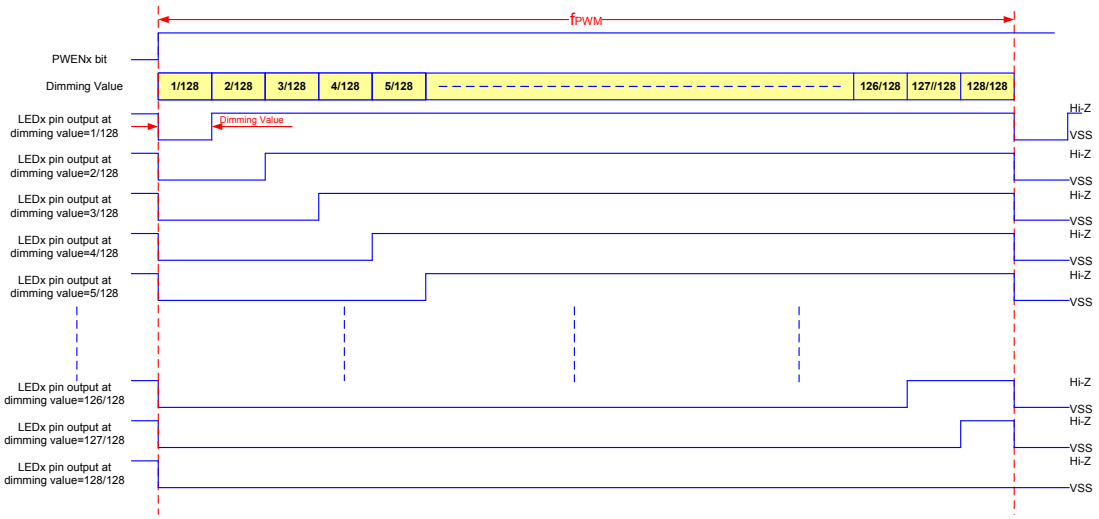
	MSB							LSB
LED output1 command	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
LED output2 command	x	x	x	x	LED11	LED10	LED9	LED8

LED Display data transfer format for I^2C or SPI bus

The luminance of each lighted LED output pin can be programmable individually using the LED PWM luminance control command after the relevant LED PWM function is enabled. When the PWM function enable bit, PWENx, is set to 1, the corresponding PWM function will be enabled. Otherwise, the LED PWM luminance function will be disabled if the PWENx bit is cleared to 0.

The dimming values contained in the LED PWM luminance control command is used to determine the low pulse on the corresponding LED output pin as the diagram shown.

The LED pins are pin-shared with the LCD segment together with key scan matrix pins and can be configured using the KX, KY and L fields in the SEG/KSL shared pin configuration command. The LED output function has the priority than the key scan matrix and LCD segment output and the LED output number is determined by configuring the "L" field in the shared pin configuration command.



LED output with PWM luminance control

Note: 1. The LEDx pin data stored in the LED output control command is set to 1.

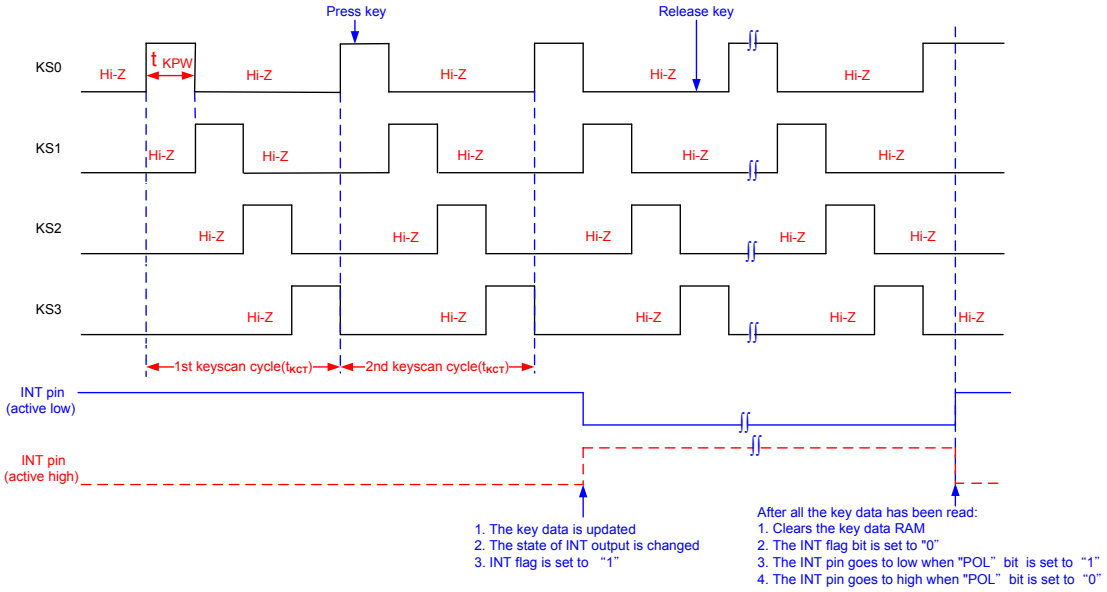
2. The notation "Hi-Z" in the diagram means that the LEDx pin is in an open-drain status.

LED output number set				Segment/key scan/LED Shared pin															
L3	L2	L1	L0	Seg51/ KSL15	Seg52/ KSL14	Seg53/ KSL13	Seg54/ KSL12	Seg55/ KSL11	Seg56/ KSL10	Seg57/ KSL9	Seg58/ KSL8	Seg59/ KSL7	Seg60/ KSL6	Seg61/ KSL5	Seg62/ KSL4	Seg63/ KSL3	Seg64/ KSL2	Seg65/ KSL1	Seg66/ KSL0
0	0	0	0	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63	Seg64	Seg65	Seg66
0	0	0	1	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63	Seg64	Seg65	LED0
0	0	1	0	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63	Seg64	LED1	LED0
0	0	1	1	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63	LED2	LED1	LED0
0	1	0	0	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	LED3	LED2	LED1	LED0
0	1	0	1	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	LED4	LED3	LED2	LED1	LED0
0	1	1	0	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	LED5	LED4	LED3	LED2	LED1	LED0
0	1	1	1	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	LED6	LED5	LED4	LED3	LED2	LED1	LED0
1	0	0	0	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
1	0	0	1	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
1	0	1	0	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
1	0	1	1	Seg51	Seg52	Seg53	Seg54	Seg55	LED10	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
1	1	0	0	Seg51	Seg52	Seg53	Seg54	LED11	LED10	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0

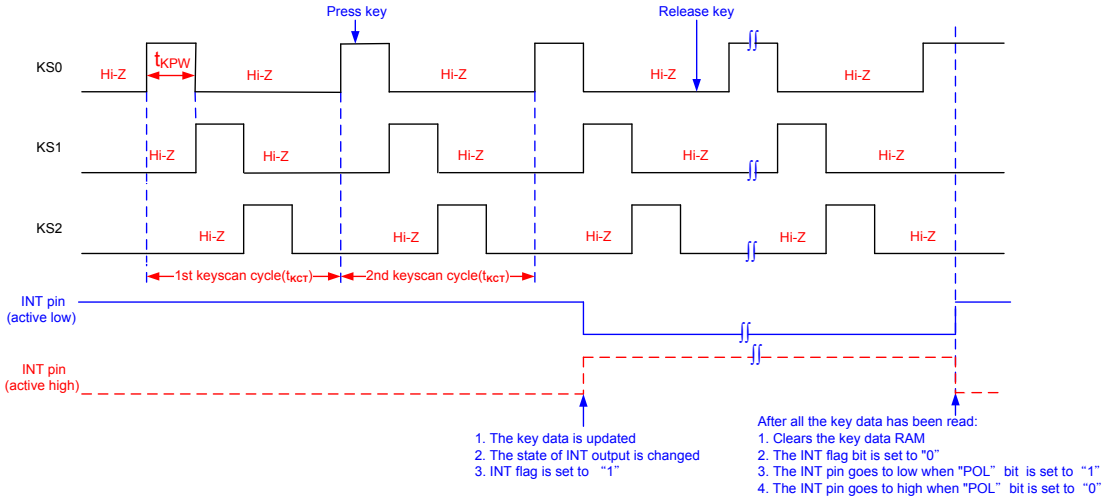
Key Scan Function

The device provides 16 keys which can be used to construct the key matrix for key scan function. These keys can be configured as key inputs or key scan outputs using the KX and KY fields in the shared pins configuration command. For example, if there are four keys, KS3~KS0, set as key scan outputs, the maximum key matrix will contain 12x4 keys. The maximum key matrix can be 12x4, 13x3, 14x2 or 15x1 keys with different key scan output number. However, if there is no key configured as key scan outputs, there are up to 16 key inputs which are externally connected to V_{LCD} voltage.

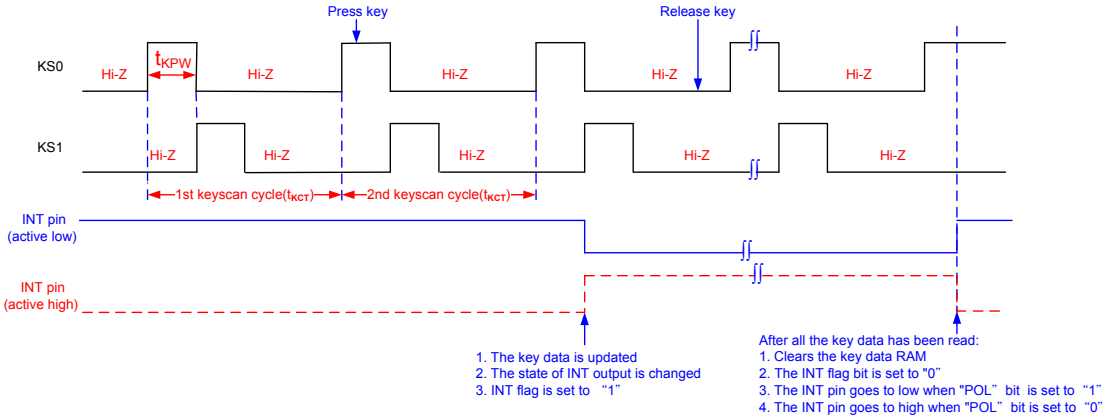
The key scan circuitry sequentially outputs a high pulse on the key scan output pins, KS0~KS3. The key scan output pulse width, t_{KPW}, can be programmable by configuring the KF field in the key scan control command. The key scan circuitry detects the key press at the tail of the key scan output pulse. The key press de-bounce time is 1~2 key scan cycles. That means that the available key press time duration must be equal to or greater than the key debounce time. Therefore, the valid key will be detected twice consecutively.



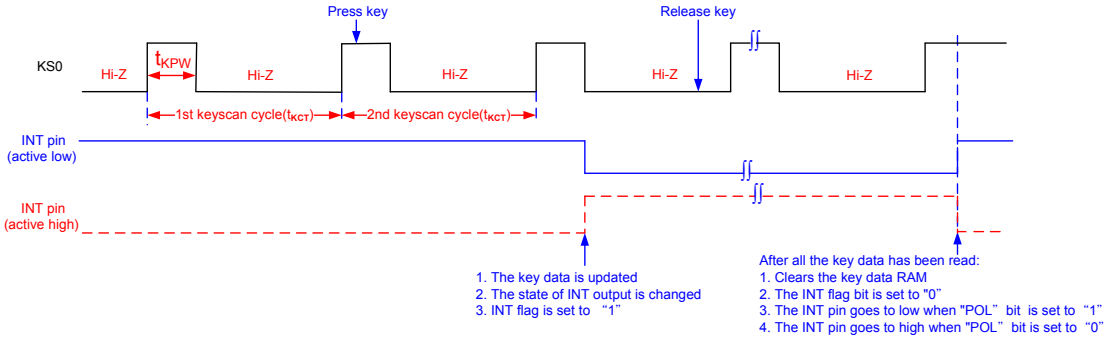
Four key scan outputs – KS0~KS3



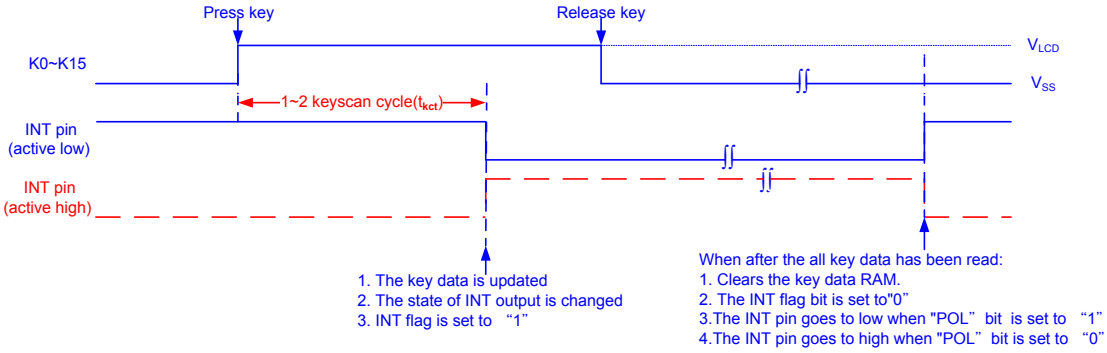
Three key scan outputs – KS0~KS2



Two key scan outputs – KS0~KS1



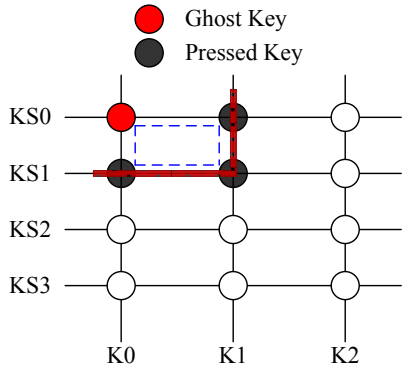
One key scan output – KS0

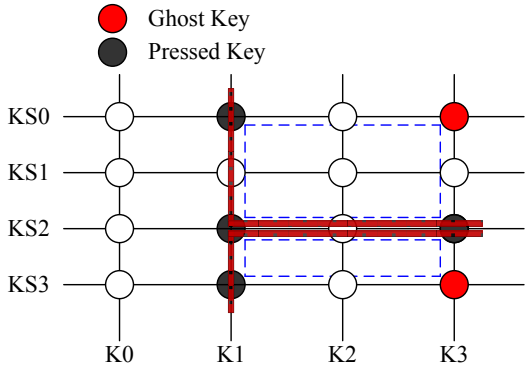


Key inputs – K0~K15

Ghost Key for Key Matrix

The Key scan circuitry can detect multiple pressed keys. However, the ghost keys may be generated when multiple keys are pressed. If three or more than three keys are pressed and the pressed keys are lined in an "L" shape, the ghost keys will be generated. As the accompanying diagram shows, the key on the 4th corner which forms a rectangle together with other three pressed keys will be the ghost key and be recognized as a pressed key no matter the relevant external key is pressed or not. Attentions must be paid to avoid from ghost keys in multiple key press applications.

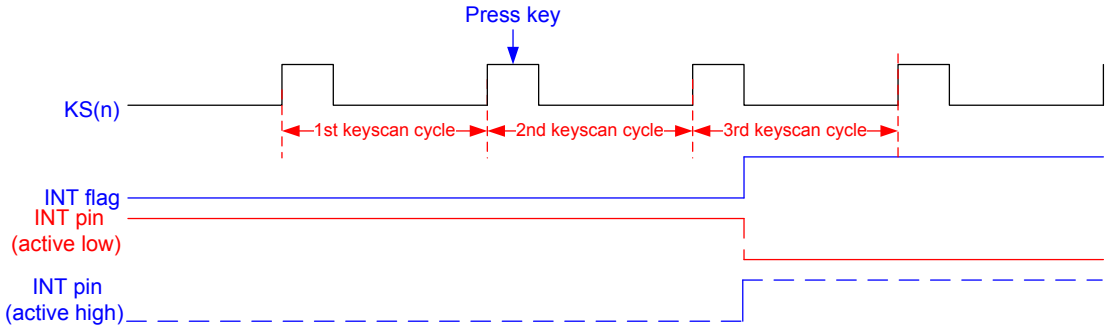


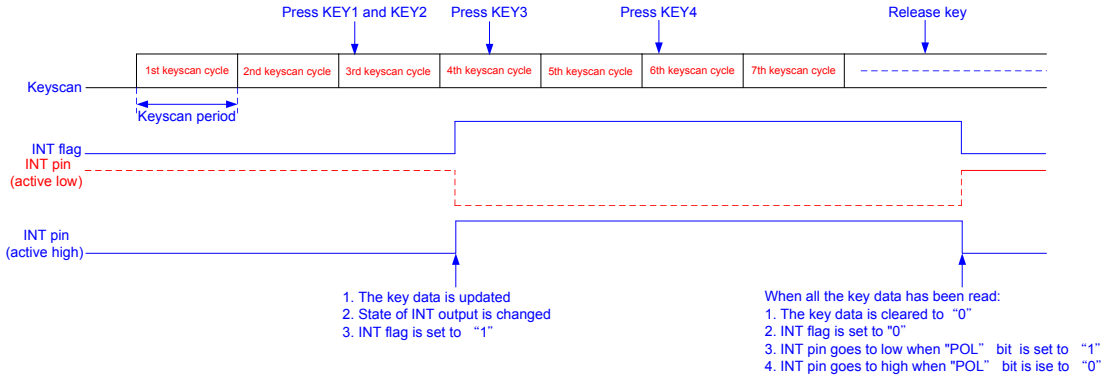


Key Scan Interrupt Function

The device provides two ways to indicate the interrupt occurrence for key scan function.

- Hardware signal
  When the valid key press is detected, the interrupt will be generated and the INT pin will change state from its inactive state to active state. The polarity of the INT output pin can be changed by configuring the POL bit in the Key scan control command via the I^2C or SPI interface. When the POL bit is set to 1, the INT pin is active high while the INT pin is active low if the POL bit is cleared to 0. After the key data has been read, all the key data will be cleared to 0 and the INT pin returns to an inactive state.
- Software indicator
  When the valid key press is detected, the interrupt flag will be set to 1 and can be read using the I^2C or SPI interface. After the key data has been read, all the key data will be cleared to 0 and the interrupt flag will also be cleared to 0. The INT interrupt flag is stored in the register bit 0 and is set and cleared by hardware.





Key Data Memory Structure

- The Key data RAM is a read-only memory and is organized into 16x4 bits which stores the key data detected by the key scan circuitry. Each key data corresponds to one key in the key matrix.
- The key data byte in the corresponding address will be cleared after the data byte is read and therefore, the successive key press can be identified again. If the key data byte is not read, the pressed key data will be successively recorded when other keys are pressed.
- The key data RAM address will be incremented automatically when the key data is read continuously. The address will be wrapped around to the start address 0x00H when the key data RAM read operation is executed successively and the RAM address is greater than the maximum available address 0x07H. It is strongly recommended to read the whole key data from the start address 0x00H sequentially via the I^2C or 3-wiredSPI interface.

Output	K15	K14	K13	K12	K11	K10	K9	K8	Addr.	K7	K6	K5	K4	K3	K2	K1	K0	Addr.
KS0									01H									00H
KS1									03H									02H
KS2									05H									04H
KS3									07H									06H
	D7	D6	D5	D4	D3	D2	D1	D0	Data	D7	D6	D5	D4	D3	D2	D1	D0	Data

Standby Mode

The standby mode is selected by setting the "S" bit in the system mode setting command to "0". It is strongly recommended that the LCD display is first switched off before the standby mode command is setup. Otherwise, the LCD display will be turned on automatically when the device standby mode is released.

When the device enters the standby mode by setting "S" bit in the system mode setting command to "0", the status in standby mode is shown as below:

- System Oscillator LCD display and key scan will be in the off state.
- All key data RAM and INT flag are cleared to "0" until the standby mode is released.
- The INT pin output is set to high when the ‘POL ’ bit in the Key scan control command is set to ‘0’.
- The INT pin output is set to low when the ‘POL’ bit in the Key scan control command is set to ‘1’.
- If the PWENx bit in the LED output control command is set to "0", the status of the corresponding LEDx output pin will not be changed after entering standby mode where "x" means 0~11.
- If the PWENx bit in the LED output control command is set to "1", the status of the corresponding LEDx output pin will be turned off after entering standby mode where "x" means 0~11.
- The K0~K15 pin are set as inputs.
- The KS0~KS3 pins are set to high.
- All common outputs and segment outputs are set to a high level of a V_{LCD} voltage.

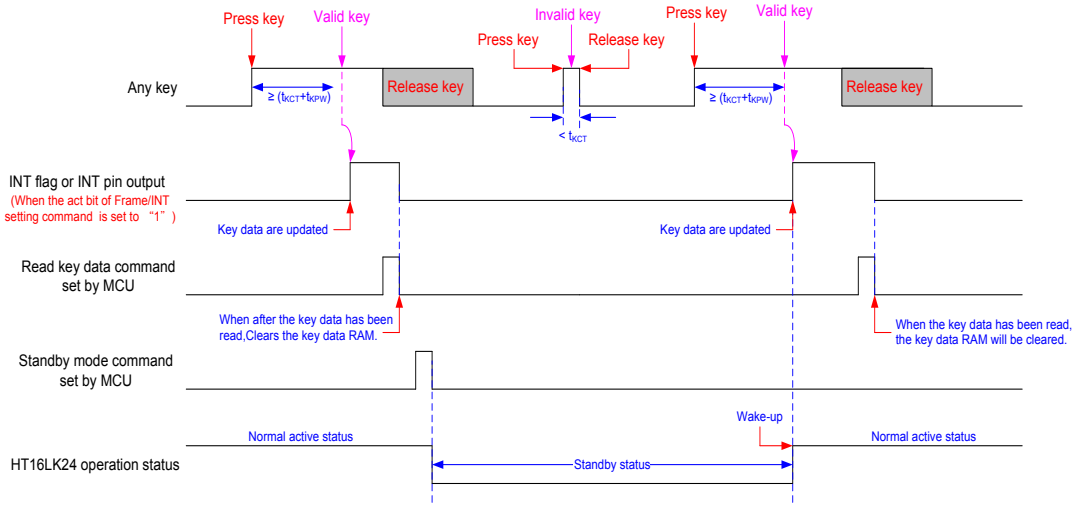
Wake-up Function

The device can be woken up by a valid key press or setting the "S" bit in the system mode setting command to"1". When the device is woken up from the standby mode, the status after wakeup is shown as below:

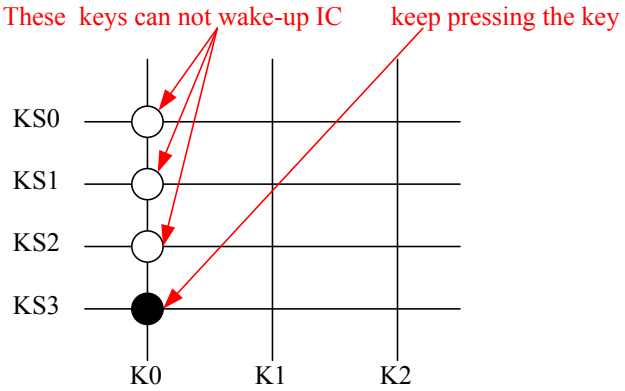
- The System Oscillator restarts.
- The key scan will be performed.
- The LED PWM function will be performed and the LEDx output will be lighted up after wakeup if the PWENx bit is set to 1 and the LEDx data value is set to 1 before entering the standby mode. Otherwise, the LEDx output is always turned off where "x" means 0~11. The relationship between the LED output status and LED PWM function at different modes is shown as below:

PWM function	System OSC	LED output status	LED PWM function
PWEN bit	S bit	Normal mode→Standby mode→ Wake up mode/ Normal mode	Normal mode→Standby mode→ Wake up mode/ Normal mode
0	1→0→1	off→off→off	off→off→off
		on→on→on	
1	1→0→1	off→off→off	on→off→on
		on→off→on	

- The relationship between the wake-up and pressing key is shown as below:



- As the following diagram shown, if the KS3-K0 key is kept in a pressed state before entering the standby mode, the device can not be woken up by the KS0-K0, KS1-K0 and KS2-K0 key presses.



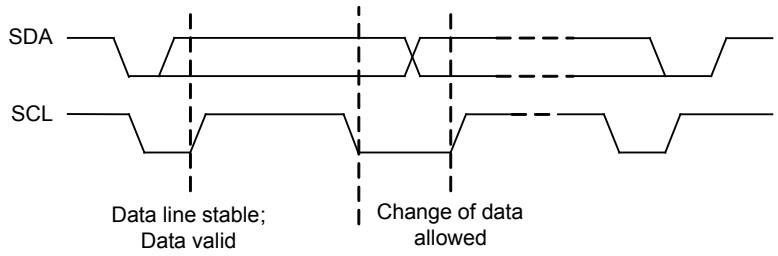
I²C Serial Interface

I²C Operation

The device supports I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7KΩ. When the bus is free, both lines are high. Devices connected to the bus must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

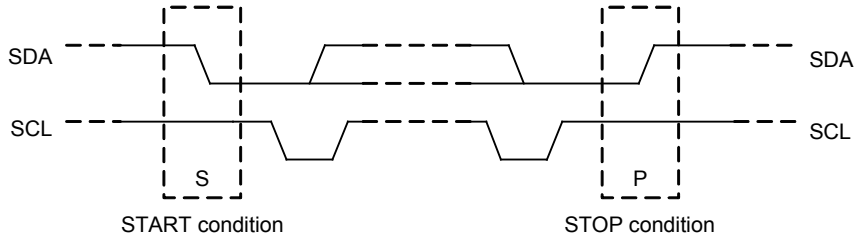
Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only change when the clock signal on the SCL line is Low as shown in the diagram.



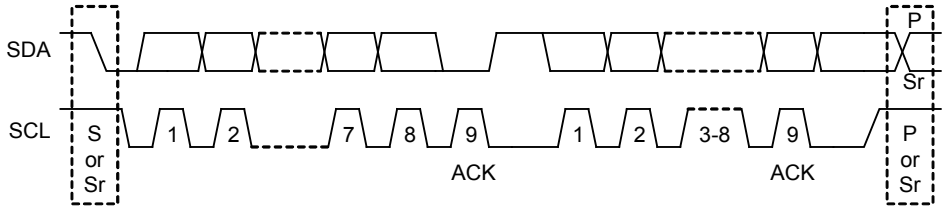
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START(S) and repeated START (Sr) conditions are functionally identical.



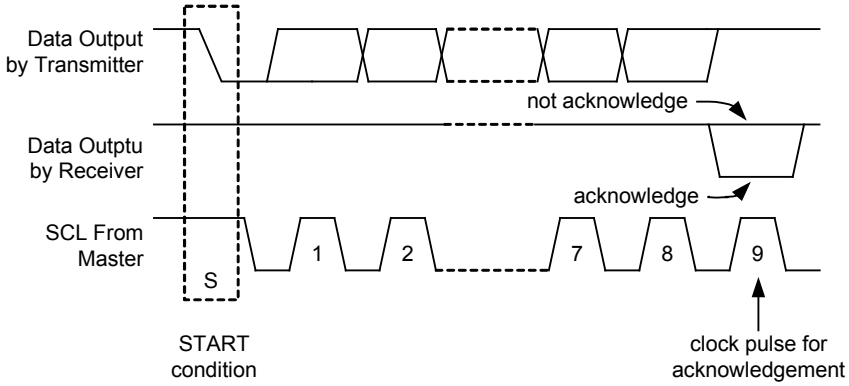
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.



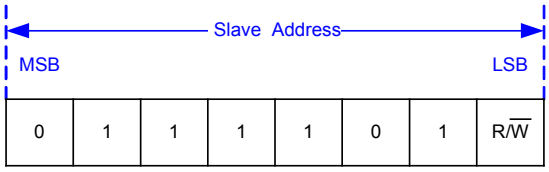
Acknowledge

- Each bytes of eight bits is followed by one acknowledge bit. This Acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an Acknowledge, ACK, after the reception of each byte.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Slave Addressing

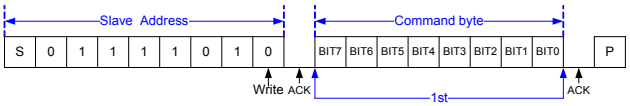
- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the R/$\overline{W}$ bit is "1", then a read operation is selected. A "0" selects a write operation.
- TheHT16LK24 address bits are "0111101". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.



I²C Interface Write Operation

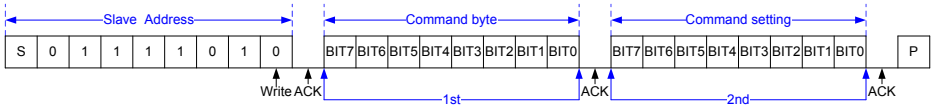
Byte Write Operation

- Single Command Type
  A Single Command write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte and a STOP condition for a single command write operation.

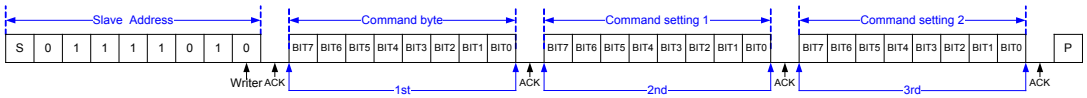


I²C Single Command Type Write Operation

- Compound Command Type
  A Compound Command write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, up to two command setting bytes and a STOP condition for a compound command write operation.

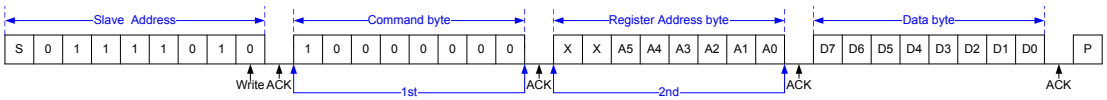


I²C Compound Command Type Write Operation – One Command Setting Byte



I²C Compound Command Type Write Operation – Two Command Setting Bytes

- Single Display RAM Data Byte
  A single display RAM data byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a display data input command byte, a valid Register Address byte, a Data byte and a STOP condition.

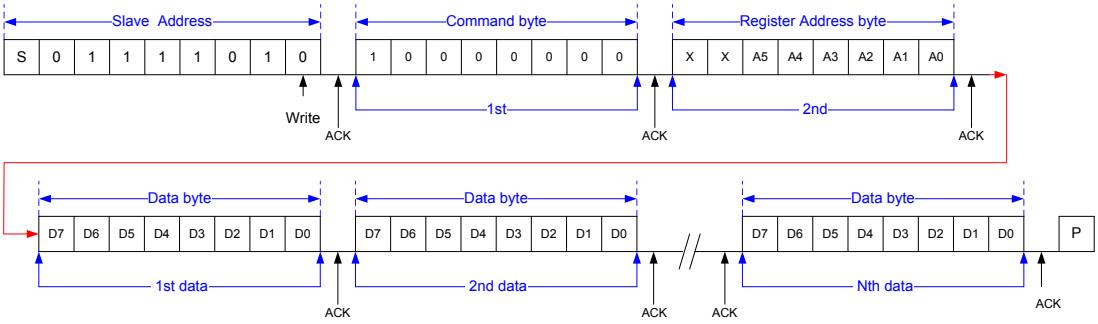


I²C Display RAM Single Data Byte Write Operation

Display RAM Page Write Operation

After a START condition the slave address with the R/$\overline{W}$ bit is placed on the bus followed with a display data input command byte and the specified display RAM Register Address of which the contents are written to the internal address pointer. The data to be written to the memory will be transmitted next and then the internal address pointer will be incremented by 1 to indicate the next memory address location after the reception of an acknowledge clock pulse. After the internal address point reaches the maximum memory address, the address pointer will be reset to 00H.

Duty	Maximum Memory Address
1/1, 1/2, 1/3, 1/4	21H
1/8	3EH

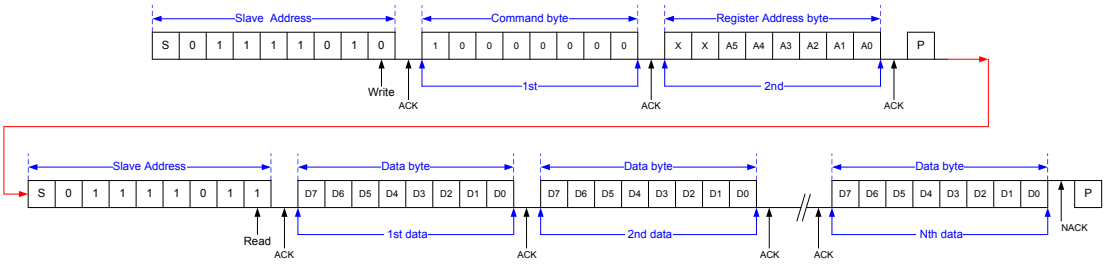


I²C Interface N Bytes Display RAM Data Write Operation

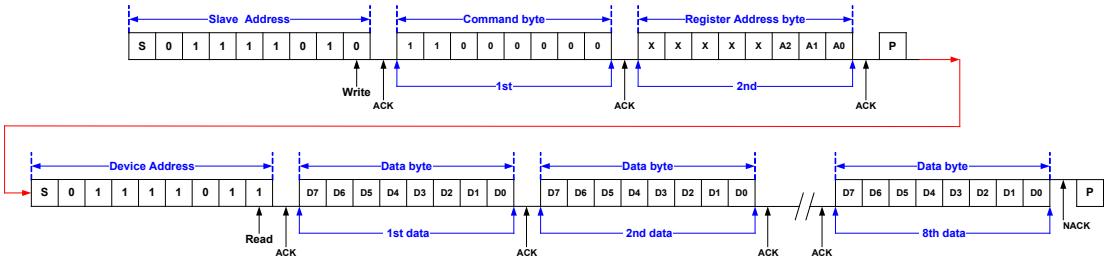
I²C Interface Read Operation – Display RAM, Key Data and INT flag

In this mode, the master reads the device data after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit, a command byte and the register address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another START condition and the slave address transferred on the bus followed by the R/$\overline{W}$ bit (="1"). Then the MSB of the data which was addressed is transmitted first on the I²C bus. The address pointer is only incremented by 1 after the reception of an acknowledge clock. That means that if the device is configured to transmit the data at the address of A_{N+1}, the master will read and acknowledge the transferred new data byte and the address pointer is incremented to A_{N+2}. After the internal address pointer reaches the maximum memory address, the address pointer will be reset to 00H.

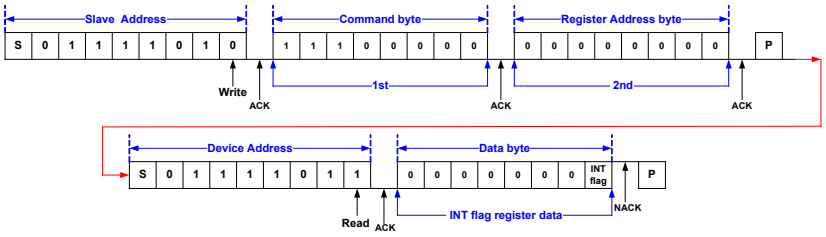
This cycle of reading consecutive addresses will continue until the master sends a STOP condition.



I²C Interface N Bytes Display RAM Data Read Operation



I²C Interface Key Data Read Operation



I²C Interface INT Flag Read Operation

SPI Serial Interface

SPI Operation

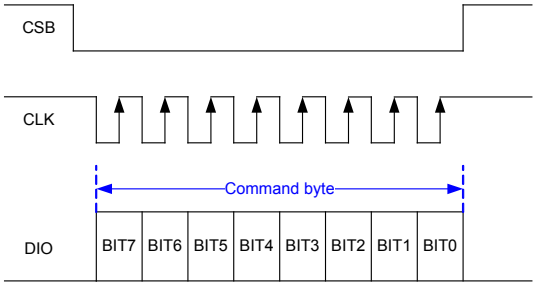
The device also includes a 3-wire SPI serial interface. The SPI operations are described as follows:

- The CSB pin is used to activate the data transfer. When the CSB pin is at a high level, the SPI operation will be reset and stopped. If the CSB pin changes state from high to low, data transmission will start.
- The data is transferred from the MSB of each byte and is shifted into the shift register during each CLK rising edge.
- The input data is automatically latched into the internal register for each 8-bit input data after the CSB signal goes low.
- For read operations, the MCU should assert a high pulse on the CSB pin to change the data transfer direction from input mode to output mode on the DIO pin after sending the command byte and the setting values. If the MCU sets the CSB signal to a high level again after receiving the output data, the data direction on the DIO pin will be changed into input mode and the read operation will end.
- For a read operation, the data is output on the DIO pin at the CLK falling edge.
- For display RAM data read/write operations using the SPI interface, the read/write control bit is contained in the Display Data Input Command. Refer to the Display Data Input Command description for more details.

SPI Interface Write Operation

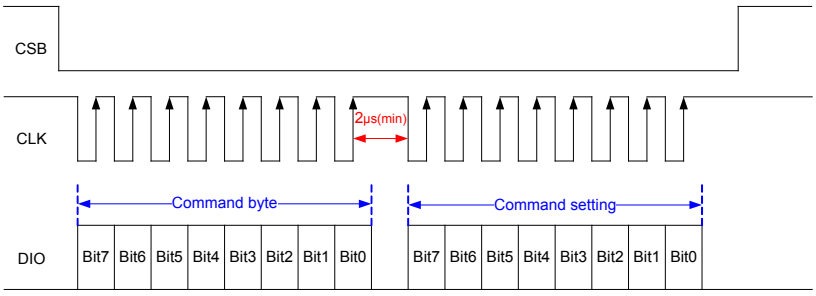
Byte Write Operation

- Single Command Type
  A Single Command write operation is activated by the CSB signal going low. The 8-bit command byte is shifted from the MSB into the shift register at each CLK rising edge.

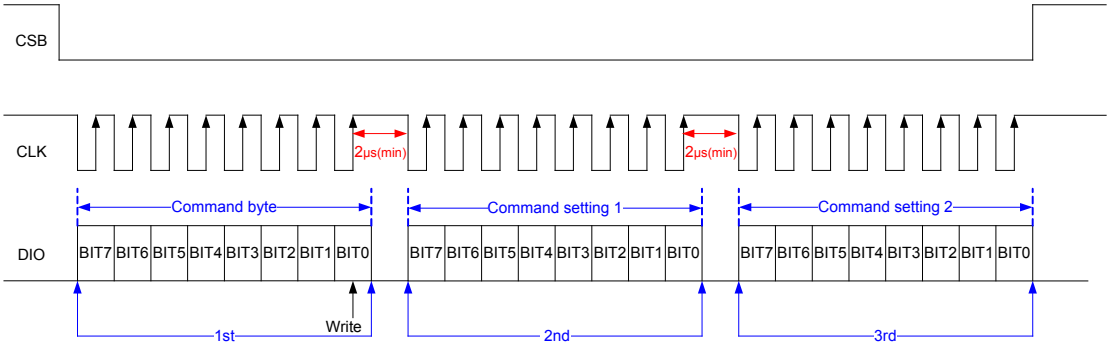


SPI Single Command Type Write Operation

- Compound Command Type
  For a compound command, an 8-bit command byte is first shifted into the shift register followed by an 8-bit command setting. Note that the CLK high pulse width, after the command byte has been shifted in, must remain at this level for at least 2μs after which the command setting data can be consecutively shifted in.

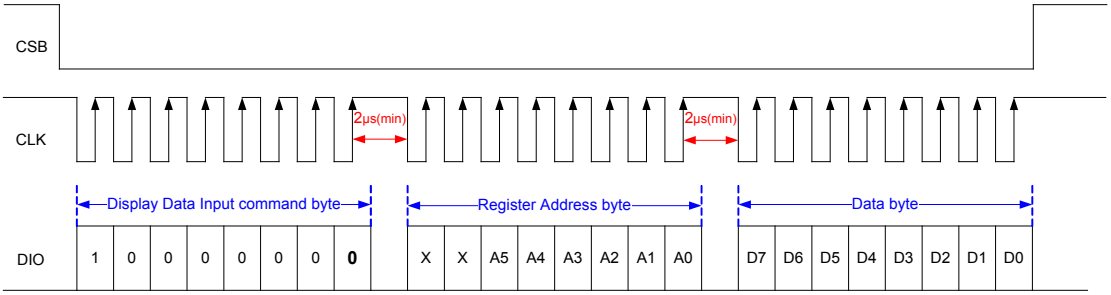


SPI Compound Command Type Write Operation – One Command Setting Byte



SPI Compound Command Type Write Operation – Two Command Setting Bytes

- Single Display RAM Data Byte
  The single display RAM data write operation consists of a display data input (write) command, a register address and a write data byte.

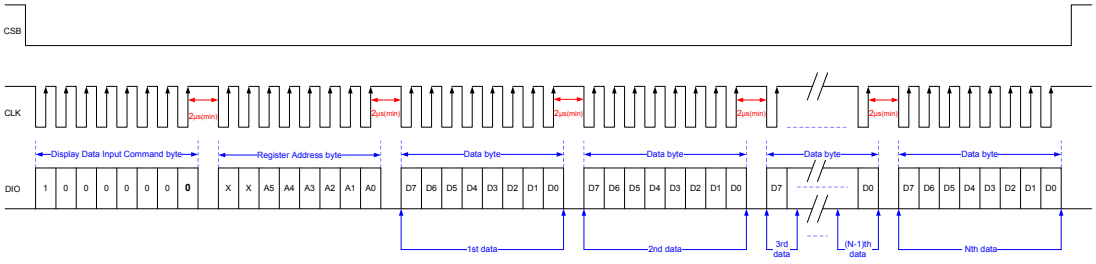


SPI Single Display RAM Data Byte Write Operation

Display RAM Page Write Operation

The display RAM Page write operation consists of a display data write command, a register address of which the contents are written to the internal address pointer followed by N bytes of written data. The data to be written to the memory will be transmitted next and then the internal address pointer will be automatically incremented by 1 to indicate the next memory address location. After the internal address point reaches the maximum memory address, the address pointer will be reset to 00H.

Duty	Maximum Memory Address
1/1, 1/2, 1/3, 1/4	21H
1/8	3EH

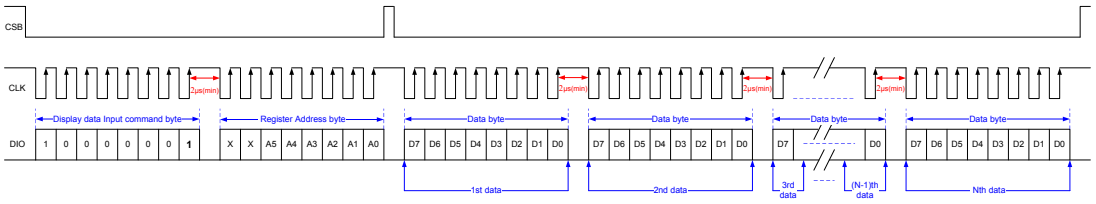


SPI Interface N Bytes Display RAM Data Write Operation

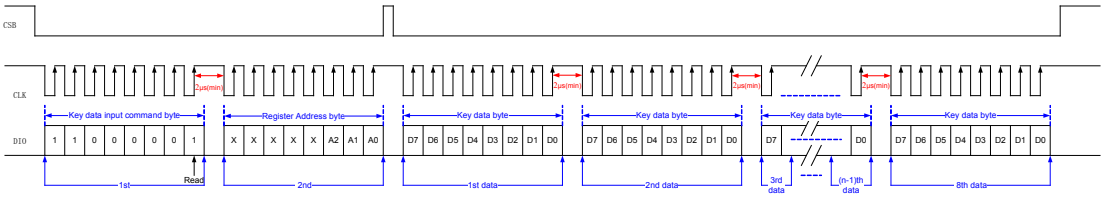
SPI Interface Read Operation – Display RAM, Key Data and INT Flag

In this mode, the master reads the HT16LK24 data after sending the Display Data Input command when the CSB pin changes state from high to low. Following the read/write control bit, which is contained in the Display Data Input command, is the register address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another CSB high pulse is placed on the bus and then the MSB of the data which was addressed is transmitted first on the SPI bus. The address pointer is only incremented by 1 after the reception of each data byte. That means that if the device is configured to transmit the data at the address of A_{N+1}, the master will read the transferred data byte and the address pointer is incremented to A_{N+2}. After the internal address pointer reaches the maximum memory address, the address pointer will be reset to 00H.

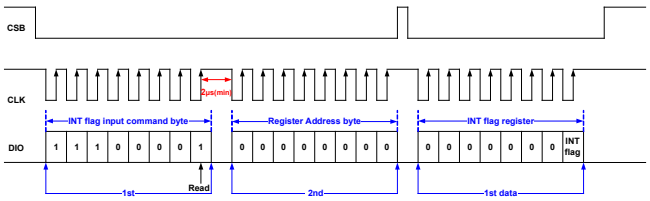
This cycle of reading consecutive addresses will continue until the master pulls the CSB line to a high level to terminate the data transfer.



SPI Interface N Bytes Display RAM Data Read Operation



SPI Interface Key Data Read Operation



SPI Interface INT Flag Read Operation

Command Summary

Software Reset Command

This command is used to initialize the device.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Soft Reset Command	1st	1	0	1	0	1	0	1	0	—	W	—

Note:

- When this software reset command is executed, all the command registers are initialized to the default values.
- After the reset command is executed, the device will experience an internal initialization for 1ms.
- Normal operation can be executed after the device initialization is complete.
- During the initialization period, no commands can be executed.
- If the programmed command is not defined, the function will not be affected.

The status of the internal circuits after initialization is as follows:

- All segment/common outputs are set to $V_{LCD.}$
- The drive mode 1/4 duty output and 1/3 bias is selected.
- The System Oscillator and the LCD bias generator are in an off state.
- The LCD Display is in an off state and the integrated regulator is disabled.
- The key scan function is disabled.
- The INT pin is set to a high level.
- The operation mode is set to normal mode.
- The Segment/KEY/LED shared pin is setup as a Segment pin.
- The Frame Frequency is set to 64Hz.
- The blinking function is switched off

Display Data Input Command

This command is used to access the display data by the MCU to the memory MAP of the device.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Display Data Input/ output Command	1st	1	0	0	0	0	0	0	0	Write operation	W	—
		1	0	0	0	0	0	0	1	Read operation for 3-wire SPI interface used only.	R	—
Address pointer	2nd	X	X	A5	A4	A3	A2	A1	A0	Display data start address of memory map	W	00H

Note:

Duty	Maximum Memory Address
1/1, 1/2, 1/3, 1/4	21H
1/8	3EH

- Power on status: the address is set to 00H
- If the programmed command is not defined, the function will not be affected.

Key Data Input Command

This command is used to access the key data by the MCU to the memory MAP of the device.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Key Data access Command	1st	1	1	0	0	0	0	0	0	Write operation	W	—
		1	1	0	0	0	0	0	1	Read operation for 3-wire SPI interface used only.	R	—
Address pointer	2nd	X	X	X	X	X	A2	A1	A0	Key data start address of memory map	W	00H

Note:

- Power on status: the address is set to 00H
- If the programmed command is not defined, the function will not be affected.

INT Flag Access Command

This command is used to access the INT flag by the MCU to the memory MAP of the device.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
INT flag access Command	1st	1	1	1	0	0	0	0	0	Write operation	W	—
		1	1	1	0	0	0	0	1	Read operation for 3-wire SPI interface used only.	R	—
Address pointer	2nd	0	0	0	0	0	0	0	0	INT flag register address, read only.	W	00H

Note:

- Power on status: the address is set to 00H
- If the programmed command is not defined, the function will not be affected.

Drive Mode Command

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Drive mode setting command	1st	1	0	0	0	0	0	1	0	—	W	—
Duty, Bias and pin-shared setting	2nd	X	Duty2	Duty1	Duty0	X	X	Bias1	Bias0	—	W	32H

Note:

Bias1	Bias0	LCD Bias
0	0	1/1 bias
0	1	1/2 bias
1	0	1/3 bias (default)
1	1	1/4 bias

Duty2	Duty1	Duty0	LCD Duty
0	0	0	1/1 duty
0	0	1	1/2 duty
0	1	0	1/3 duty
0	1	1	1/4 duty (default)
1	x	x	1/8 duty

- Power on status: The drive mode 1/4 duty output and 1/3 bias is selected and also the segment output pins are selected.
- If the programmed command is not defined, the function will not be affected.

System Mode Command

This command controls the internal system oscillator on/off and display on/off.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
System mode setting command	1st	1	0	0	0	0	1	0	0	—	W	—
System oscillator and Display on/off Setting	2nd	X	X	X	X	X	X	S	E	—	W	00H

Note:

Bit		Internal System oscillator	LCD Display
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

- Power on status: Display off and disable the internal system oscillator.
- If the programmed command is not defined, the function will not be affected.

Frame/PWM Frequency Setting Command

This command is used to select the LCD display frame frequency, the PWM frequency and the PWM level setting.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Frequency command	1st	1	0	0	0	0	1	1	0	—	W	—
Frequency setting	2nd	X	PWS	X	PF1	PF0	X	F1	F0	—	W	02H

Note:

Bit [1:0]	LCD Frame Frequency	
F1, F0	1/1, 1/2, 1/4, 1/8 duty	1/3 duty
00	85.3 Hz	91 Hz
01	170.6 Hz	182 Hz
10	64 Hz (default)	68.3 Hz (default)
11	128 Hz	136.5 Hz

Bit [4:3] PF1, PF0	PWM Frequency (f_{PWM})
00	85.3 Hz
01	128 Hz
10	170.6 Hz
11	256 Hz

PWS	PWM step selection
0	64
1	128

Note:

If the LED driver is used for back light application, it is suggested to set the PWM frequency as the following table shown to avoid from the display flicker. If the LED driver is not used for back light application, there is no limitation for the PWM frequency selection.

Frame Frequency	PWM Frequency	
	PWM step= 64 steps	PWM step =128 steps
64Hz	85.3 Hz or170.6Hz	85.3 Hz or170.6Hz
85.3Hz	128Hz or 256Hz	128Hz or 256Hz
128Hz	170.6Hz	invalid
170.6 Hz	256 Hz	invalid

- Power on status: LCD Frame frequency is set to 64Hz and PWM frequency is set to 85.3Hz.
- If the programmed command is not defined, the function will not be affected.

Blinking Frequency Command

This command defines the blinking frequency of the display modes.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Blinking Frequency command	1st	1	0	0	0	1	0	0	0	—	W	—
Blinking Frequency setting	2nd	X	X	X	X	X	X	BK1	BK0	—	W	00H

Note:

Bit		Blinking Frequency
BK1	BK0	
0	0	Blinking off (default)
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

- Power on status: Blinking function is switched off.
- If the programmed command is not defined, the function will not be affected.

Internal Voltage Adjustment (IVA) Setting Command

The internal voltage (V_{LCD}) adjustment can provide eight kinds of regulator voltage adjustment options by setting the LCD operating voltage adjustment command.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Internal Voltage Adjustment (IVA) Setting	1st	1	0	0	0	1	0	1	0	—	W	—
Internal Voltage Adjust control	2nd	X	X	X	VE	X	V2	V1	V0	—	W	00H

Note:

VE	Regulator adjustment
0	Off - bias voltage is supplied from VLCD pin (default)
1	On - bias voltage is supplied from the internal regulator

V2	V1	V0	Regulator output voltage (V)
0	0	0	3.0V
0	0	1	3.2V
0	1	0	3.3V
0	1	1	3.4V
1	0	0	4.4V
1	0	1	4.5V
1	1	0	4.6V
1	1	1	5.0V

- Power on status: disable the internal regulator.
- When the VLCD voltage is lower than 3.5V, it is recommended to disable the internal regulator so that the V_{LCD} voltage is directly connected to the internal Bias voltage generator.
- Caution: use the internal regulator when the "Regulator output voltage < V_{LCD} -0.5V "
- If the programmed command is not defined, the function will not be affected.

LED Output1 Control Command

This command defines the LED0~LED7 data and control the corresponding LED PWM dimming function.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
LED output1 control	1st	1	0	0	1	0	1	0	0	—	W	—
LEDn PWM enable control	2nd	PWEN7	PWEN6	PWEN5	PWEN4	PWEN3	PWEN2	PWEN1	PWEN0	—	W	00H
LED0~LED7 output data	3rd	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0	—	W	00H

PWENn	LEDn PWM Function Control	Note
0	Off	The LED output status will not be changed by System oscillator and LCD display On/Off control setting.
1	On	The LED output will be switched off when the device enters the standby mode and turned on again after it is woken up.

LEDn	LEDn Data
0	0 – LEDn is switched off
1	1 – LEDn is turned on

Note:

- "n" ranges from 0~7
- Power on reset status: All LED output pins are set to a high level with a voltage of V_{LCD}.
- The LED and PWM registers and latches are cleared after a new configuration is written into the KX, KY and L fields in the SEG/KSL shared pin configuration setting command.
- If the programmed command is not defined, the function will not be affected.

LED Output2 Control Command

This command defines the LED8~LED11 data and control the corresponding LED PWM dimming function.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
LED output2 control	1st	1	0	0	1	0	1	1	0	—	W	—
LEDn PWM enable control	2nd	x	x	x	x	PWEN11	PWEN10	PWEN9	PWEN8	—	W	00H
LED8~LED11 output data	3rd	x	x	x	x	LED11	LED10	LED9	LED8	—	W	00H

PWENn	LEDn PWM Function Control	Note
0	Off	The LED output status will not be changed by System oscillator and LCD display On/Off control setting.
1	On	The LED output will be switched off when the device enters the standby mode and turned on again after it is woken up.

LEDn	LEDn Data
0	0 – LEDn is switched off
1	1 – LEDn is turned on

Note:

- "n" ranges from 8~11
- Power on reset status: All LED output pins are set to a high level with a voltage of V_{LCD}.
- The LED and PWM registers and latches are cleared after a new configuration is written into the KX, KY and L fields in the SEG/KSL shared pin configuration setting command.
- If the programmed command is not defined, the function will not be affected.

SEG/KSL Shared Pin Configuration Command

This command defines the segment, Key input, Key scan output and LED pin number on the shared pins. It is recommended that the SEG/KSL shared pin configuration should be changed when the LCD display is switched off. Otherwise, the unpredictable results will occur.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Shared pin configuration	1st	1	0	0	0	1	1	1	0	—	W	—
LED pin number setting	2nd	x	x	x	x	L3	L2	L1	L0	L: LED pin setting	W	00H
Key input and Key scan output pin number setting	3rd	KX2	KX1	KX0	KY4	KY3	KY2	KY1	KY0	KX: Key output setting KY: Key input setting	W	00H

L [3:0]	LED pin number (N_{LED})	LED Pin Configuration Descriptions
0000	0	No LED pin selected
0001	1	LED0 selected
0010	2	LED0~LED1 selected
0011	3	LED0~LED2 selected
0100	4	LED0~LED3 selected
0101	5	LED0~LED4 selected
0110	6	LED0~LED5 selected
0111	7	LED0~LED6 selected
1000	8	LED0~LED7 selected
1001	9	LED0~LED8 selected
1010	10	LED0~LED9 selected
1011	11	LED0~LED10 selected
1100~1111	12	LED0~LED11 selected

KX [2:0]	Key Scan output pin number (N_{KS})	Key Scan Pin (KS) Configuration Descriptions
000	0	No KS pin selected
001	1	KS0 selected
010	2	KS0~KS1 selected
011	3	KS0~KS2 selected
100~111	4	KS0~KS3 selected

KY [4:0]	Key input pin number (N_K)	Key input Pin (K) Configuration Descriptions
00000	0	No Key input selected
00001	1	1 Key input selected
00010	2	2 Key input selected
00011	3	3 Key input selected
00100	4	4 Key input selected
00101	5	5 Key input selected
00110	6	6 Key input selected
00111	7	7 Key input selected
01000	8	8 Key input selected
01001	9	9 Key input selected
01010	10	10 Key input selected
01011	11	11 Key input selected
01100	12	12 Key input selected
01101	13	13 Key input selected
01110	14	14 Key input selected
01111	15	15 Key input selected
10000~11111	16	16 Key input selected

Note:

- The maximum SEG/KSL shared pin number is 16, i.e., (N_{LED}+N_{KS}+N_K+N_{SEG}) = 16.
  N_{SEG}: Segment pin number, up to 16.
  N_K: Key input pin number, up to 16.
  N_{KS}: Key scan output pin number, up to 4.
  N_{LED}: LED output pin number, up to 12.
- The pin-shared function priority: LED > Key Scan output > Key input > Segment output.
- The LED data and Key data are cleared and INT output is changed to its inactive level after a new configuration is written into the KX, KY or L field in the SEG/KSL shared pin configuration setting command.
- Power on reset status: The shared pin is set as a segment output pin.
- If the programmed command is not defined, the function will not be affected

• SEG/KSL Shared Pin Configuration example:

Shared pins Configuration setting			SEG / KSL Shared pins															
Key Input/Output number setting		LED number setting																
KX [2:0]	KY [4:0]	L [3:0]	Seg51_ KSL15	Seg52_ KSL14	Seg53_ KSL13	Seg54_ KSL12	Seg55_ KSL11	Seg56_ KSL10	Seg57_ KSL9	Seg58_ KSL8	Seg59_ KSL7	Seg60_ KSL6	Seg61_ KSL5	Seg62_ KSL4	Seg63_ KSL3	Seg64_ KSL2	Seg65_ KSL1	Seg66_ KSL0
000b	00000b	0000b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63	Seg64	Seg65	Seg66
000b	00000b	0001b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63	Seg64	Seg65	LED0
000b	00000b	0010b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63	Seg64	LED1	LED0
000b	00000b	0011b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63	LED2	LED1	LED0
000b	00000b	0100b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	LED3	LED2	LED1	LED0
000b	00000b	0101b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	LED4	LED3	LED2	LED1	LED0
000b	00000b	0110b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	LED5	LED4	LED3	LED2	LED1	LED0
000b	00000b	0111b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	LED6	LED5	LED4	LED3	LED2	LED1	LED0
000b	00000b	1000b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
000b	00000b	1001b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
000b	00000b	1010b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
000b	00000b	1011b	Seg51	Seg52	Seg53	Seg54	Seg55	LED10	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
000b	00000b	1100b	Seg51	Seg52	Seg53	Seg54	LED11	LED10	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
100b	00100b	0100b	Seg51	Seg52	Seg53	Seg54	K11	K10	K9	K8	KS3	KS2	KS1	KS0	LED3	LED2	LED1	LED0
100b	01000b	0100b	K15	K14	K13	K12	K11	K10	K9	K8	KS3	KS2	KS1	KS0	LED3	LED2	LED1	LED0
000b	01100b	0100b	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	LED3	LED2	LED1	LED0
001b	00111b	1000b	K15	K14	K13	K12	K11	K10	K9	KS0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
010b	00110b	1000b	K15	K14	K13	K12	K11	K10	KS1	KS0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
011b	00101b	1000b	K15	K14	K13	K12	K11	KS2	KS1	KS0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
100b	00100b	1000b	K15	K14	K13	K12	KS3	KS2	KS1	KS0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
000b	01000b	1000b	K15	K14	K13	K12	K11	K10	K9	K8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
001b	00011b	1100b	K15	K14	K13	KS0	LED11	LED10	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
010b	00010b	1100b	K15	K14	KS1	KS0	LED11	LED10	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
011b	00001b	1100b	K15	KS2	KS1	KS0	LED11	LED10	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
000b	00100b	1100b	K15	K14	K13	K12	LED11	LED10	LED9	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
001b	01111b	0000b	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	KS0
010b	01110b	0000b	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	KS1	KS0
011b	01101b	0000b	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	KS2	KS1	KS0
100b	01100b	0000b	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	KS3	KS2	KS1	KS0
100b	00100b	0000b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	K7	K6	K5	K4	KS3	KS2	KS1	KS0
000b	01000b	0000b	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	K7	K6	K5	K4	K3	K2	K1	K0
000b	10000b	0000b	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0

Key Scan Control Command

This command defines the INT pin polarity and Key scan pulse width.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Key scan control command	1st	1	0	0	1	0	0	0	0	—	W	—
Key scan pulse setting	2nd	POL	x	x	x	x	x	KF1	KF0	—	W	01H

The KF field is used to define the Key scan pulse width.

KF1	KF0	Key Scan Pulse Width (t_{KPW})	Key Scan Cycle (t_{KCT})	Key Press De-bounce Time (t_{KCT})
0	0	1 ms	4 ms	4 ms ~ 8 ms
0	1	2 ms	8 ms	8 ms ~ 16 ms
1	0	3 ms	12 ms	12 ms ~ 16 ms
1	1	4 ms	16 ms	16 ms ~ 32 ms

The POL bit is used to define the INT output pin polarity.

POL	INT Output Pin Polarity
0	Active Low
1	Active High

Note:

- Power on reset status: The key scan pulse width is set to 2 ms and the INT output level is set to high.
- If the programmed command is not defined, the function will not be affected.

LED PWM Luminance Control Command

This command is used to select the LED output pin and define the corresponding LED PWM luminance duty.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
LED PWM Luminance control command	1st	1	0	0	1	0	0	1	0	—	W	—
LED PWM output selection	2nd	x	x	x	x	LS3	LS2	LS1	LS0	—	W	00H
PWM dimming value	3rd	x	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0	—	W	00H

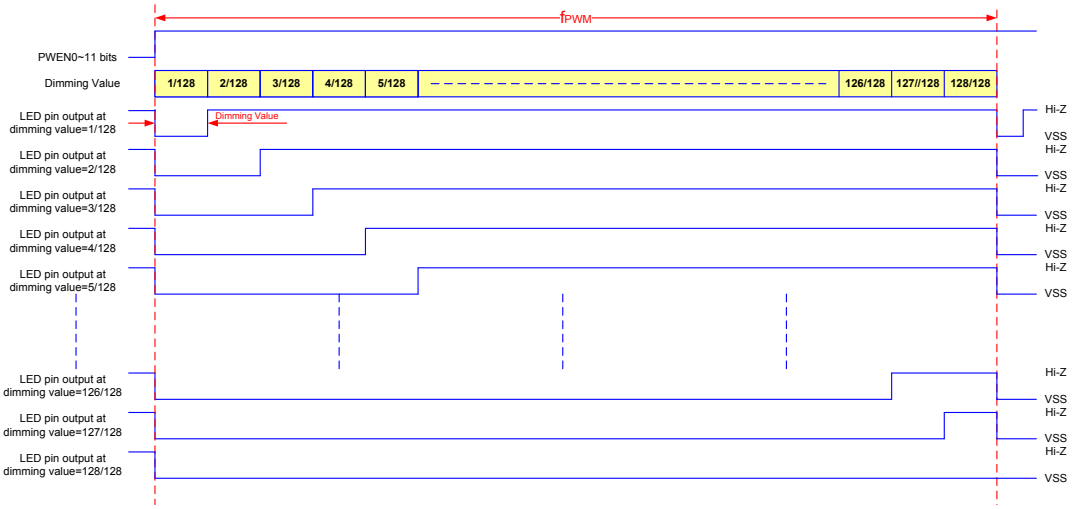
The LS field is used to select the LED output pin with the PWM luminance function as the relevant PWM function is enabled.

LS [3:0]	LED Output Selected
0000	LED0
0001	LED1
0010	LED2
0011	LED3
0100	LED4
0101	LED5
0110	LED6
0111	LED7
1000	LED8
1001	LED9
1010	LED10
1011	LED11
1100~1111	Invalid

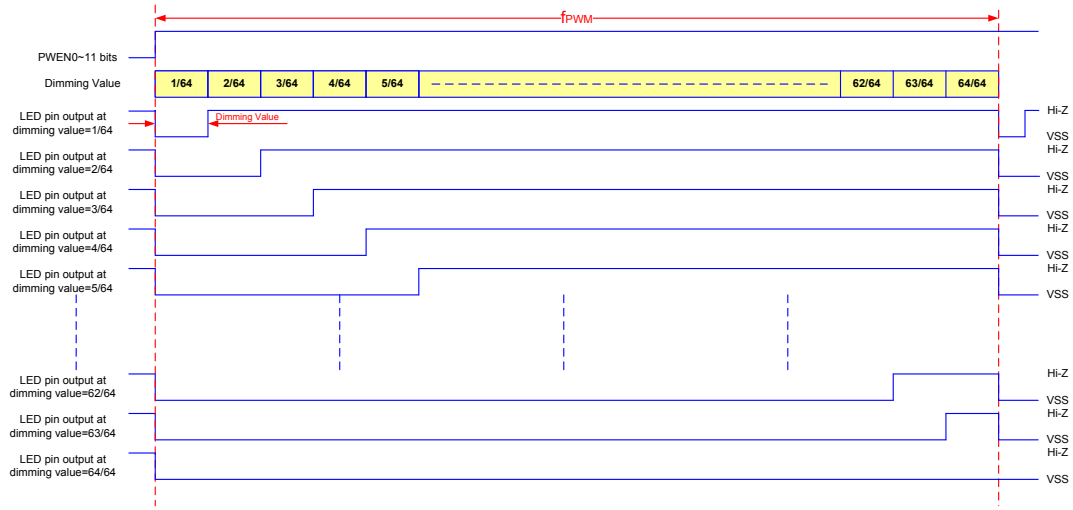
The PWM field is used to define the selected LED output PWM dimming value.

PWM [6:0]	Dimming Values	Note
0000000	1/128	Lowest LED luminance.
0000001	2/128	—
0000010	3/128	—
0000011	4/128	—
0000100	5/128	—
:	:	:
0111101	62/128	—
0111110	63/128	—
0111111	64/128	Highest LED luminance for 64-step PWM setting.
1000000	65/128	—
1000001	66/128	—
:	:	:
1111100	125/128	
1111101	126/128	
1111110	127/128	
1111111	128/128	Highest LED luminance for 128-step PWM setting.

If the PWM dimming level is set as 64 steps, the PWM6 bit has no effect on changing the PWM dimming value.



128-step PWM Dimming level



64-step PWM Dimming level

Note: 1. The LED0~LED11 data bits in the LED output control command are set to 1 in the above diagram.

2. The "Hi-Z" notation means that the relevant LED pin is in an NMOS open-drain status.

Note:

- Power on reset status: The dimming value is set to 00H.
- If the programmed command is not defined, the function will not be affected.

LCD Driving Current Control Command

This command is used to Select the Current mode according to the characteristics of the LCD panel for achieving high display quality.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
LCD driving current control	1st	1	0	0	1	1	0	0	0	—	W	—
Current mode select	2nd	0	0	0	0	0	P2	P1	P0	—	W	01H

The P field is used to select the LCD charge current.

P [2:0]	Current mode	Current consumption (I_{LCD1})
000	High current	X 1.8
001	Normal current	X 1.0 (default)
010	Low current 1	X 0.67
011	Low current 2	X 0.50

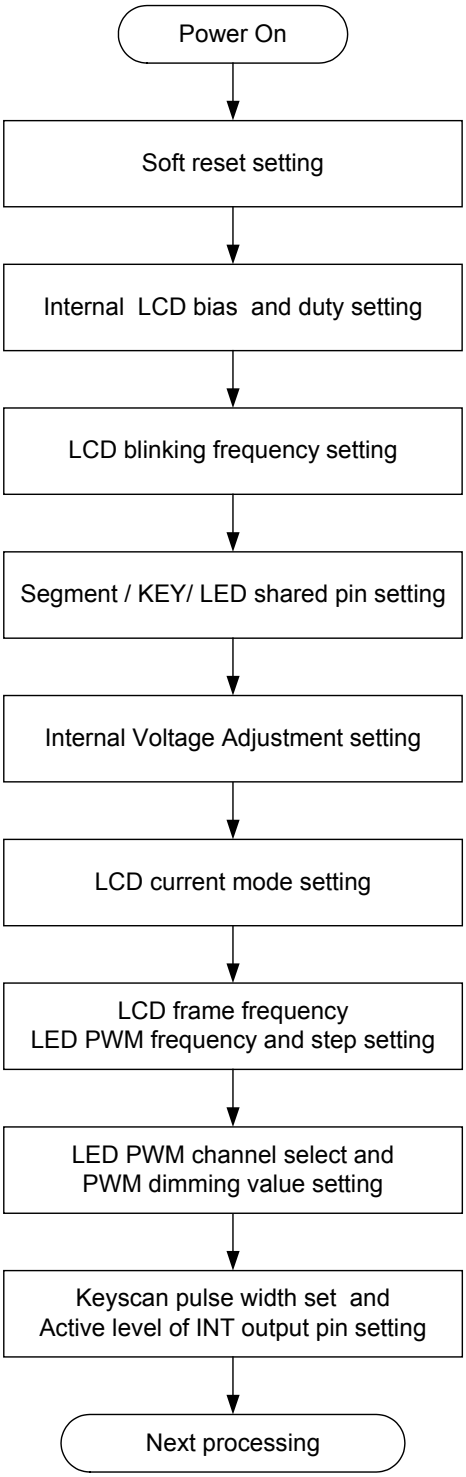
Note:

- Power on reset status: normal current mode.
- If the programmed command is not defined, the function will not be affected.

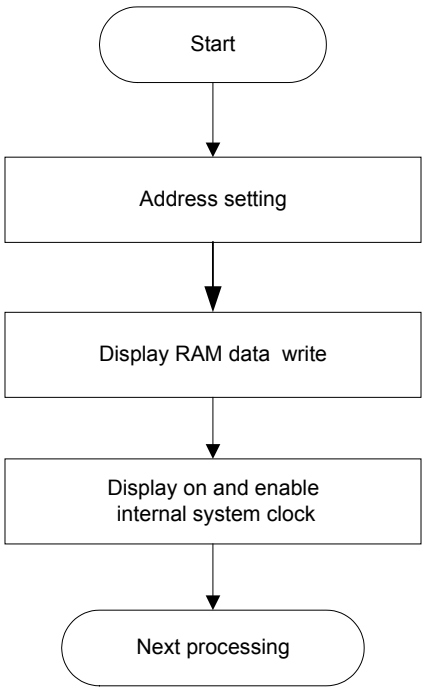
Operation Flow Chart

Access procedures are illustrated below using flowcharts.

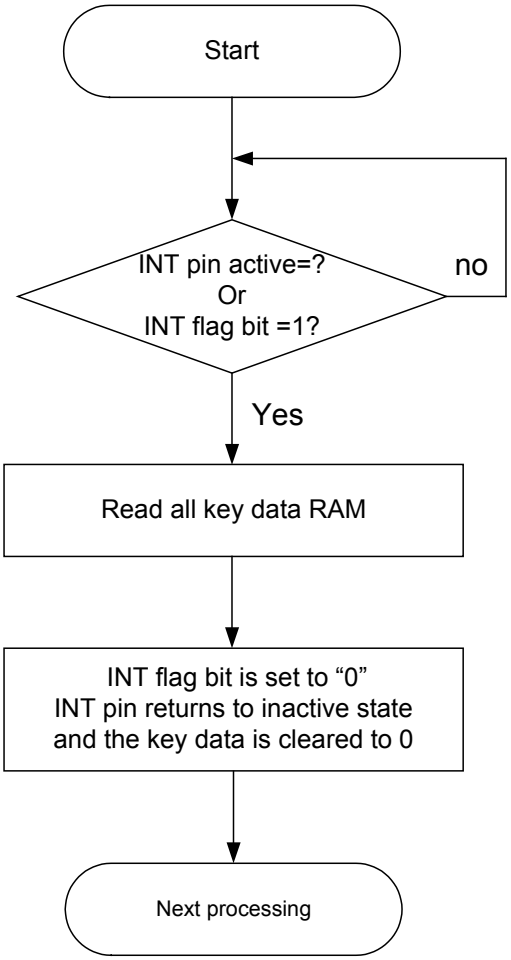
Initialization



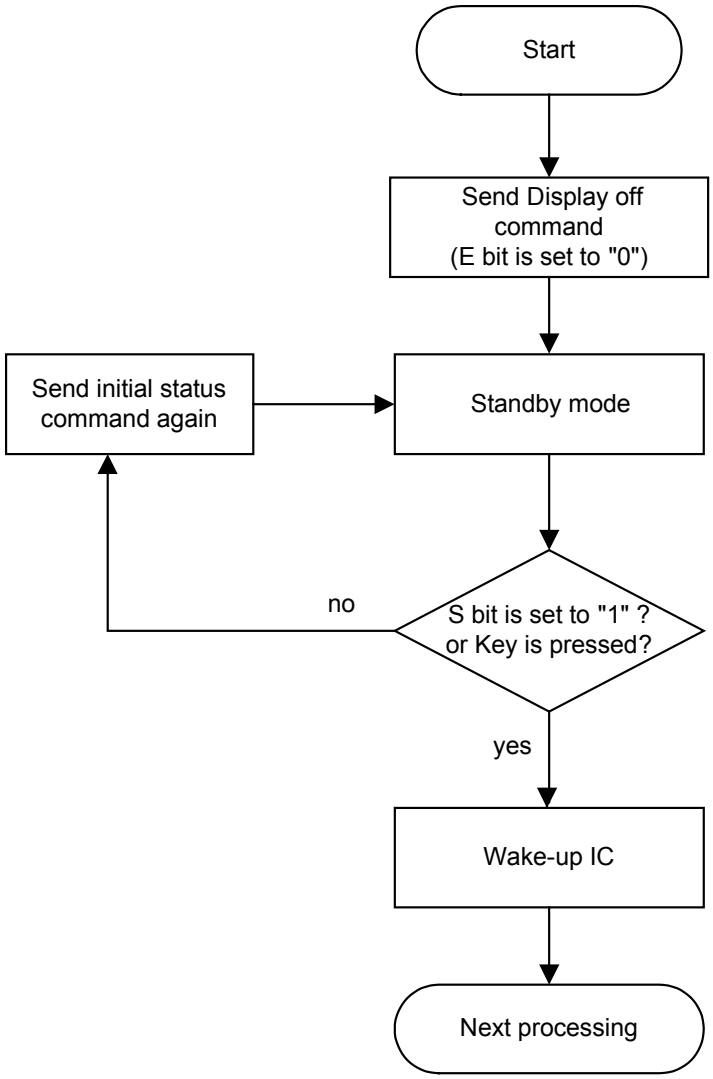
Display Data Write (Address Setting)



Key Data Read



Standby Mode Setting



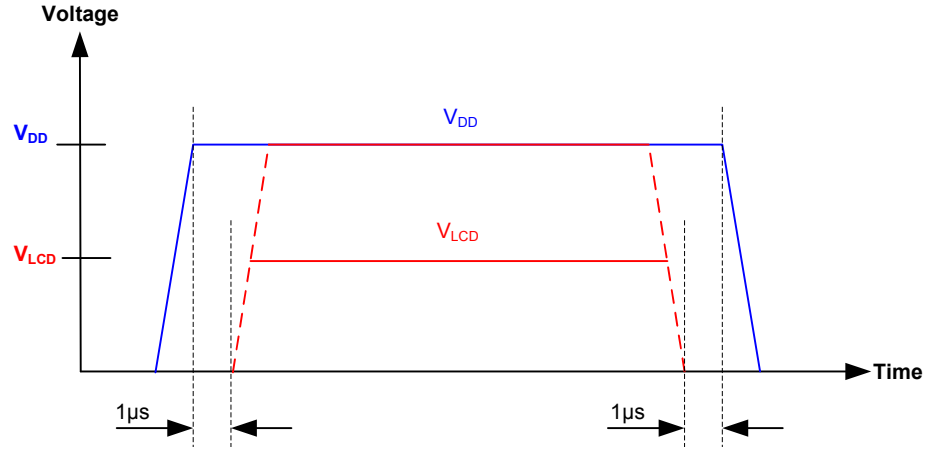
Power Supply Sequence

- If the power is individually supplied on the LCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

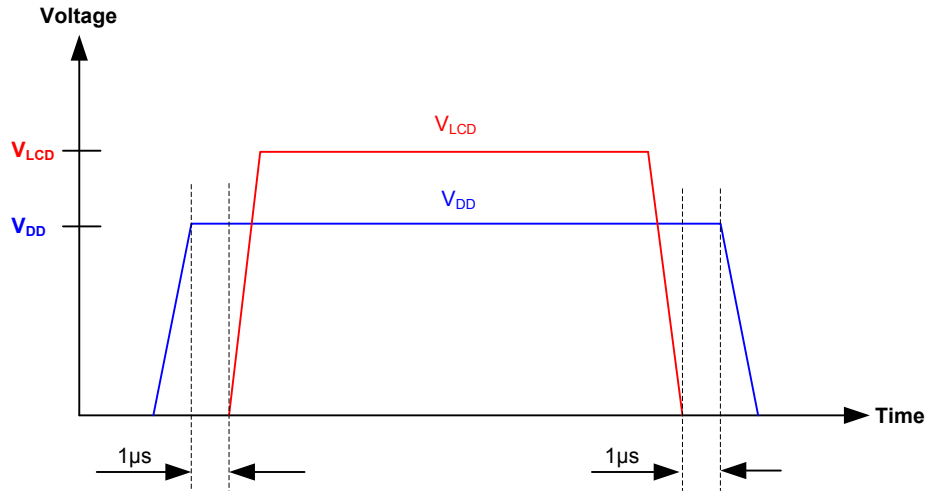
Holtek Power Supply Sequence Requirement:

1. Power-on sequence:
   Turn on the logic power supply V_{DD} first and then turn on the LCD driver power supply V_{LCD}.
2. Power-off sequence:
   Turn off the LCD driver power supply V_{LCD}. First and then turn off the logic power supply V_{DD}.
3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the V_{LCD} voltage is higher than the V_{DD} voltage.

- When the V_{LCD} voltage is smaller than or is equal to V_{DD} voltage application



- When the V_{LCD} voltage is greater than V_{DD} voltage application



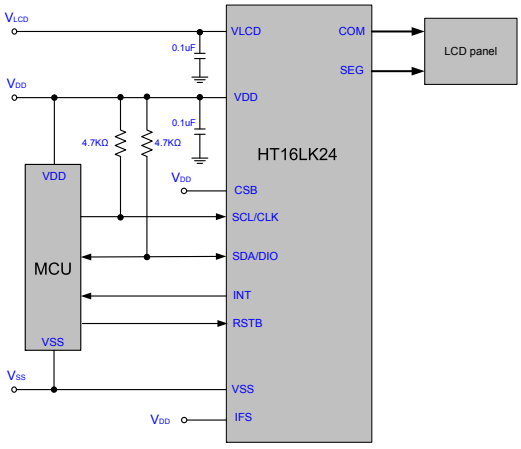
Application Circuit

(1) The SEG/KSL shared pin configuration is 16 segment outputs.

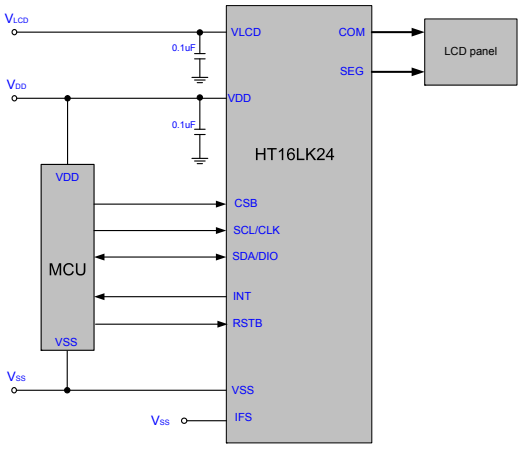
Shared Pins Configuration Setting Command			Duty	Key Circuit		LED Output	COM Output	SEG Output	LCD panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM Output	SEG Output
000b	00000b	0000b	1/1	none	none	none	COM0	SEG0~66	COM0	SEG0~66
			1/2	none	none	none	COM0~1	SEG0~66	COM0~1	SEG0~66
			1/3	none	none	none	COM0~2	SEG0~66	COM0~2	SEG0~66
			1/4	none	none	none	COM0~3	SEG0~66	COM0~3	SEG0~66
			1/8	none	none	none	COM0~7	SEG4~66	COM0~7	SEG0~62

- The RSTB pin is connected to a MCU

I²C Interface:

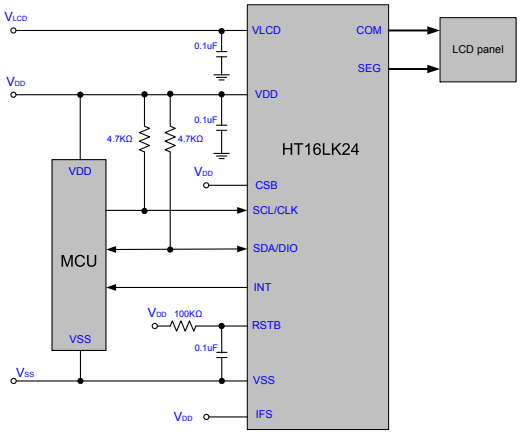


SPI 3-wire Interface:

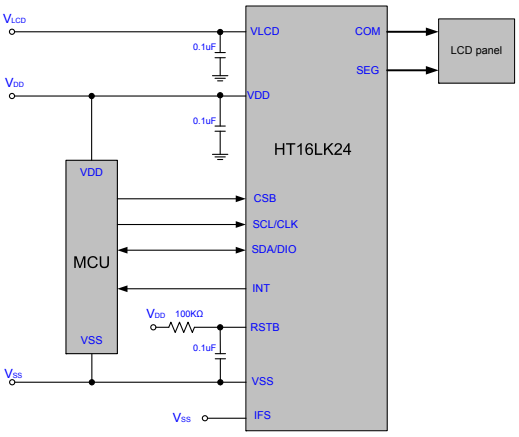


- RSTB pin is connected to external resistor and capacitor.

I²C Interface:



SPI 3-wire Interface:



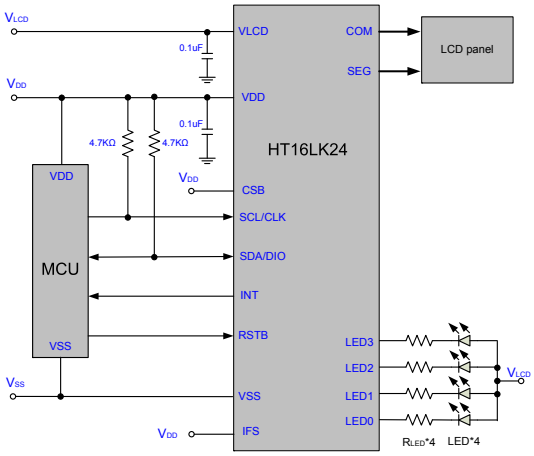
Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

(2) The SEG/KSL shared pin configuration is 12 segment outputs and 4 LED outputs.

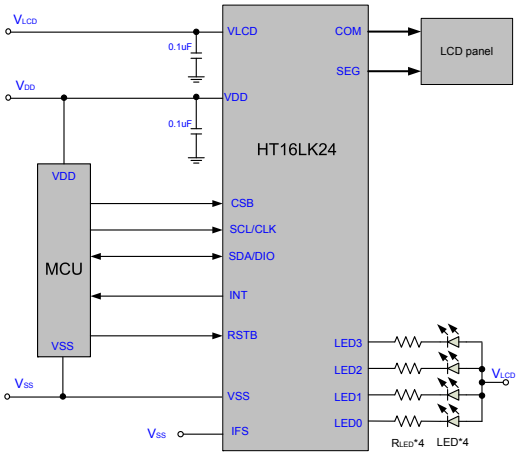
Shared pins Configuration setting command			Duty	Key circuit		LED output	COM output	SEG output	LCD panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM output	SEG output
000b	00000b	0100b	1/1	none	none	LED0~3	COM0	SEG0~62	COM0	SEG0~62
			1/2	none	none	LED0~3	COM0~1	SEG0~62	COM0~1	SEG0~62
			1/3	none	none	LED0~3	COM0~2	SEG0~62	COM0~2	SEG0~62
			1/4	none	none	LED0~3	COM0~3	SEG0~62	COM0~3	SEG0~62
			1/8	none	none	LED0~3	COM0~7	SEG4~62	COM0~7	SEG0~58

- The RSTB pin is connected to a MCU.

I²C Interface:

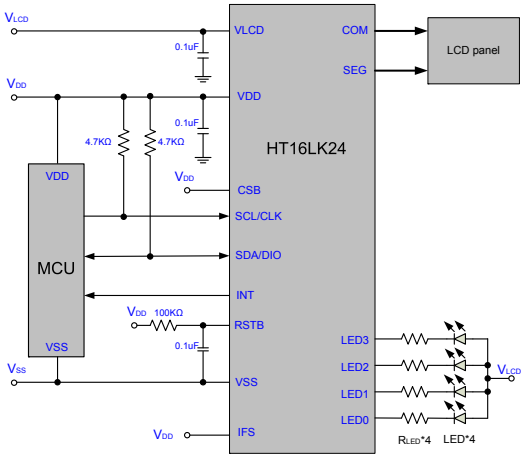


SPI 3-wire Interface:

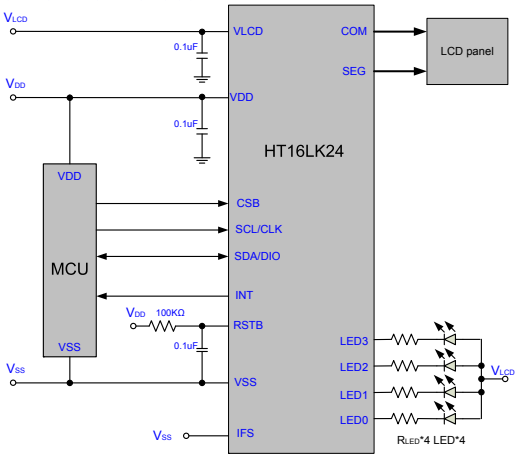


- The RSTB pin is connected to external resistor and capacitor.

I²C Interface:



SPI 3-wire Interface:



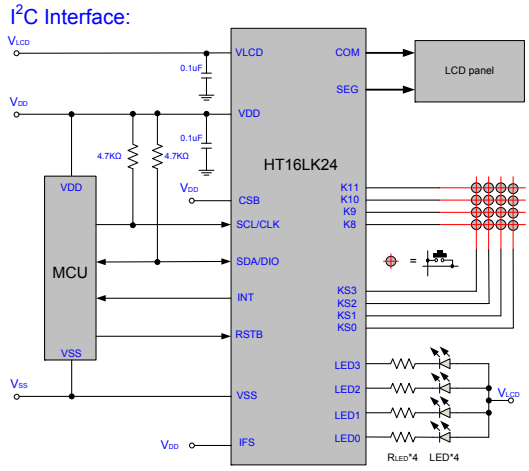
Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

(3) The SEG/KSL shared pin configuration is 4 segment outputs, 4 LED outputs, 4 key scan outputs and 4 key inputs.

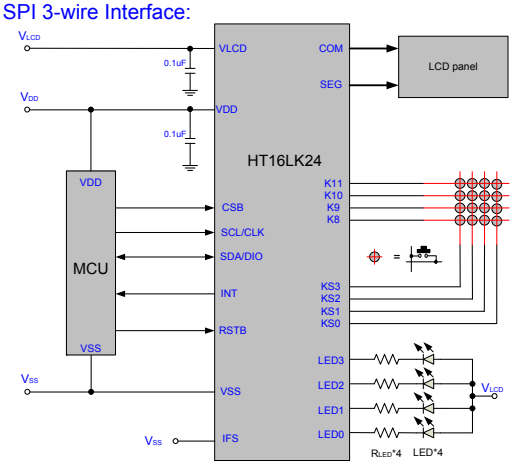
Shared Pins Configuration Setting Command			Duty	Key Circuit		LED Output	COM Output	SEG Output	LCD Panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM Output	SEG Output
100b	00100b	0100b	1/1	KS0~3	K8~11	LED0~3	COM0	SEG0~54	COM0	SEG0~54
			1/2	KS0~3	K8~11	LED0~3	COM0~1	SEG0~54	COM0~1	SEG0~54
			1/3	KS0~3	K8~11	LED0~3	COM0~2	SEG0~54	COM0~2	SEG0~54
			1/4	KS0~3	K8~11	LED0~3	COM0~3	SEG0~54	COM0~3	SEG0~54
			1/8	KS0~3	K8~11	LED0~3	COM0~7	SEG4~54	COM0~7	SEG0~50

- The RSTB pin is connected to a MCU.

I²C Interface:

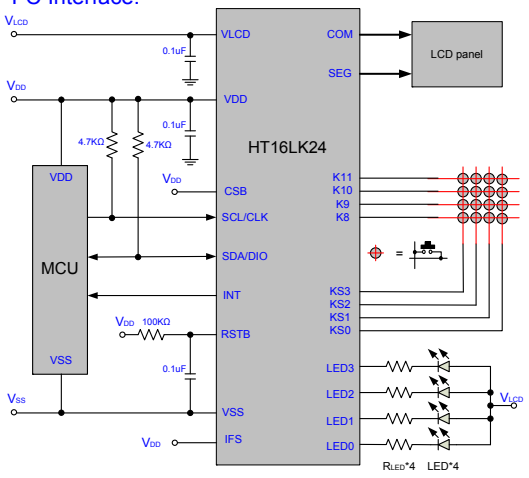


SPI 3-wire Interface:

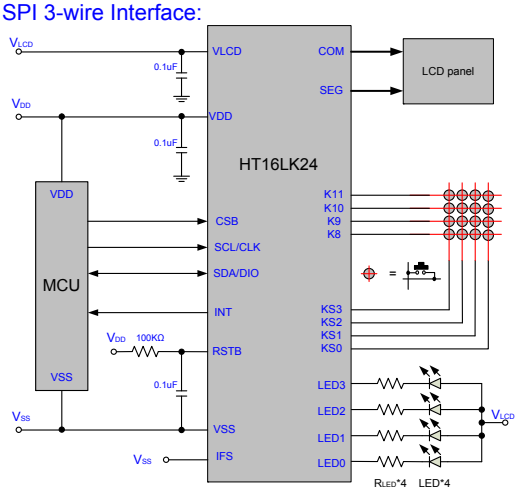


- The RSTB pin is connected to external resistor and capacitor.

I²C Interface:



SPI 3-wire Interface:



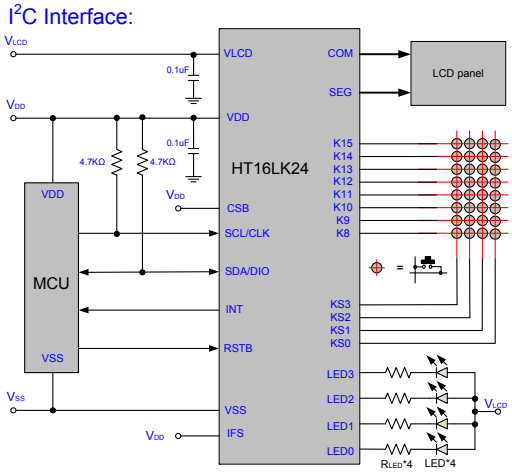
Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

(4) The SEG/KSL shared pin configuration is 4 LED outputs, 4 key scan outputs and 8 key inputs.

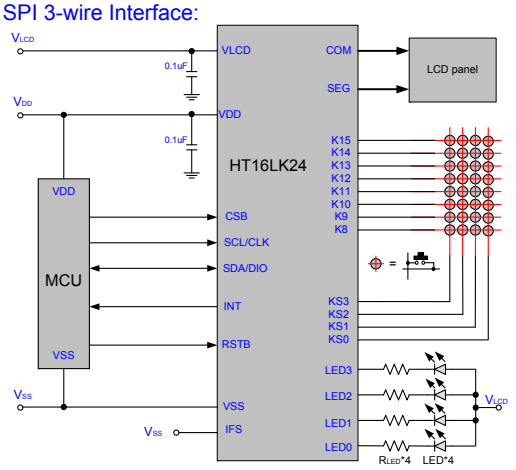
Shared pins Configuration setting command			Duty	Key circuit		LED output	COM output	SEG output	LCD panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM output	SEG output
100b	01000b	0100b	1/1	KS0~3	K8~K15	LED0~3	COM0	SEG0~50	COM0	SEG0~50
			1/2	KS0~3	K8~K15	LED0~3	COM0~1	SEG0~50	COM0~1	SEG0~50
			1/3	KS0~3	K8~K15	LED0~3	COM0~2	SEG0~50	COM0~2	SEG0~50
			1/4	KS0~3	K8~K15	LED0~3	COM0~3	SEG0~50	COM0~3	SEG0~50
			1/8	KS0~3	K8~K15	LED0~3	COM0~7	SEG4~50	COM0~7	SEG0~46

- The RSTB pin is connected to a MCU.

I²C Interface:

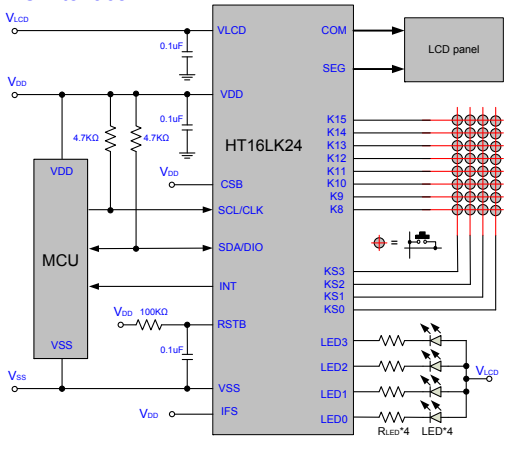


SPI 3-wire Interface:

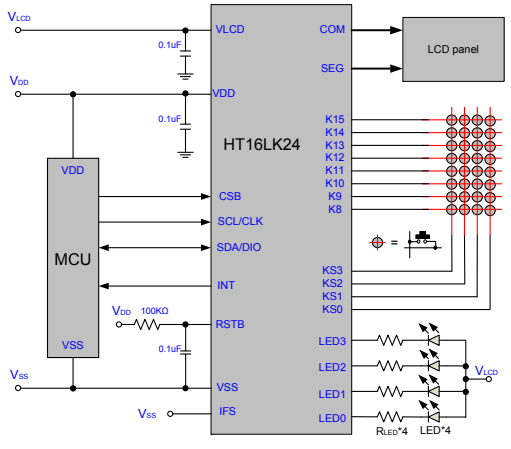


- The RSTB pin is connected to external resistor and capacitor.

I²C Interface:



SPI 3-wire Interface:



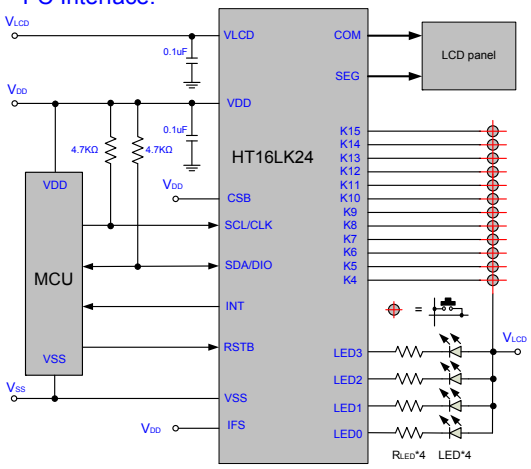
Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

(5) The SEG/KSL shared pin configuration is 4 LED outputs and 12 key inputs.

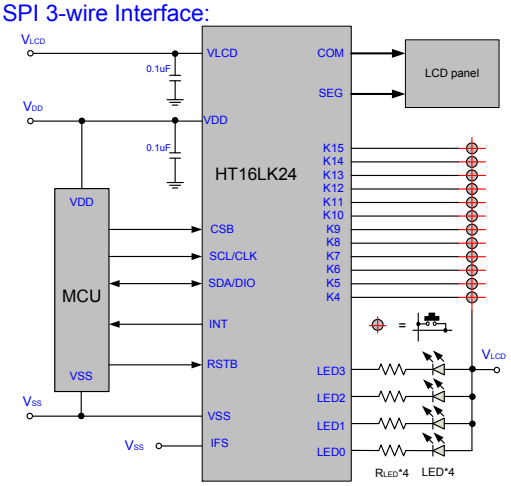
Shared pins Configuration setting command			Duty	Key circuit		LED output	COM output	SEG output	LCD panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM output	SEG output
000b	01100b	0100b	1/1	none	K4~K15	LED0~3	COM0	SEG0~50	COM0	SEG0~50
			1/2	none	K4~K15	LED0~3	COM0~1	SEG0~50	COM0~1	SEG0~50
			1/3	none	K4~K15	LED0~3	COM0~2	SEG0~50	COM0~2	SEG0~50
			1/4	none	K4~K15	LED0~3	COM0~3	SEG0~50	COM0~3	SEG0~50
			1/8	none	K4~K15	LED0~3	COM0~7	SEG4~50	COM0~7	SEG0~46

- The RSTB pin is connected to a MCU.

I²C Interface:

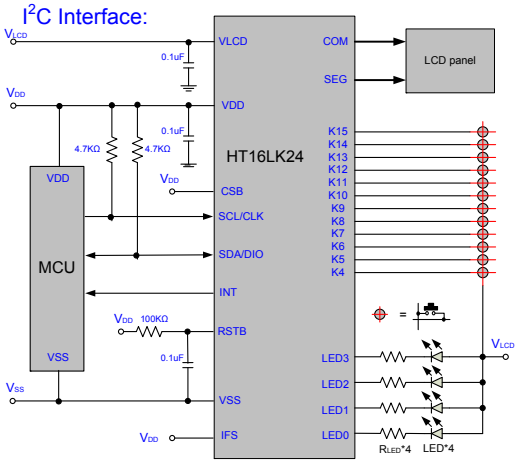


SPI 3-wire Interface:

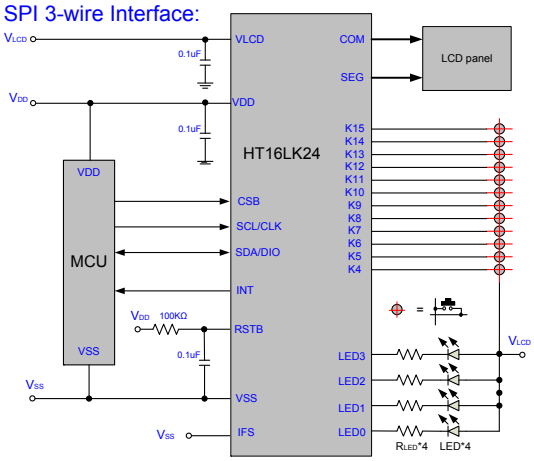


- The RSTB pin is connected to external resistor and capacitor.

I²C Interface:



SPI 3-wire Interface:



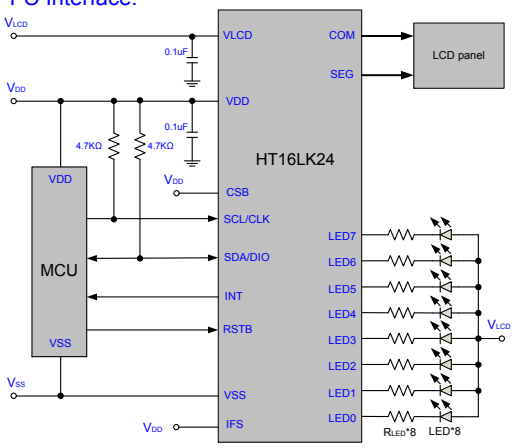
Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

(6) The SEG/KSL shared pin configuration is 8 segment outputs and 8 LED outputs.

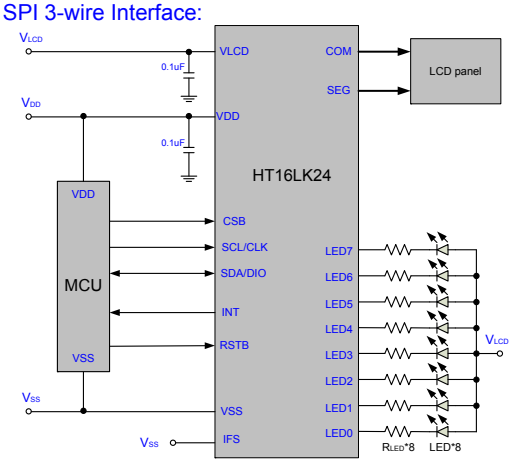
Shared pins Configuration setting command			Duty	Key circuit		LED output	COM output	SEG output	LCD panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM output	SEG output
000b	00000b	1000b	1/1	none	none	LED0~7	COM0	SEG0~58	COM0	SEG0~58
			1/2	none	none	LED0~7	COM0~1	SEG0~58	COM0~1	SEG0~58
			1/3	none	none	LED0~7	COM0~2	SEG0~58	COM0~2	SEG0~58
			1/4	none	none	LED0~7	COM0~3	SEG0~58	COM0~3	SEG0~58
			1/8	none	none	LED0~7	COM0~7	SEG4~58	COM0~7	SEG0~54

- The RSTB pin is connected to a MCU.

I²C Interface:

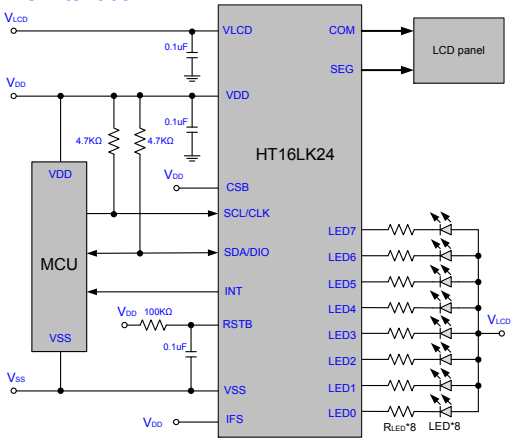


SPI 3-wire Interface:

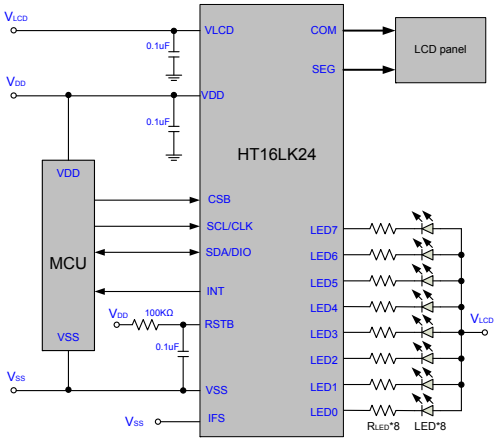


- The RSTB pin is connected to external resistor and capacitor.

I²C Interface:



SPI 3-wire Interface:



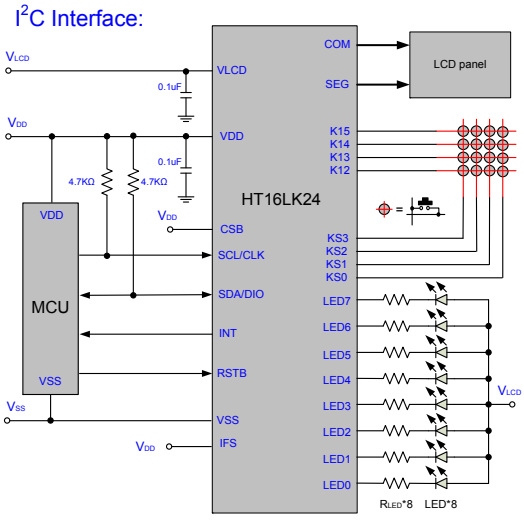
Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

(7) The SEG/KSL shared pin configuration is 8 LED outputs, 4 key scan outputs and 4 key inputs.

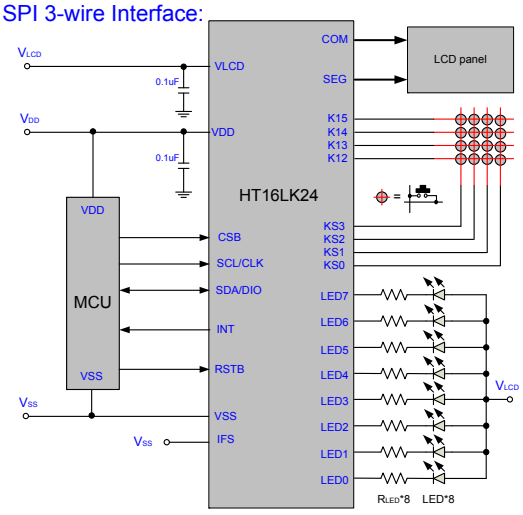
Shared pins Configuration setting command			Duty	Key circuit		LED output	COM output	SEG output	LCD panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM output	SEG output
100b	00100b	1000b	1/1	KS0~3	K12~15	LED0~7	COM0	SEG0~50	COM0	SEG0~50
			1/2	KS0~3	K12~15	LED0~7	COM0~1	SEG0~50	COM0~1	SEG0~50
			1/3	KS0~3	K12~15	LED0~7	COM0~2	SEG0~50	COM0~2	SEG0~50
			1/4	KS0~3	K12~15	LED0~7	COM0~3	SEG0~50	COM0~3	SEG0~50
			1/8	KS0~3	K12~15	LED0~7	COM0~7	SEG4~50	COM0~7	SEG0~46

- The RSTB pin is connected to a MCU.

I²C Interface:

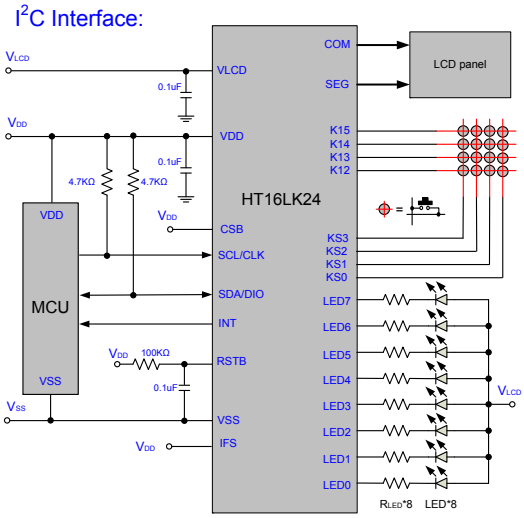


SPI 3-wire Interface:

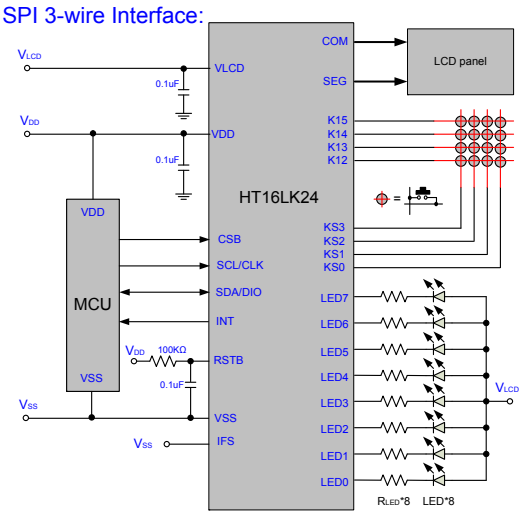


- The RSTB pin is connected to external resistor and capacitor.

I²C Interface:



SPI 3-wire Interface:

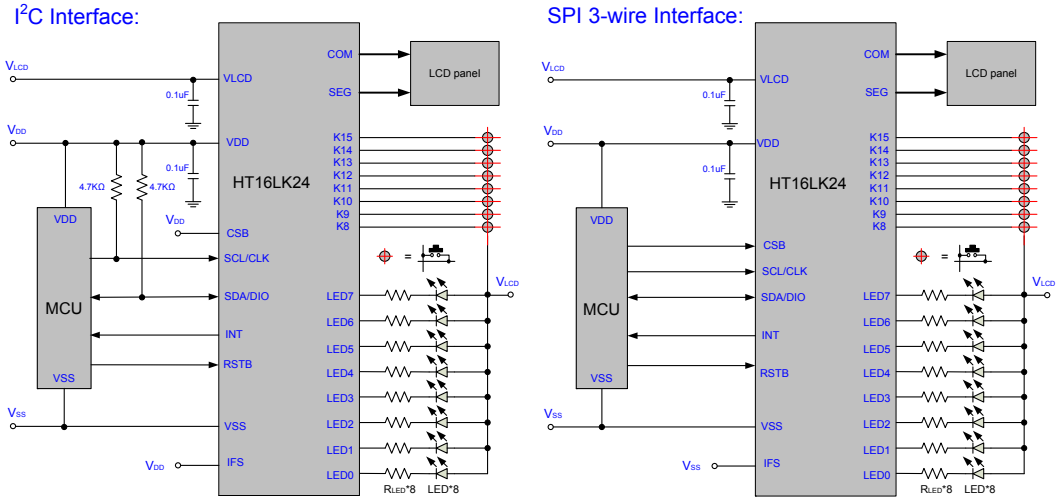


Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

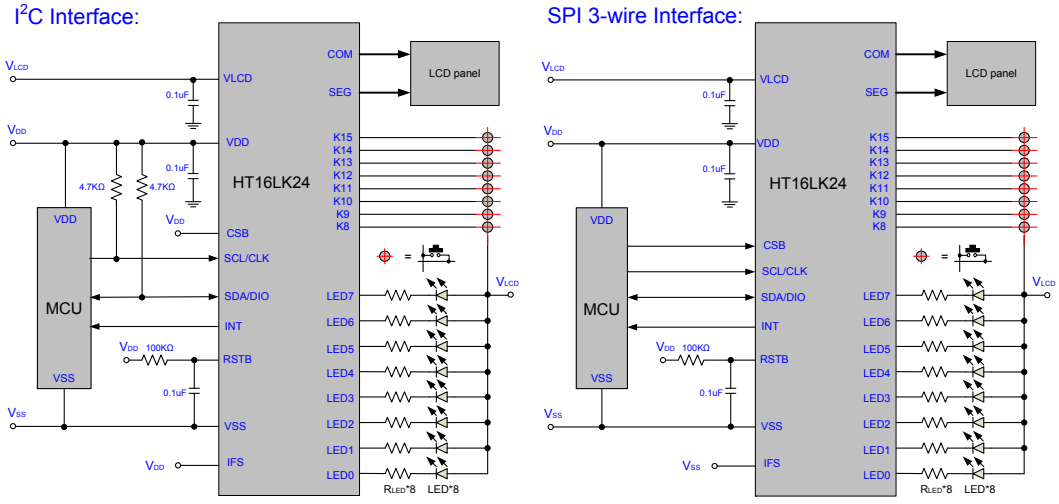
(8) The SEG/KSL shared pin configuration is 8 LED outputs and 8 key inputs.

Shared pins Configuration setting command			Duty	Key circuit		LED output	COM output	SEG output	LCD panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM output	SEG output
000b	01000b	1000b	1/1	none	K8~15	LED0~7	COM0	SEG0~50	COM0	SEG0~50
			1/2	none	K8~15	LED0~7	COM0~1	SEG0~50	COM0~1	SEG0~50
			1/3	none	K8~15	LED0~7	COM0~2	SEG0~50	COM0~2	SEG0~50
			1/4	none	K8~15	LED0~7	COM0~3	SEG0~50	COM0~3	SEG0~50
			1/8	none	K8~15	LED0~7	COM0~7	SEG4~50	COM0~7	SEG0~46

- The RSTB pin is connected to a MCU.



- The RSTB pin is connected to external resistor and capacitor.

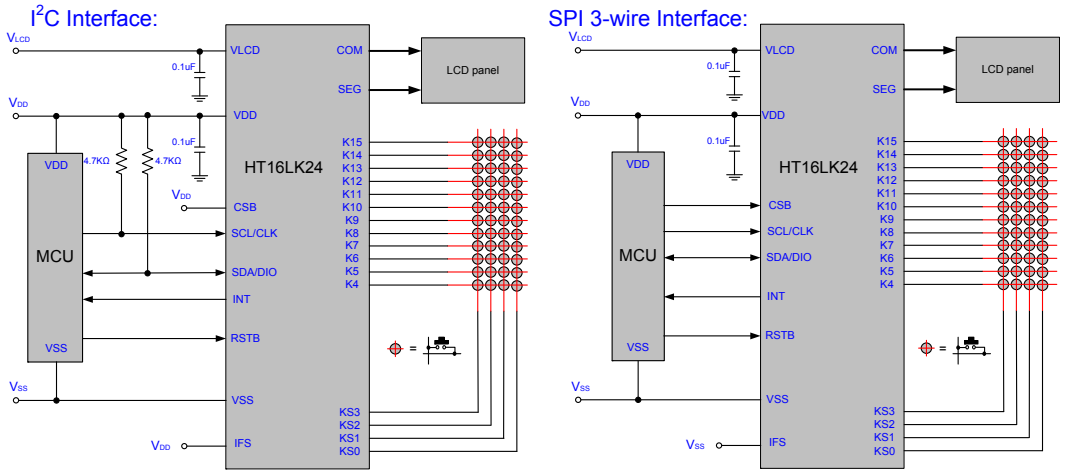


Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

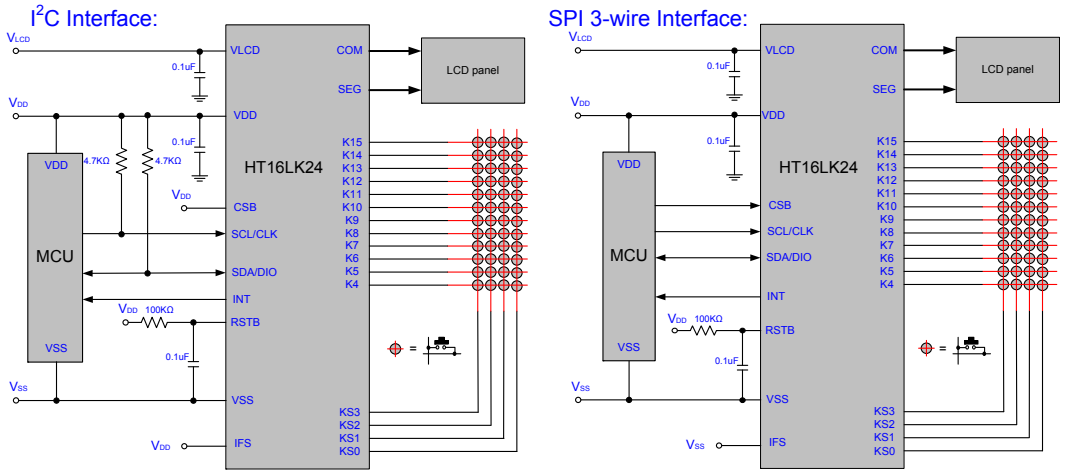
(9) The SEG/KSL shared pin configuration is 4 key scan outputs and 12 key inputs.

Shared pins Configuration setting command			Duty	Key circuit		LED output	COM output	SEG output	LCD panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM output	SEG output
100b	01100b	0000b	1/1	KS0~3	K4~15	none	COM0	SEG0~50	COM0	SEG0~50
			1/2	KS0~3	K4~15	none	COM0~1	SEG0~50	COM0~1	SEG0~50
			1/3	KS0~3	K4~15	none	COM0~2	SEG0~50	COM0~2	SEG0~50
			1/4	KS0~3	K4~15	none	COM0~3	SEG0~50	COM0~3	SEG0~50
			1/8	KS0~3	K4~15	none	COM0~7	SEG4~50	COM0~7	SEG0~46

- The RSTB pin is connected to a MCU.



- The RSTB pin is connected to external resistor and capacitor.



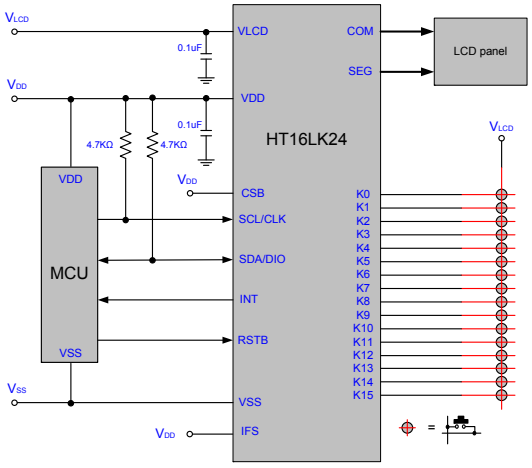
Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

(10) The SEG/KSL shared pin configuration is 16 key inputs.

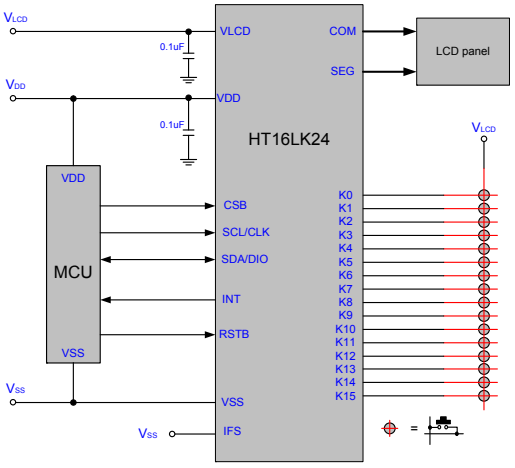
Shared pins Configuration setting command			Duty	Key circuit		LED output	COM output	SEG output	LCD panel	
KX[2:0]	KY[4:0]	L[3:0]		Output (KS)	Input (K)				COM output	SEG output
000b	10000b	0000b	1/1	none	K0~15	none	COM0	SEG0~50	COM0	SEG0~50
			1/2	none	K0~15	none	COM0~1	SEG0~50	COM0~1	SEG0~50
			1/3	none	K0~15	none	COM0~2	SEG0~50	COM0~2	SEG0~50
			1/4	none	K0~15	none	COM0~3	SEG0~50	COM0~3	SEG0~50
			1/8	none	K0~15	none	COM0~7	SEG4~50	COM0~7	SEG0~46

- The RSTB pin is connected to a MCU.

I²C Interface:

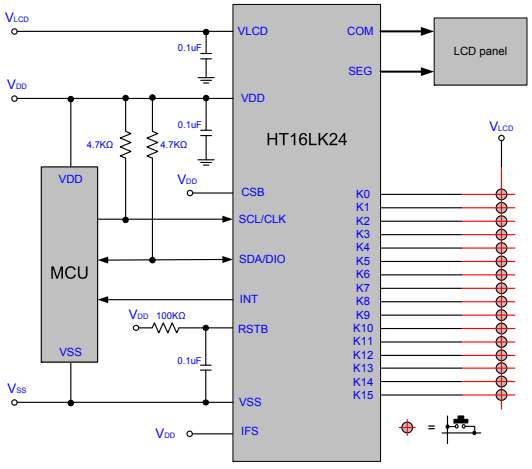


SPI 3-wire Interface:

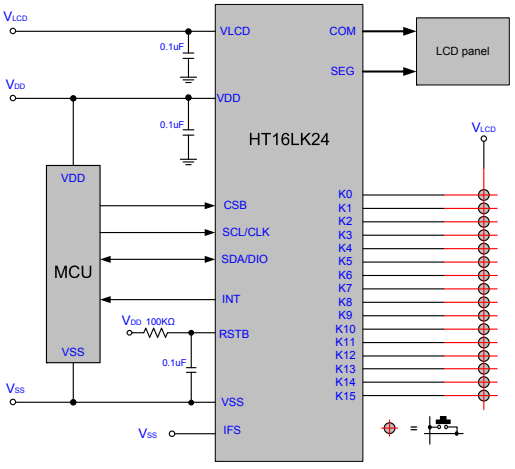


- The RSTB pin is connected to external resistor and capacitor.

I²C Interface:



SPI 3-wire Interface:



Note: If only the internal power on reset circuit is used, the RSTB pin must be connected to V_{DD}.

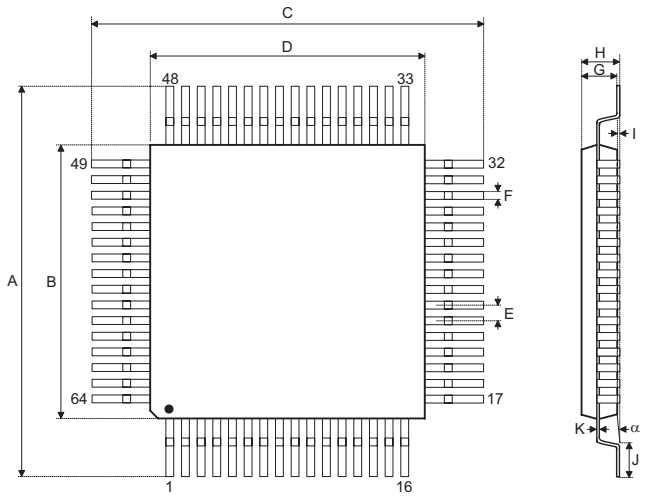
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

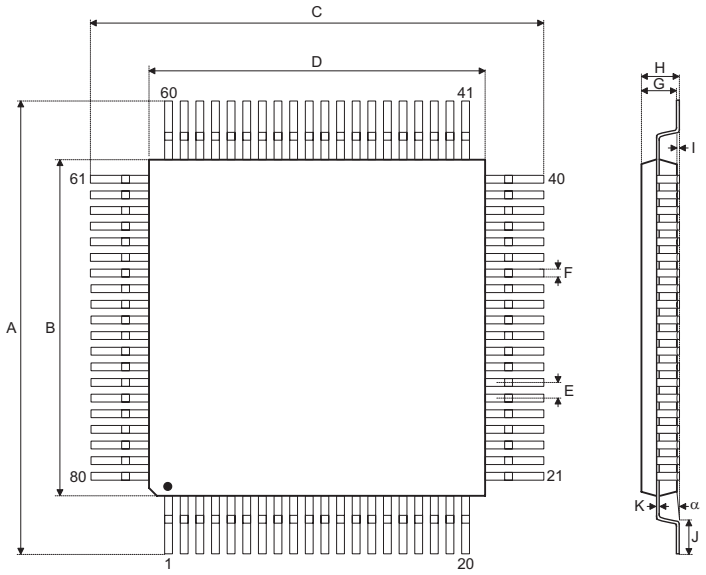
64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

80-pin LQFP (10mm×10mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.472 BSC	—
B	—	0.394 BSC	—
C	—	0.472 BSC	—
D	—	0.394 BSC	—
E	—	0.016 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	12.00 BSC	—
B	—	10.00 BSC	—
C	—	12.00 BSC	—
D	—	10.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°