HT2263

Current Mode PWM Controller

GENERAL DESCRIPTION

HT2263 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in sub 30W range.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with HT2263. A large value resistor could thus be used in the startup circuit to minimize the standby power.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense(CS) input removes the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design.

HT2263 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). The Gate-drive output is clamped to maximum 18V to protect the power MOSFET.

Excellent EMI performance is achieved with frequency shuffling technique together with soft switching control at the totem pole gate drive output.

Tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation. HT2263 is offered in SOT23-6, SOP-8 and DIP-8 packages.

FEATURES

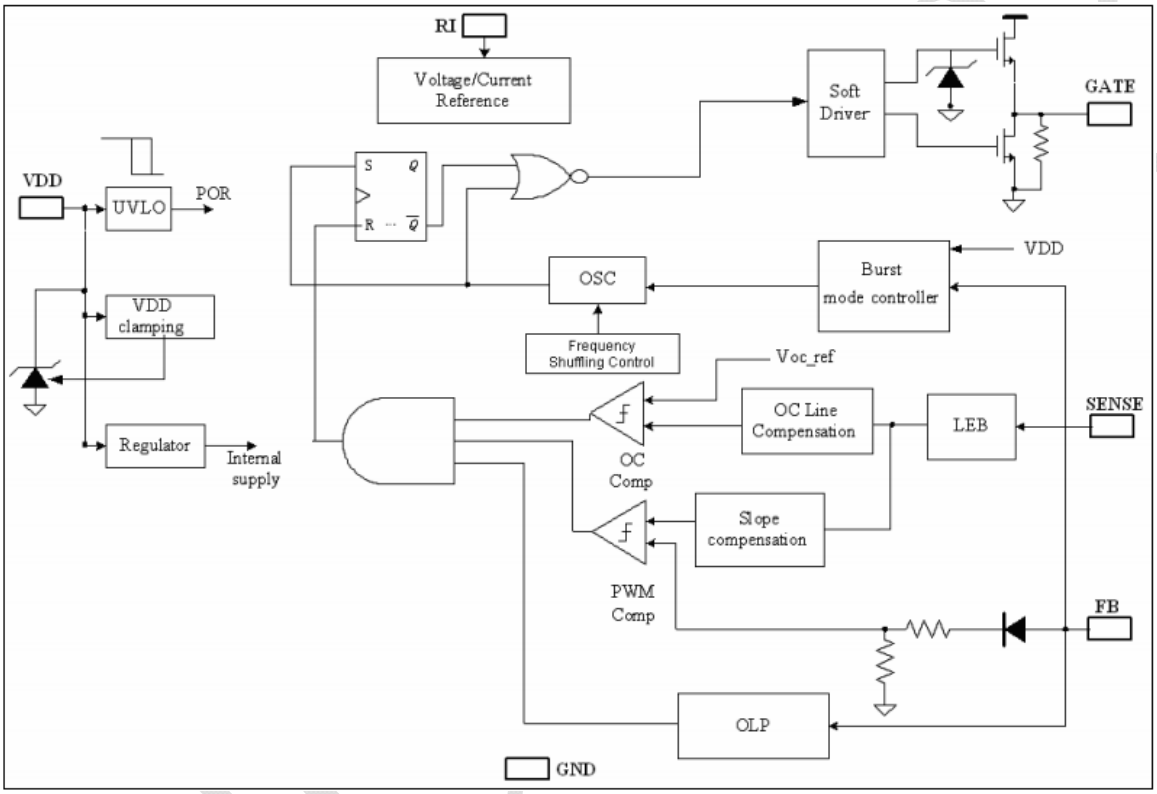
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design.
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current (1.4mA)
- Leading Edge Blanking on Current Sense Input
- Good Protection Coverage With Auto Self-Recovery
- VDD Over Voltage Clamp and Under Voltage Lockout with Hysteresis (UVLO)
- Gate Output Maximum Voltage Clamp (18V)
- Line Input Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Power Limiting Over Universal Input Voltage Range.
- Overload Protection (OLP)

APPLICATIONS

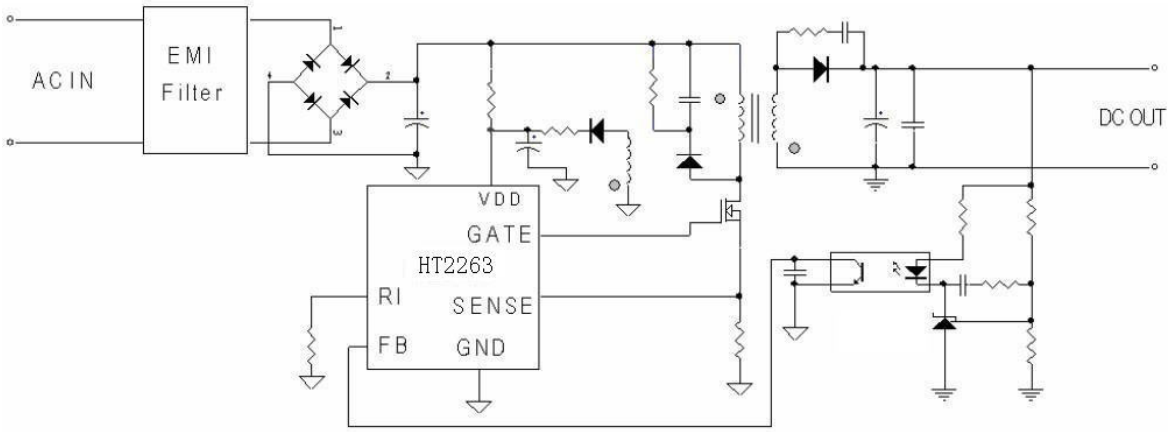
Offline AC/DC flyback converter for

- Battery Charger
- Power Adaptor
- Set-Top Box Power Supplies
- Open-frame SMPS

BLOCK DIAGRAM



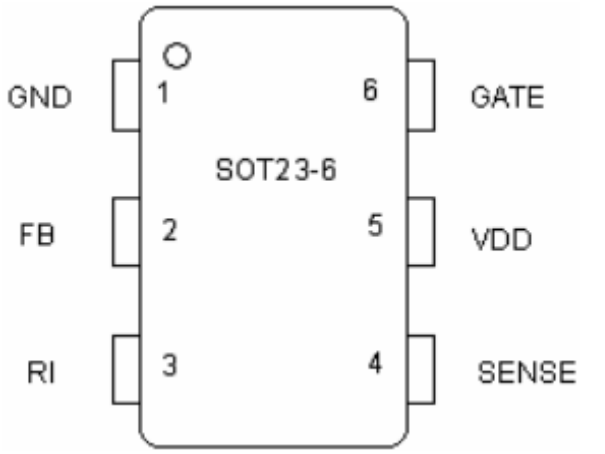
TYPICAL APPLICATION

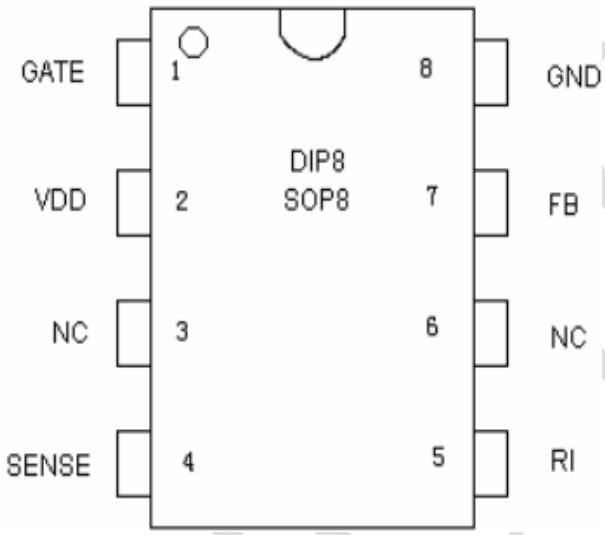


GENERAL INFORMATION

Pin Configuration

The HT2263 is offered in SOT23-6, DIP8 and SOP8 packages, shown as below.





Ordering Information

Part Number	Description
HT2263MP	SOT23-6, Pb-free
HT2263AP	DIP8, Pb-free
HT2263CP	SOP8, Pb-free

Package Dissipation Rating

Package	RθJA (°C/W)
DIP8	90
SOP8	150
SOT23-6	200

Absolute Maximum Ratings

Parameter	Value
VDD DC Supply Voltage	30 V
VDD Zener Clamp Voltage[Note]	VDD_Clamp+0.1V
VDD DC Clamp Current	10 mA
V_{FB} Input Voltage	-0.3 to 7V
V_{SENSE} Input Voltage to Sense Pin	-0.3 to 7V
V_{RI} Input Voltage to RI Pin	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-20 to 150 °C
Min/Max Storage Temperature T_{stg}	-55 to 160 °C

Note: VDD_Clamp has a nominal value of 34V.

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
GND	P	Ground
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input.
RI	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
VDD	P	Chip DC power supply pin.
GATE	O	Totem-pole gate drive output for the power MOSFET.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min — Max	Unit
VDD	VDD Supply Voltage	10 to 30	V
RI	RI Resistor Value	100	Kohm
T_A	Operating Ambient Temperature	-20 to 85	^oC

ELECTRICAL CHARACTERISTICS

(TA = 25OC if not otherwise noted)

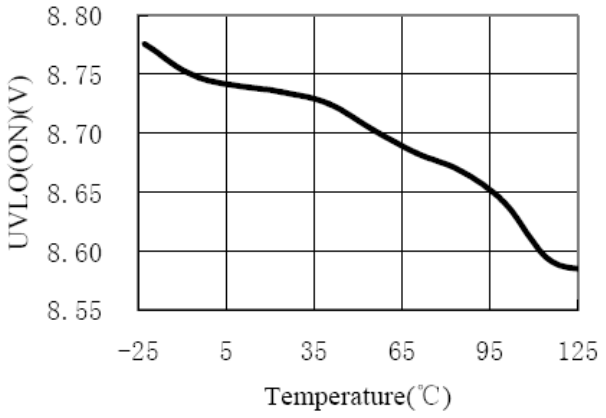
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
I_VDD_Startup	VDD Start up Current	VDD =12.5V, RI=100K Measure Leakage current into VDD		3	20	uA
I_VDD_Ops	Operation Current	VDD=16V, RI=100Kohm, V_{FB}=3V		1.4		mA
UVLO(ON)	VDD Under Voltage Lockout Enter		7.5	8.5	9.5	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		13.5	14.5	15.5	V
VDD_Clamp	VDD Zener Clamp Voltage	I_{VDD} = 5 mA		34		V
Feedback Input Section(FB Pin)						
A_{VCS}	PWM Input Gain	$\Delta V_{FB} / \Delta V_{cs}$		2.0		V/V
V_{FB}_Open	V_{FB} Open Loop Voltage			4.8		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		1		mA
V_{TH}_0D	Zero Duty Cycle FB Threshold Voltage	VDD = 16V, RI=100Kohm			0.75	V

V_{TH}_PL	Power Limiting FB Threshold Voltage			3.7		V
T_D_PL	Power limiting Debounce Time			47		mSec
Z_{FB}_IN	Input Impedance			6		Kohm
DC_MAX	Maximum Duty Cycle	VDD=18V,RI=100Kohm, FB=3V, CS=0		75		%
Current Sense Input(Sense Pin)						
T_blanking	Leading edge blanking time	RI = 100 Kohm		330		ns
Z_{SENSE}_IN	Input Impedance			40		Kohm
T_D_OC	OCP Control Delay	GATE with 1nF to GND		120		nSec
V_{TH}_OC	Over Current Threshold Voltage at zero Duty Cycle	FB=3.3V, RI=100 Kohm	0.70	0.75	0.80	V
Oscillator						
F_{OSC}	Normal Oscillation Frequency	RI = 100 Kohm	60	65	70	KHZ
∆f_Temp	Frequency Temperature Stability	VDD = 16V, RI=100Kohm, T_A -20°C to 85 °C		5		%
∆f_VDD	Frequency Voltage Stability	VDD = 12-25V, RI=100Kohm		5		%
RI_range	Operating RI Range		50	100	150	Kohm
V_RI_open	RI open load voltage			2		V
Fosc_BM	Burst Mode Base Frequency	VDD = 16V, RI = 100Kohm		22		KHZ
Gate Drive Output						
VOL	Output Low Level	VDD = 16V, Io = -20 mA			0.8	V
VOH	Output High Level	VDD = 16V, Io = 20 mA	10			V
V_Clamp	Output Clamp Voltage Level			18		V
T_r	Output Rising Time	VDD = 16V, CL = 1nf		200		nSec
T_f	Output Falling Time	VDD = 16V, CL = 1nf		70		nSec
Frequency Shuffling						
∆f_OSC	Frequency Modulation range /Base frequency	RI=100K	-3		3	%
f_shuffling	Shuffling Frequency	RI=100K		64		HZ

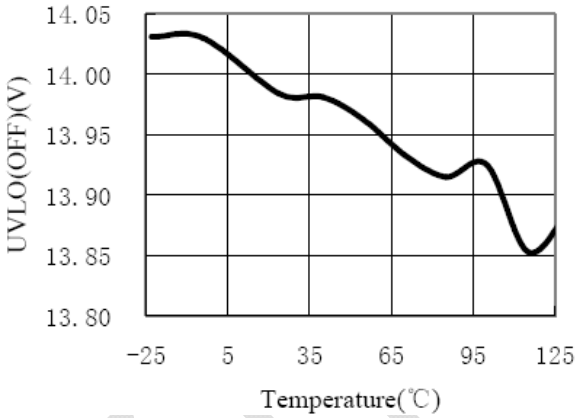
CHARACTERIZATION PLOTS

VDD = 16V, RI = 100 Kohm, TA = 25°C condition applies if not otherwise noted.

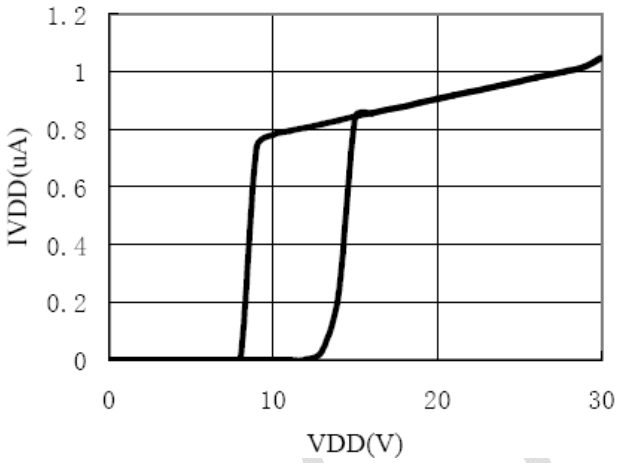
UVLO(ON) vs Temperature



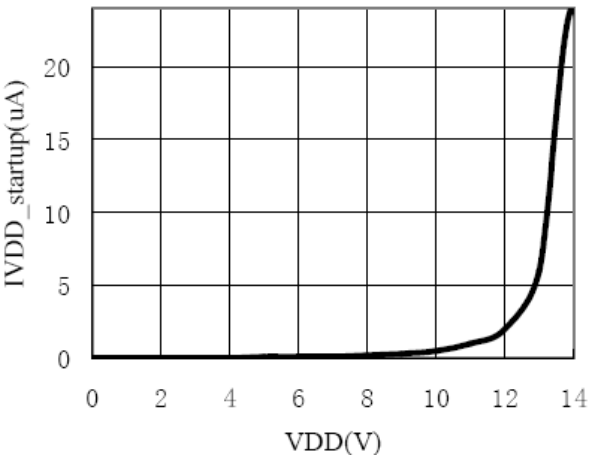
UVLO(OFF) vs Temperature



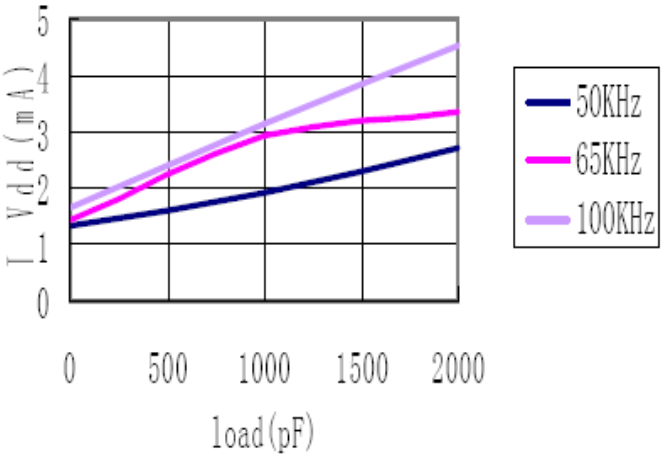
IVDD vs VDD



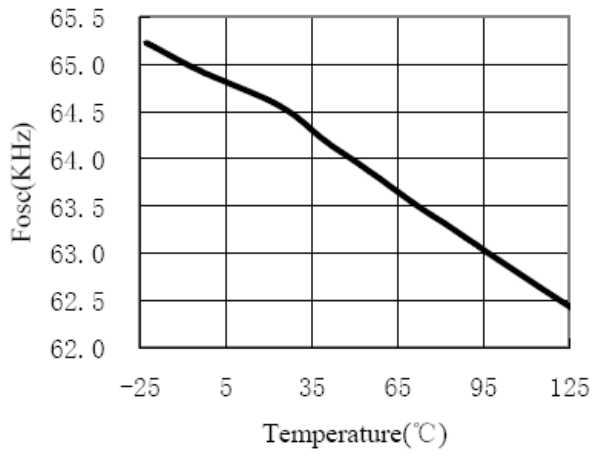
IVDD_startup vs VDD



I_Vdd vs Gate load



Fosc vs Temperature



OPERATION DESCRIPTION

The HT2263 is a highly integrated PWM controller IC optimized for offline flyback converter

applications in sub 30W power range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of HT2263 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet provides reliable startup in application. For AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

- **Operating Current**

The Operating current of HT2263 is low at 1.4mA. Good efficiency is achieved with HT2263 low operating current together with extended burst mode control features.

- **Frequency shuffling for EMI improvement**

The frequency Shuffling/jittering (switching frequency modulation) is implemented in HT2263. The oscillation frequency is modulated with a random source so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore reduces system design challenge.

- **Extended Burst Mode Operation**

At zero load or light load condition, majority of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. HT2263 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state tominimize the switching loss and reduces the standby power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

- **Oscillator Operation**

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$F_{osc} = \frac{6500}{RI(Kohm)}(Khz)$$

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in HT2263 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on

sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Gate Drive**

HT2263 Gate is connected to an external MOSFET gate for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp

is added for MOSFET gate protection at higher than expected VDD input.

- **Protection Controls**

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO).

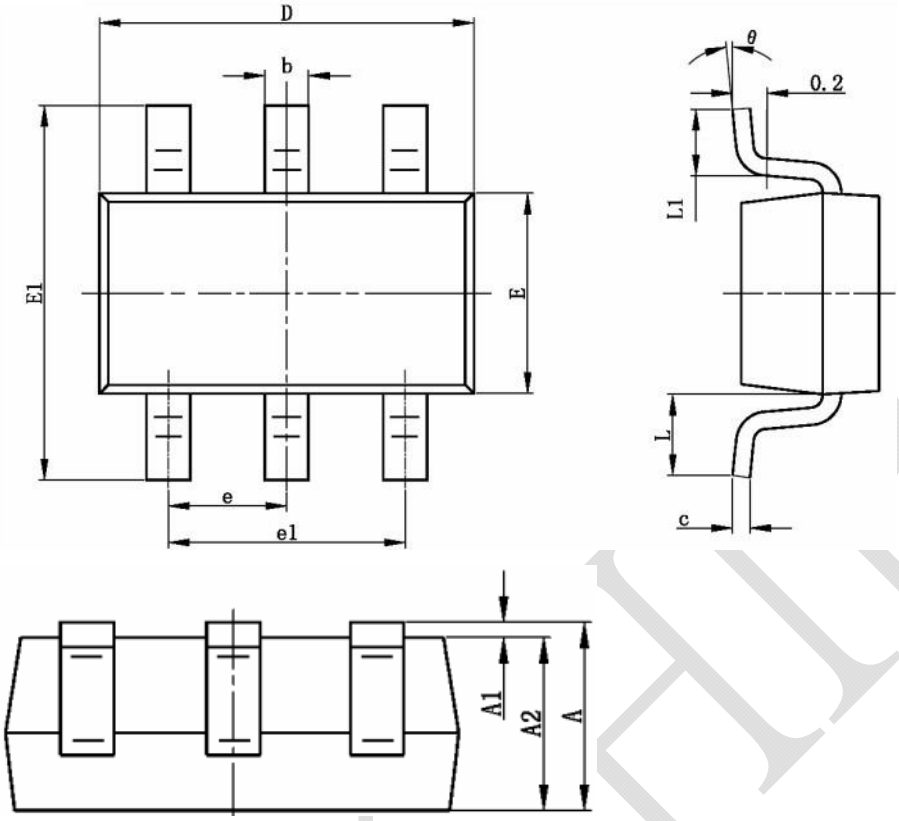
The OCP threshold tracks PWM Duty cycles and is line voltage compensated to achieve constant output power limit over the universal input voltage range with recommended reference design.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit.

VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

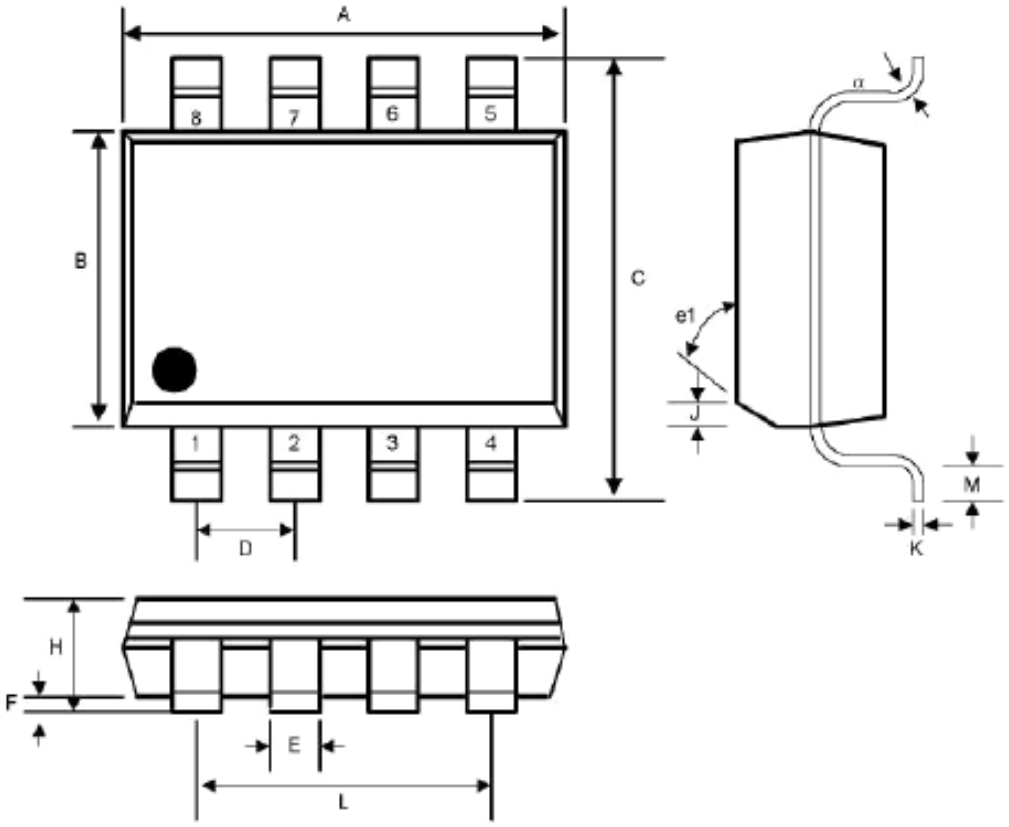
PACKAGE MECHANICAL DATA

SOT-23-6 PACKAGE OUTLINE DIMENSIONS



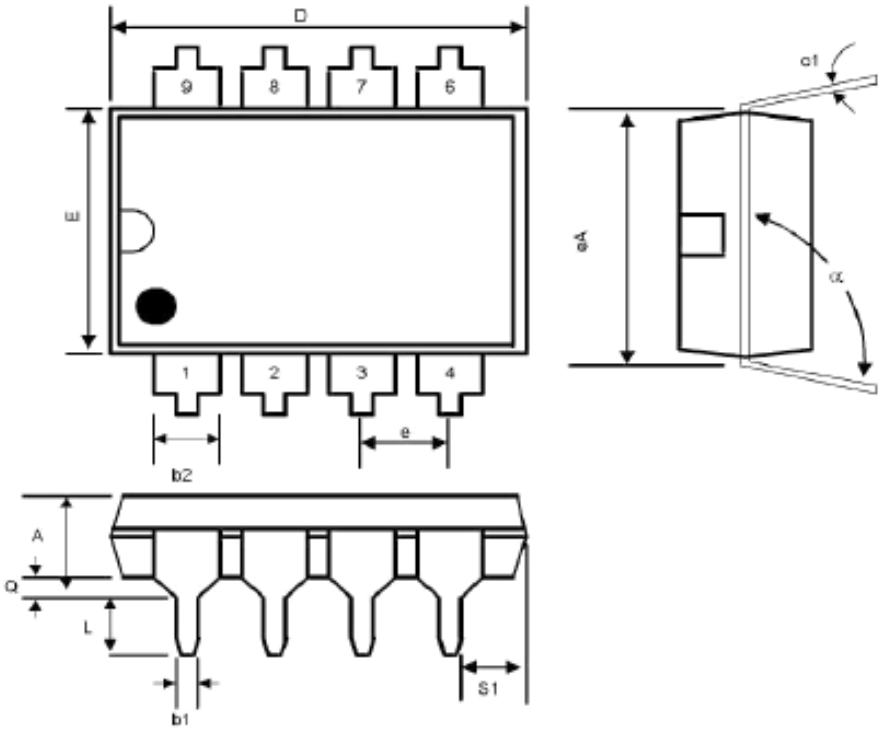
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0^0	8^0	0^0	8^0

SOP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.188	0.197	4.80	5.00	-
B	0.149	0.158	3.80	4.00	-
C	0.228	0.244	5.80	6.20	-
D	0.050 BSC		1.27 BSC		-
E	0.013	0.020	0.33	0.51	-
F	0.004	0.010	0.10	0.25	-
H	0.053	0.069	1.35	1.75	-
J	0.011	0.019	0.28	0.48	
K	0.007	0.010	0.19	0.25	-
M	0.016	0.050	0.40	1.27	
L	0.150 REF		3.81 REF		-
e1	45^0		45^0		-
α	0^0	8^0	0^0	8^0	-

DIP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b1	0.014	0.023	0.36	0.58	-
b2	0.045	0.065	1.14	1.65	-
c1	0.008	0.015	0.20	0.38	-
D	0.355	0.400	9.02	10.16	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	-
s1	0.005	-	0.13	-	-
α	90^0	105^0	90^0	105^0	-