

## GENERAL DESCRIPTION

HT2269 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with HT2269. A large value resistor could thus be used in the startup circuit to minimize the standby power.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery. This greatly helps to reduce the external component count and system cost in application.

HT2269 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), VDD over voltage protection (OVP) and under voltage lockout (UVLO). The Gate-drive output is clamped at 18V to protect the power MOSFET.

In HT2269, OCP threshold slope is internally optimized to reach constant output power limit over universal AC input range.

Excellent EMI performance is achieved

frequency shuffling technique together with soft switching control at the totem pole gate drive output.

The tone energy at below 20KHZ is minimized in operation. Consequently, audio noise performance is greatly improved. HT2269 is offered in both SOP-8 and DIP-8 packages.

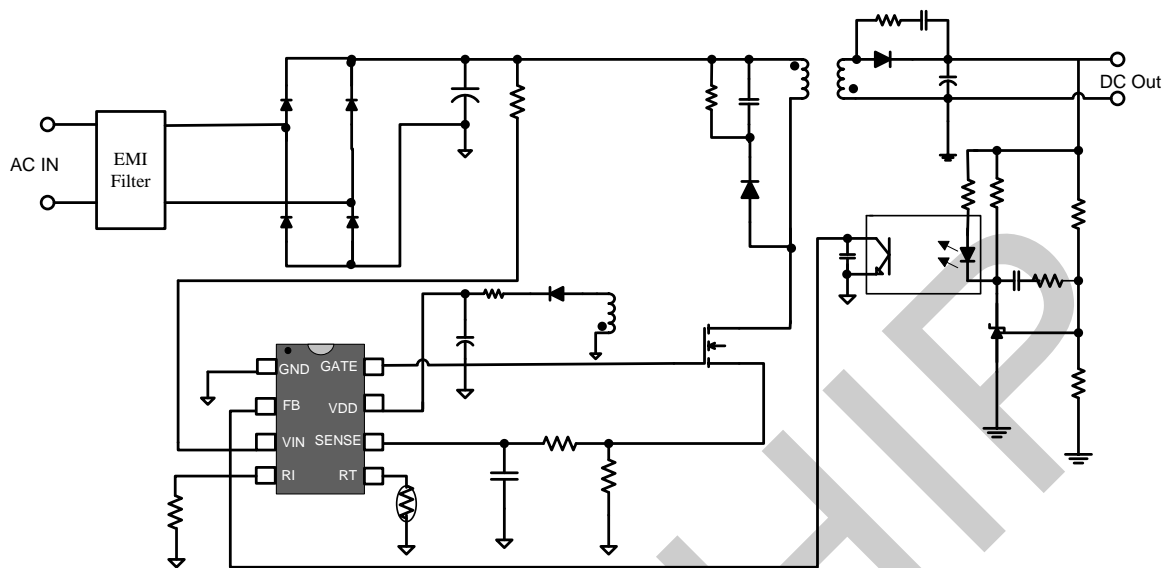
## FEATURES

- ◆ Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design.
- ◆ Audio Noise Free Operation
- ◆ External Programmable PWM Switching Frequency
- ◆ Internal Synchronized Slope Compensation
- ◆ Low VIN/VDD Startup Current(6.5uA) and Low Operating Current (2.3mA)
- ◆ Leading Edge Blanking on Current Sense Input
- ◆ Complete Protection Coverage With Auto Self-Recovery
- ◆ External Programmable Over Temperature Protection (OTP)
- ◆ On-chip VDD OVP for System OVP Under Voltage Lockout with Hysteresis (UVLO)
- ◆ Gate Output Maximum Voltage Clamp (18V)
- ◆ Line Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Current Limiting Over Universal Input Voltage Range (OCP)
- ◆ Over Load Protection. (OLP)

## APPLICATIONS

- ◆ Laptop Power Adaptor
- ◆ PC/TV/Set-Top Box Power
- ◆ Supplies Open-frame SMPS
- ◆ Battery Charge

**TYPICAL APPLICATION**



**PIN CONFIGURATION**

		Pin Name	Pin Num	Description
		GND	1	Ground
		FB	2	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6.
		VIN	3	Connected through a large value resistor to rectified line input for Startup IC supply and line voltage sensing.
		RI	4	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
		RT	5	Temperature sensing input pin. Connected through a NTC resistor to GND.
		SENSE	6	Current sense input pin. Connected to MOSFET current sensing resistor node.
		VDD	7	DC power supply pin.
		GATE	8	Totem-pole gate drive output for power MOSFET.

1	GND	GATE	8
2	FB	VDD	7
3	VIN	SENSE	6
4	RI	RT	5

**PACKAGE DISSIPATION RATING**

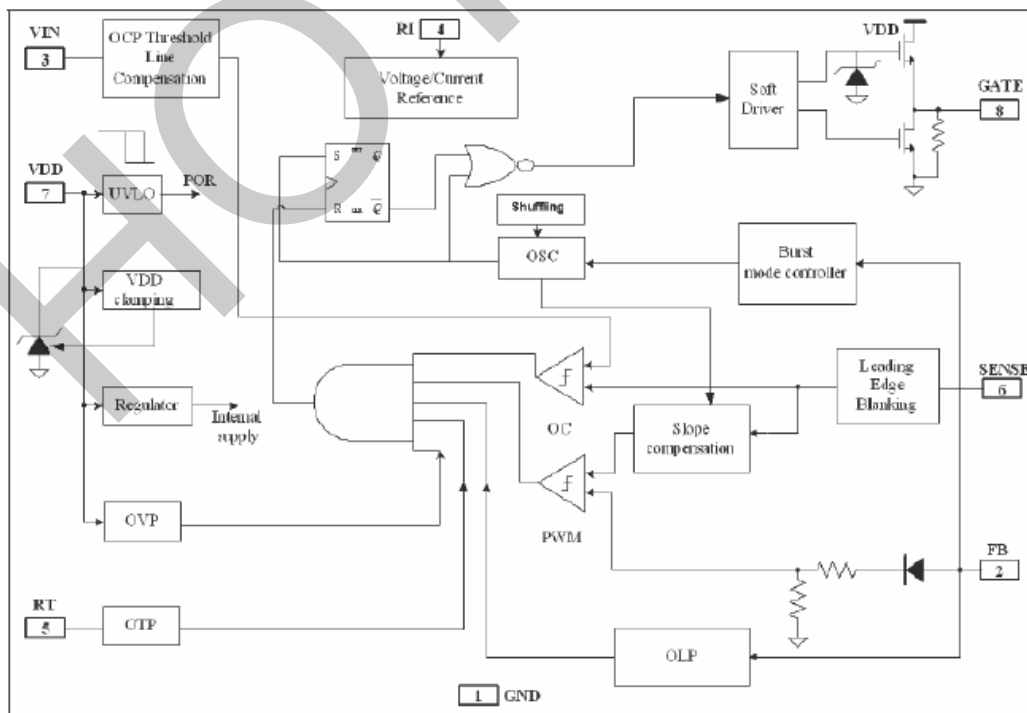
Package	R $\theta$ JA (°C/W)
DIP8	90
SOP8	150

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Value
VDD/VIN DC Supply Voltage	30 V
VDD Zener Clamp Voltage <sup>Note</sup>	VDD_Clamp+ 0.1V
VDD Clamp Continuous Current	10 mA
V <sub>FB</sub> Input Voltage	-0.3 to 7V
V <sub>SENSE</sub> Input Voltage to sense Pin	-0.3 to 7V
V <sub>RT</sub> Input Voltage to RT Pin	-0.3 to 7V
V <sub>RI</sub> Input Voltage to RI Pin	-0.3 to 7V
Min/Max Operating Junction Temperature T <sub>J</sub>	-20 to 150 C
Min/Max Storage Temperature T <sub>stg</sub>	-55 to 150 °C
Lead Temperature (Soldering,10secs)	260°C

Note: VDD\_Clamp has a nominal value of 35V.

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

**BLOCK DIAGRAM**


**RECOMMENDED OPERATING CONDITION**

Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	12	23	V
RI	RI Resistor Value	24	31	Kohm
T <sub>A</sub>	Operating Ambient Temperature	-20	85	C

**ESD INFORMATION**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HBM	Human Body Model on All Pins Except VIN and VDD	MIL-STD		3		KV
MM	Machine Model on All Pins	JEDEC-STD		250		V

Note: HBM all pins pass 3KV except High Voltage Input pin. The details are VIN passes 1kV, VDD passes 1.5KV, all other I/Os pass 3KV. In system application, High Voltage Input pin is either a high impedance input or connected to a cap. The lower rating has minimum impacts on system ESD performance.

**ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = 25°C, VDD=16V, RI=24Kohm if not otherwise noted)

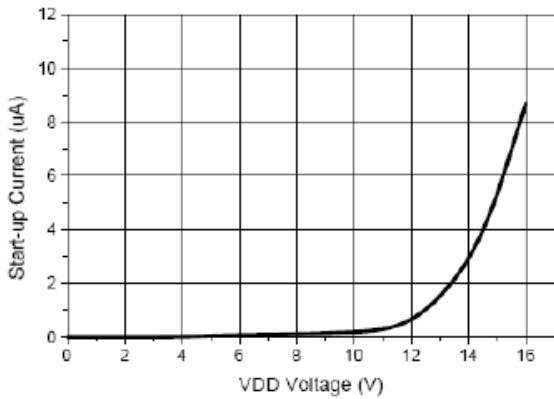
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
I_VDD_Startup	VDD Start up Current	VDD =15V, Measurecurrent into VDD		6.5	20	uA
I_VDD_Operation	Operation Current	V <sub>FB</sub> =3V		2.3		mA
UVLO(Enter)	VDD Under Voltage Lockout Enter		9.5	10.5	11.5	V
UVLO(Exit)	VDD Under Voltage Lockout Exit (Startup)		16	17	18	V
OVP(ON) <sup>*Optional</sup>	VDD Over Voltage Protection Enter		23.5	25	26.5	V
OVP(OFF) <sup>*Optional</sup>	VDD Over Voltage Protection Exit (Recovery)		21.5	23.2	24.7	V
OVP_Hys <sup>*Optional</sup>	OVP Hysteresis	OVP(ON)-OVP(OFF)		2		V
T <sub>D_OVP</sub>	VDD OVP Debounce time			80		uSec
V <sub>DD_Clamp</sub>	V <sub>DD</sub> Zener Clamp Voltage	I(V <sub>DD</sub> ) =5mA		36		V

Feedback Input Section(FB Pin)						
AVCS	PWM Input Gain	$\Delta V_{FB} / \Delta V_{cs}$		2.6		V/V
V <sub>FB_Open</sub>	V <sub>FB</sub> Open Voltage			6		V
I <sub>FB_Short</sub>	FB pin short circuit current	Short FB pin to GND, measure current		0.8		mA
V <sub>TH_0D</sub>	Zero Duty Cycle FB Threshold Voltage				0.95	V
V <sub>TH_BM</sub>	Burst Mode FB Threshold Voltage			1.7		V
V <sub>TH_PL</sub>	Power Limiting FB Threshold Voltage			4.4		V
T <sub>D_PL</sub>	Power limiting Debounce Time			80		mSec
Z <sub>FB_IN</sub>	Input Impedance			7.5		Kohm
Current Sense Input(Sense Pin)						
T <sub>blanking</sub>	Sense Input Leading Edge Blanking Time			300		nS
Z <sub>SENSE_IN</sub>	Sense Input Impedance			39		Kohm
TD_OC	Over Current Detection and Control Delay	CL=1nf at GATE,		120		nSec
V <sub>TH_OC_0</sub>	Current Limiting Threshold at No Compensation	I(VIN) = 0uA		0.9	0.95	V
V <sub>TH_OC_1</sub>	Current Limiting Threshold at Compensation	I(VIN) = 150uA		0.81		V
Oscillator						
F <sub>osc</sub>	Normal Oscillation Frequency		60	65	70	KHZ
$\Delta f_{Temp}$	Frequency Temperature Stability	-20°C to 100°C		2		%

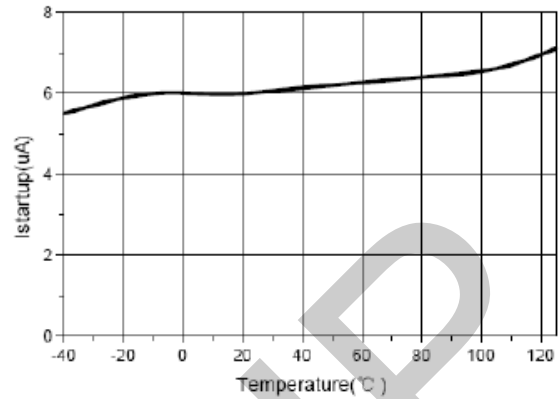
$\Delta f_{VDD}$	Frequency Voltage Stability	VDD = 12-25V		2		%
RI_range	Operating RI Range		12	24	60	Kohm
V_RI_open	RI open voltage			2		V
F_BM	Burst Mode Base Frequency			22		KHZ
DC_max	Maximum Duty Cycle		75	80	85	%
DC_min	Minimum Duty Cycle		-	-	0	%
Gate Drive Output						
VOL	Output Low Level	Io = -20 mA			0.3	V
VOH	Output High Level	Io = +20 mA	11			V
VG_Clamp	Output Clamp Voltage Level	VDD=20V		18		V
T_r	Output Rising Time	CL = 1nf		120		nSec
T_f	Output Falling Time	CL = 1nf		50		nSec
Over Temperature Protection						
I_RT	Output Current of RT pin			70		uA
V <sub>TH_OTP</sub>	OTP Threshold Voltage		1	1.065	1.13	V
V <sub>TH_OTP_off</sub>	OTP Recovery Threshold Voltage			1.165		V
T <sub>D_OTP</sub>	OTP De-bounce Time			100		uSec
V_RT_Open	RT Pin Open Voltage			3.5		V
Frequency Shuffling						
$\Delta f_{OSC}$	Frequency Modulation range /Base frequency		-3		3	%
Freq_Shuffling	Shuffling Frequency	RI = 24Kohm		32		HZ

**CHARACTERIZATION PLOTS**

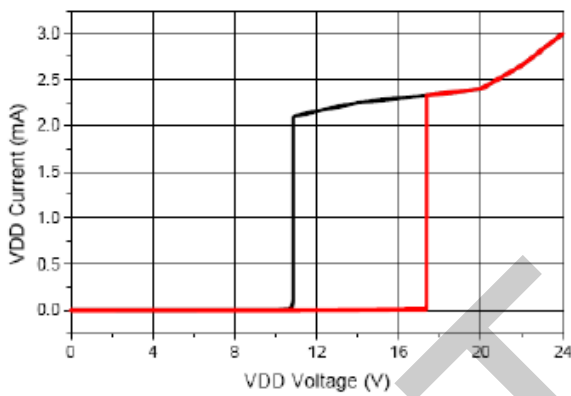
VDD Start-up Current vs Voltage



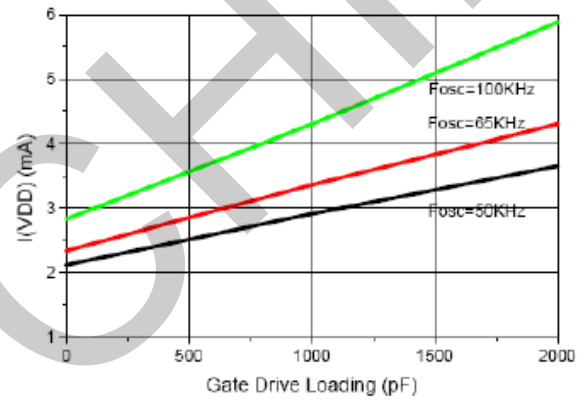
VDD Startup Current vs Temperature



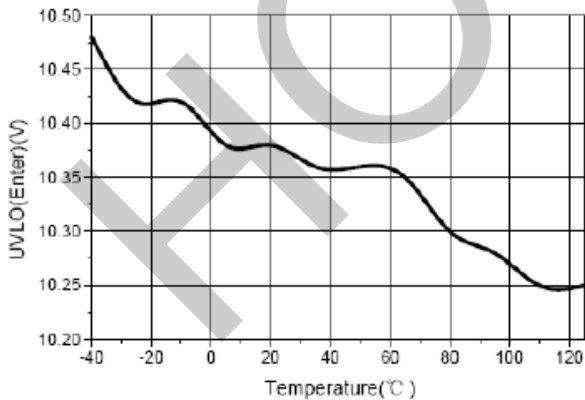
VDD UVLO and Operation Current



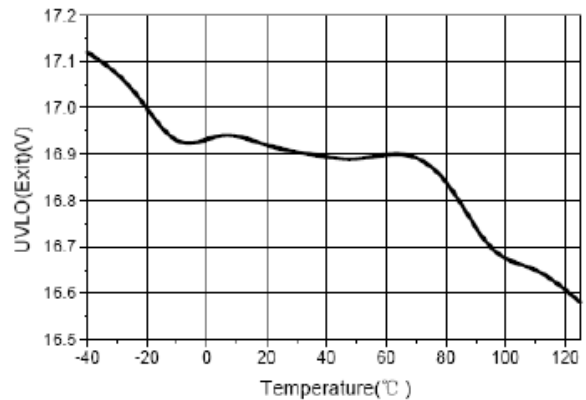
VDD Operation Current vs Load

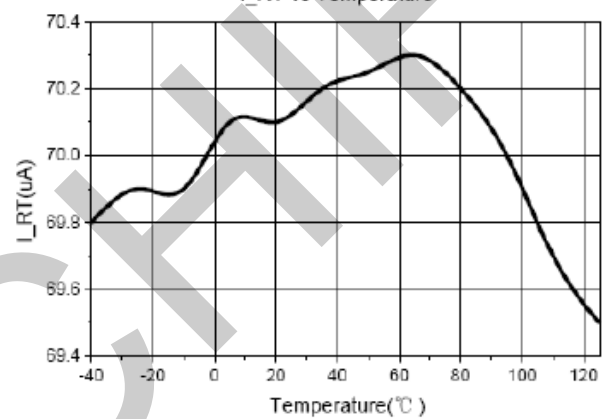
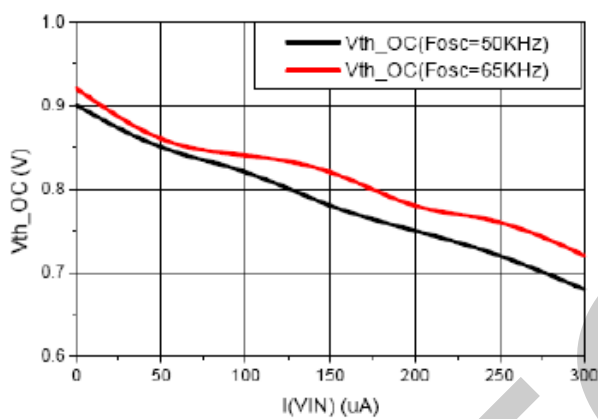
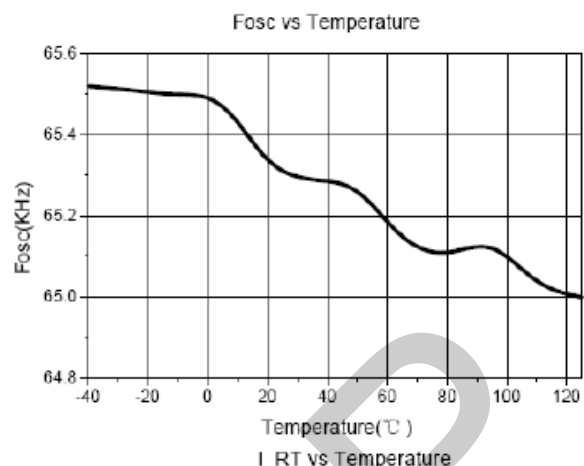
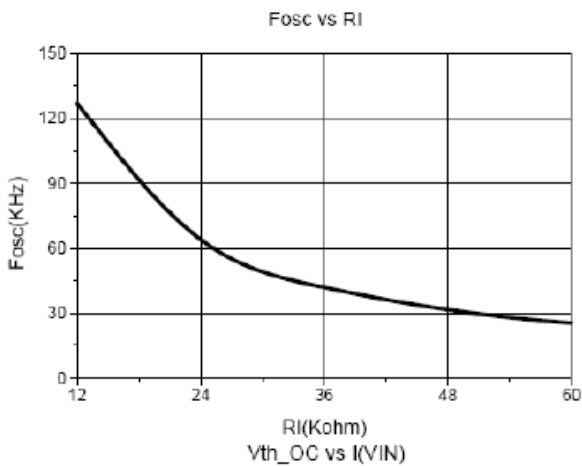


VDD UVLO(Enter) vs Temperature



VDD UVLO(Exit) vs Temperature





## OPERATION DESCRIPTION

### Startup Current and Start up Control

Startup current of HT2269 is designed to be very low so that VDD could be charged up above UVLO(exit) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

### Operating Current

The Operating current of HT2269 is low at 2.3mA. Good efficiency is achieved with B2269C low

operating current together with extended burst mode control schemes

### Frequency shuffling for EMI improvement

The frequency Shuffling/jittering (switching frequency modulation) is implemented in HT2269. The oscillation frequency is modulated with a internally generated random source so that the tone energy is evenly spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

### Burst Mode Operation

At zero load or light load condition, most of the



power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time.

Reducing switching events leads to the reduction on the power loss and thus conserves the energy.

HT2269 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level (1.8V). Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend.

The nature of high frequency switching also reduces the audio noise at any loading conditions.

### **Oscillator Operation**

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined.

The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$F_{ocs} = \frac{1560}{RI(\text{Kohm})} (\text{Khz})$$

### **Current Sensing and Leading Edge**

#### **Blanking**

Cycle-by-Cycle current limiting is offered in HT2269 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

#### **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

#### **Over Temperature Protection**

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises.

With the fixed internal current IRT flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal

OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than  $V_{TH\_OTP}$ .

### Gate Drive

HT2269 Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

### Protection Controls

Good system reliability is achieved with HT2269's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on-chip VDD over voltage protection (OVP, optional) and under voltage lockout (UVLO). The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is

achieved with recommended OCP compensation scheme on HT2269.

At output overload condition, FB voltage is biased higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET.

Similarly, control circuit shutdowns the power MOSFET when an Over Temperature condition is detected. HT2269 resumes the operation when temperature drops below the hysteresis value.

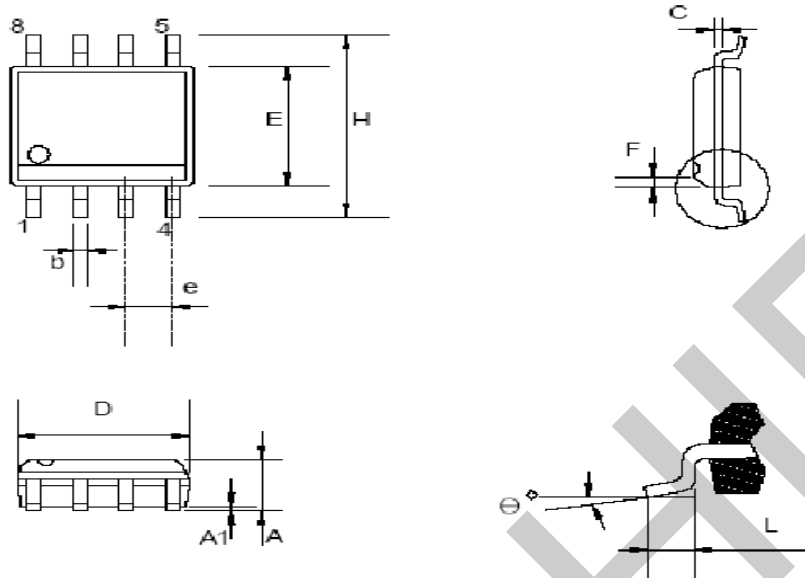
VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on startup sequence thereafter.

### ESD protection measures

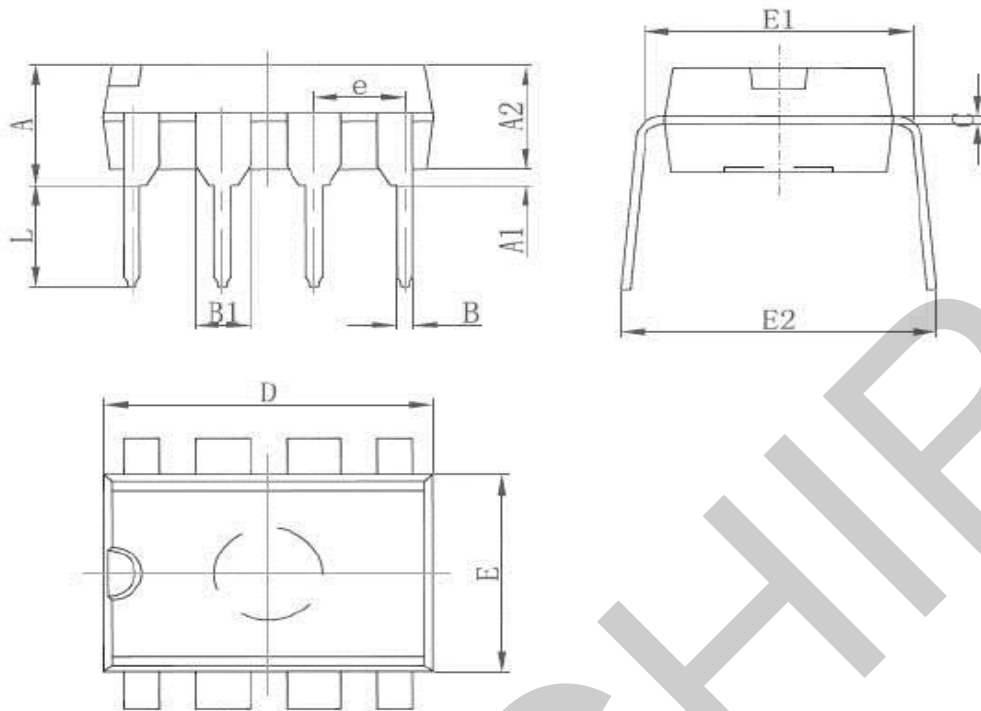
The MOS circuits are electrostatic sensitive devices, they need to take the following precautions in the production and transport to effectively prevent damages to the MOS circuits due to the electrostatic discharge:

- 1.The operator must touchdown by the anti-static hand strap;
- 2.The housing of production equipments must be grounded;
- 3.The tools used during the assembly must be grounded;
- 4.Packaging or transport must be packed by conductive or antistatic packaging materials.

**Package Information**



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Typ.	Max	Min	Typ.	Max
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D	4.648		4.978	0.183		0.196
E	3.810		3.987	0.150		0.157
e	1.016	1.270	1.524	0.040	0.050	0.060
F		0.381*45°			0.015*45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°

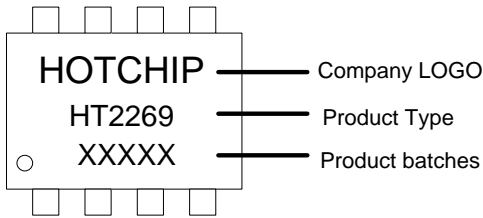


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.500		0.020	
A2	3.200	3.600	0.126	0.142
B	0.350	0.650	0.014	0.026
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.500	0.354	0.374
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.000	0.323	0.354

### Ordering Information

Device Identification and Ordering

Information



封装形式	芯片标识	采购器件名称	包装	最小包装数量
SOP8 Pb-free	HT2269	HT2269	盘装	2500PCS

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