CMOS 64K×8-Bit SPI Serial OTP EPROM

Features

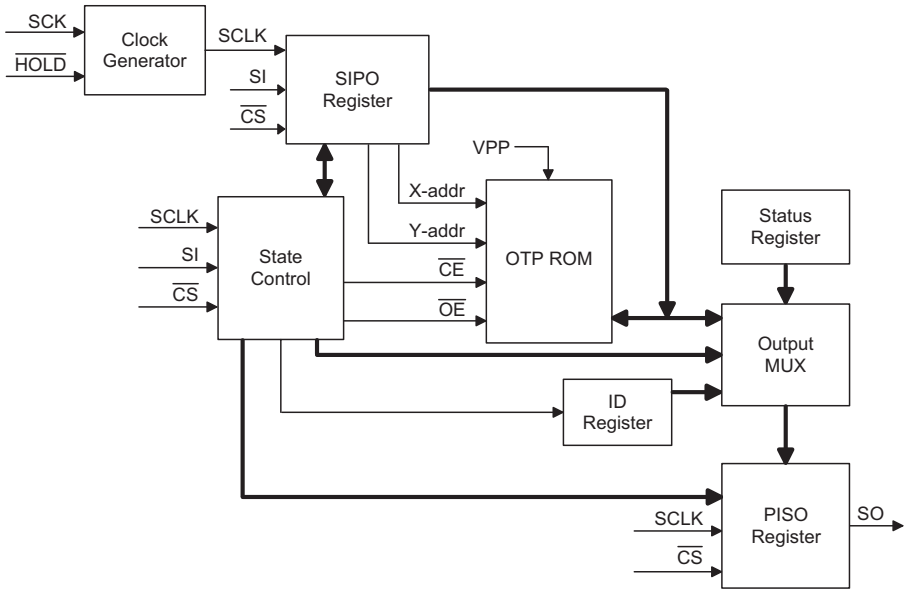
- Operating voltage: 2.7V~3.6V
- Programming voltage
  - V_{PP}=12.5V±0.2V
  - V_{CC}=6.0V±0.2V
- 512K-bit OTP ROM, access command compatible with AT25F512
- 64K×8-bit organization
- 12MHz max. clock frequency @VCC=2.7V
  15MHz max. clock frequency @VCC=3.0V
- Serial interface architecture
- Serial Peripheral Interface (SPI) compatible - modes 0 and 3
- CMOS and TTL compatible inputs and outputs
- Pin assignment compatible with AT25F512
- Commercial temperature range (0°C to +70°C)
- 8-pin SOP package

General Description

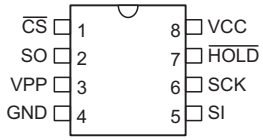
The HT25LC512 is a 512K-bit OTP ROM of which function and pin assignment are compatible with AT25F512 and can directly replace the AT25F512 for cost down purposes when the memory in the system is just read only. There are 512K bits of memory which are organized as 65536 words of 8 bits each. The HT25LC512 uses a serial interface to sequentially access its data. The simple serial interface facilitates hardware layout, increase system reliability, minimize switching noise, and reduce package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power consumption are essential. The device operates at clock frequencies up to 10MHZ.

The HT25LC512 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK). The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

Block Diagram



Pin Assignment



HT25LC512
－8 SOP-A

Pin Description

Pin No.	Pin Name	Description
1	$\overline{CS}$	Chip select
2	SO	Serial Output
3	VPP	Program voltage supply
4	GND	Negative power supply, ground
5	SI	Serial input
6	SCK	Serial clock
7	$\overline{HOLD}$	Suspends serial input
8	VCC	Positive power supply

Absolute Maximum Rating

Operation Temperature Commercial ..... 0°C to +70°C

Storage Temperature ..... –65℃ to 125 °C

Applied VCC Voltage with Respect to VSS ..... –0.6V to 7.0V

Applied Voltage on Input Pin with Respect to VSS ..... –0.6V to 7.0V

Applied Voltage on Output Pin with Respect to VSS ..... –0.6V to V_{CC}+0.5V

Applied VPP Voltage with Respect to VSS ..... –0.6V to 13.5V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=0°C to +70°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
Read operation							
V_{CC}	Supply Voltage	—	—	2.7	—	3.6	V
V_{IL}	Input Low Voltage	—	—	–0.5	—	$0.2V_{CC}$	V
V_{IH}	Input High Voltage	—	—	$0.7V_{CC}$	—	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	2.7V~3.6V	I_{OL}=0.15mA; 2.7V≤ V_{CC}≤ 3.6V	—	—	0.2	V
V_{OH}	Output High Voltage	2.7V~3.6V	I_{OH}=–100μA	V_{CC}–0.2	—	—	V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
I_{STB}	Standby Current	2.7V~3.6V	$\overline{CS}$=V_{CC}=3.6V, all inputs at CMOS levels	—	2	10	μA
I_{CC}	Active Current, Read Operation	2.7V~3.6V	f=10MHz; SO=open V_{CC}=3.6V	—	10	15	mA
I_{IL}	Input Leakage Current	2.7V~3.6V	V_{IN}=0V to V_{CC}	–3	—	3	μA
I_{OL}	Output Leakage Current	2.7V~3.6V	V_{IN}=0V to V_{CC}	–3	—	3	μA
Programming operation							
V_{CC}	Supply Voltage	—	—	5.8	6.0	6.2	V
V_{PP}	Supply Voltage	—	—	12.3	12.5	12.7	V
V_{IL}	Input Low Voltage	6.0V	—	–0.5	—	0.2V_{CC}	V
V_{IH}	Input High Voltage	6.0V	—	0.7V_{CC}	—	V_{CC}+0.5	V

Note: V_{PP} overshoot/undershoot riaging caused by fast rising time must not go below 11V or above 13V.

A.C. Characteristics

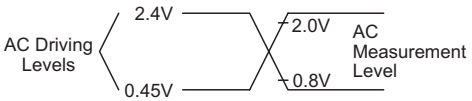
Ta=0°C to +70°C, V_{CC}=2.7V to 3.6V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SCK}	SCK Frequency	V_{CC}=2.7V~3.0V	0	—	12	MHz
		V_{CC}=3.0V~3.6V	0	—	15	MHz
t_{WH}	SCK High Time	V_{CC}=2.7V~3.0V	36	—	—	ns
		V_{CC}=3.0V~3.6V	28	—	—	ns
t_{WL}	SCK Low Time	V_{CC}=2.7V~3.0V	36	—	—	ns
		V_{CC}=3.0V~3.6V	28	—	—	ns
t_{CS}	Minimum $\overline{CS}$ High Time	V_{CC}=2.7V~3.6V	25	—	—	ns
t_{CSS}	$\overline{CS}$ Setup Time	V_{CC}=2.7V~3.6V	25	—	—	ns
t_{CSH}	$\overline{CS}$ Hold Time	V_{CC}=2.7V~3.6V	25	—	—	ns
t_{SU}	Data in Setup Time	V_{CC}=2.7V~3.6V	20	—	—	ns
t_H	Data in Hold Time	V_{CC}=2.7V~3.6V	5	—	—	ns
t_{CD}	$\overline{HOLD}$ Setup Time	V_{CC}=2.7V~3.6V	20	—	—	ns
t_{HD}	$\overline{HOLD}$ Hold Time	V_{CC}=2.7V~3.6V	15	—	—	ns
t_{HO}	Output Hold Time	V_{CC}=2.7V~3.6V	0	—	—	ns
t_{DIS}	Output Disable Time	V_{CC}=2.7V~3.6V	—	—	100	ns
t_V	Output Valid	V_{CC}=2.7V~3.0V	—	—	36	ns
		V_{CC}=3.0V~3.6V	—	—	28	ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z	V_{CC}=2.7V~3.6V	—	—	200	μs
t_{HZ}	$\overline{HOLD}$ to Output High Z	V_{CC}=2.7V~3.6V	—	—	200	μs

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Programming the OTP ROM						
f_{SCK}	SCK Frequency		48	70	160	kHz
t_{WH}	SCK High Time		3	7.5	10.5	μs
t_{WL}	SCK Low Time		3	7.5	10.5	μs
t_{CS}	Minimum $\overline{CS}$ High Time		2	—	—	μs
t_{CSS}	$\overline{CS}$ Setup Time		2	—	—	μs
t_{CSH}	$\overline{CS}$ Hold Time		2	—	—	μs
t_{SU}	Data in Setup Time		100	—	—	ns
t_H	Data in Hold Time		100	—	—	ns

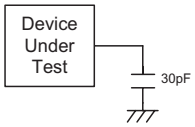
Note: For normal READ operation, don't use the 99H instruction.

Test Waveforms and Measurements



t_R, t_F< 5ns (10% to 90%)

Output Test Load



Functional Description

Device Operation

The HT25LC512 operation is controlled by instructions from the host processor. The HT25LC512 has only 3 kinds of instructions, Memory Read, Status Register read and Product ID Read. Any invalid instruction will be ignored without response from the HT25LC512. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the memory address location through the SI (serial input) pin. All instructions, addresses and data are transferred with the most significant bit (MSB) first.

- Memory read

  Reading the HT25LC512 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ instruction is transmitted via the SI line followed by the byte address to read. Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The READ instruction can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ instruction.

Memory read, bit sequence is shown as follows:

Bit Sequential	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit data	0	0	0	0	x	0	1	1	x	x	x	x	x	x	x	0

Bit Sequential	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Bit data	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Note: "x" don't care

- Status register read
  - Status register format

Bit Sequential	0	1	2	3	4	5	6	7
Bit Data	0	0	1	1	0	0	0	1

The data in the status register will always be 8CH. To read the status register, the bit sequence is shown below. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK is being toggled) starting again with bit 7.

  - Status register read

Bit sequence is shown as follows:

Bit Sequential	0	1	2	3	4	5	6	7
Bit Data	0	0	0	0	x	1	0	1

Note: ″x″ don't care

- Product ID read

The RDID instruction allows the user to read the manufacturer and product ID of the device. The first byte after the instruction will be the manufacture code (1CH= HOLTEK), followed by the device code (83H for 512K OTP ROM).

Product ID read, bit sequence is shown as follows:

Bit Sequential	0	1	2	3	4	5	6	7
Bit Data	0	0	0	1	x	1	0	1

Note: x: don't care

- $\overline{HOLD}$

The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the HT25LC512. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

Power-on State

When power is first applied to the device, the SO pin will be in a high-impedance state, and a high-to-low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

Programming the OTP ROM

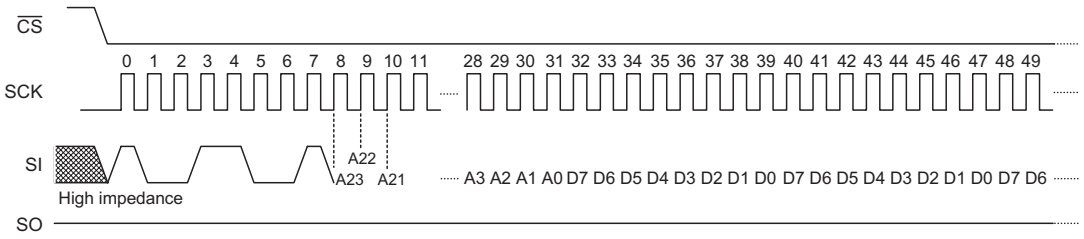
Programming the OTP ROM of the HT25LC512 via the SI (Serial Input) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the programming instruction is transmitted via the SI line followed by the byte address to the program. Then the programming data are transmitted following the address. If only one byte is to be programmed, the $\overline{CS}$ line should be driven high after one byte data has been transmitted. The programming instruction can be continued since the byte address is automatically incremented and data will continue to be shifted in. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be programmed in one continuous programming instruction.

Programming the OTP ROM, bit sequence is shown as follows:

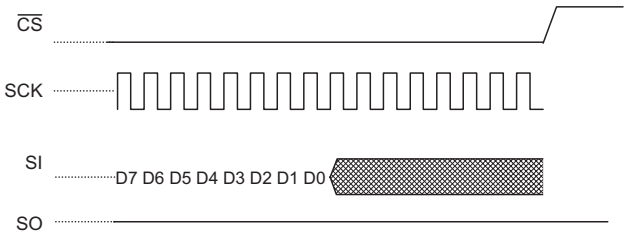
Bit Sequential	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit Data	1	0	0	1	1	0	0	1	A23	A22	A21	A20	A19	A18	A17	A16

Bit Sequential	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Bit Data	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

- Programming the OTP ROM timing (V_{PP}=12.5V)



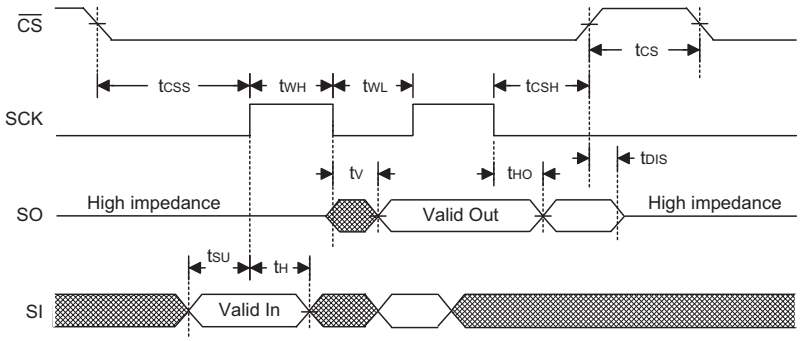
(Continue)



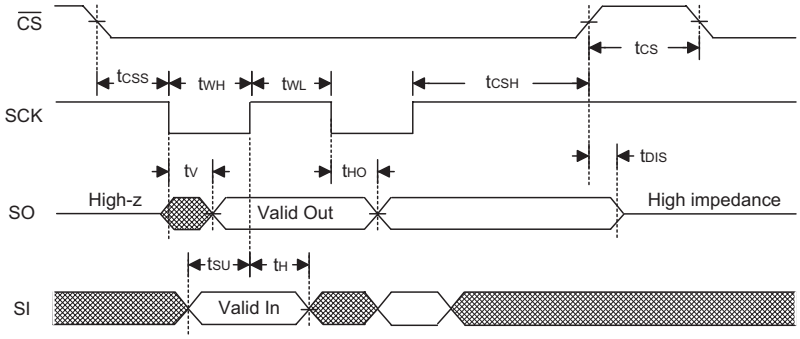
Serial Interface Waveform

Two different timing diagrams are shown. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal. Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

- Waveform 1 - Inactive clock polarity low

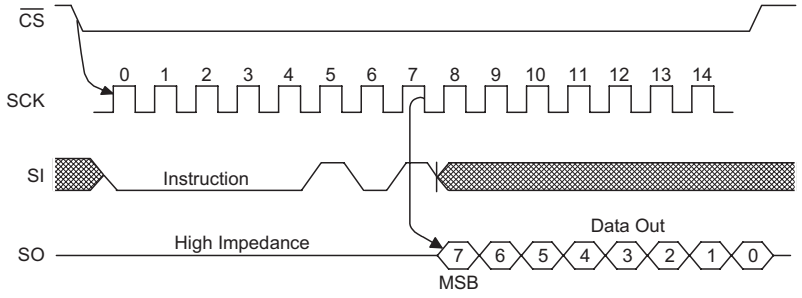


- Waveform 2 - Inactive clock polarity high

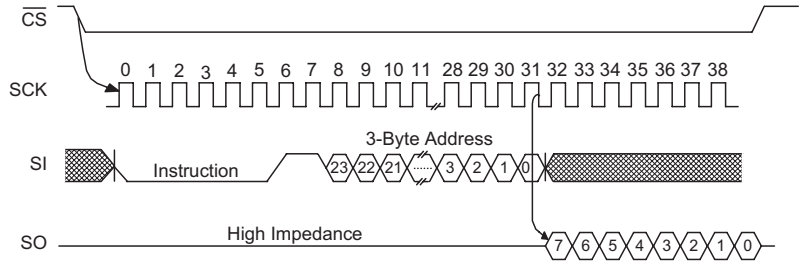


Timing Diagrams

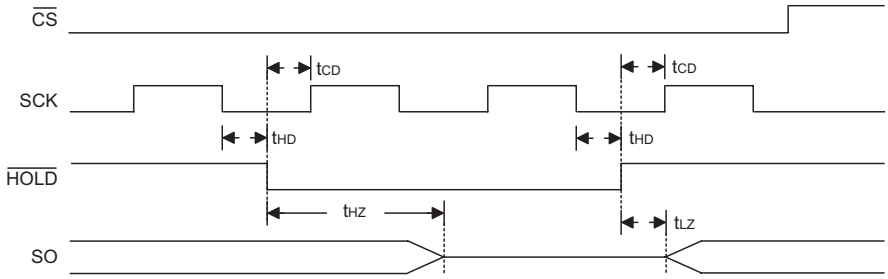
RDSR Timing



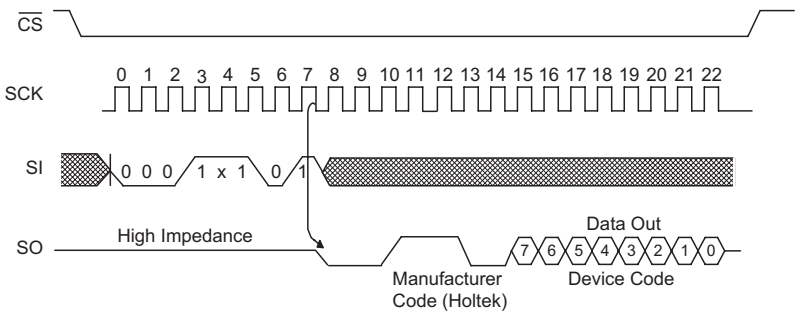
READ Timing



$\overline{\text{HOLD}}$ Timing

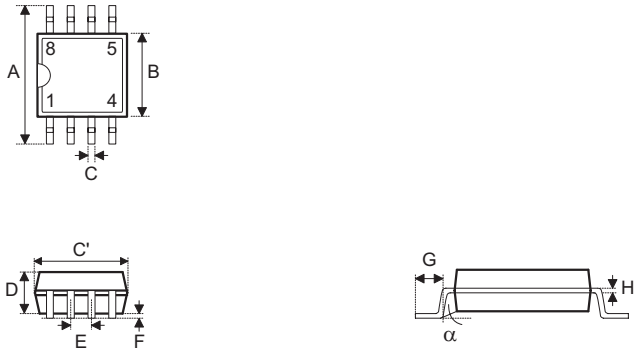


RDID Timing



Package Information

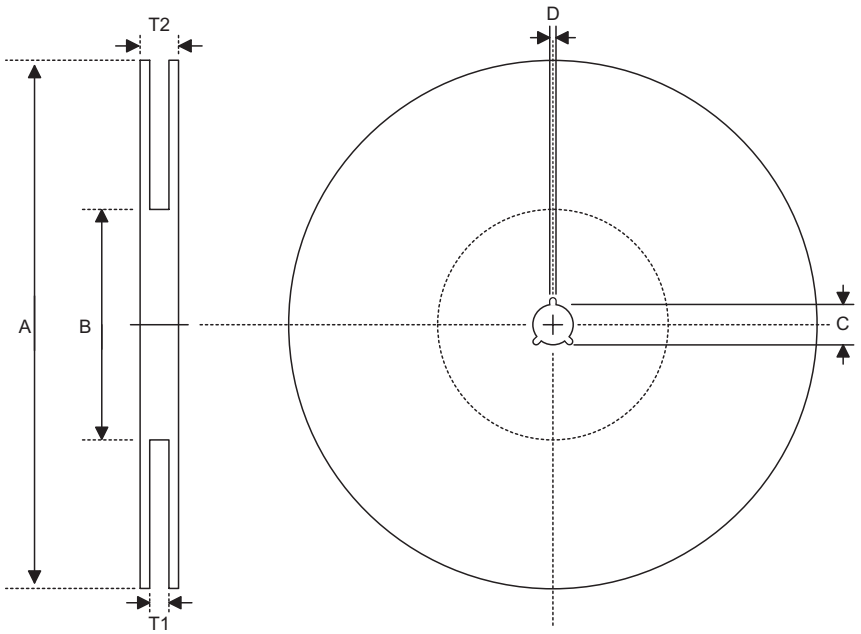
8-pin SOP (150mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	149	—	157
C	14	—	20
C′	189	—	197
D	53	—	69
E	—	50	—
F	4	—	10
G	22	—	28
H	4	—	12
α	0°	—	10°

Product Tape and Reel Specifications

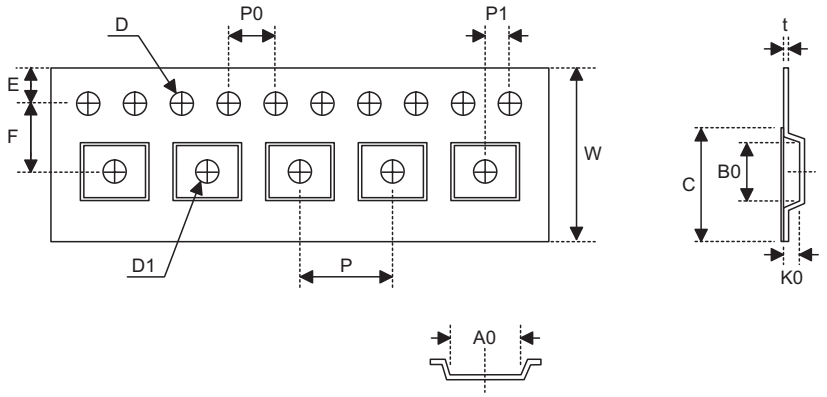
Reel Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 −0.2
D	Key Slit Width	2.0±0.15
T1	Space Between Flange	12.8+0.3 −0.2
T2	Reel Thickness	18.2±0.2

Carrier Tape Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0+0.3 −0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.20±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	9.3

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