DVD/CD RECEIVER
SERVICE MANUAL

MODEL: HT303PD
(HT303PD-D0, SH33PD-F/S/W)

P/NO : AFN73178958

JUNE, 2009

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LG

[CONTENTS]

SECTION 1. GENERAL

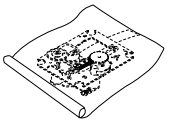
SERVICING PRECAUTIONS

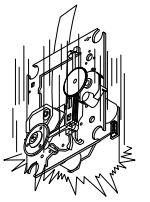
NOTES REGARDING HANDLING OF THE PICK-UP

1. Notes for transport and storage

1) The pick-up should always be left in its conductive bag until immediately prior to use.
2) The pick-up should never be subjected to external pressure or impact.

Storage in conductive bag

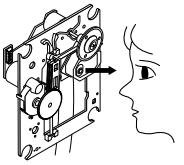




Drop impact

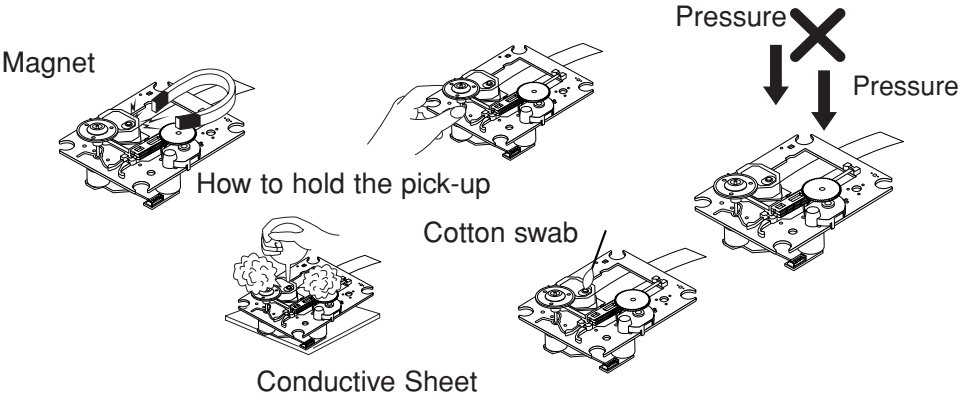
2. Repair notes

1) The pick-up incorporates a strong magnet, and so should never be brought close to magnetic materials.
2) The pick-up should always be handled correctly and carefully, taking care to avoid external pressure and impact. If it is subjected to strong pressure or impact, the result may be an operational malfunction and/or damage to the printed-circuit board.
3) Each and every pick-up is already individually adjusted to a high degree of precision, and for that reason the adjustment point and installation screws should absolutely never be touched.
4) Laser beams may damage the eyes!
   Absolutely never permit laser beams to enter the eyes!
   Also NEVER switch ON the power to the laser output part (lens, etc.) of the pick-up if it is damaged.



NEVER look directly at the laser beam, and don't allow contact with fingers or other exposed skin.

5) Cleaning the lens surface
   If there is dust on the lens surface, the dust should be cleaned away by using an air bush (such as used for camera lens). The lens is held by a delicate spring. When cleaning the lens surface, therefore, a cotton swab should be used, taking care not to distort lens.



6) Never attempt to disassemble the pick-up.
   Spring has excess pressure. If the lens is extremely dirty, apply isopropyl alcohol to the cotton swab. (Do not use any other liquid cleaners, because they will damage the lens.) Take care not to use too much of this alcohol on the swab, and do not allow the alcohol to get inside the pick-up.

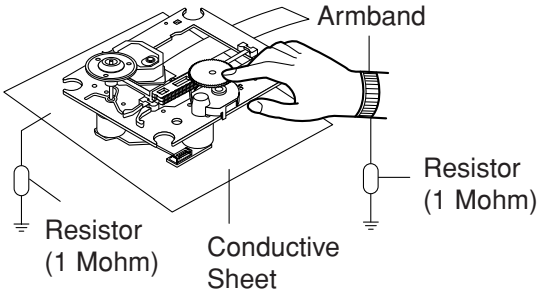
NOTES REGARDING COMPACT DISC PLAYER REPAIRS

1. Preparations

1) Compact disc players incorporate a great many ICs as well as the pick-up (laser diode). These components are sensitive to, and easily affected by, static electricity. If such static electricity is high voltage, components can be damaged, and for that reason components should be handled with care.
2) The pick-up is composed of many optical components and other high-precision components. Care must be taken, therefore, to avoid repair or storage where the temperature or humidity is high, where strong magnetism is present, or where there is excessive dust.

2. Notes for repair

1) Before replacing a component part, first disconnect the power supply lead wire from the unit
2) All equipment, measuring instruments and tools must be grounded.
3) The workbench should be covered with a conductive sheet and grounded.
   When removing the laser pick-up from its conductive bag, do not place the pick-up on the bag. (This is because there is the possibility of damage by static electricity.)
4) To prevent AC leakage, the metal part of the soldering iron should be grounded.
5) Workers should be grounded by an armband (1M Ω)
6) Care should be taken not to permit the laser pick-up to come in contact with clothing, in order to prevent static electricity changes in the clothing to escape from the armband.
7) The laser beam from the pick-up should NEVER be directly facing the eyes or bare skin.



ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will by installed.

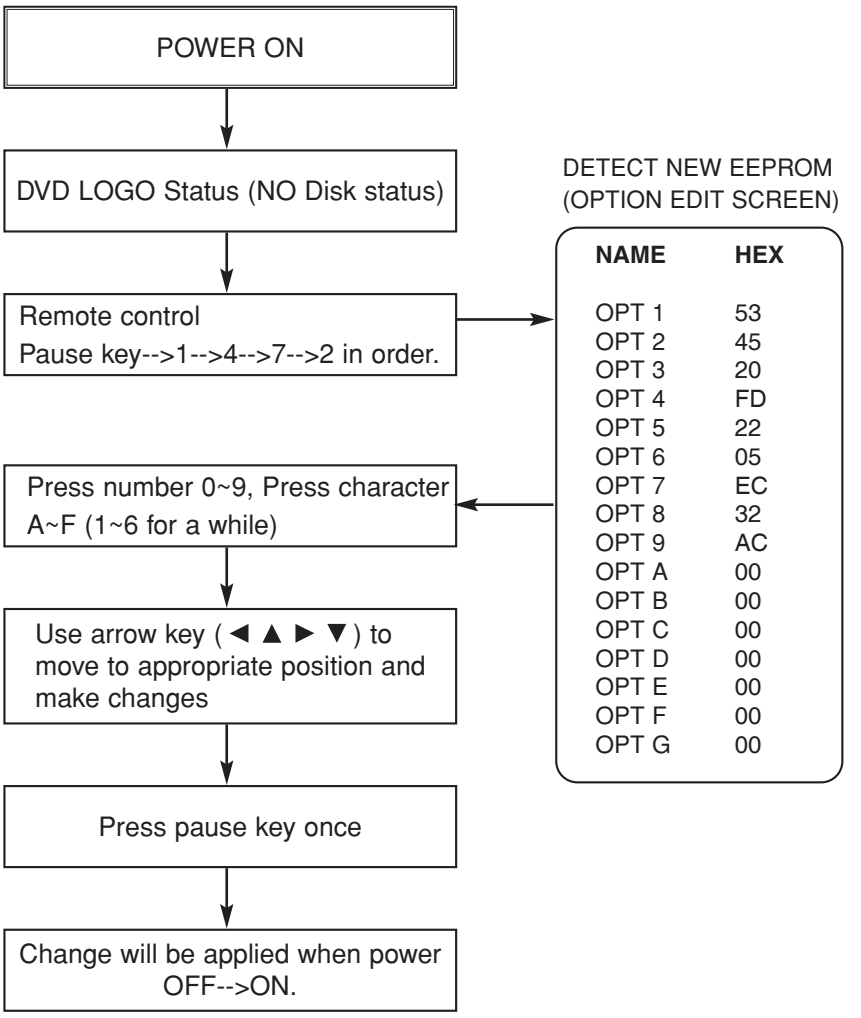
CAUTION : BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handing unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

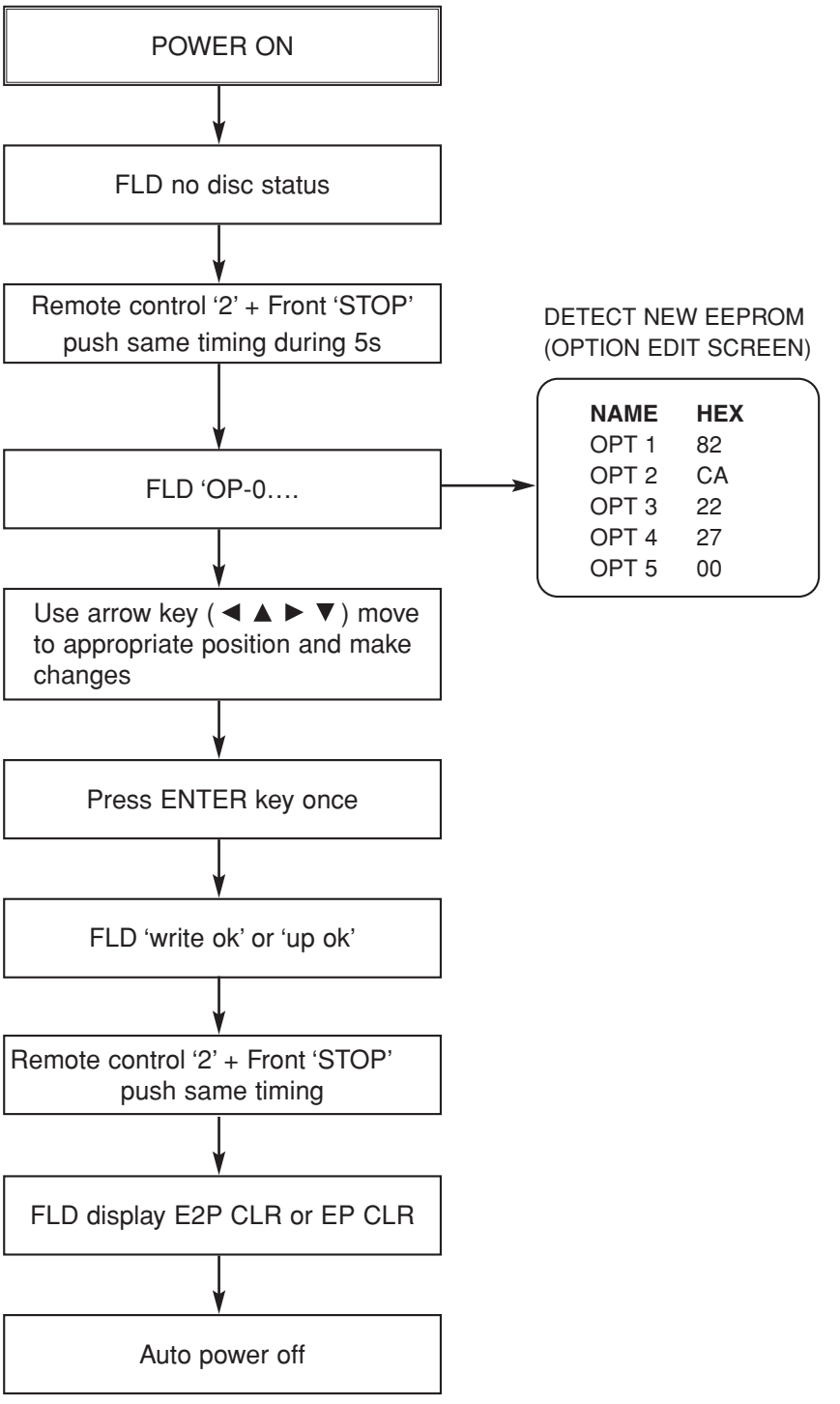
CAUTION. GRAPHIC SYMBOLS

	THE LIGHTNING FLASH WITH APROWHEAD SYMBOL. WITHIN AN EQUILATERAL TRIANGLE, IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF UNINSULATED “DANGEROUS VOLTAGE” THAT MAY BE OF SUFFICIENT MAGNITUDE TO CONSTITUTE A RISK OF ELECTRIC SHOCK.
	THE EXCLAMATION POINT WITHIN AN EQUILATERAL TRIANGLE IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF IMPORTANT SAFETY INFORMATION IN SERVICE LITERATURE.

SERVICE INFORMATION FOR EEPROM (DVD PART)



SERVICE INFORMATION FOR EEPROM (MICOM PART)



HOW TO UPDATE AUDIO MICOM & DVD PROGRAMS

1. How to update AUDIO MICOM program.

[Update using CD]

1. Change the filename to download as “(MODEL NAME)_(Version).HEX”. Only upper cases are permitted.
   ex) HT303PD : “HT303PD_0709081.HEX”
2. Copy the file to the root folder of a CD and burn it.
3. Insert the CD to the SET, and move to the DVD function. Then the upgrade process will be started with the upgrade information.
4. If the upgrade process is complete, the set will be rebooted with “Complete” message.

[Update using USB]

1. Change the filename to download as “(MODEL NAME)_(Version).HEX”. Only upper cases are permitted.
   ex) HT303PD : “HT303PD_0709081.HEX”
2. Copy the file to the root folder of USB storage.
3. Put the USB into the SET, and move to the USB function. Then the upgrade process will be started with the upgrade information.
4. If the upgrade process is complete, the set will be rebooted with “Complete” message.

2. How to update DVD program.

[Update using CD]

1. Rename the filename to download as “TARGET.BIN” in upper cases.
2. Copy the file to “\MTK_UPG\” folder of CD, and burn it.
   ex) P:\MTK_UPG\TARGET.BIN
3. Insert the CD to the SET, then after a while the CD tray will be opened with upgrade information on the screen.
4. Remove the CD, and press UP key in remote controller.
5. Remove and reconnect the power cable when it changes to logo screen from upgrade information. Then the upgrade process is completed.

[Update using USB]

1. Rename the filename to download as “TARGET.BIN” in upper cases.
2. Copy the file to “\MTK_UPG\” folder of the formatted USB, and burn it.
   ex) P:\MTK_UPG\TARGET.BIN
3. Move to the USB function, and insert the USB to the set. The upgrade information will be shown on the screen.
4. Remove the USB, press UP key of the remote control.
5. Remove and reconnect the power cable when it changes to logo screen from upgrade information. Then the upgrade process is completed.

SPECIFICATIONS

GENERAL

Power supply	Refer to main label
Power consumption	Refer to main label
Net Weight	2.5 kg
External dimensions (W x H x D)	360 x 62 x 305 mm
Operating conditions	Temperature: 5°C to 35°C, Operation status: Horizontal
Operating humidity	5% to 85%

AMPLIFIER

Output Power (* Depending on the sound mode settings and the source, there may be no sound output.)	Front: 45 W + 45 W (Rated Output Power 30 W, THD 10 %) Centre*: 45 W Surround*: 45 W + 45 W (Rated Output Power 30 W, 4 Ωat 1 kHz, THD 10 %) Subwoofer*: 75 W (Rated Output Power 60 W, 8 Ωat 30 Hz, THD 10 %)

SPEAKERS

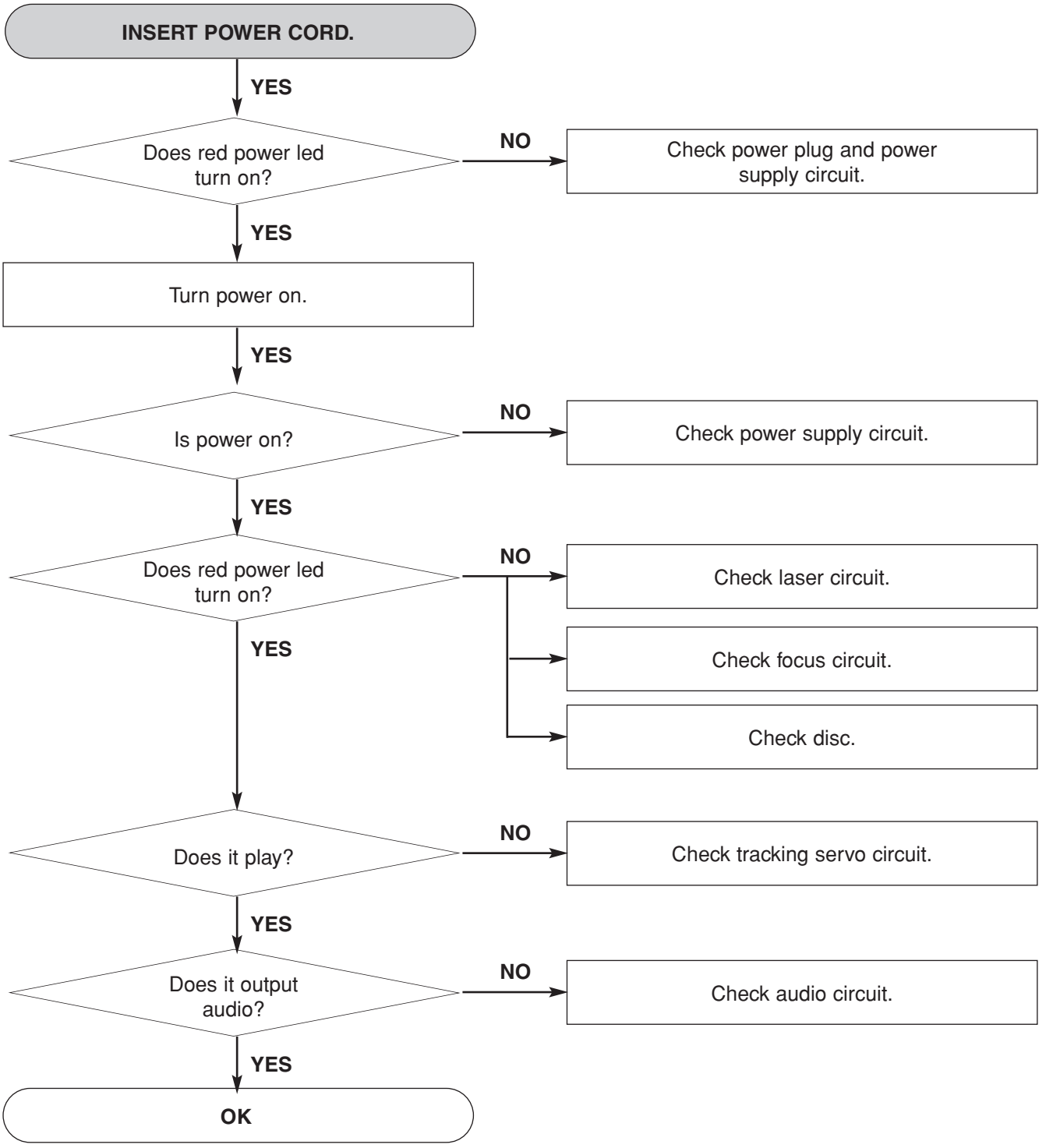
	Front Speaker	Center/Rear Speaker	Passive Subwoofer
	SH33PD-F	SH33PD-S	SH33PD-W
Impedance	4 Ω	4 Ω	8 Ω
Net Dimensions (W x H x D)	260 x 1100 x 260 mm	99 x 114 x 86 mm	156 x 325 x 320 mm
Net Weight (1EA)	3.0 kg	0.37 kg	3.5 kg

Designs and specifications are subject to change without notice.

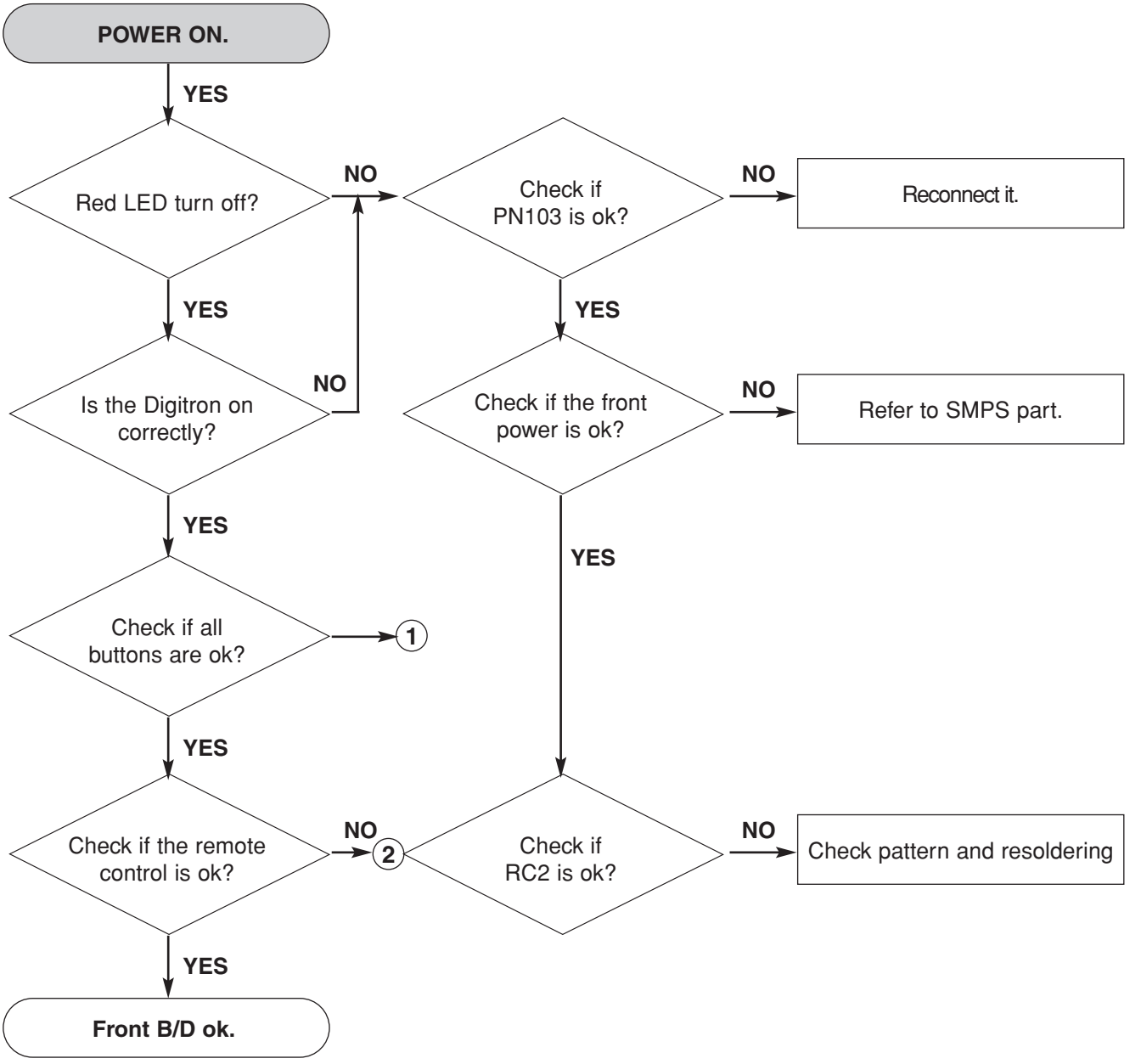
SECTION 2. ELECTRICAL PART

TROUBLESHOOTING GUIDE

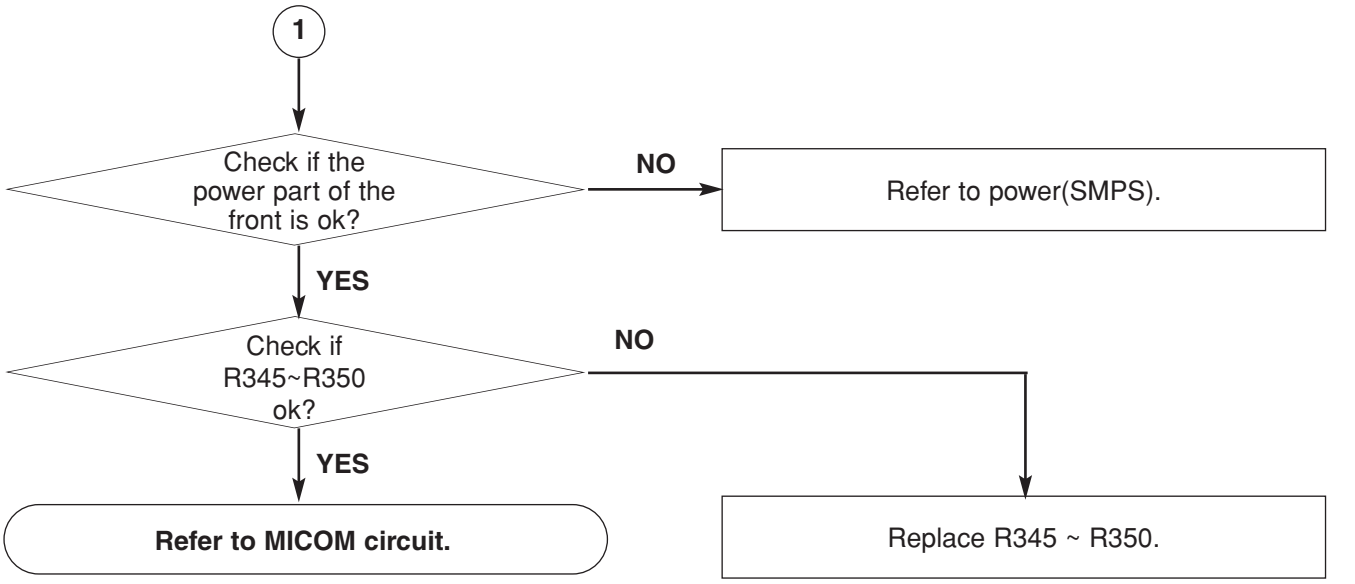
1. Power Supply Circuit

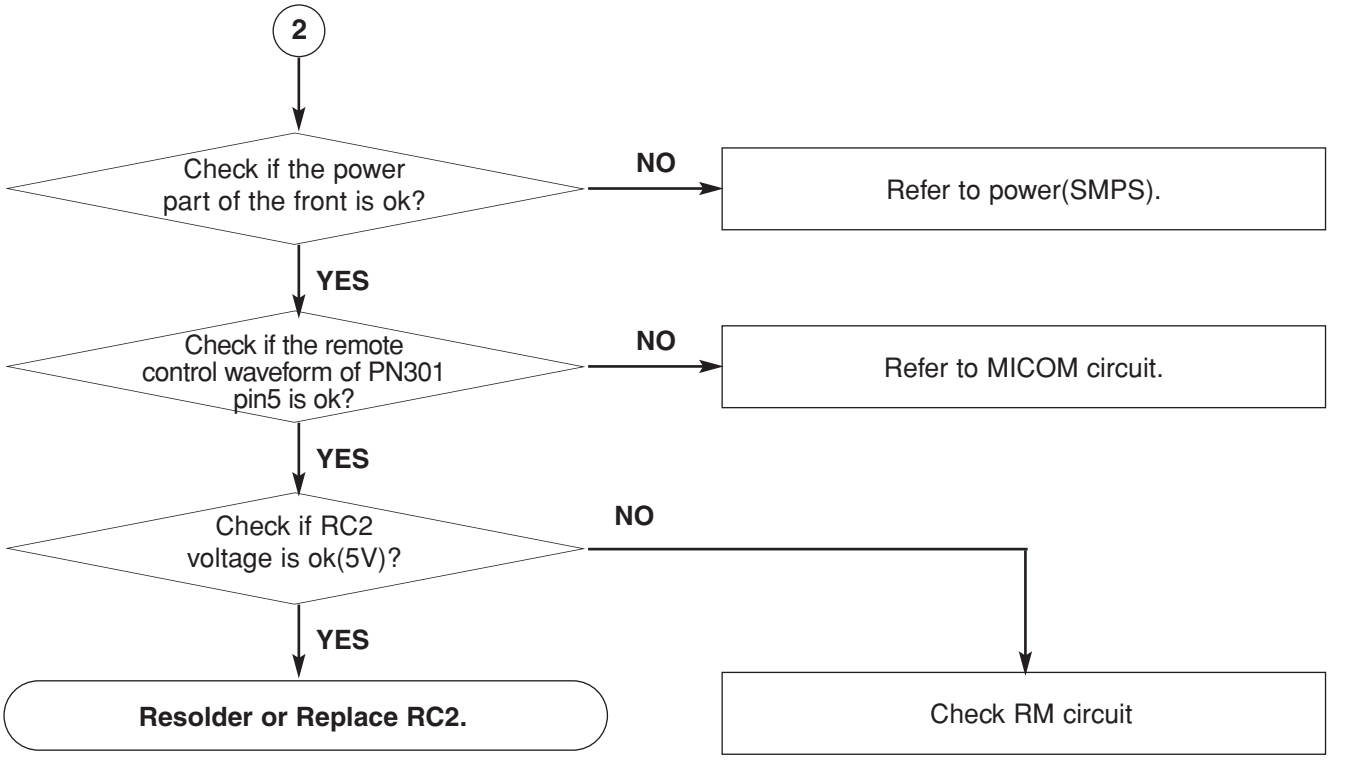


2. Front circuit (1/2)

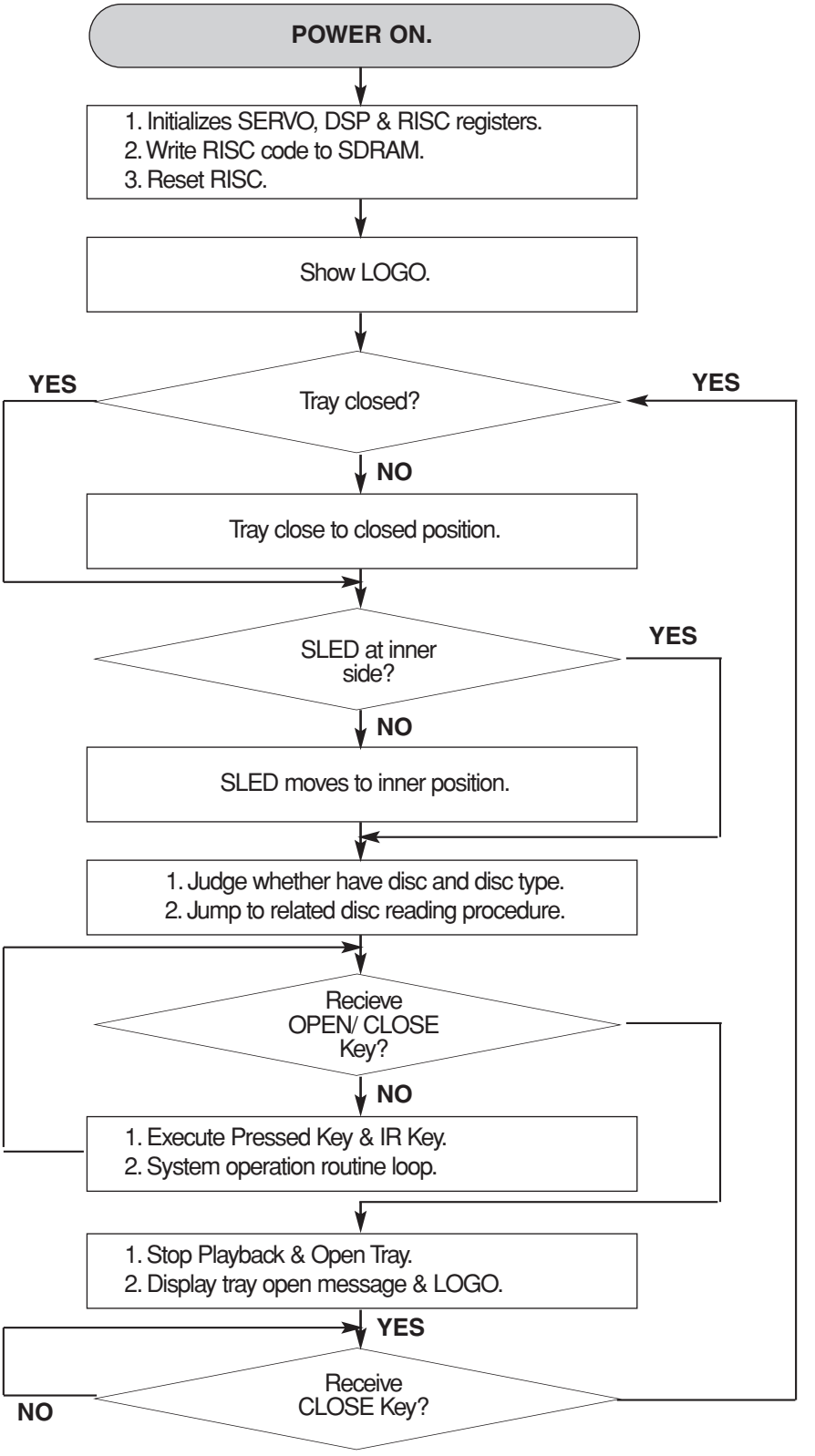


3. Front circuit (2/2)

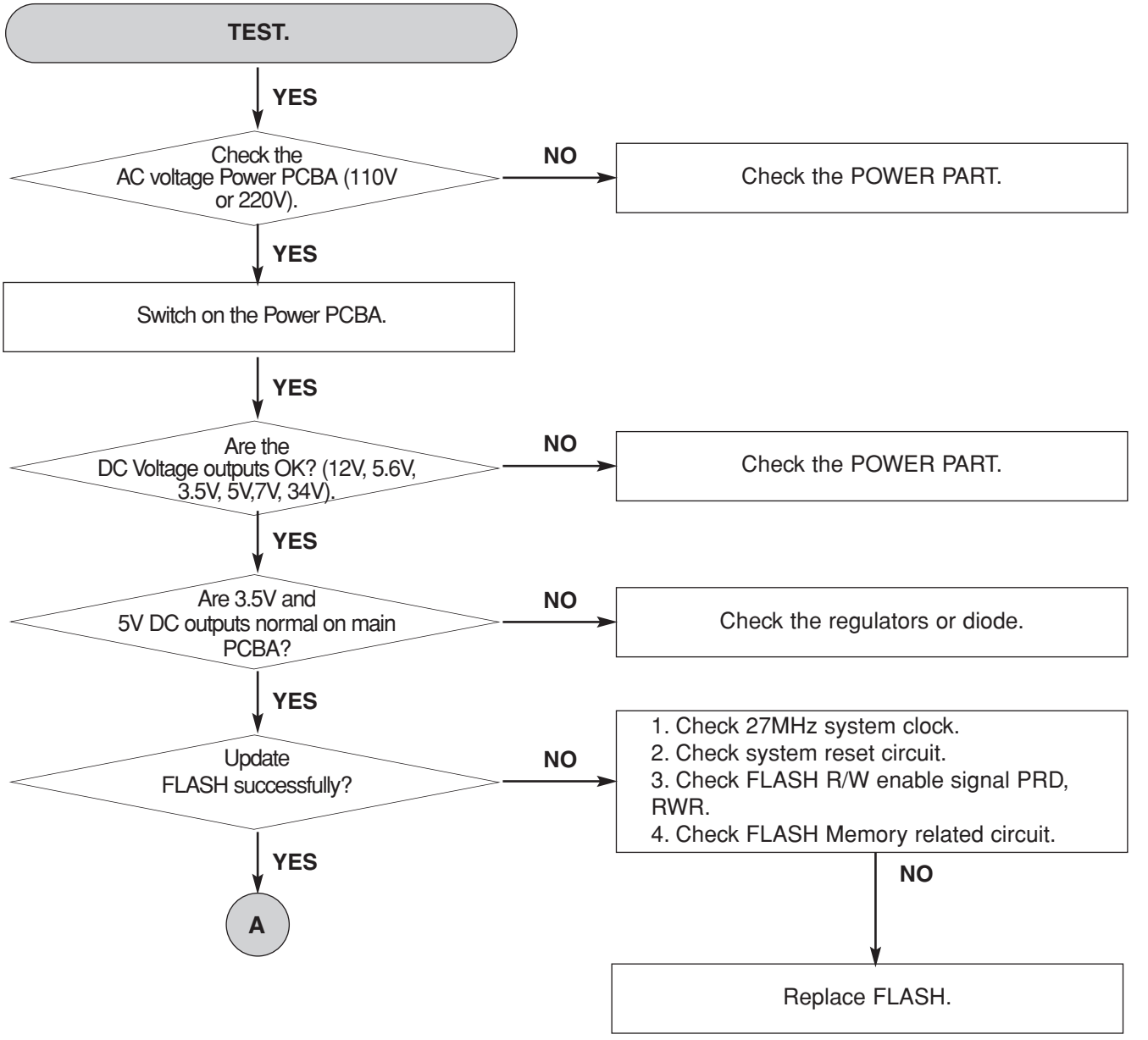


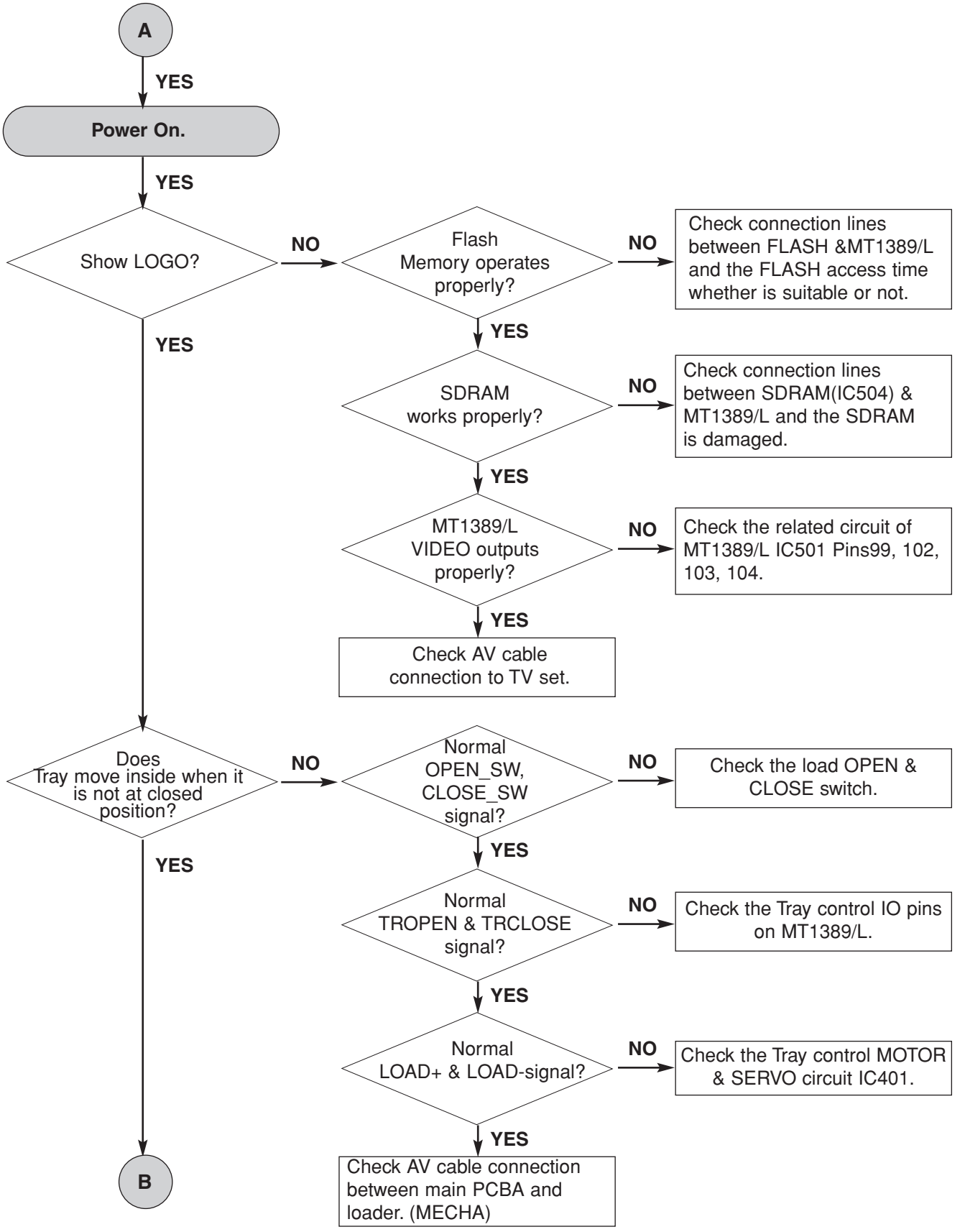


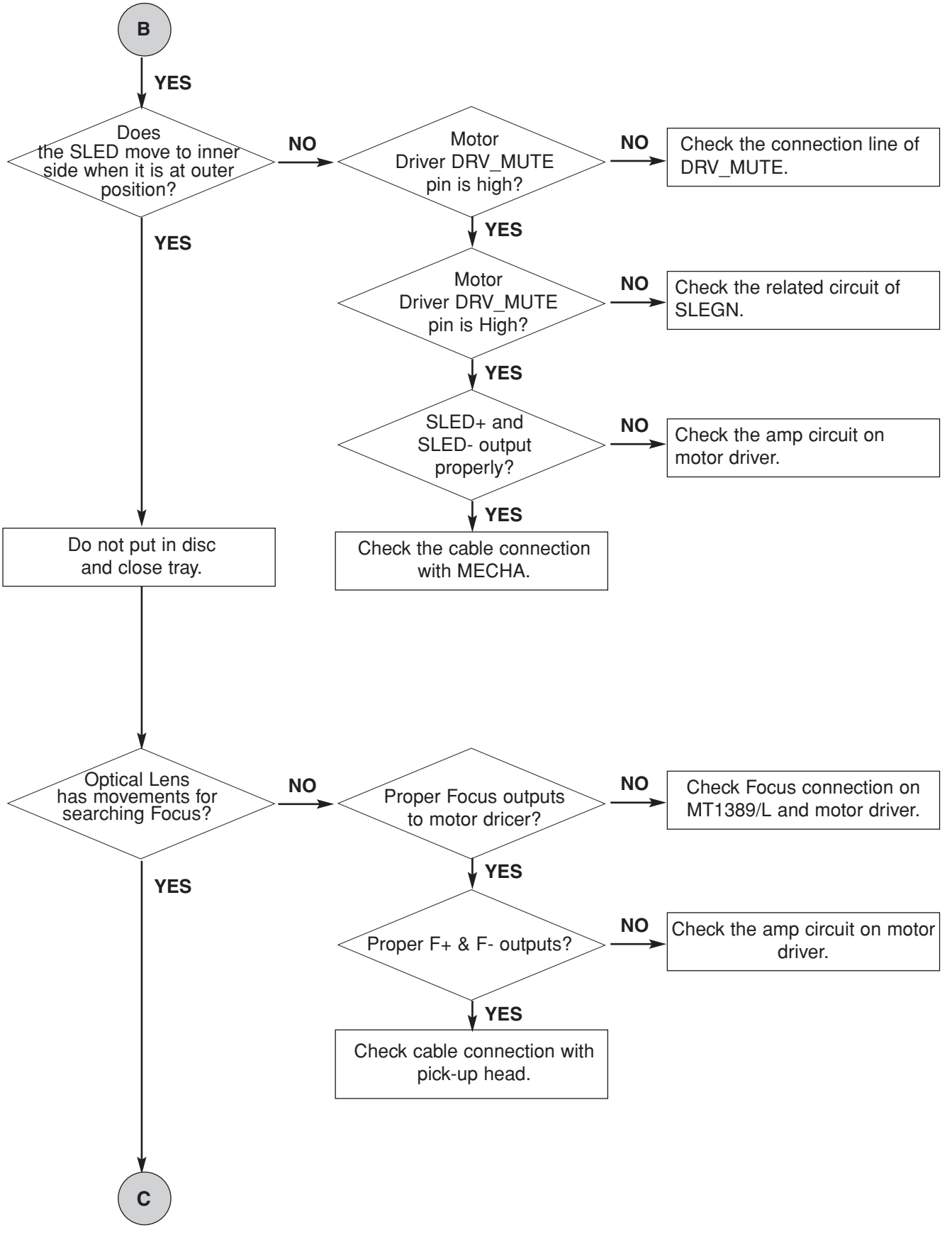
4. System operation flow

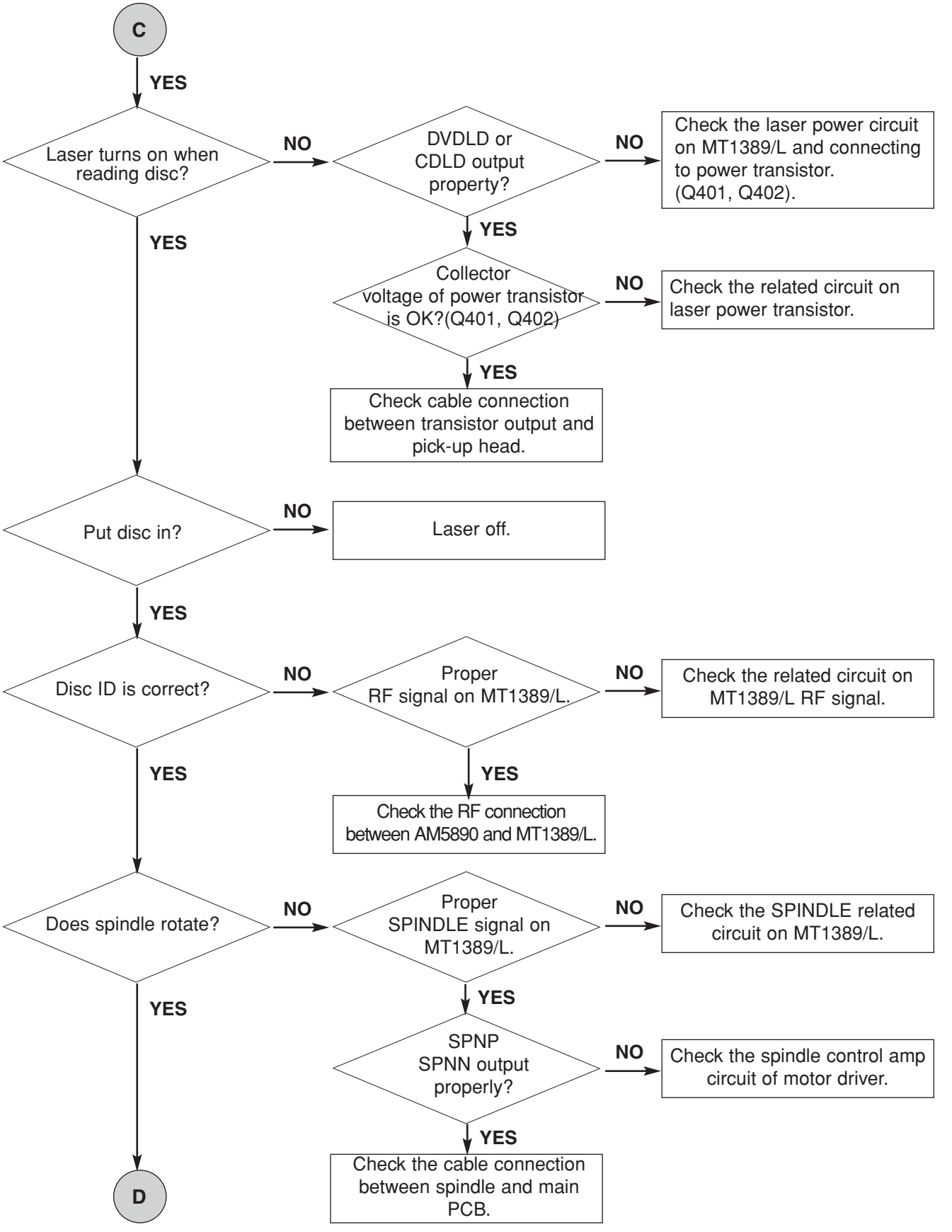


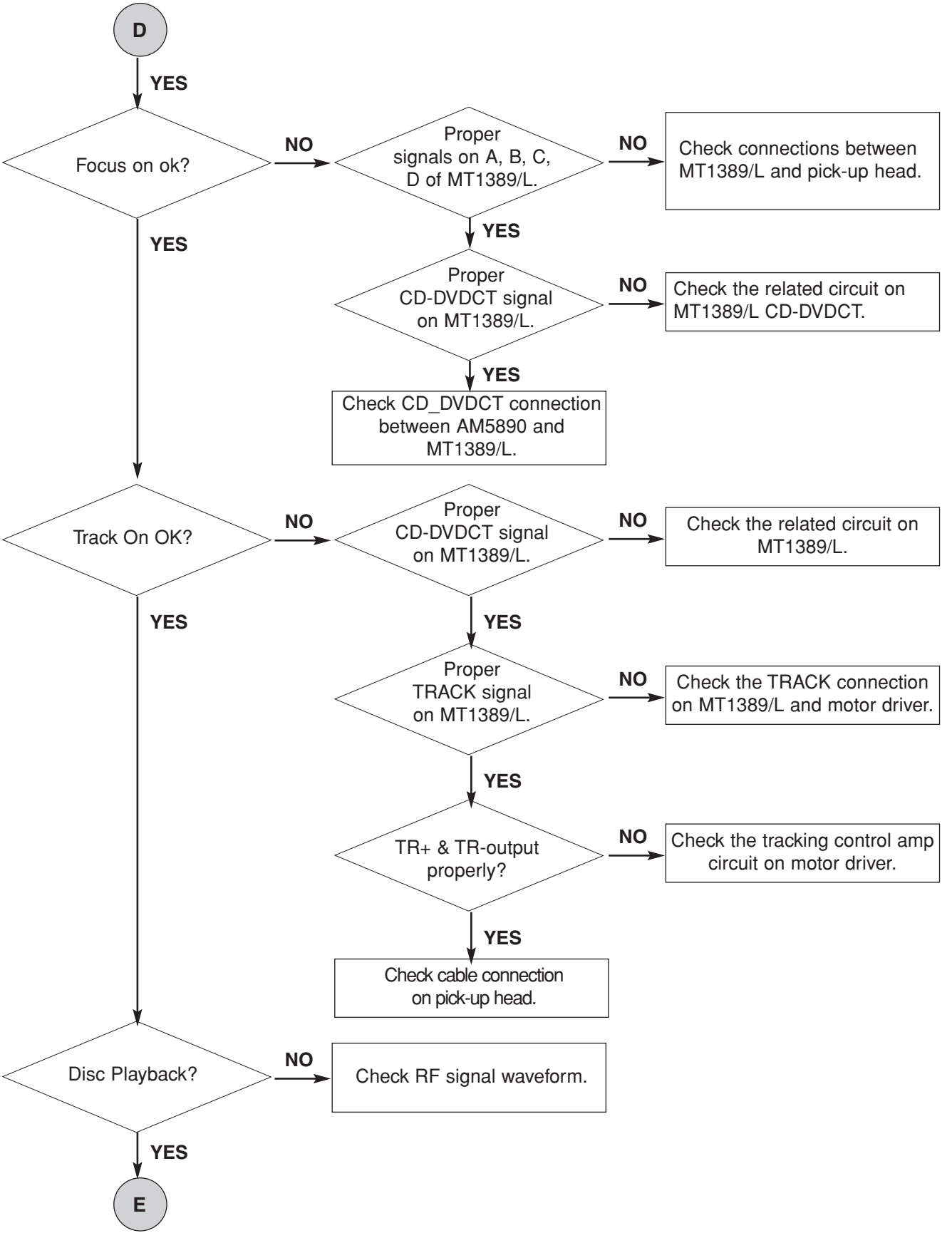
5. Test & debug flow

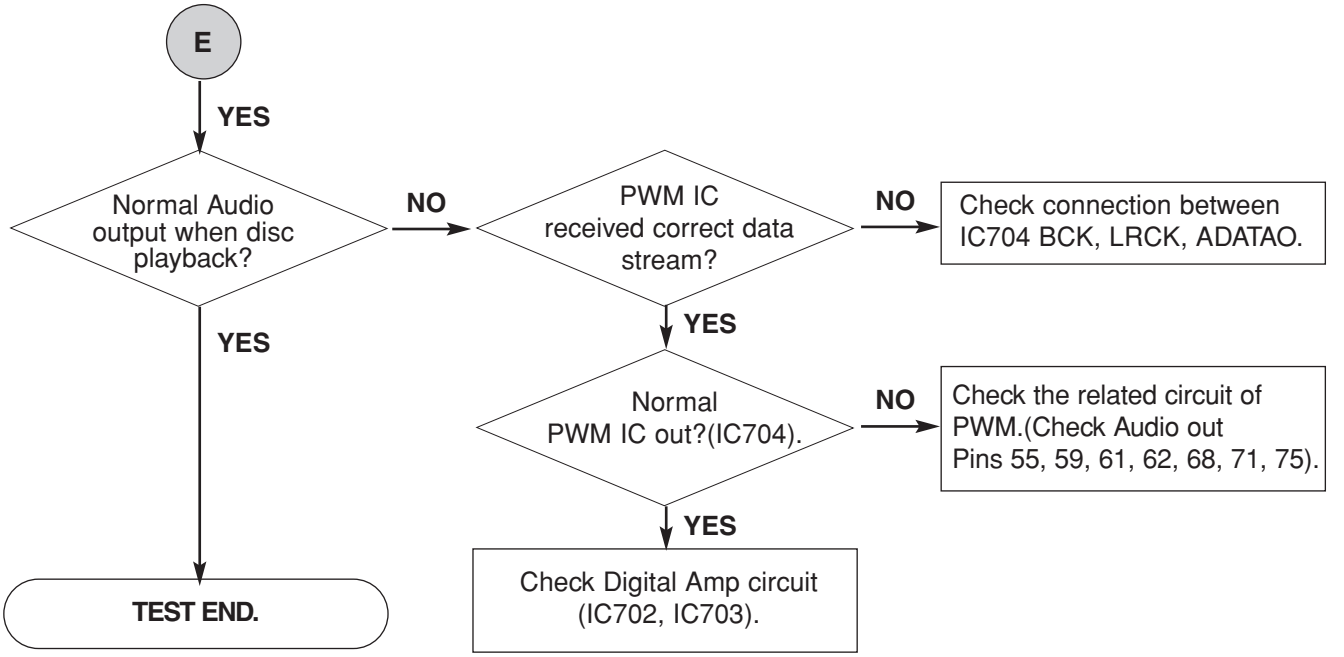




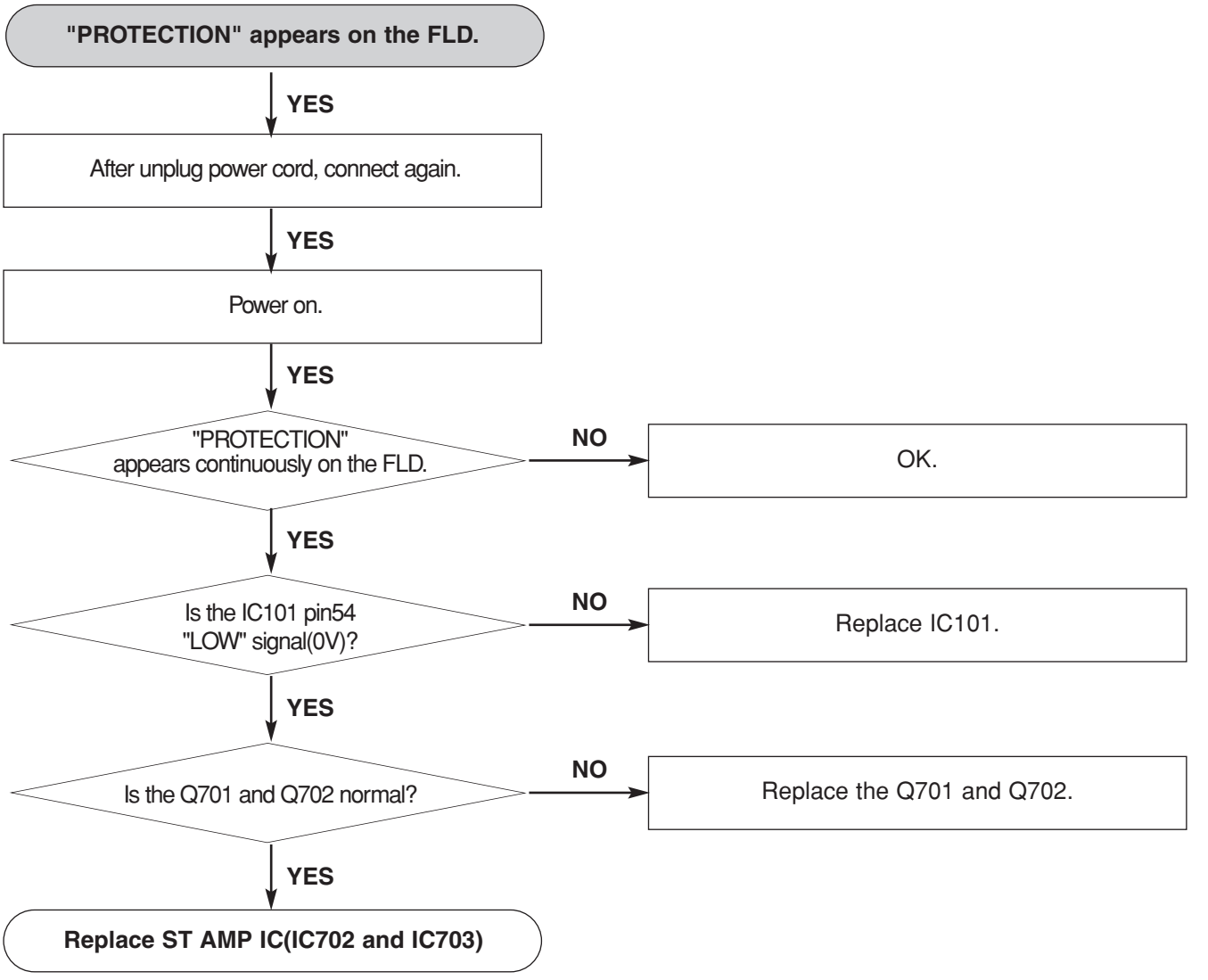




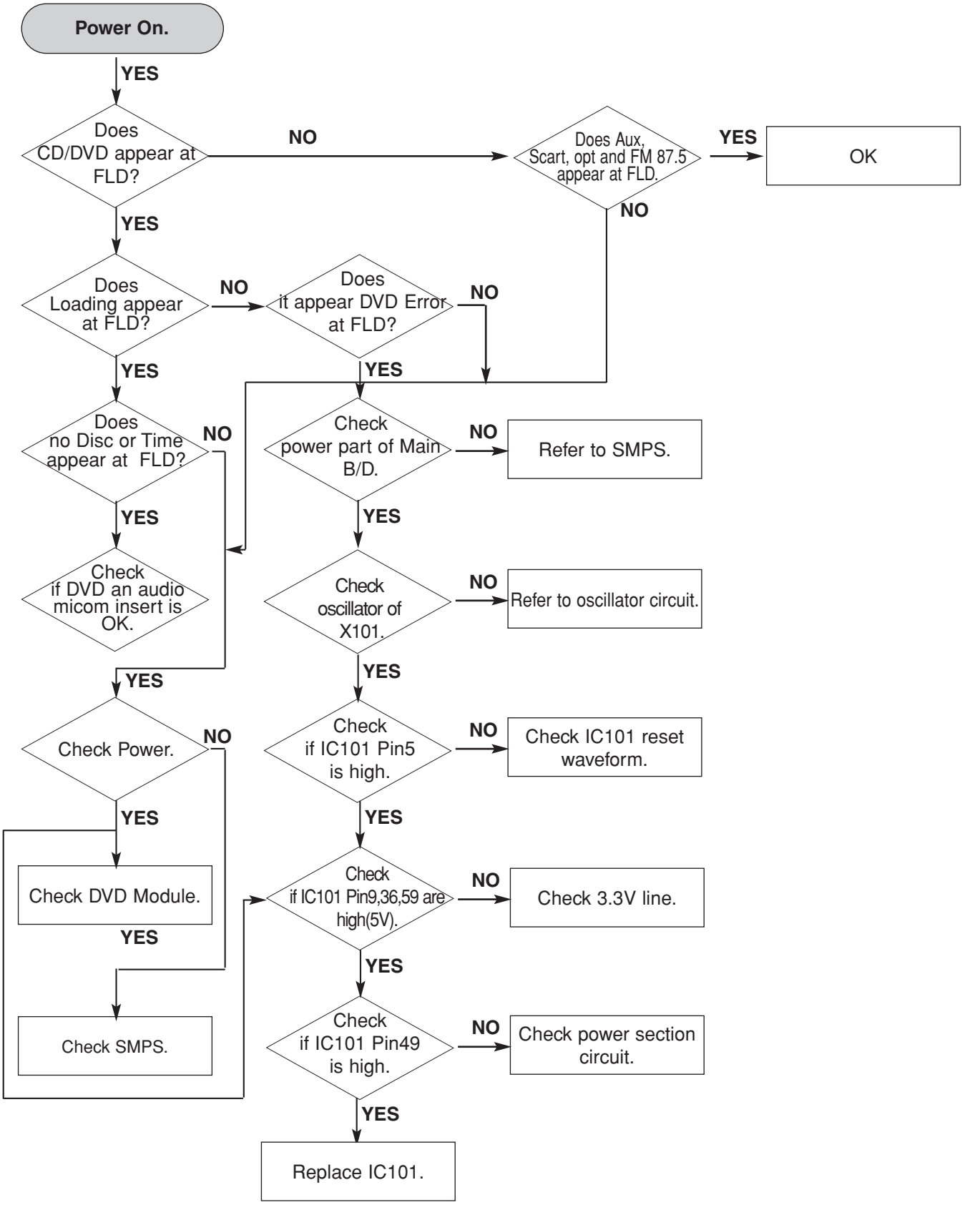




6. AMP Protection



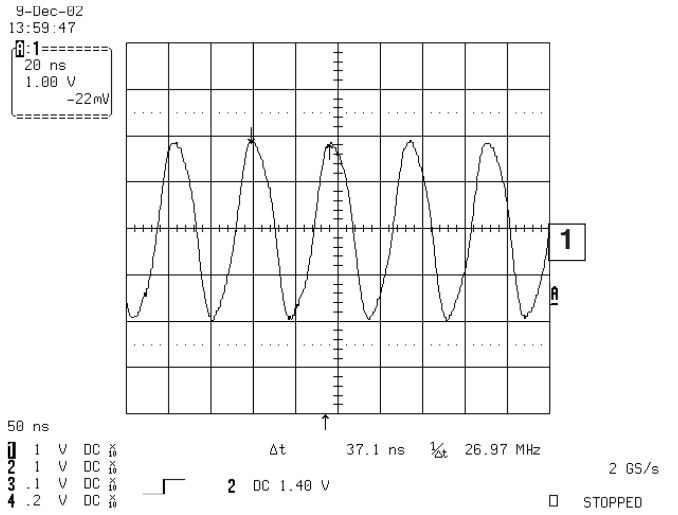
7. AUDIO µ-COM Circuit(DVD & AMP)



DETAILS AND WAVEFORMS ON SYSTEM TEST AND DEBUGGING

1. SYSTEM 27MHz CLOCK,RESET,FLASH R/W SIGNAL

1) MT1389/L main clock is at 27MHz(X501)



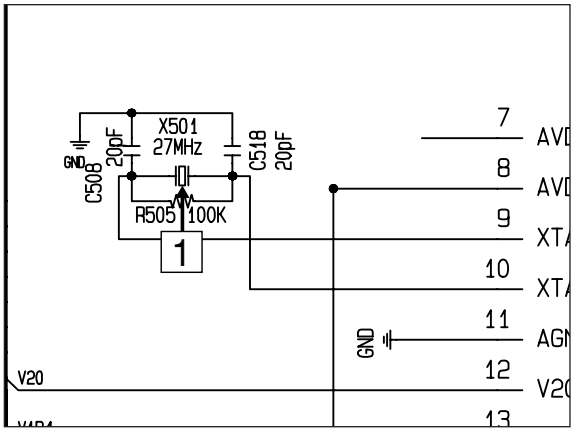


FIG 1-1

2) MT1389/L reset is high active.

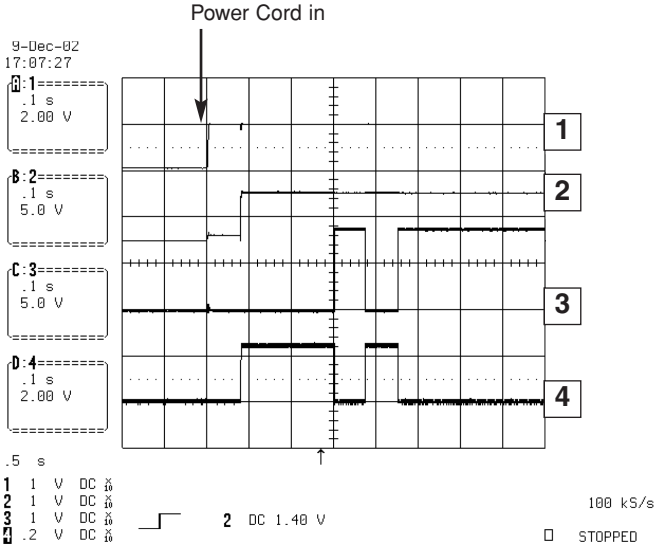
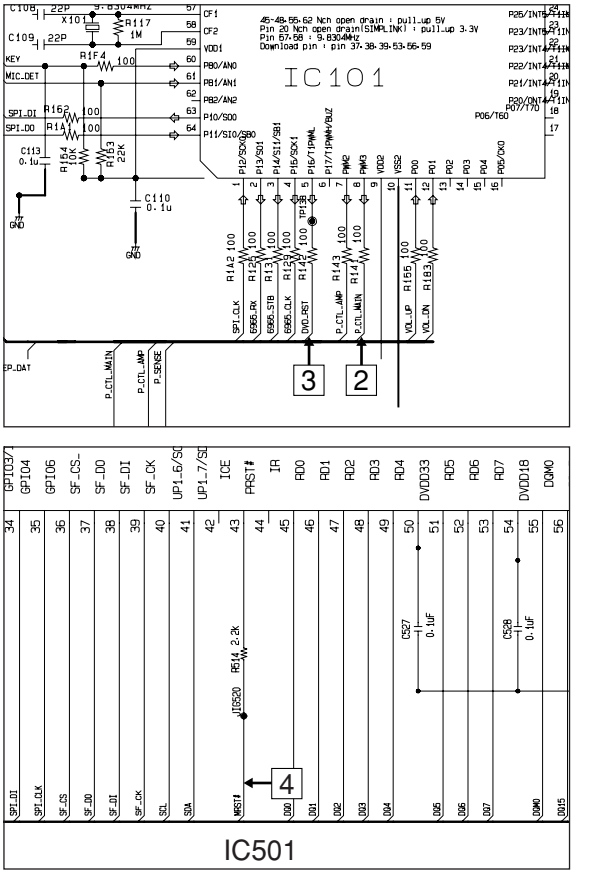


FIG 1-2



3) Flash R/W enable signal during download(Downloading)

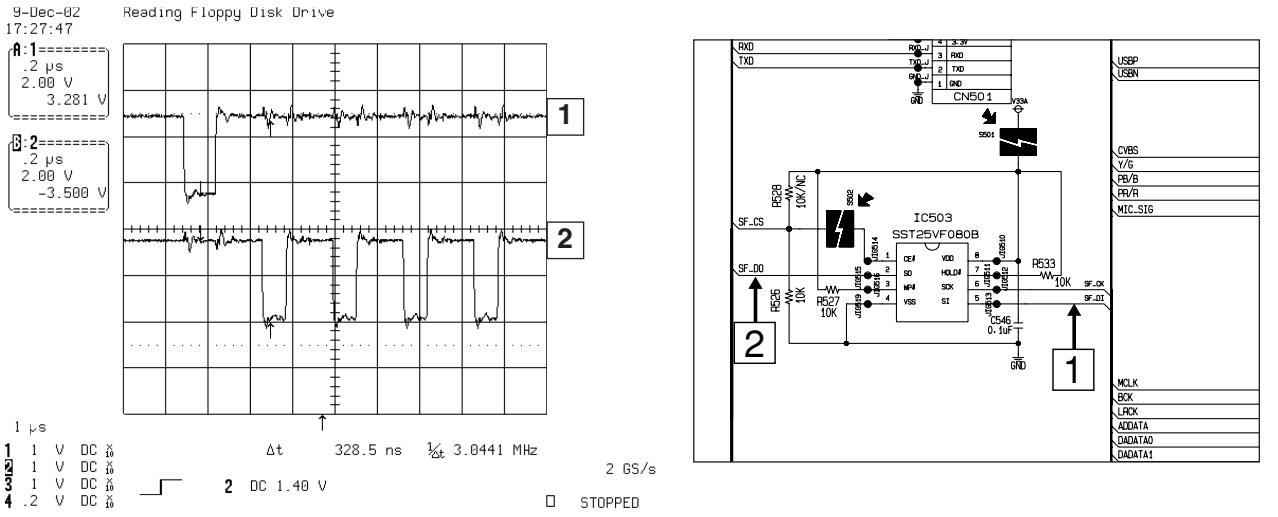


FIG 1-4

2. SDRAM CLOCK

1) MT1389/L main clock is at 27MHz(X501)

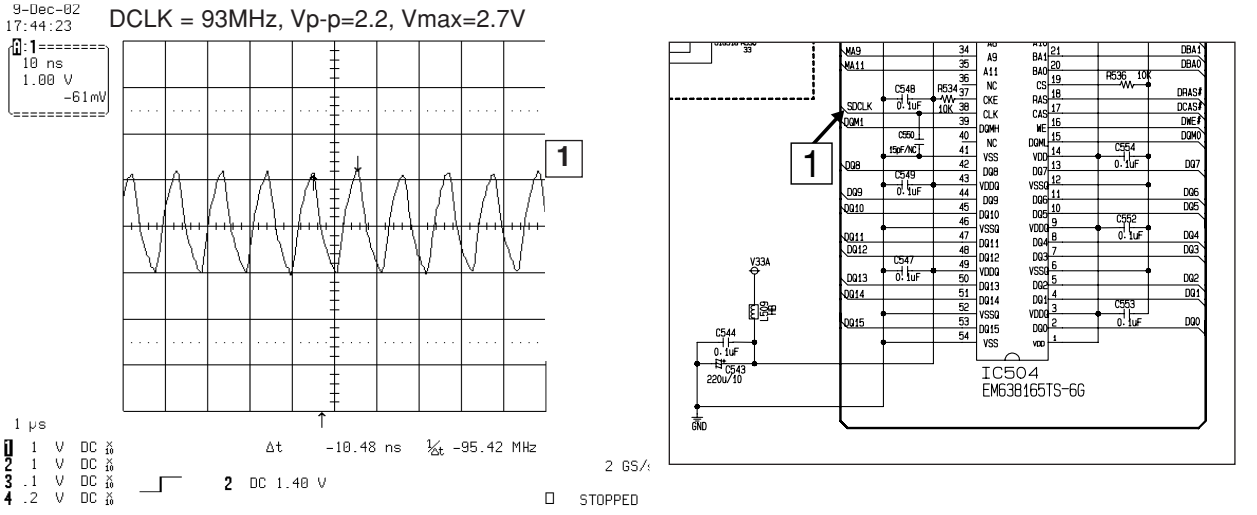


FIG 2-1

3. TRAY OPEN/CLOSE SIGNAL

1) Tray open/close waveform

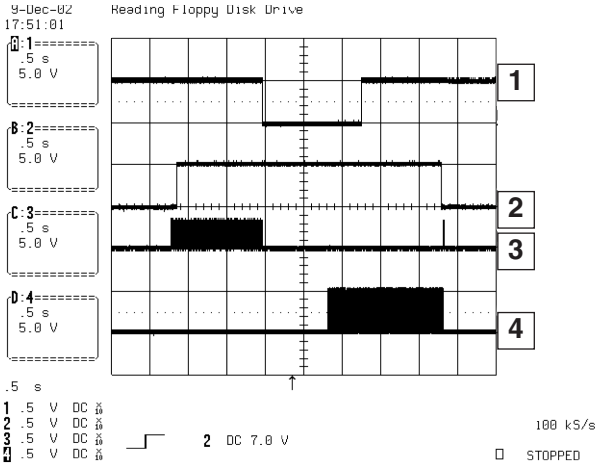


FIG 3-1

2) Tray close waveform

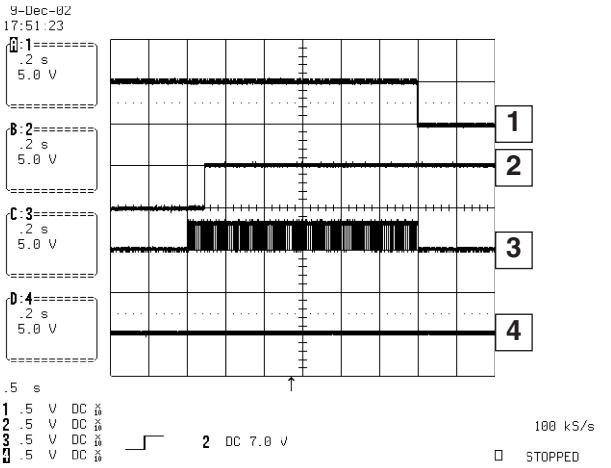


FIG 3-2

3) Tray open waveform

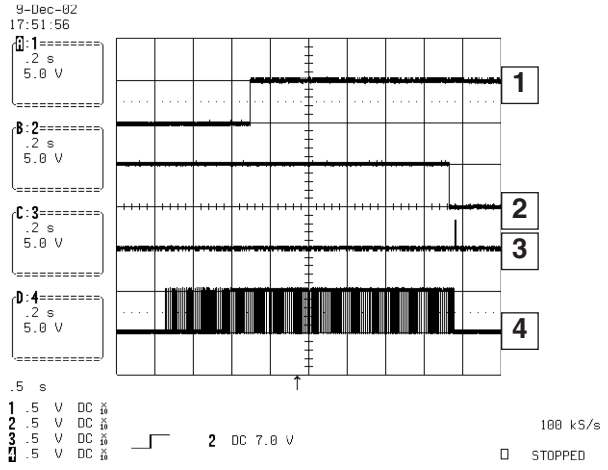
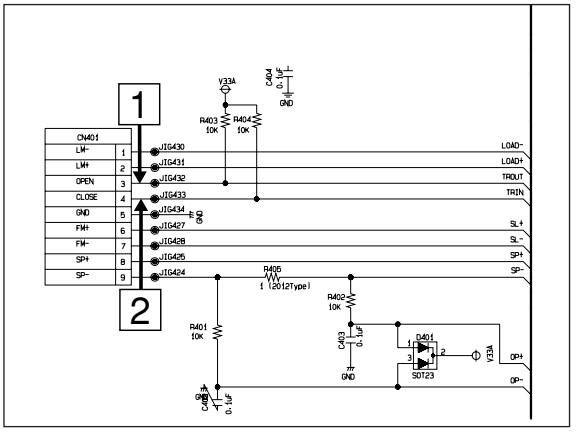
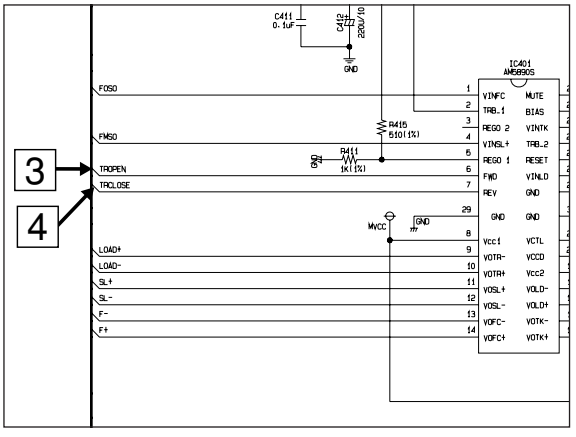


FIG 3-3





4. SLED CONTROL RELATED SIGNAL (NO DISC CONDITION)

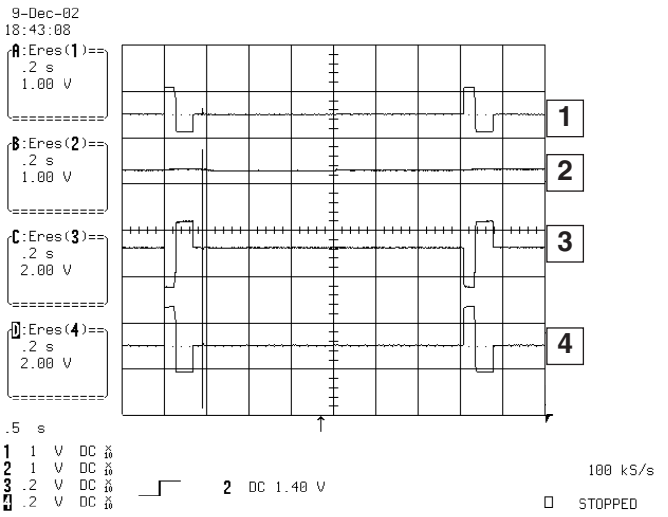
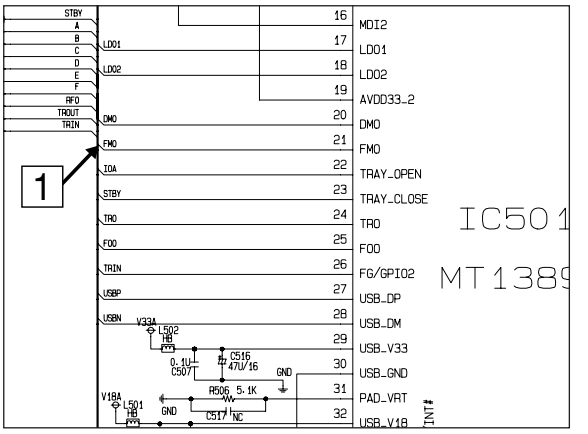
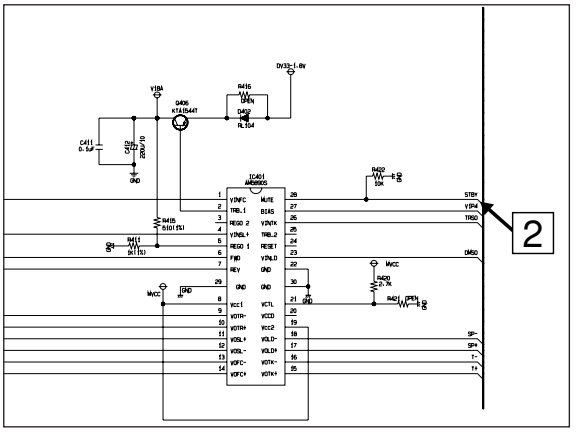
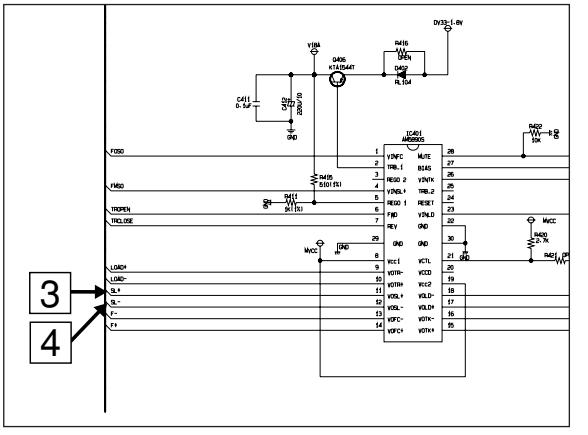


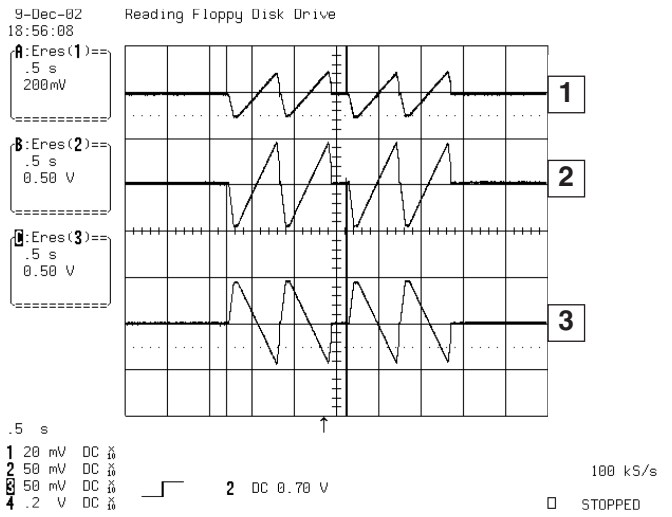
FIG 4-1

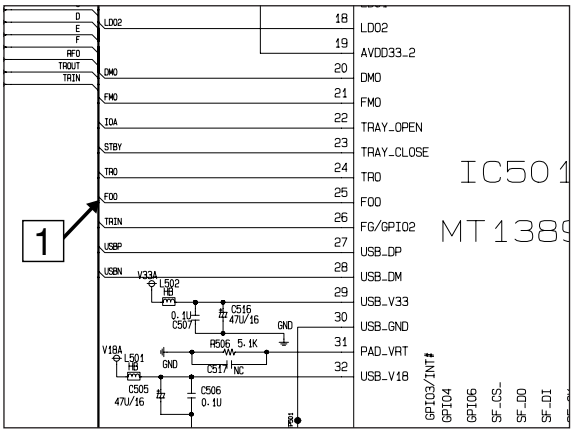






5. LENS CONTROL RELATED SIGNAL(NO DISC CONDITION)





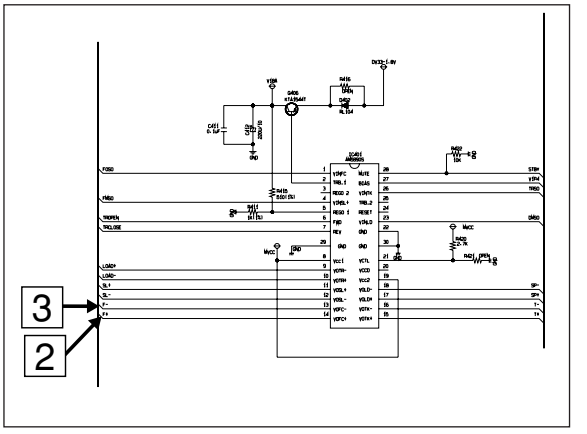
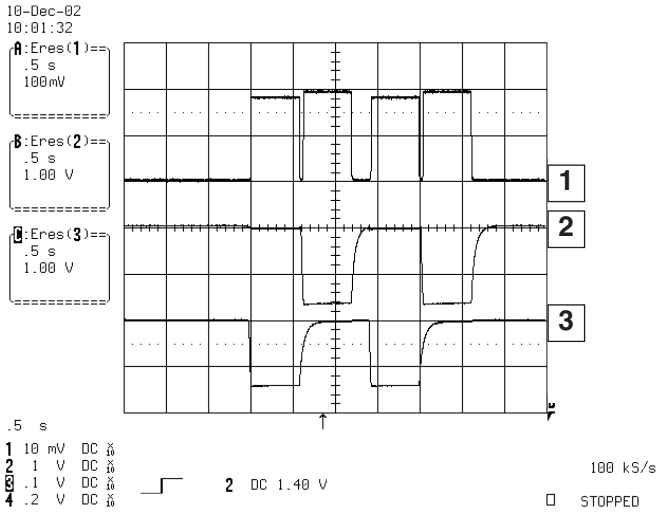


FIG 5-1

6. LASER POWER CONTROL RELATED SIGNAL(NO DISC CONDITION)



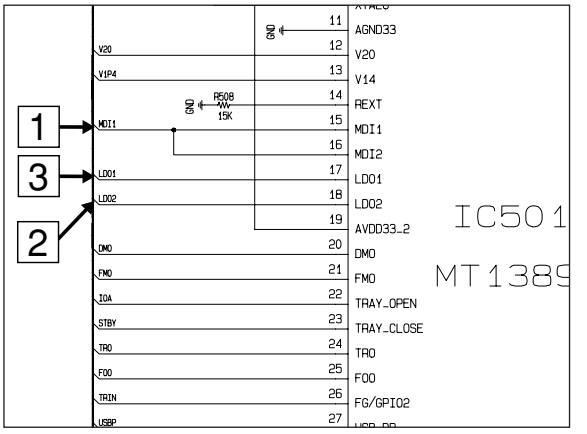


FIG 6-1

7. DISC TYPE JUDGEMENT WAVEFORMS

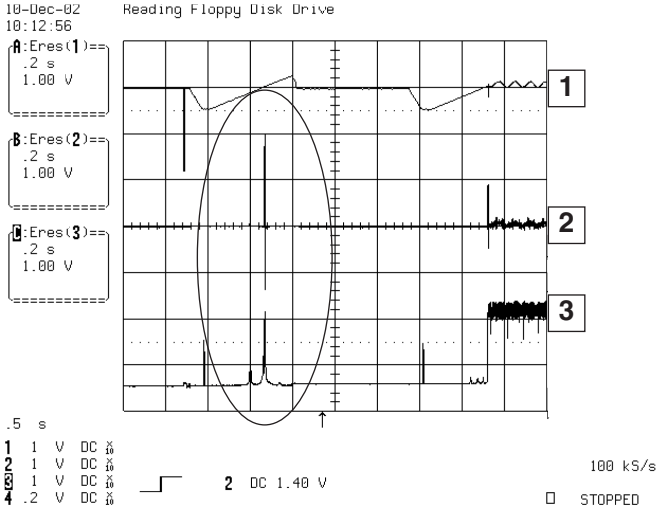


FIG 7-1 (DVD)

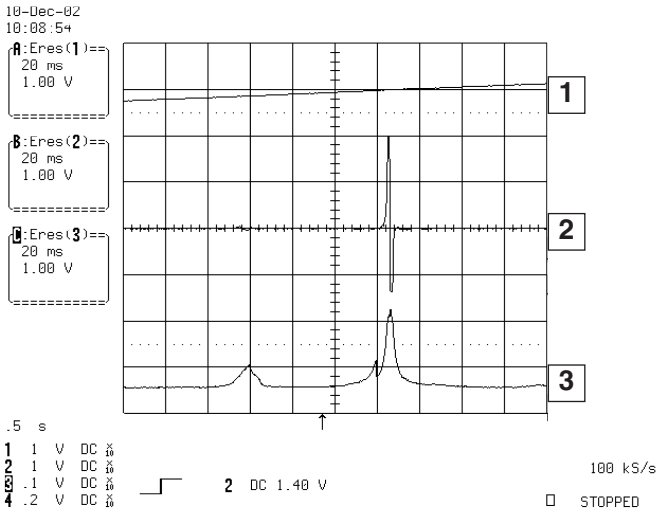
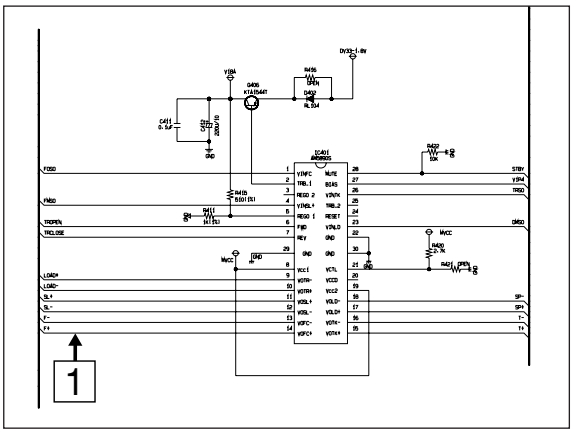
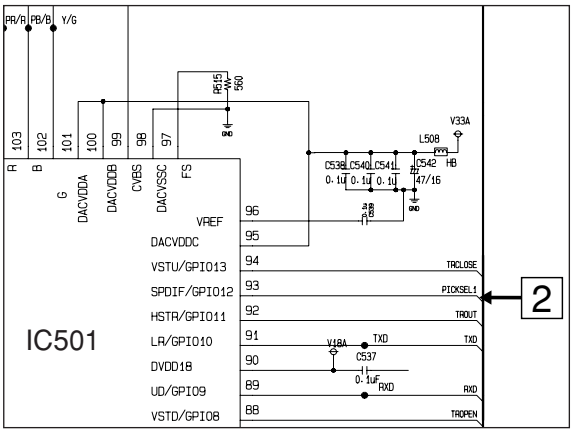
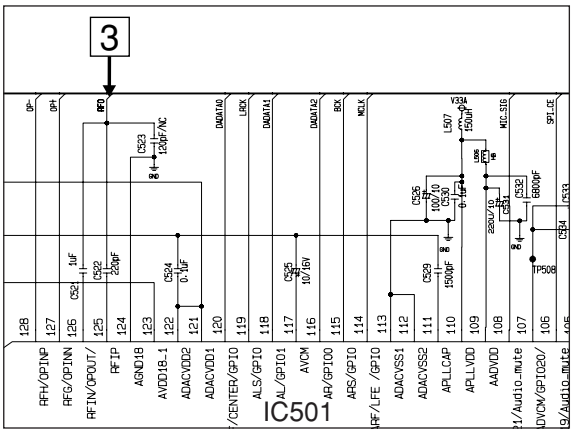
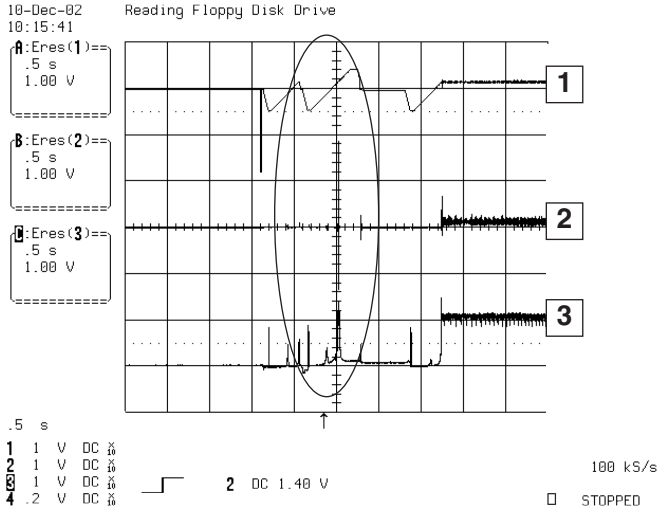


FIG 7-2 (DVD)









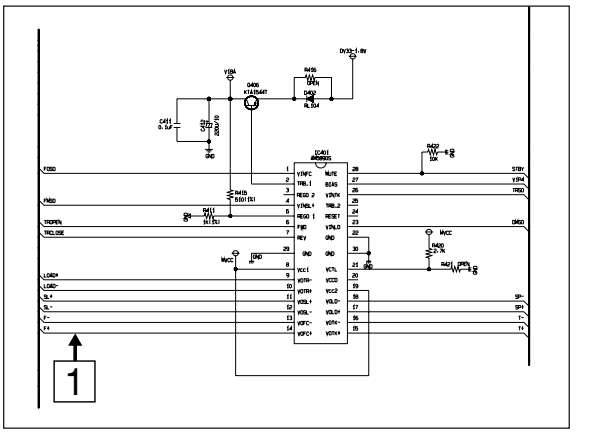
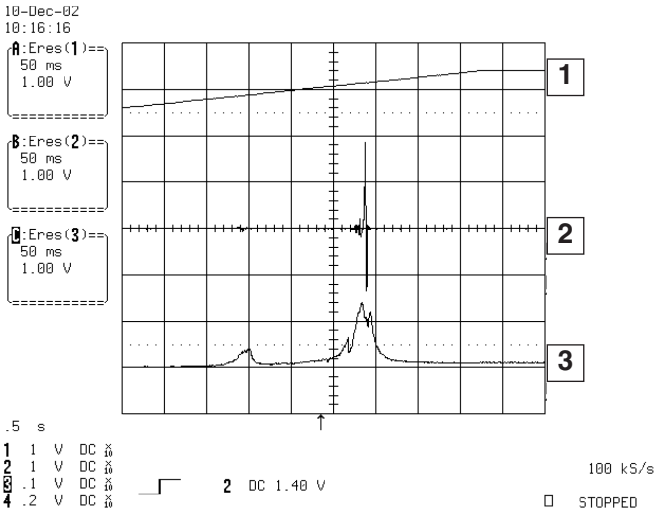


FIG 7-3 (CD)



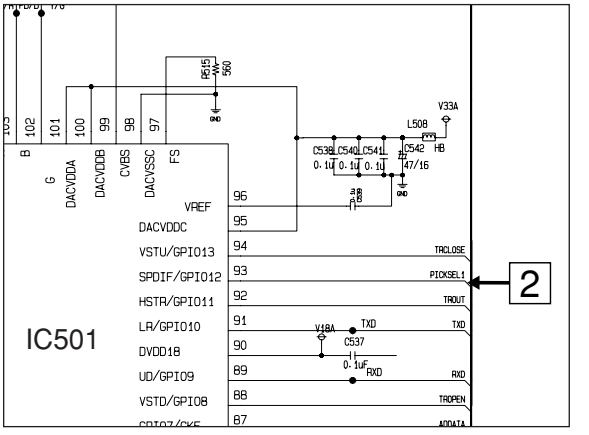
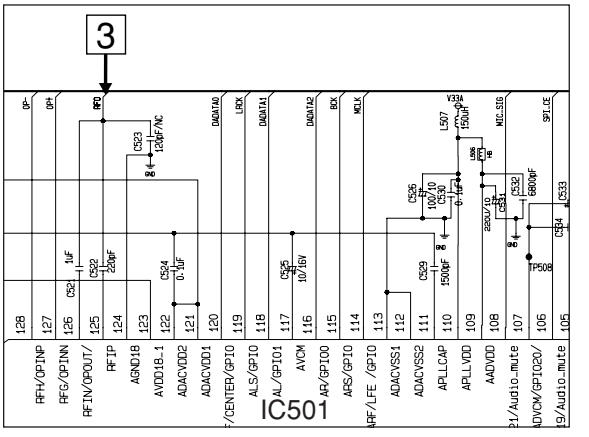
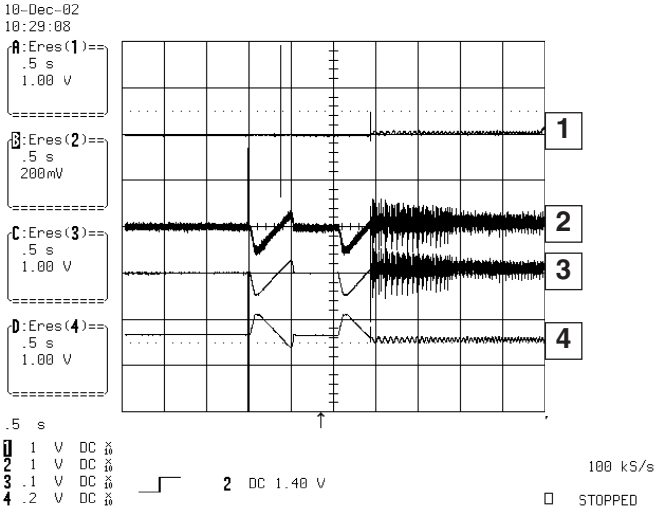


FIG 7-4 (CD)



8. FOCUS ON WAVEFORMS



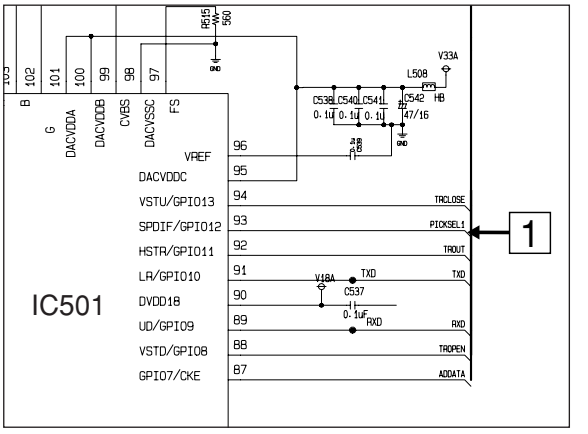
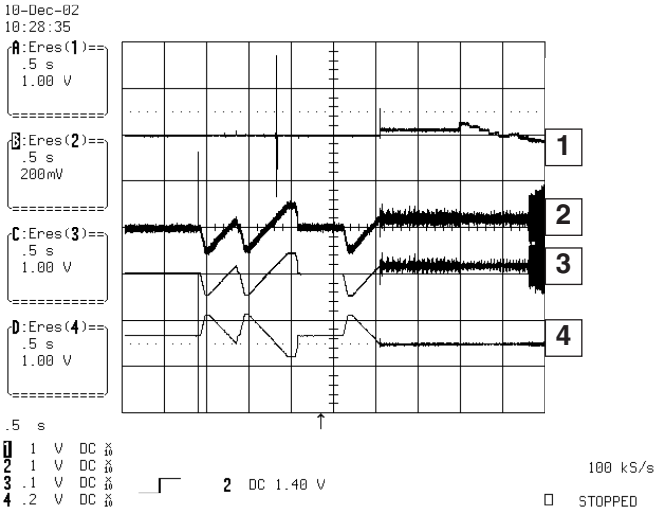


FIG 8-1 (DVD)



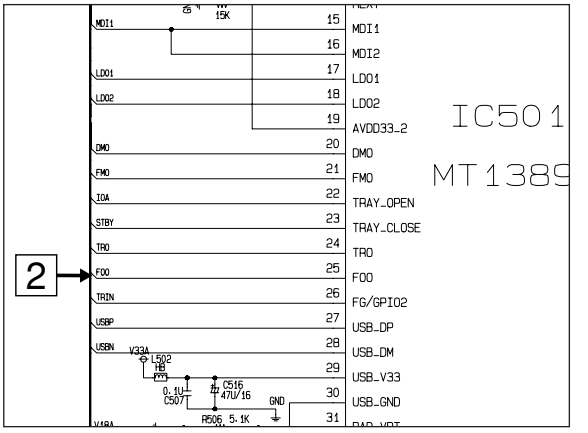
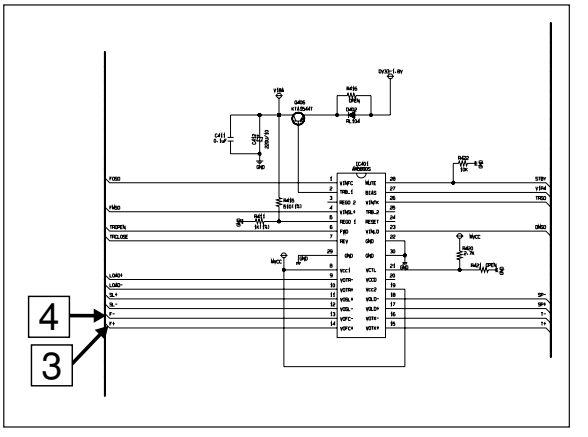


FIG 8-2 (CD)



9. SPINDLE CONTROL WAVEFORMS (NO DISC CONDITION)

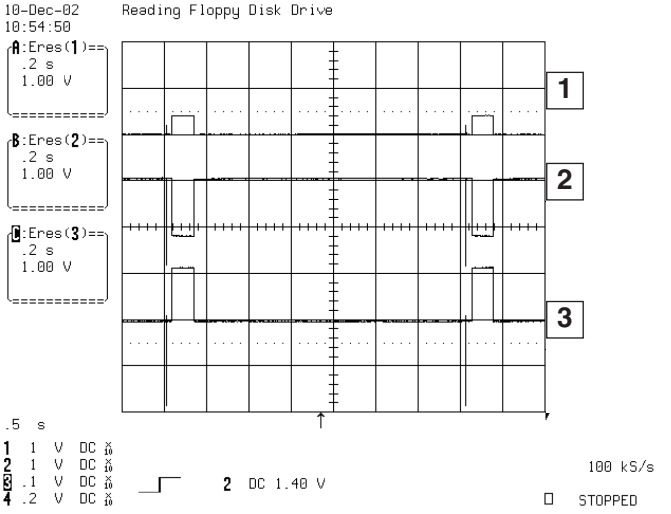
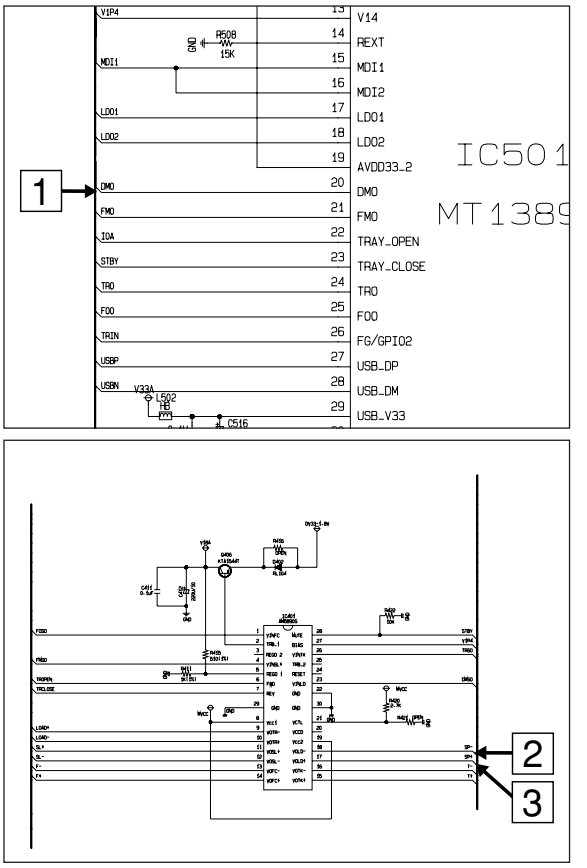


FIG 9-1



10. TRACKING CONTROL RELATED SIGNAL(System checking)

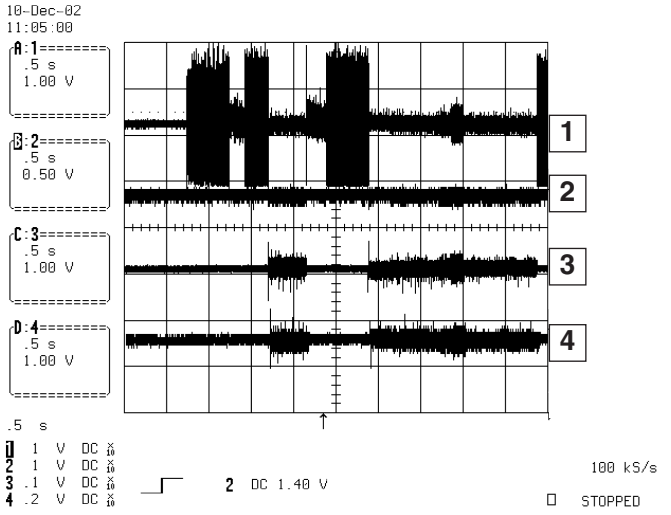
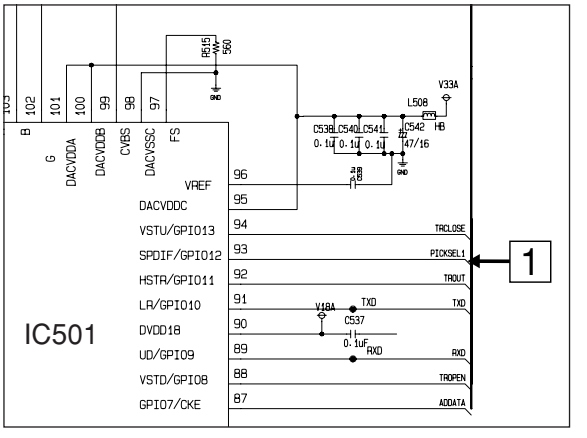


FIG 10-1(DVD)



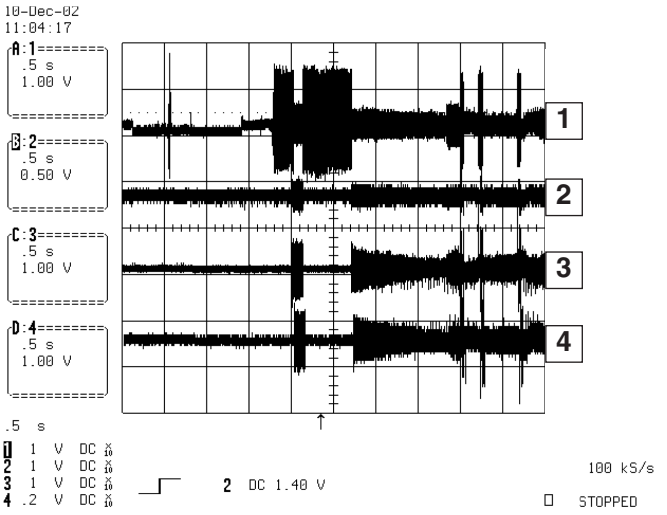
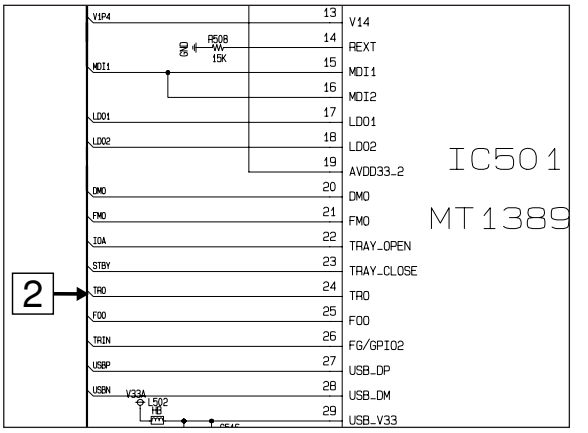
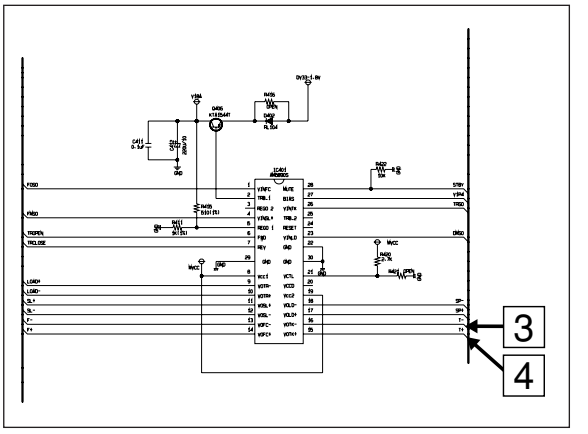


FIG 10-2(CD)





11. MT1389/L VIDEO OUTPUT WAVEFORMS

1) Full colorbar signal(COMPOSIT)

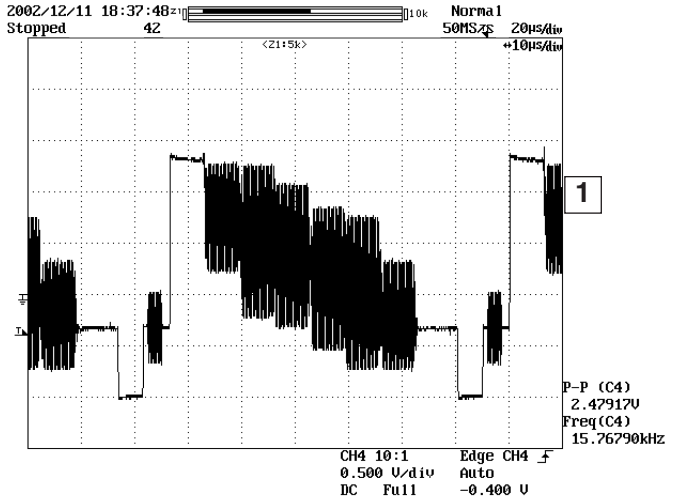
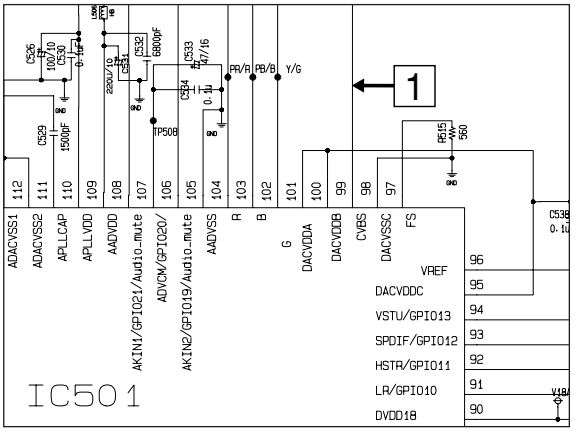
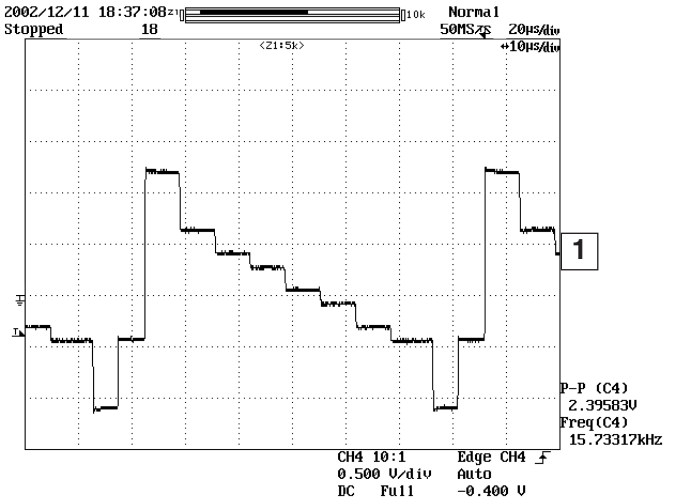


FIG 11-1



2) Y



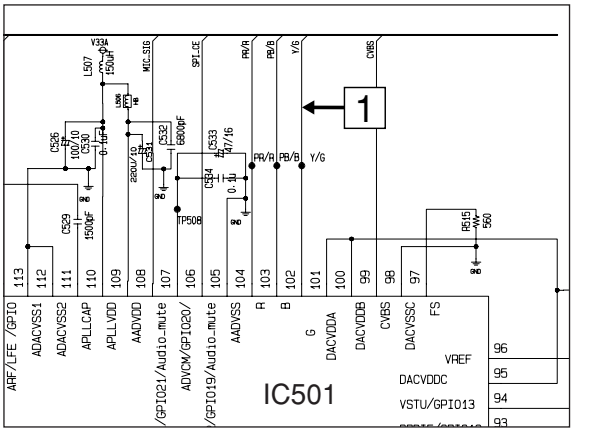
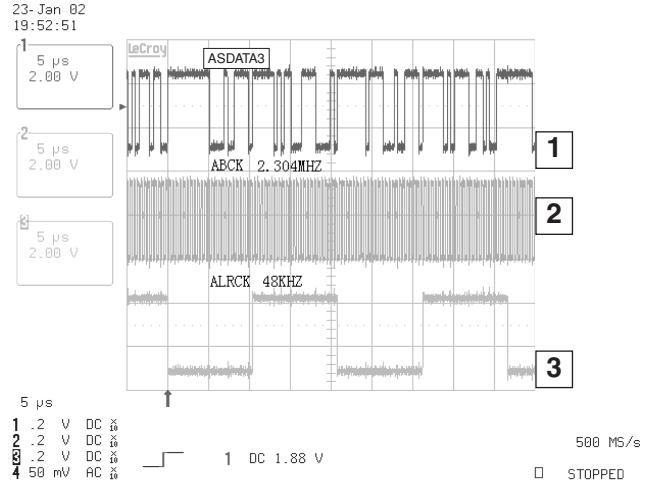


FIG 11-2

12. AUDIO OUTPUT FROM mt1389/L

1) Audio related Signal



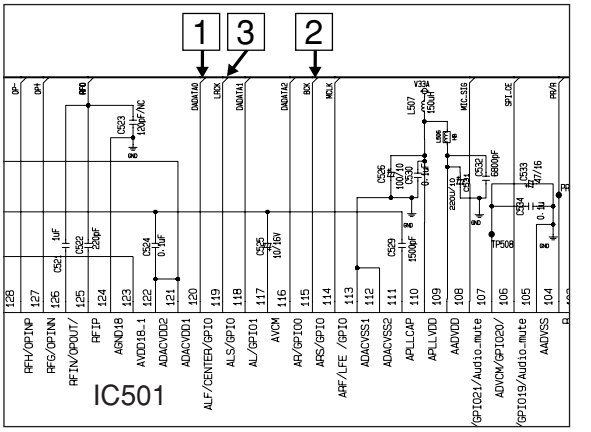
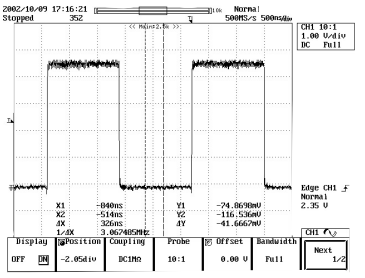


FIG 12-1

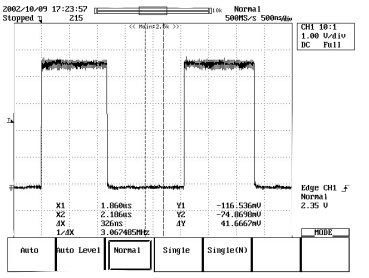
13. DVD & AMP WAVEFORMS

1)



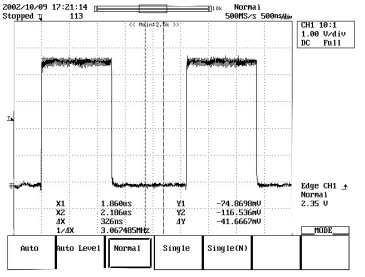
• R703 → TP704

2)



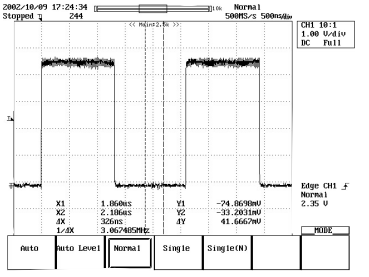
• R720 → TP711

3)



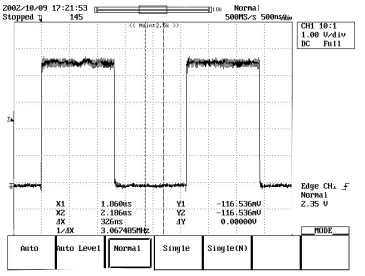
• R704 → TP707
or
R717 → TP705

4)



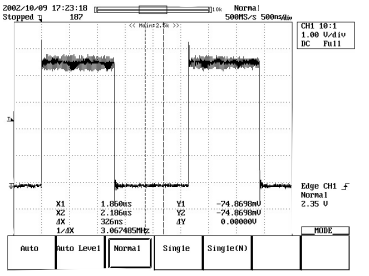
• R709 → TP713

5)

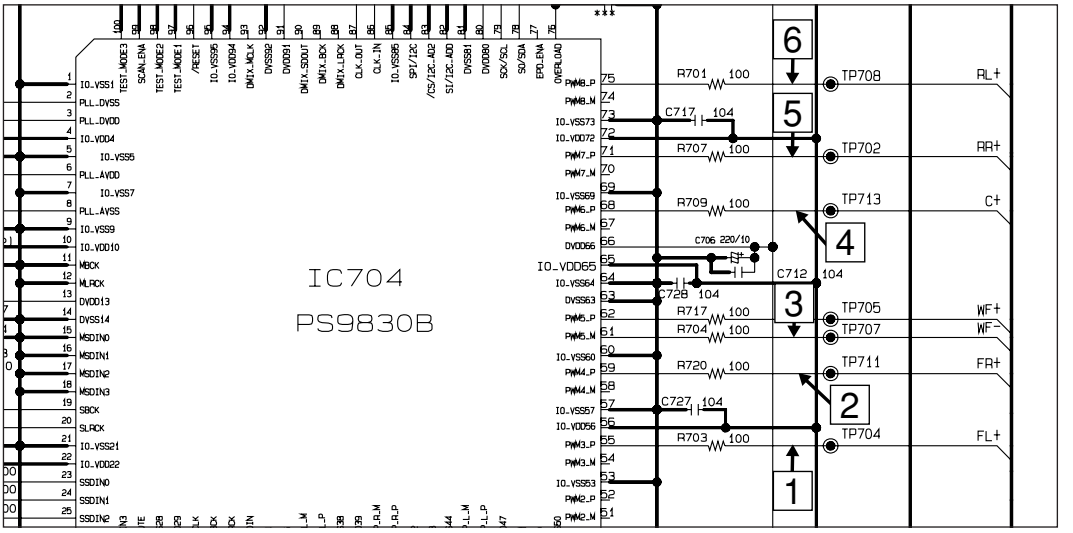


• R707 → TP702

6)



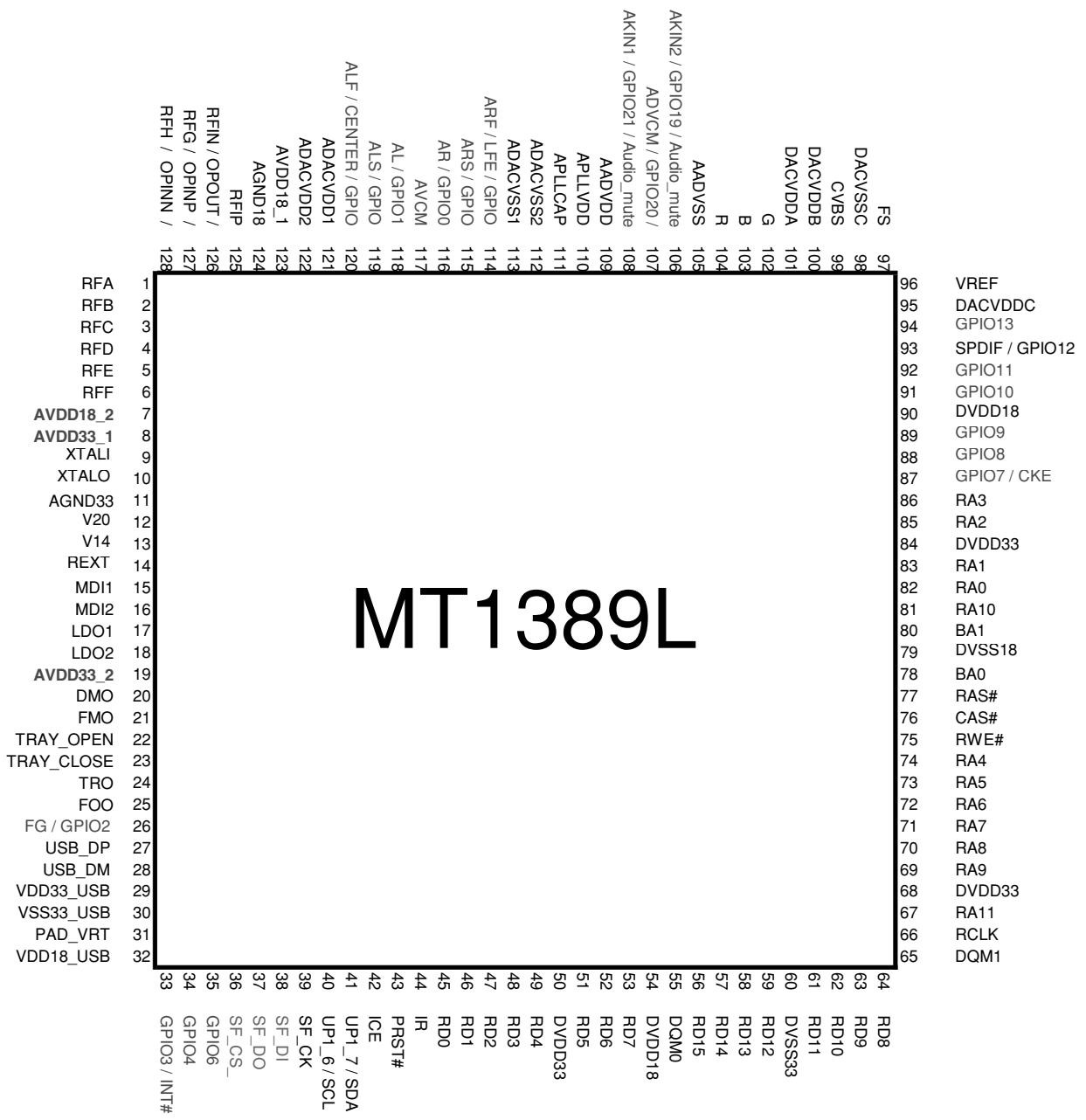
• R701 → TP708



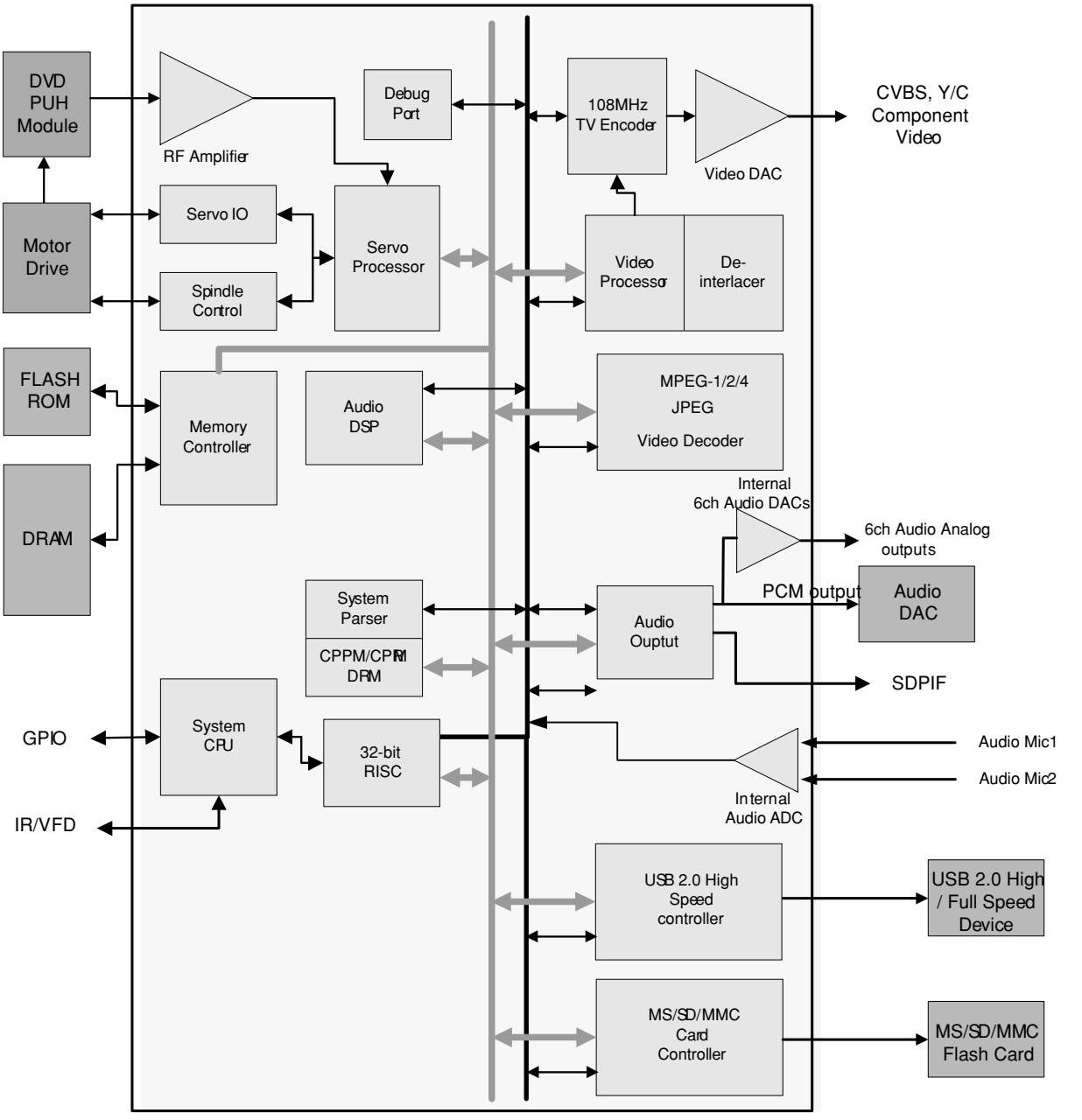
INTERNAL BLOCK DIAGRAM OF ICs

1. IC501 MPEG(MT1389L)

• PIN CONFIGURATION



• BLOCK DIAGRAM



• PIN DESCRIPTION

• Abbreviations:
SR: Slew Rate
PU: Pull Up
PD: Pull Down
SMT: Schmitt Trigger
4mA~16mA: Output buffer driving strength.

Pin	Main	Alt.	Type	Description
			Analog I nterface (66)	
125	RFIP		Analog Input	AC coupled DVD RF signal input RFIP
126	RFIN	OPOUT	Analog Input	AC coupled DVD RF signal input RFIN
127	RFG	OPINP	Analog Input	Main beam, RF AC input path
128	RFH	OPINN	Analog Input	Main beam, RF AC input path
1	RFA		Analog Input	RF main beam input A
2	RFB		Analog Input	RF main beam input B
3	RFC		Analog Input	RF main beam input C
4	RFD		Analog Input	RF main beam input D
5	RFE		Analog Input	RF sub beam input E
6	RFF		Analog Input	RF sub beam input E
7	AVDD18_2		Analog power	Analog 1.8V power
8	AVDD33_1		Analog power	Analog 3.3V power
9	XTALI		Input	27MHz crystal input
10	XTALO		Output	27MHz crystal output
11	AGND33		Analog Ground	Analog Ground
12	V20		Analog output	Reference voltage 2.0V
13	V14		Analog output	Reference voltage 1.4V
14	REXT		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS
15	MDI1		Analog Input	Laser power monitor input
16	MDI2		Analog Input	Laser power monitor input
17	LDO1		Analog Output	Laser driver output
18	LDO2		Analog Output	Laser driver output
19	AVDD33_2		Analog Power	Analog 3.3V power
20	DMO		Analog Output	Disk motor control output. PWM output
21	FMO		Analog Output	Feed motor control. PWM output
22	TRAY_OPEN		Analog Output	Tray PWM output/Tray open output
23	TRAY_CLOSE		Analog Output	Tray PWM output/Tray close output
24	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator
25	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
26	FG	GPIO2	Analog	1) Motor Hall sensor input 2) GPIO
27	USB_DP		Analog Input	USB port DPLUS analog pin
28	USB_DM		Analog Input	USB port DMINUS analog pin
29	VDD33_USB		USB Power	USB Power pin 3.3V
30	VSS33_USB		USB Ground	USB ground pin
31	PAD_VRT		Analog Inout	USB generating reference current
32	VDD18_USB		USB Power	USB Power pin 1.8V
95	DACVDDC		Power	Power
96	VREF		Analog	Bandgap reference voltage
97	FS		Analog	Full scale adjustment (suggest to use 560 ohm)
98	DACVSSC		Ground	Ground pin for video DAC circuitry
99	CVBS		Analog	Analog composite output

Pin	Main	Alt.	Type	Description
100	DACVDDB		Power	3.3V power pin for video DAC circuitry
101	DACVDDA		Power	3.3V power pin for video DAC circuitry
102	Y/G		Analog	Green, Y, SY, or CVBS
103	B/CB/PB		Analog	Blue, CB/PB, or SC
104	R/CR/PR		Analog	Red, CR/PR, CVBS, or SY
105	AADVSS		Ground	Ground pin for 2ch audio ADC circuitry
106	AKIN2		Analog	1) Audio ADC input 2 2) MS_CLK set B 3) MCDATA 4) Audio Mute 5) HSYN/VSYN output 6) C5 7) GPIO
107	ADVCM		Analog	1) 2ch audio ADC reference voltageC 2) C6 3) GPIO
108	AKIN1		Analog	1) Audio ADC input 1 2) MS_D0 set B 3) Audio Mute 4) HSYN/VSYN output 5) C7 6) GPIO
109	AADVDD		Power	3.3V power pin for 2ch audio ADC circuitry
110	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
111	APLLCAP		Analog InOut	APLL external capacitance connection
112	ADACVSS2		Ground	Ground pin for audio DAC circuitry
113	ADACVSS1		Ground	Ground pin for audio DAC circuitry
114	ARF / LFE	GPIO	Analog Output	1) Audio DAC sub-woofer channel output 2) While internal audio DAC not used: a. ACLK b. GPIO
115	ARS	GPIO	Analog Output	1) Audio DAC right Surround channel output 2) While internal audio DAC not used: a. ABCK b. GPIO
116	AR		Analog Output	1) Audio DAC right channel output 2) While internal audio DAC not used: a. SDATA2 b. GPIO c. RXD2
117	AV CM		Analog	Audio DAC reference voltage
118	AL	GPIO	Analog Output	1) Audio DAC left channel output 2) While internal audio DAC not used: a. SDATA1 b. GPIO c. RXD1
119	ALS	GPIO	Analog Output	1) Audio DAC left Surround channel output 2) While internal audio DAC not used: a. ALRCK b. GPIO
120	ALF /CENTER	GPIO	Analog Output	1) Audio DAC center channel output 2) While internal audio DAC not used: a. ASDATA0 b. GPIO
121	ADACVDD1		Analog Power	3.3V power pin for audio DAC circuitry
122	ADACVDD2		Analog Power	3.3V power pin for audio DAC circuitry
123	AVDD18_1		Analog Power	Analog 1.8V power
124	AGND18		Analog Ground	Analog Ground
			General Power/ Ground (7)	
54, 90	DVDD18		Power	1.8V power pin for internal digital circuitry

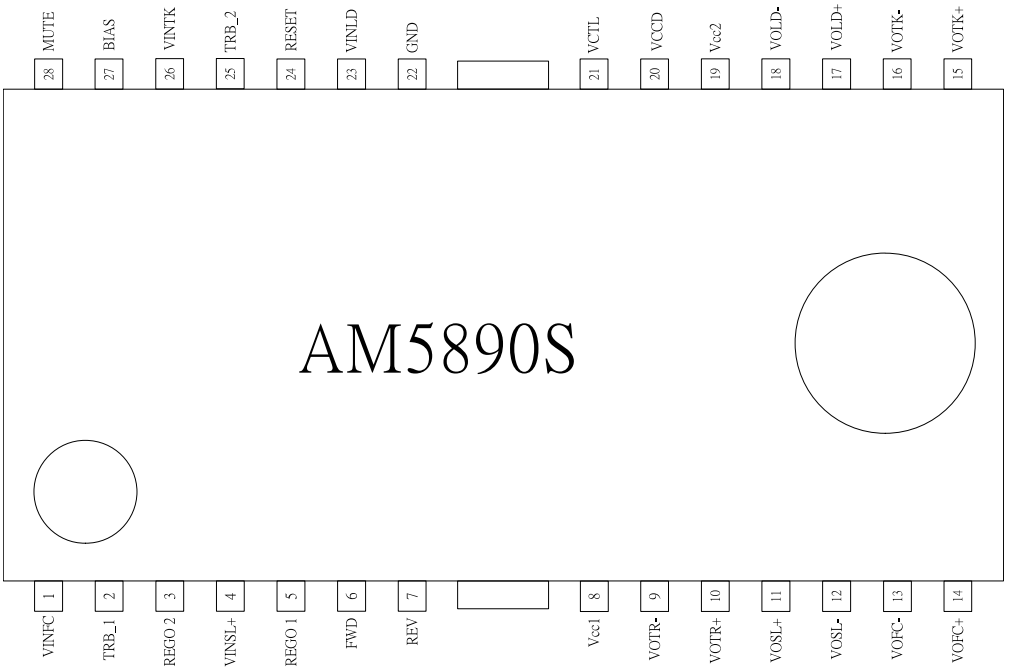
Pin	Main	Alt.	Type	Description
79	DVSS18		Ground	1.8V Ground pin for internal digital circuitry
50, 68,84	DVDD33		Power	3.3V power pin for internal digital circuitry
60	DVSS		Ground	3.3V Ground pin for internal digital circuitry
Micro Controller , Flash I nterface and GPIO(12)				
33	GPIO3	INT#	InOut 8mA, SR PD, SMT	1) General purpose IO 3 2) Microcontroller external interrupt 1
34	GPIO4		InOut 4mA, PD	General purpose IO 4
35	GPIO6		InOut 4mA, PD	General purpose IO 6
36	SF_CS_		InOut 8mA, SR PU, SMT	Serial Flash Chip Select
37	SF_DO		InOut 8mA, SR PD, SMT	Serial Flash Dout
38	SF_DI		InOut 8mA, SR PU, SMT	Serial Flash Din
39	SF_CK		InOut 8mA, SR PD, SMT	Serial Flash Clock
40	UP1_6	SCL	InOut 8mA, SR PU, SMT	1) Microcontroller port 1-6 2) I2C clock pin
41	UP1_7	SDA	InOut 4mA, SR PU, SMT	1) Microcontroller port 1-7 2) I2C data pin
42	ICE		Input PD, SMT	Microcontroller ICE mode enable
43	PRST#		Input PU, SMT	Power on reset input, active low
44	IR		Input SMT	IR control signal input
Dram Interface (37) (Sorted by position)				
45	RD0		InOut 4mA	DRAM data 0
46	RD1		InOut 4mA	DRAM data 1
47	RD2		InOut 4mA	DRAM data 2
48	RD3		InOut 4mA	DRAM data 3
49	RD4		InOut 4mA	DRAM data 4
51	RD5		InOut 4mA	DRAM data 5
52	RD6		InOut 4mA	DRAM data 6
53	RD7		InOut 4mA	DRAM data 7
55	DQM0		InOut 4mA, PD	Data mask 0
56	RD15		InOut 4mA	DRAM data 15
57	RD14		InOut 4mA	DRAM data 14
58	RD13		InOut 4mA	DRAM data 13

Pin	Main	Alt.	Type	Description
59	RD12		InOut 4mA	DRAM data 12
61	RD11		InOut 4mA	DRAM data 11
62	RD10		InOut 4mA	DRAM data 10
63	RD9		InOut 4mA	DRAM data 9
64	RD8		InOut 4mA	DRAM data 8
65	DQM1		InOut 4mA, PD	Data mask 1
66	RCLK		InOut 4mA, PD	Dram clock
67	RA11		InOut 4mA, PD	DRAM address bit 11
69	RA9		InOut 4mA, PD	DRAM address 9
70	RA8		InOut 4mA, PD	DRAM address 8
71	RA7		InOut 4mA, PD	DRAM address 7
72	RA6		InOut 4mA, PD	DRAM address 6
73	RA5		InOut 4mA, PD	DRAM address 5
74	RA4		InOut 4mA, PD	DRAM address 4
75	RWE#		Output 4mA, PD	DRAM Write enable, active low
76	CAS#		Output 4mA, PD	DRAM column address strobe, active low
77	RAS#		Output 4mA, PD	DRAM row address strobe, active low
78	BA0		InOut 4mA, PD	DRAM bank address 0
80	BA1		InOut 4mA, PD	DRAM bank address 1
81	RA10		InOut 4mA, PD	DRAM address 10
82	RA0		InOut 4mA, PD	DRAM address 0
83	RA1		InOut 4mA, PD	DRAM address 1
85	RA2		InOut 4mA, PD	DRAM address 2
86	RA3		InOut 4mA, PD	DRAM address 3
87	GPIO7	CKE	InOut 4mA, PD	1) GPIO 7 2) Dram Clock Enable 3) MS_CLK set A 4) Audio Mute 5) HSYN/VSYN input 6) C0
			GPIO (6)	
88	GPIO8		InOut 4mA, PD	1) GPIO8 2) MS_BS set A 3) SD_CLK set A 4) ASDATA2 5) ACLK

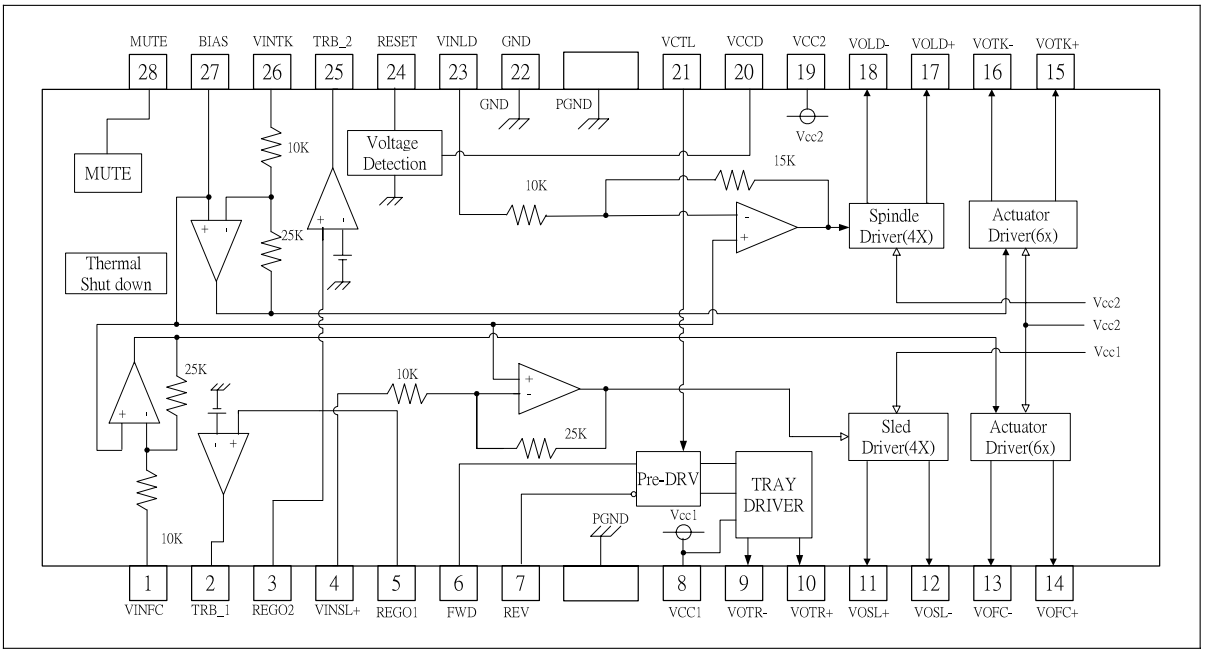
Pin	Main	Alt.	Type	Description
				6) Audio Mute 7) HSYN/VSYN input 8) C1
89	GPIO9		InOut 4mA, PD	1) GPIO9 2) MS_D0 set A 3) SD_CMD set A 4) ASDATA1 5) ABCK 6) C2 7) RXD1
91	GPIO10		InOut 4mA, PD	1) GPIO10 2) SD_CLK set B 3) SD_D0 set A 4) ASDATA0 5) ALRCK 6) HSYN/VSYN output 7) C3 8) TXD1
92	GPIO11		InOut 4mA, PD	1) GPIO11 2) SD_CMD set B 3) MS_BS set B 4) Audio Mute 5) HSYN/VSYN output 6) C4
93	SPDIF	GPIO12	InOut 2mA, PD	1) SPDIF output 2) GPIO12
94	GPIO13		InOut 4mA, PD	1) GPIO13 2) SD_D0 set B 3) ALRCK 4) Audio Mute 5) YUVCLK

2. IC401 MOTOR DRIVER

• PIN CONFIGURATION



• BLOCK DIAGRAM



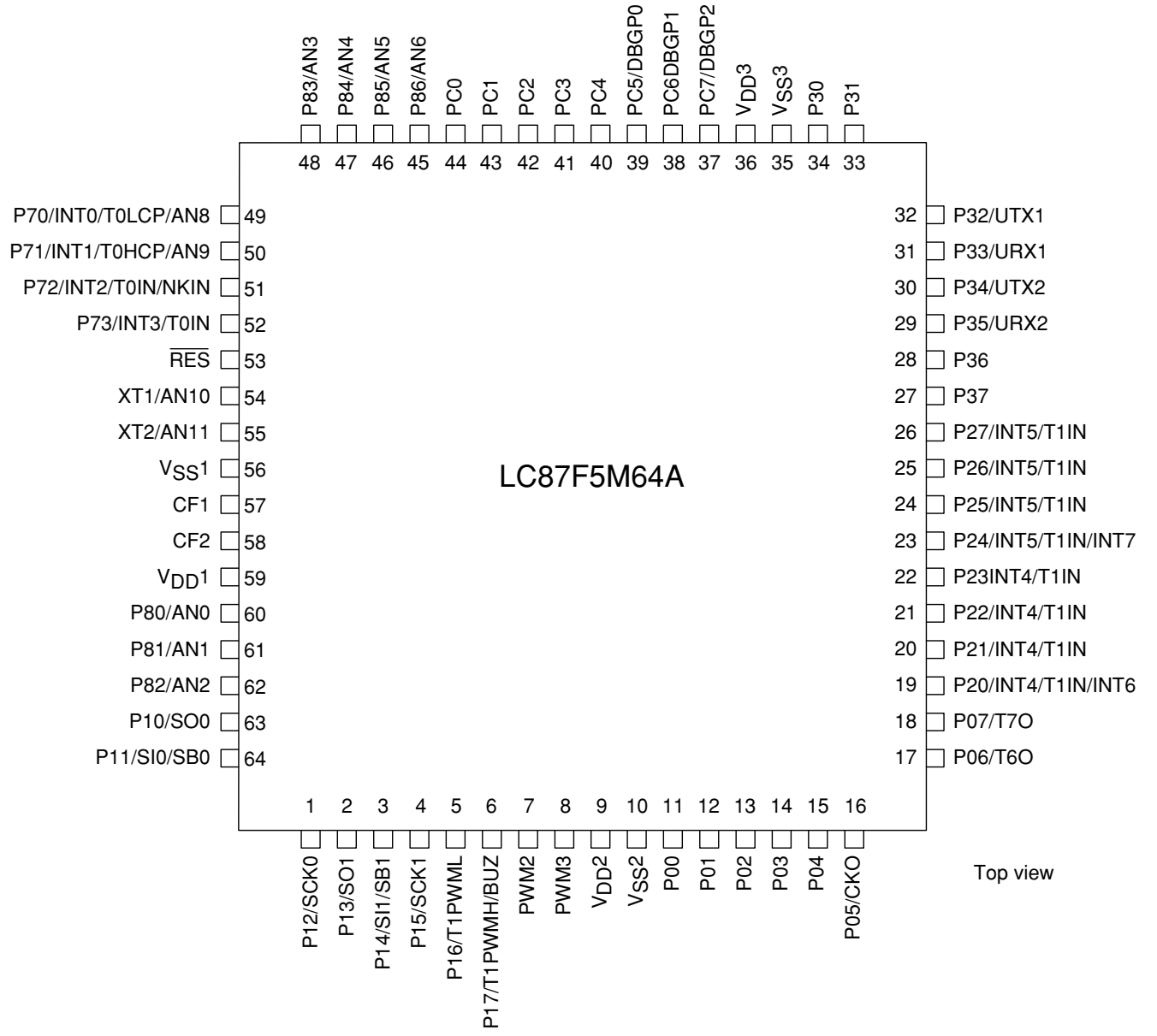
• PIN DESCRIPTION

PIN No	Pin Name	Function
1	VINFC	Input for focus driver
2	TRB_1	Connect to external transistor base
3	REGO2	Regulator voltage output, connect to external transistor collector
4	VINSL+	Input for the sled driver
5	REGO1	Regulator voltage output, connect to external transistor collector
6	FWD	Tray driver forward input
7	REV	Tray driver reverse input
8	Vcc1	Vcc for pre-drive block and power block of sled and tray
9	VOTR-	Tray driver output (-)
10	VOTR+	Tray driver output (+)
11	VOSL+	Sled driver output (+)
12	VOSL-	Sled driver output (-)
13	VOFC-	Focus driver output (-)
14	VOFC+	Focus driver output (+)
15	VOTK+	Tracking driver output (+)
16	VOTK-	Tracking driver output (-)
17	VOLD+	Spindle driver output (+)
18	VOLD-	Spindle driver output (-)
19	Vcc2	Vcc for power block of spindle, tracking and focus
20	VCCD	Inpu for voltage detection
21	VCTL	Speed control input of tray driver
22	GND	Ground
23	VINLD	Input for spindle driver
24	RSET	Output for voltage detection
25	TRB_2	Connect to external transistor base
26	VINTK	Input for tracking driver
27	BIAS	Input for reference voltage
28	MUTE	Input for mute control

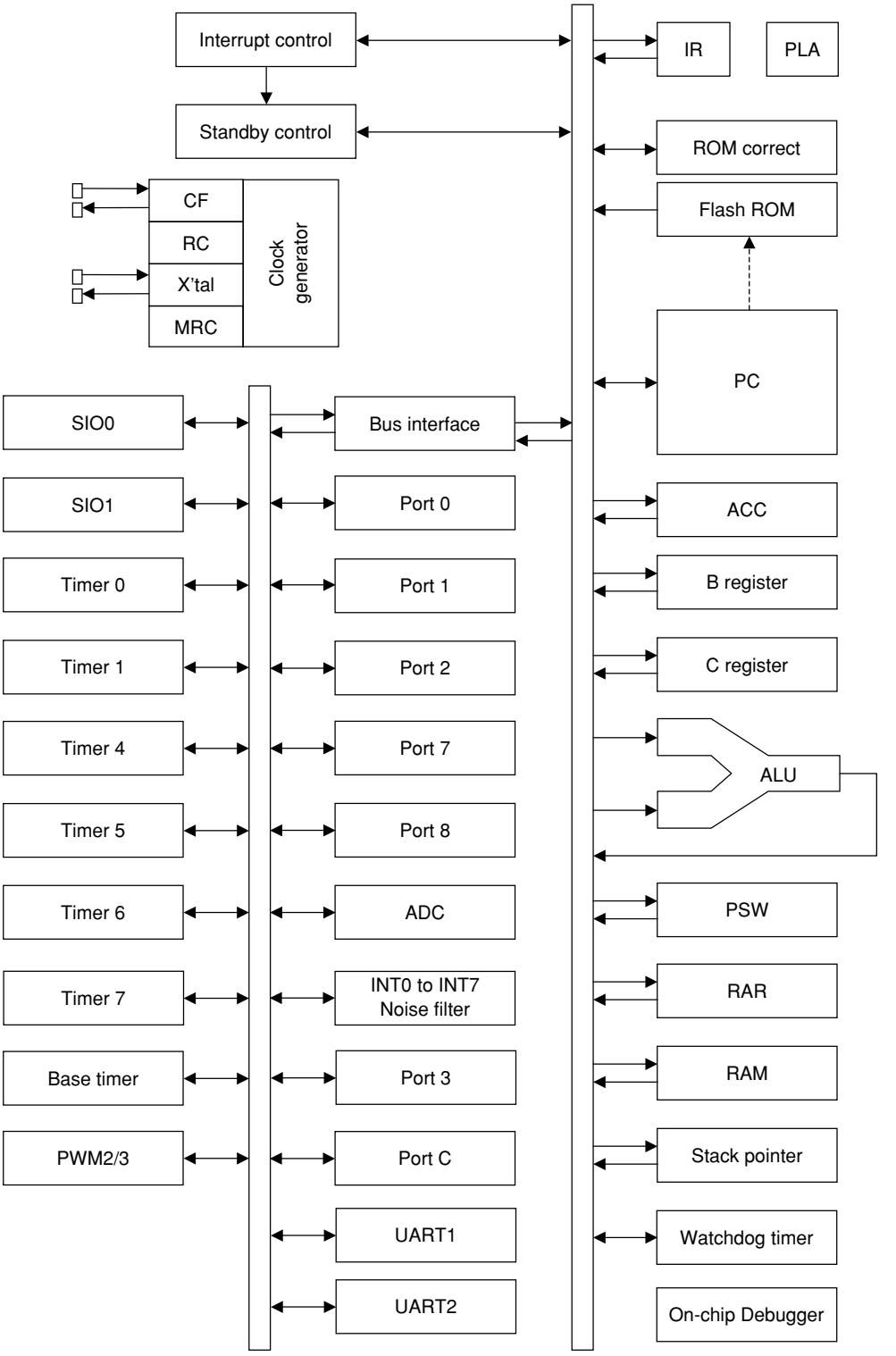
Notes) Symbol of + and – (output of drivers) means polarity to input pin.
(For example, if voltage of pin1 is high, pin14 is high.)

3. IC101 MICOM

• PIN CONFIGURATION



• BLOCK DIAGRAM



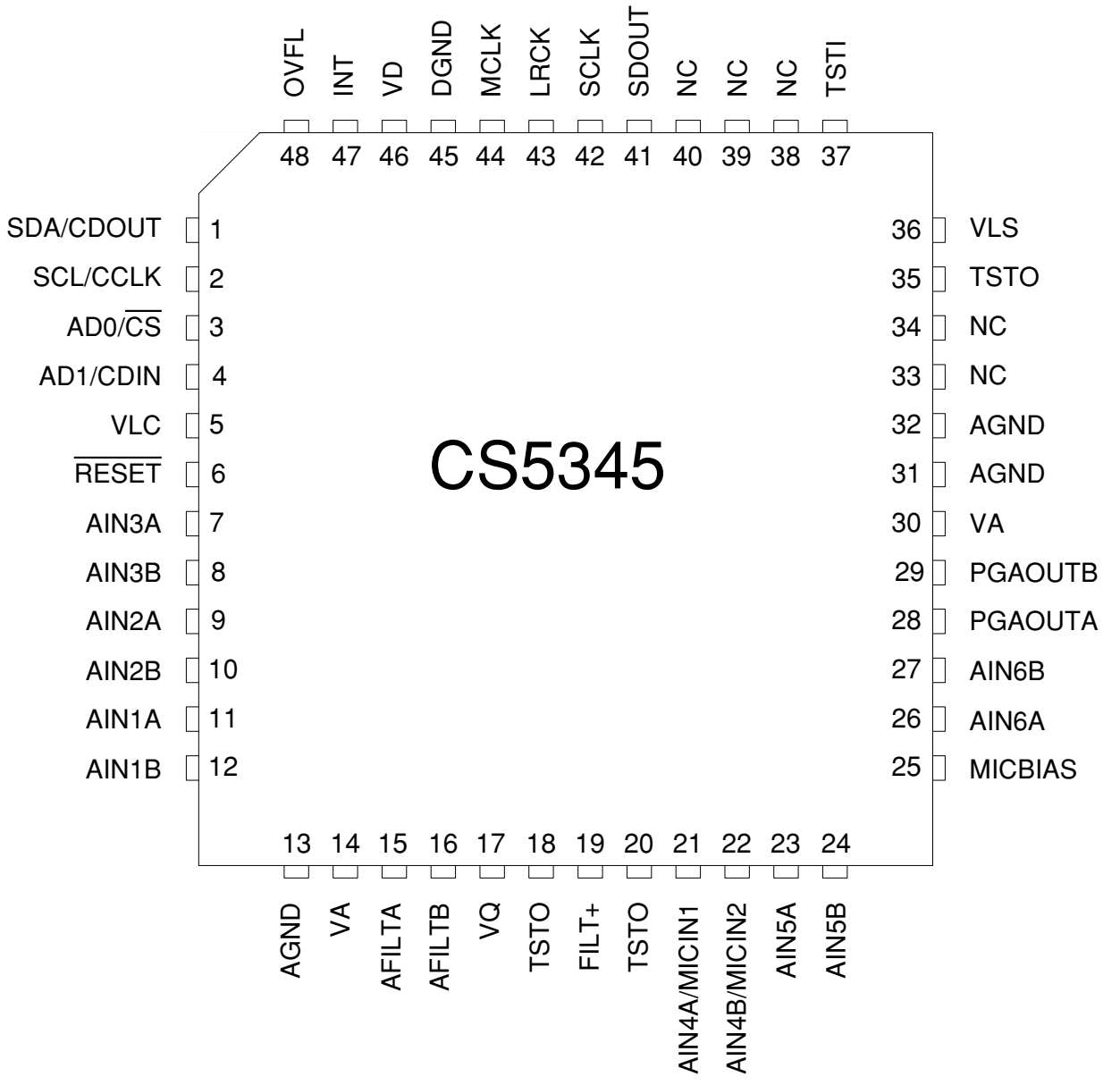
• PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$
$V_{SS}3$</td><td>-</td><td>- Power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$
$V_{DD}3$</td><td>-</td><td>+ Power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistor can be turned on and off in 4-bit units
• HOLD release input
• Port 0 interrupt input
• Shared Pins
P05 : Clock output (system clock / can selected from sub clock)
P06 : Timer 6 toggle output
P07 : Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P10 : SIO0 data output
P11 : SIO0 data input/bus I/O
P12 : SIO0 clock I/O
P13 : SIO1 data output
P14 : SIO1 data input/bus I/O
P15 : SIO1 clock I/O
P16 : Timer 1 PWML output
P17 : Timer 1 PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
P20: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/
timer 0H capture input/INT6 input/timer 0L capture 1 input
P21 to P23 : INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/
timer 0H capture input
P24: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/
timer 0H capture input/INT7 input/timer 0H capture 1 input
P25 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/
timer 0H capture input
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
</table>

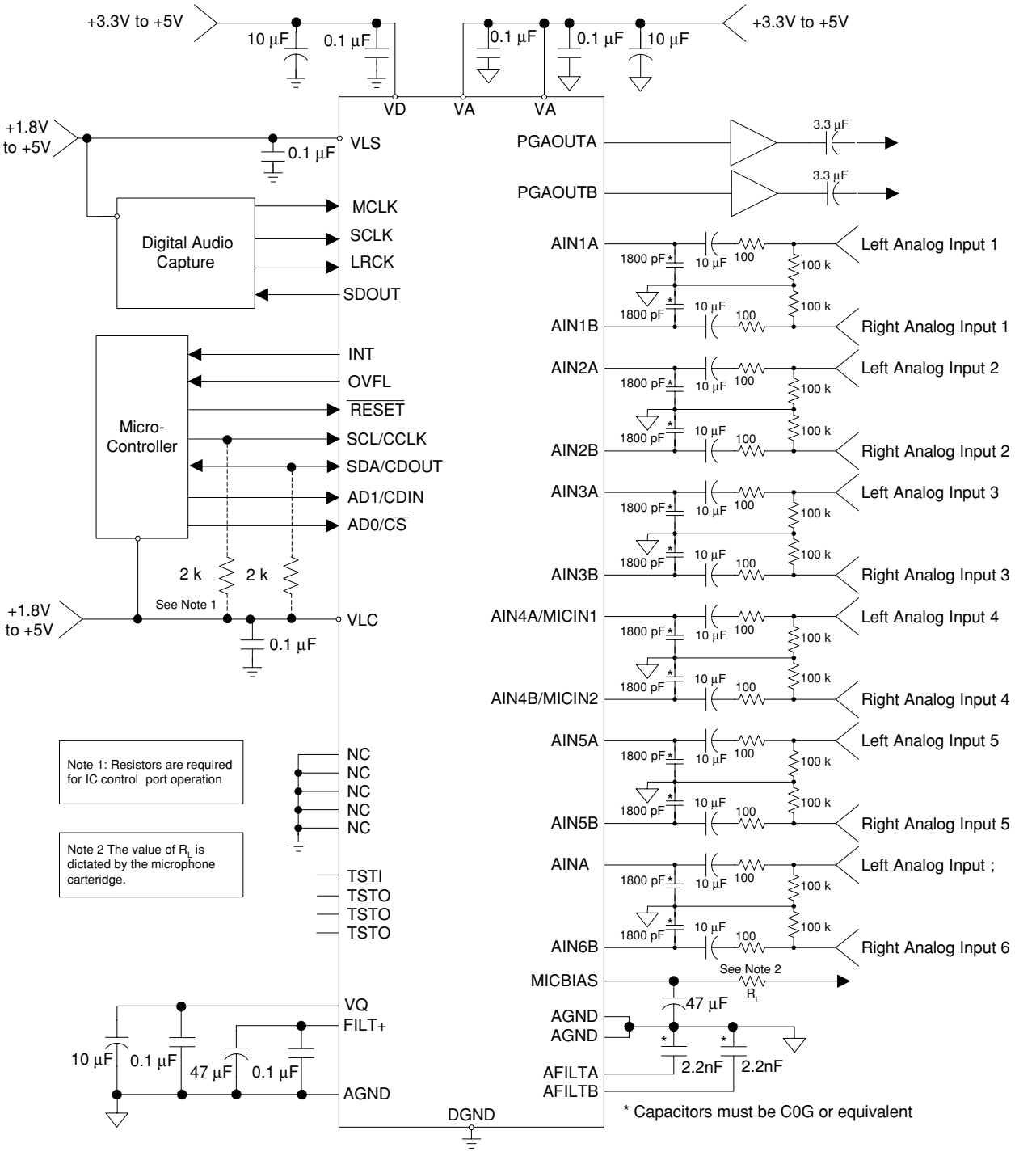
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Shared pins
P70 : INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output
P71 : INT1 input/HOLD reset input/timer 0H capture input
P72 : INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/
high speed clock counter input
P73 : INT3 input (with noise filter)/timer 0 event input/timer 0H capture input
AD converter input port: AN8 (P70), AN9 (P71)
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>Port 8
P80 to P86</td><td>I/O</td><td>• 7-bit I/O port
• I/O specifiable in 1-bit units
• Shared pins
AD converter input port : AN0 (P80) to AN6 (P86)</td><td>No</td></tr>
<tr><td>PWM2
PWM3</td><td>I/O</td><td>• PWM2 and PWM3 output ports
• General-purpose I/O available</td><td>No</td></tr>
<tr><td>Port 3
P30 to P37</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P32: UART1 transmit
P33: UART1 receive
P34: UART2 transmit
P35: UART2 receive</td><td>Yes</td></tr>
<tr><td>Port C
PC0 to PC7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
PC5 to PC7: On-chip Debugger</td><td>Yes</td></tr>
<tr><td>$\overline{RES}$</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input pin
• Shared pins
General-purpose input port
AD converter input port : AN10
Must be connected to $V_{DD}1$ if not to be used.</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output pin
• Shared pins
General-purpose I/O port
AD converter input port : AN11
Must be set for oscillation and kept open if not to be used.</td><td>No</td></tr>
<tr><td>CF1</td><td>Input</td><td>Ceramic resonator input pin</td><td>No</td></tr>
<tr><td>CF2</td><td>Output</td><td>Ceramic resonator output pin</td><td>No</td></tr>
</table>

4. IC201 ADC(CS5345)

• PIN CONFIGURATION



• BLOCK DIAGRAM

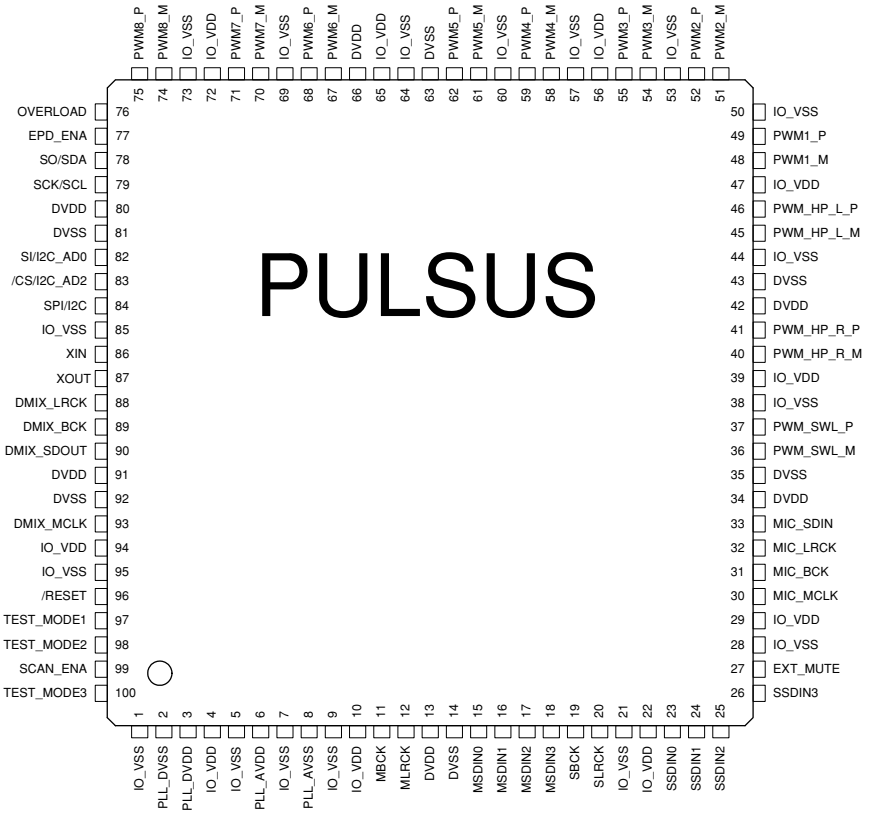


• PIN DESCRIPTION

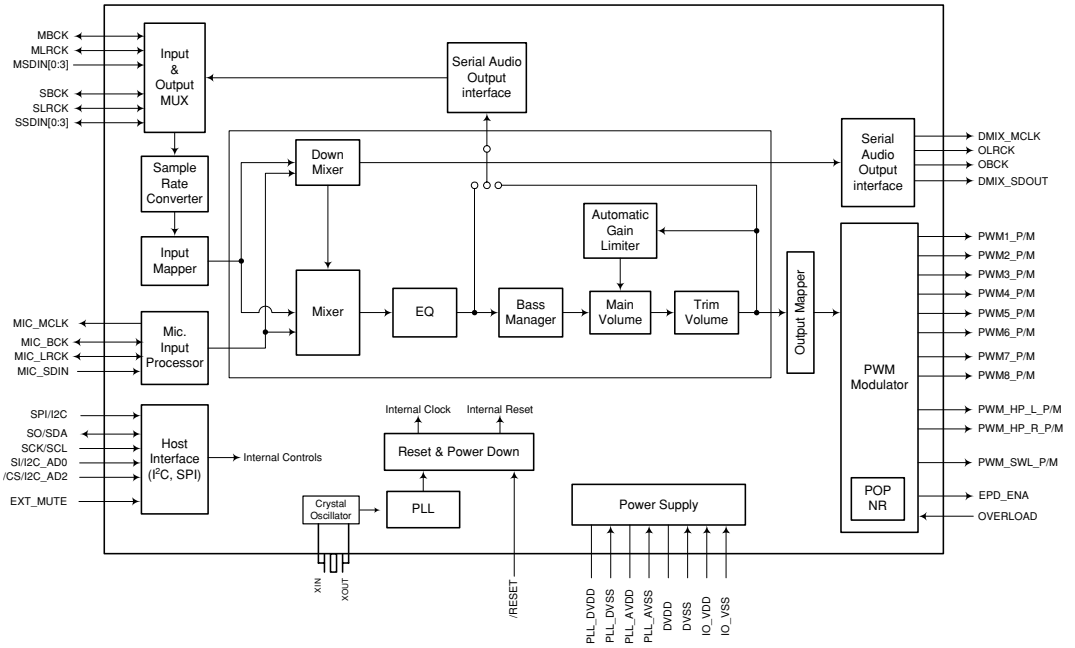
SDA/CDOUT	1	**Serial Control Data** (Input/Output) - SDA is a data I/O in I²C® Mode. CDOUT is the output data line for the control port interface in SPI™ Mode.
SCL/CCLK	2	**Serial Control Port Clock** (Input) - Serial clock for the serial control port.
AD0/$\overline{CS}$	3	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (Input) - AD0 is a chip address pin in I²C Mode; $\overline{CS}$ is the chip-select signal for SPI format.
AD1/CDIN	4	**Address Bit 1 (I²C) / Serial Control Data Input (SPI)** (Input) - AD1 is a chip address pin in I²C Mode; CDIN is the input data line for the control port interface in SPI Mode.
VLC	5	**Control Port Power** (Input) - Determines the required signal level for the control port interface. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{RESET}$	6	**Reset** (Input) - The device enters a low-power mode when this pin is driven low.
AIN3A AIN3B	7 8	**Stereo Analog Input 3** (Input) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN2A AIN2B	9 10	**Stereo Analog Input 2** (Input) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN1A AIN1B	11 12	**Stereo Analog Input 1** (Input) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AGND	13	**Analog Ground** (Input) - Ground reference for the internal analog section.
VA	14	**Analog Power** (Input) - Positive power for the internal analog section.
AFILTA	15	**Antialias Filter Connection** (Output) - Antialias filter connection for the channel A ADC input.
AFILTB	16	**Antialias Filter Connection** (Output) - Antialias filter connection for the channel B ADC input.
VQ	17	**Quiescent Voltage** (Output) - Filter connection for the internal quiescent reference voltage.
TSTO	18	**Test Pin** (Output) - This pin must be left unconnected.
FILT+	19	**Positive Voltage Reference** (Output) - Positive reference voltage for the internal sampling circuits.
TSTO	20	**Test Pin -** This pin must be left unconnected.
AIN4A/MICIN1 AIN4B/MICIN2	21 22	**Stereo Analog Input 4 / Microphone Input 1 & 2** (Input) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN5A AIN5B	23 24	**Stereo Analog Input 5** (Input) - The full-scale level is specified in the ADC Analog Characteristics specification table.
MICBIAS	25	**Microphone Bias Supply** (Output) - Low-noise bias supply for external microphone. Electrical characteristics are specified in the DC Electrical Characteristics specification table.
AIN6A AIN6B	26 27	**Stereo Analog Input 6** (Input) - The full-scale level is specified in the ADC Analog Characteristics specification table.
PGAOUTA PGAOUTB	28 29	**PGA Analog Audio Output** (Output) - Either an analog output from the PGA block or high impedance.
VA	30	**Analog Power** (Input) - Positive power for the internal analog section.
AGND	31 32	**Analog Ground** (Input) - Ground reference for the internal analog section.
NC	33 34	**No Connect** - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
TSTO	35	**Test Pin** (Output) - This pin must be left unconnected.
VLS	36	**Serial Audio Interface Power** (Input) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
TSTI	37	**Test Pin** (Input) - This pin must be connected to ground.
NC	38, 39, 40	**No Connect** - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
SDOUT	41	**Serial Audio Data Output** (Output) - Output for two's complement serial audio data.
SCLK	42	**Serial Clock** (Input/Output) - Serial clock for the serial audio interface.
LRCK	43	**Left Right Clock** (Input/Output) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	44	**Master Clock** (Input/Output) - Clock source for the ADC's delta-sigma modulators.
DGND	45	**Digital Ground** (Input) - Ground reference for the internal digital section.
VD	46	**Digital Power** (Input) - Positive power for the internal digital section.
INT	47	**Interrupt** (Output) - Indicates an interrupt condition has occurred.
OVFL	48	**Overflow** (Output) - Indicates an ADC overflow condition is present.

5. IC704 PWM

• PIN CONFIGURATION



• BLOCK DIAGRAM



• PIN DESCRIPTION

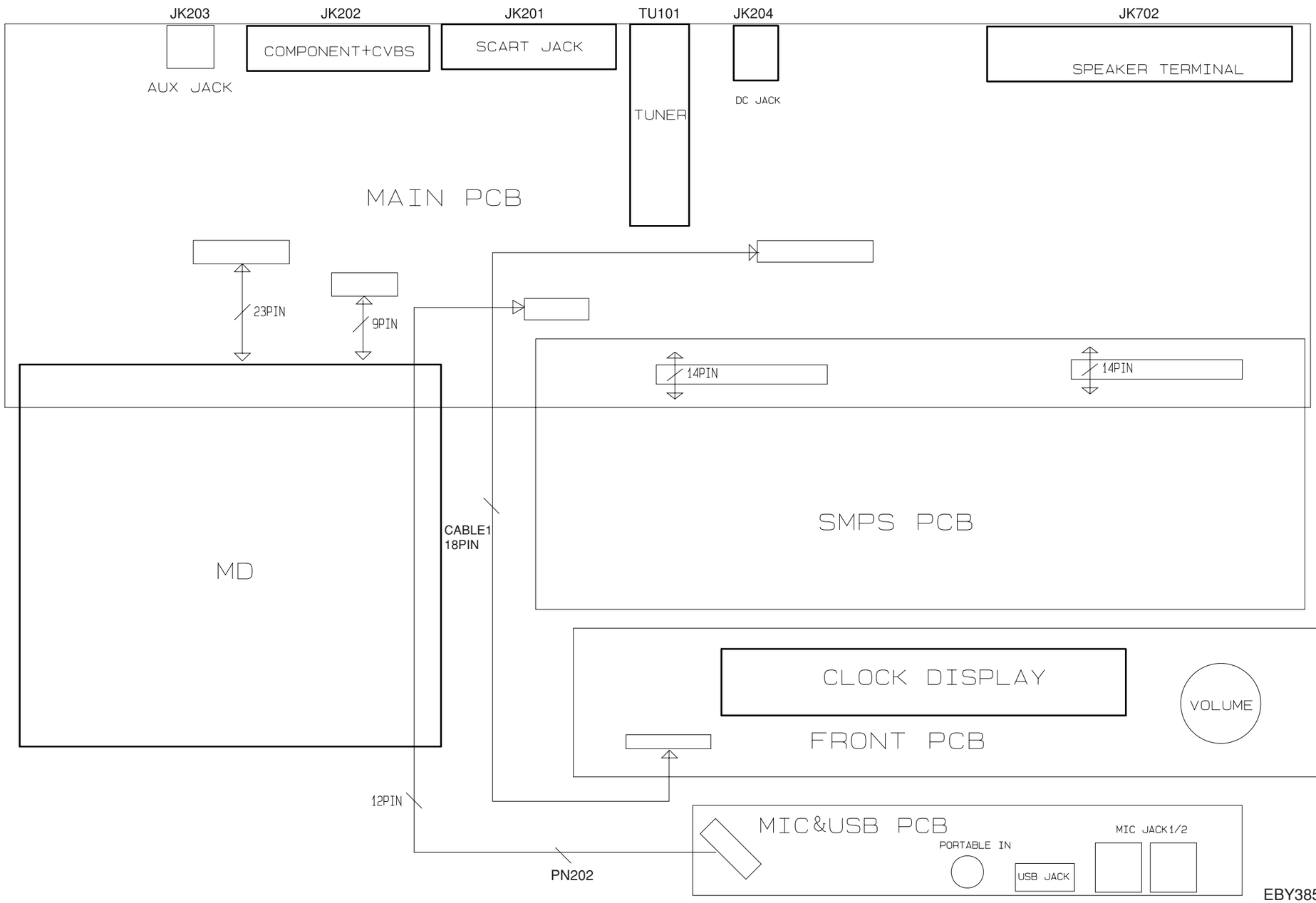
Name	Pin NO.	Type	Description
Power and Ground			
PLL_AVDD	6	Analog Power	PLL analog power supply.
PLL_AVSS	8	Analog Ground	PLL analog ground.
PLL_DVDD	3	PLL Power	PLL digital power supply.
PLL_DVSS	2	PLL Ground	PLL digital ground.
DVDD	13, 34, 42, 66, 80, 91	Power	Core power supply.
DVSS	14, 35, 43, 63, 81, 92	Ground	Core digital ground.
IO_VDD	4, 10, 22, 29, 39, 47, 56, 65, 72, 94	Power	I/O power supply. 3.3V Digital power supply.
IO_VSS	1, 5, 7, 9, 21, 28, 38, 44, 50, 53, 57, 60, 64, 69, 73, 85, 95	Ground	I/O digital ground.
Reset and Clock			
/RESET	96	I	H/W reset signal. Active Low Schmitt-Trigger input. The Schmitt-Trigger input allows a slowly rising input to reset the chip reliably. The RESET signal must be asserted 'Low' during power up. De-assert 'High' for normal operation.
XIN	86	Analog	Crystal Oscillator input pin.
XOUT	87	Analog	Crystal Oscillator output pin.
PCM Audio Input/Output Interface			
MBCK	11	I/O	PCM bit clock input/output of main 8-channel audio. User can select the master/slave mode of this signal. Schmitt-Trigger input.
MLRCK	12	I/O	PCM Word clock (left-right clock) input/output of main 8-channel audio. User can select the master/slave mode of this signal. Schmitt-Trigger input.
MSDIN [3:0]	15, 16, 17, 18	I	PCM serial data input of main 8-channel audio. Schmitt-Trigger input.
SBCK	19	I/O	PCM bit clock input/output of 8-channel audio. User can select the master/slave mode of this signal. Schmitt-Trigger input.
SLRCK	20	I/O	PCM word clock (left-right clock) input/output of sub 8-channel audio. User can select the master/slave mode of this signal. Schmitt-Trigger input.
SSDIN [3:0]	23, 24, 25, 26	I/O	PCM serial data input of sub-channel audio. User can set this sub-channel data input pins to PCM serial data output pins. See the Control Register Description part. Schmitt-Trigger input

MIC_MCLK	30	O	Main clock for external microphone input A/DC. Clock frequency can be selected between 6.144MHz, 12.288MHz, and 24.576MHz.
MIC_BCK	31	I/O	PCM bit clock input/output of external microphone. Bit clock frequency is 3.072MHz (48kHz x 64, fixed)
MIC_LRCK	32	I/O	PCM Word clock (left-right clock) input/output of external microphone. Word clock rate is 48kHz (fixed).
MIC_SDIN	33	I	PCM serial data input of external microphone. Schmitt-Trigger input.
DMIX_MCLK	93	O	Main clock for external down-mix line output D/AC.
DMIX_BCK	89	O	PCM bit clock output of down-mix signal. Bit clock frequency is 6.144MHz (96kHz x 64, fixed)
DMIX_LRCK	88	O	PCM Word clock (left-right clock) output of down-mix signal. Word clock rate is 96kHz (fixed).
DMIX_SDOUT	90	O	PCM serial data output of down-mix signal.
PWM Audio Output			
PWM1_P	49	O	Positive PWM output of channel 1.
PWM1_M	48	O	Negative PWM output of channel 1.
PWM2_P	52	O	Positive PWM output of channel 2.
PWM2_M	51	O	Negative PWM output of channel 2.
PWM3_P	55	O	Positive PWM output of channel 3.
PWM3_M	54	O	Negative PWM output of channel 3.
PWM4_P	59	O	Positive PWM output of channel 4.
PWM4_M	58	O	Negative PWM output of channel 4.
PWM5_P	62	O	Positive PWM output of channel 5.
PWM5_M	61	O	Negative PWM output of channel 5.
PWM6_P	68	O	Positive PWM output of channel 6.
PWM6_M	67	O	Negative PWM output of channel 6.
PWM7_P	71	O	Positive PWM output of channel 7.
PWM7_M	70	O	Negative PWM output of channel 7.
PWM8_P	75	O	Positive PWM output of channel 8.
PWM8_M	74	O	Negative PWM output of channel 8.
PWM_HP_L_P	46	O	Positive PWM output of headphone left channel.
PWM_HP_L_M	45	O	Negative PWM output of headphone left channel.
PWM_HP_R_P	41	O	Positive PWM output of headphone right channel.
PWM_HP_R_M	40	O	Negative PWM output of headphone right channel.
PWM_SWL_P	37	O	Positive PWM output of subwoofer line output.
PWM_SWL_M	36	O	Negative PWM output of subwoofer line output.
System Control Interface			
SPI/I2C	84	I	Host interface mode (SPI or I2C) selector. Assert 'HIGH' for SPI mode. De-assert 'LOW' for I2C mode. Internal pull-down resistor.
SO/SDA	78	I/O	SO for SPI mode or SDA for I2C mode.

SCK/SCL	79	I	SCK for SPI mode or SCL for I2C mode. Schmitt-Trigger input.
SI/I2C_AD0	82	I	SI for SPI mode or Slave Address 0 for I2C mode. Schmitt-Trigger input. Internal pull-down resistor.
/CS/I2C_AD2	83	I	Chip selector (CS) for SPI mode or Slave Address 2 for I2C mode. Schmitt-Trigger input. Internal pull-down resistor.
Special Control Interface			
EXT_MUTE	27	I	External mute control input. Active High. Assert 'HIGH' to mute audio output. Internal pull-down resistor.
OVERLOAD	76	I	Power stage overload indication input. Polarity is programmable. Schmitt-Trigger input. When OVERLOAD is asserted, all PWM audio outputs go to "LOW". That shutdown process is programmable. Internal pull-down resistor.
EPD_ENA	77	O	External amplifier power device enable output. Active High.
Test Mode			
TEST_MODE1	97	I	Test mode selection pin 1. In normal operation, it should be "LOW" or not connected. Internal pull-down resistor.
TEST_MODE2	98	I	Test mode selection pin 2. In normal operation, it should be "LOW" or not connected. Internal pull-down resistor.
SCAN_ENA	99	I	Scan enable. Active High. In normal operation, it should be "LOW" or not connected. Internal pull-down resistor.
TEST_MODE3	100	I	Test mode selection pin 3. In normal operation, it should be "LOW" or not connected. Internal pull-down resistor.

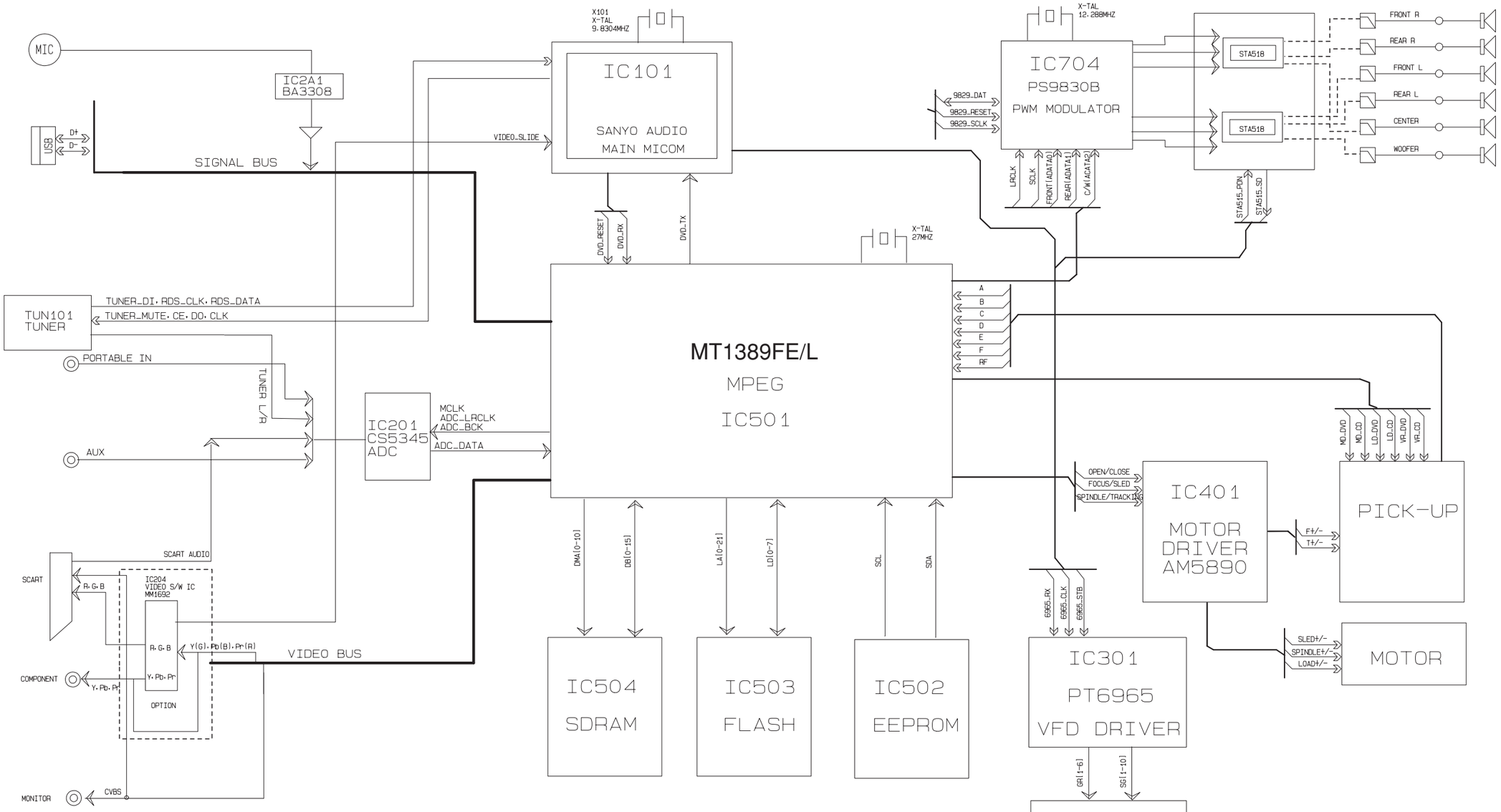
All inputs and bi-directional inputs are 5 Volt tolerant. The corresponding pins can be connected to the buses that can swing between 0V and 5V. The output-only pins are not 5V tolerant and the buses they are connected to can swing only between 0V and 3.3V.

WIRING DIAGRAM



WIRING DIAGRAM
HT303/HT353
EBY38558901(#8) REV 8.2
2008.12.16

OVERALL BLOCK DIAGRAM



BLOCK DIAGRAM
HT303/HT353
EBY38558901(#7) REV 8.2
2008.12.16

CIRCUIT DIAGRAMS

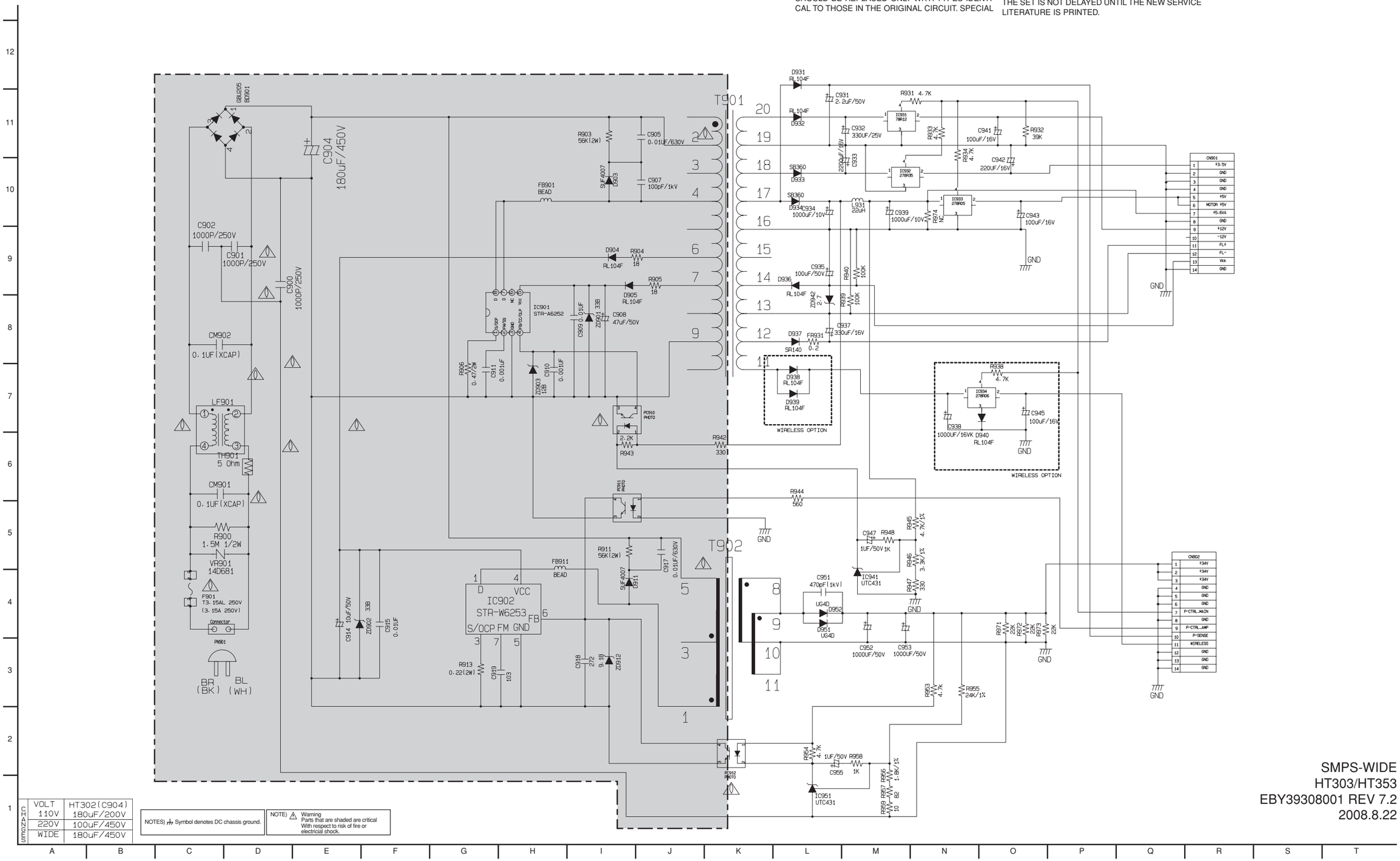
1. SMPS(POWER) CIRCUIT DIAGRAM

IMPORTANT SAFETY NOTICE

WHEN SERVICING THIS CHASSIS, UNDER NO CIRCUMSTANCES SHOULD THE ORIGINAL DESIGN BE MODIFIED OR ALTERED WITHOUT PERMISSION FROM THE LG CORPORATION. ALL COMPONENTS SHOULD BE REPLACED ONLY WITH TYPES IDENTICAL TO THOSE IN THE ORIGINAL CIRCUIT. SPECIAL COMPONENTS ARE SHADED ON THE SCHEMATIC FOR EASY IDENTIFICATION.
THIS CIRCUIT DIAGRAM MAY OCCASIONALLY DIFFER FROM THE ACTUAL CIRCUIT USED. THIS WAY, IMPLEMENTATION OF THE LATEST SAFETY AND PERFORMANCE IMPROVEMENT CHANGES INTO THE SET IS NOT DELAYED UNTIL THE NEW SERVICE LITERATURE IS PRINTED.

NOTE :

1. Shaded(▩) parts are critical for safety. Replace only with specified part number.
2. Voltages are DC-measured with a digital voltmeter during Play mode.



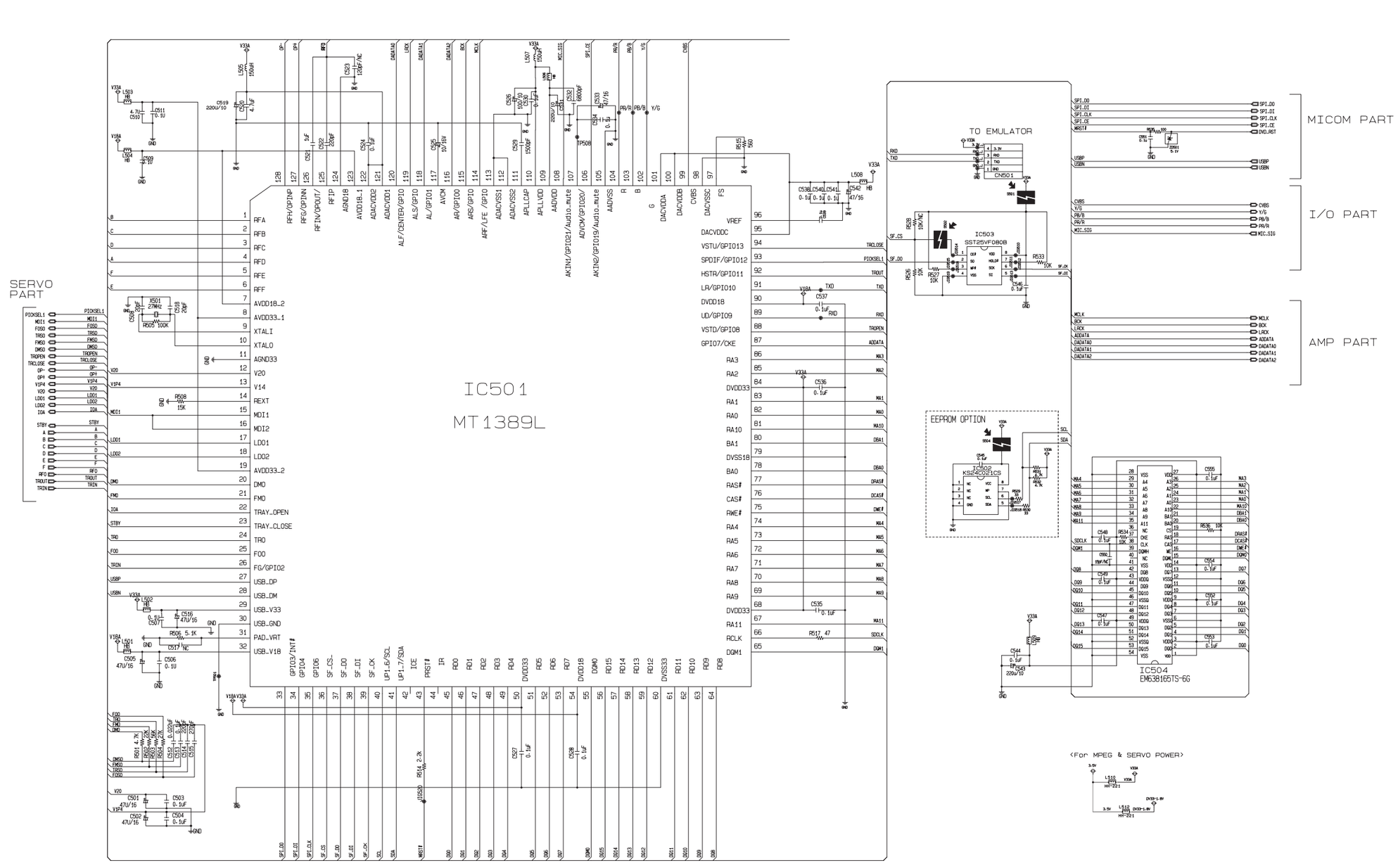
VOLT	HT302(C904)
110V	180uF/200V
220V	100uF/450V
WIDE	180uF/450V

NOTES) ⏚ Symbol denotes DC chassis ground.

NOTE) ⚠ Warning
Parts that are shaded are critical With respect to risk of fire or electricial shock.

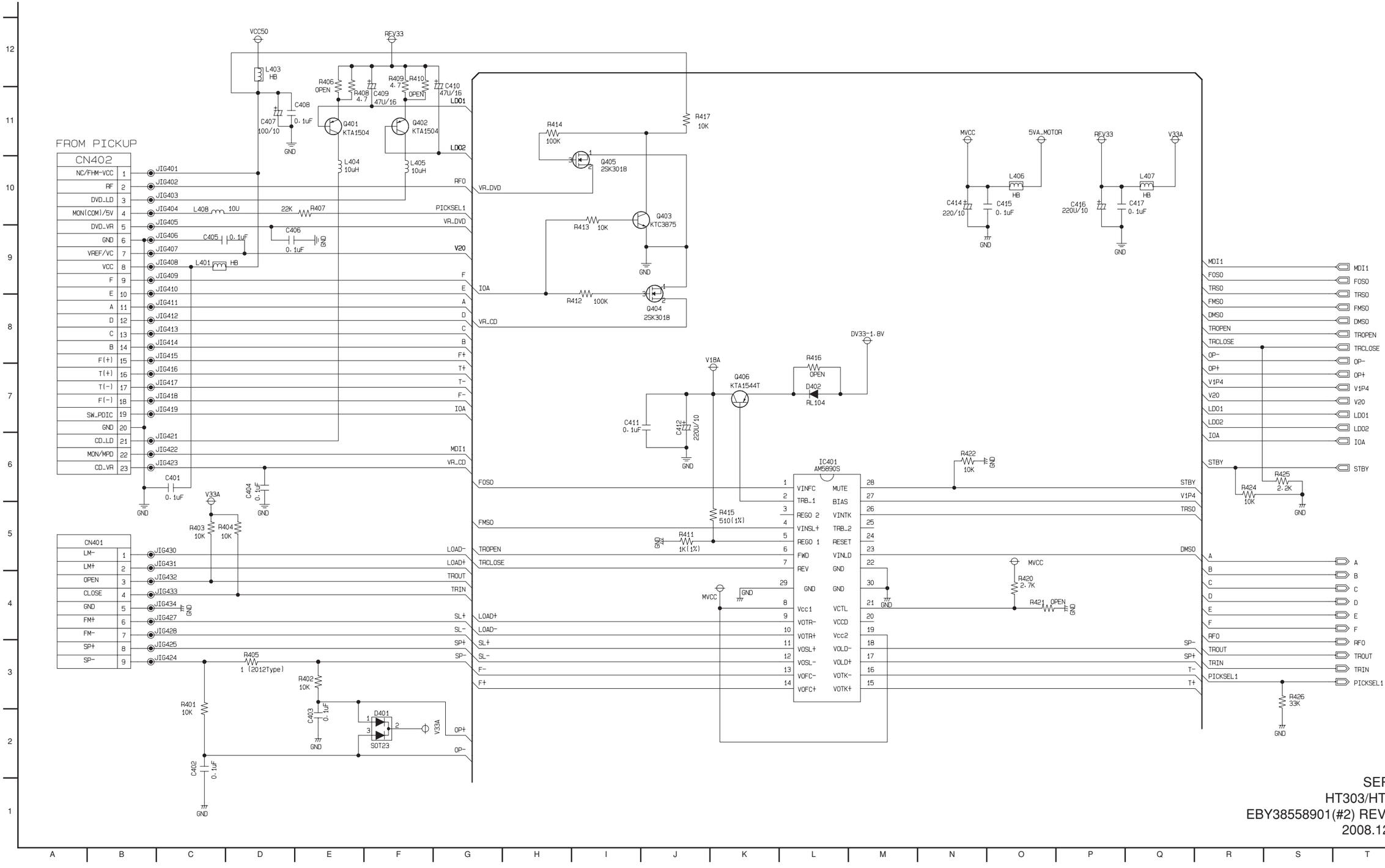
SMPS-WIDE
HT303/HT353
EBY39308001 REV 7.2
2008.8.22

2. MPEG CIRCUIT DIAGRAM



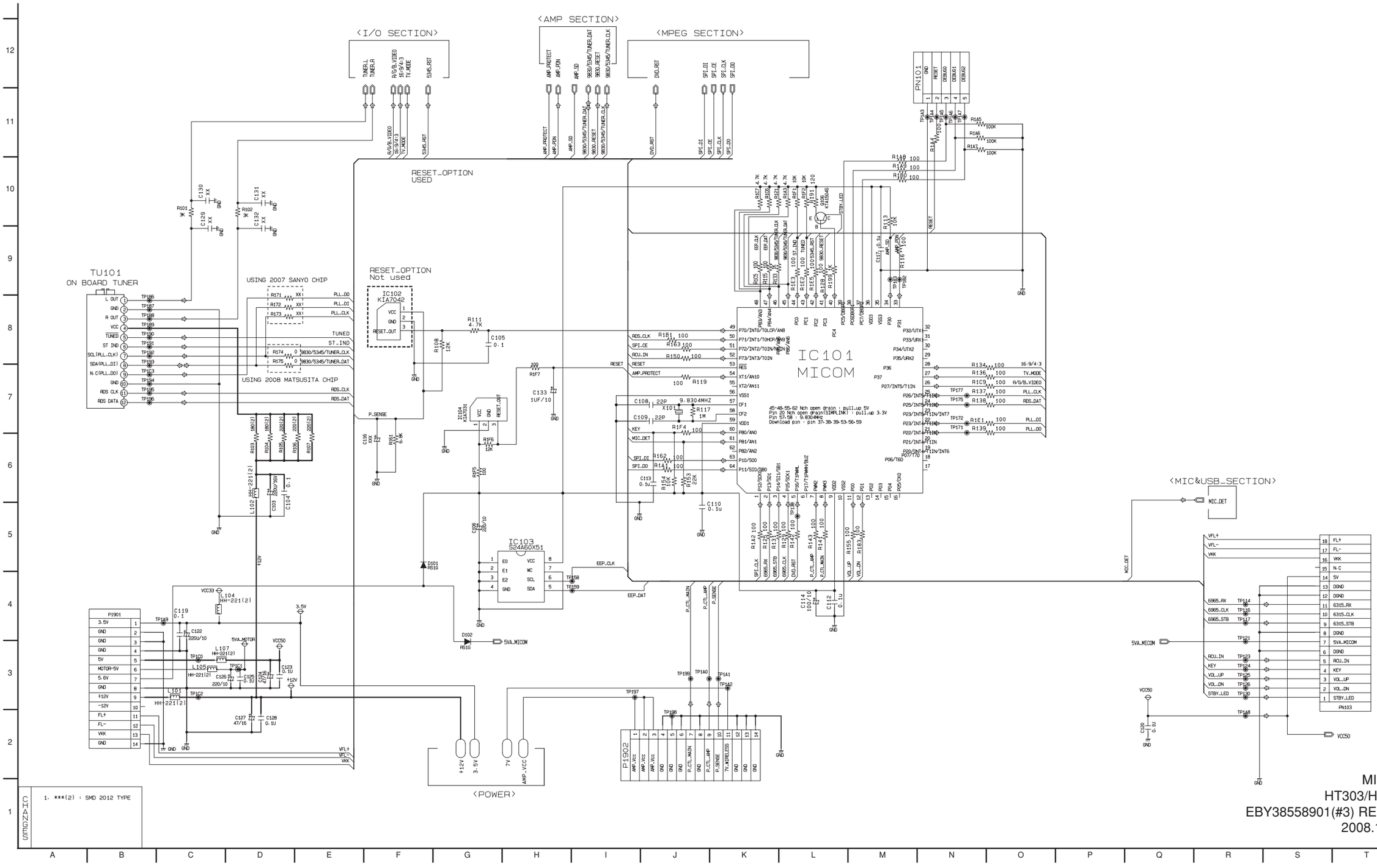
MPEG PART
HT303/HT353
EBY38558901(#1) REV 8.2
2008.12. 16

3. SERVO CIRCUIT DIAGRAM



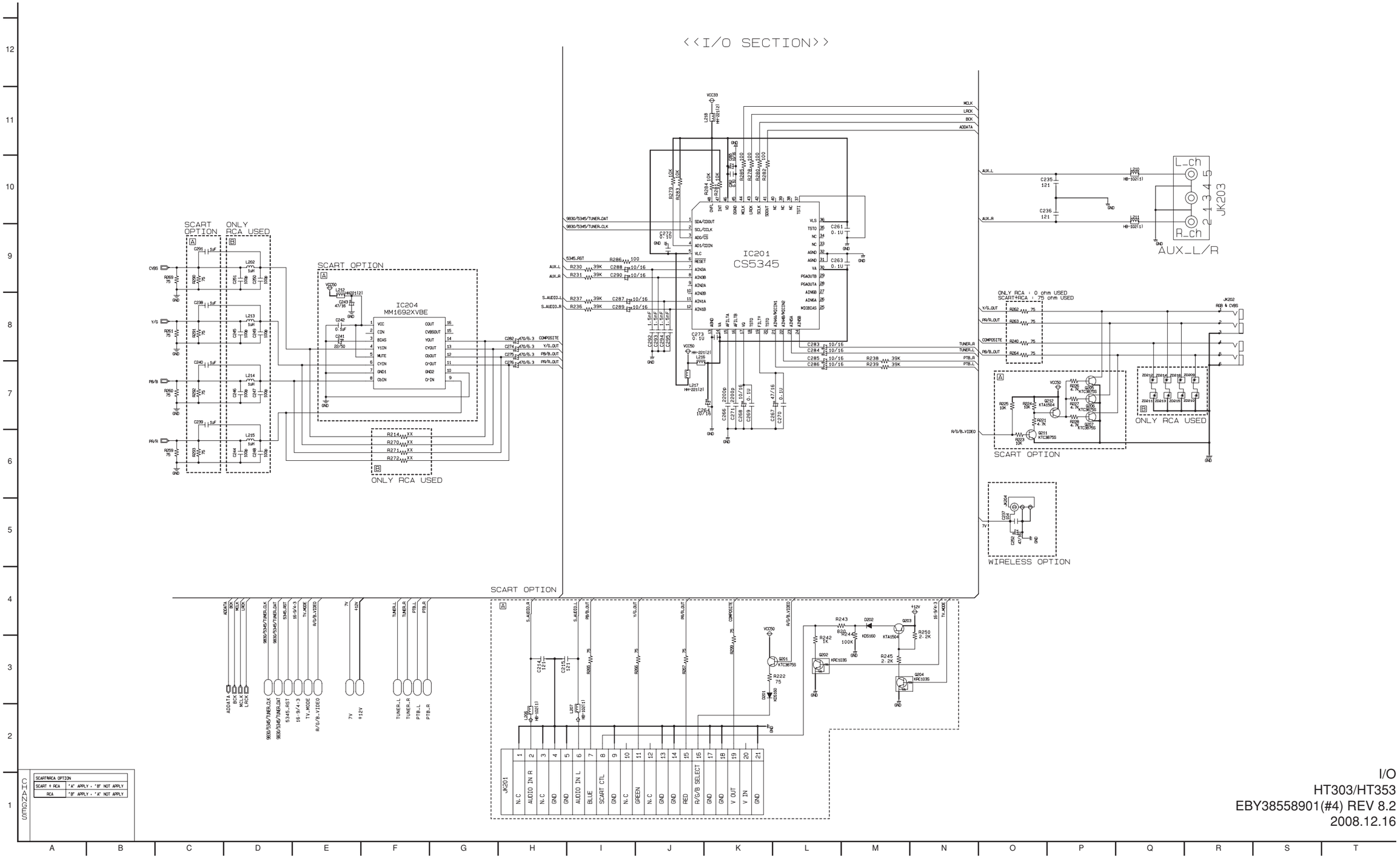
SERVO
HT303/HT353
EBY38558901(#2) REV 8.2
2008.12.16

4. MICOM CIRCUIT DIAGRAM

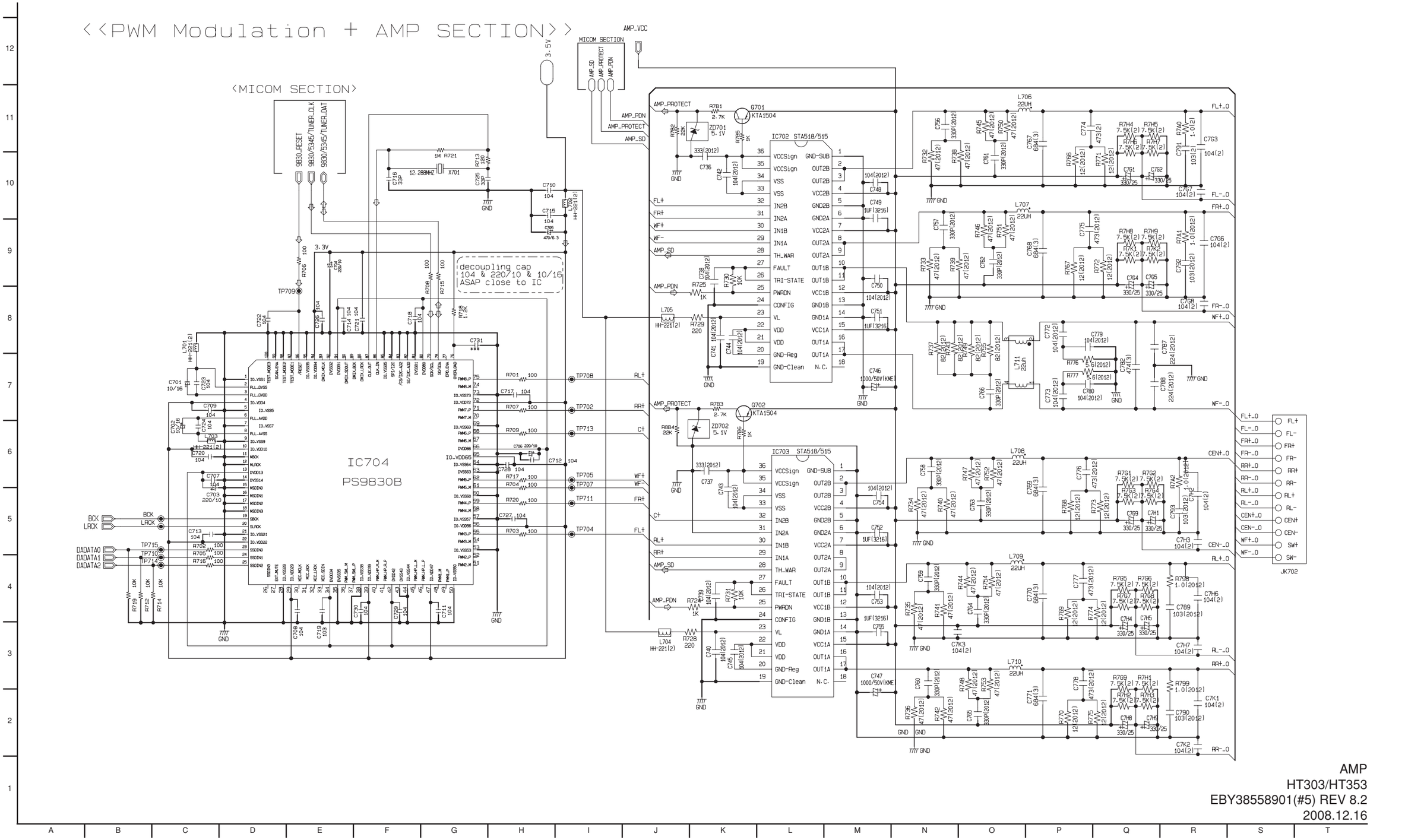


MICOM
HT303/HT353
EBY38558901(#3) REV 8.2
2008.12.16

5. I/O CIRCUIT DIAGRAM

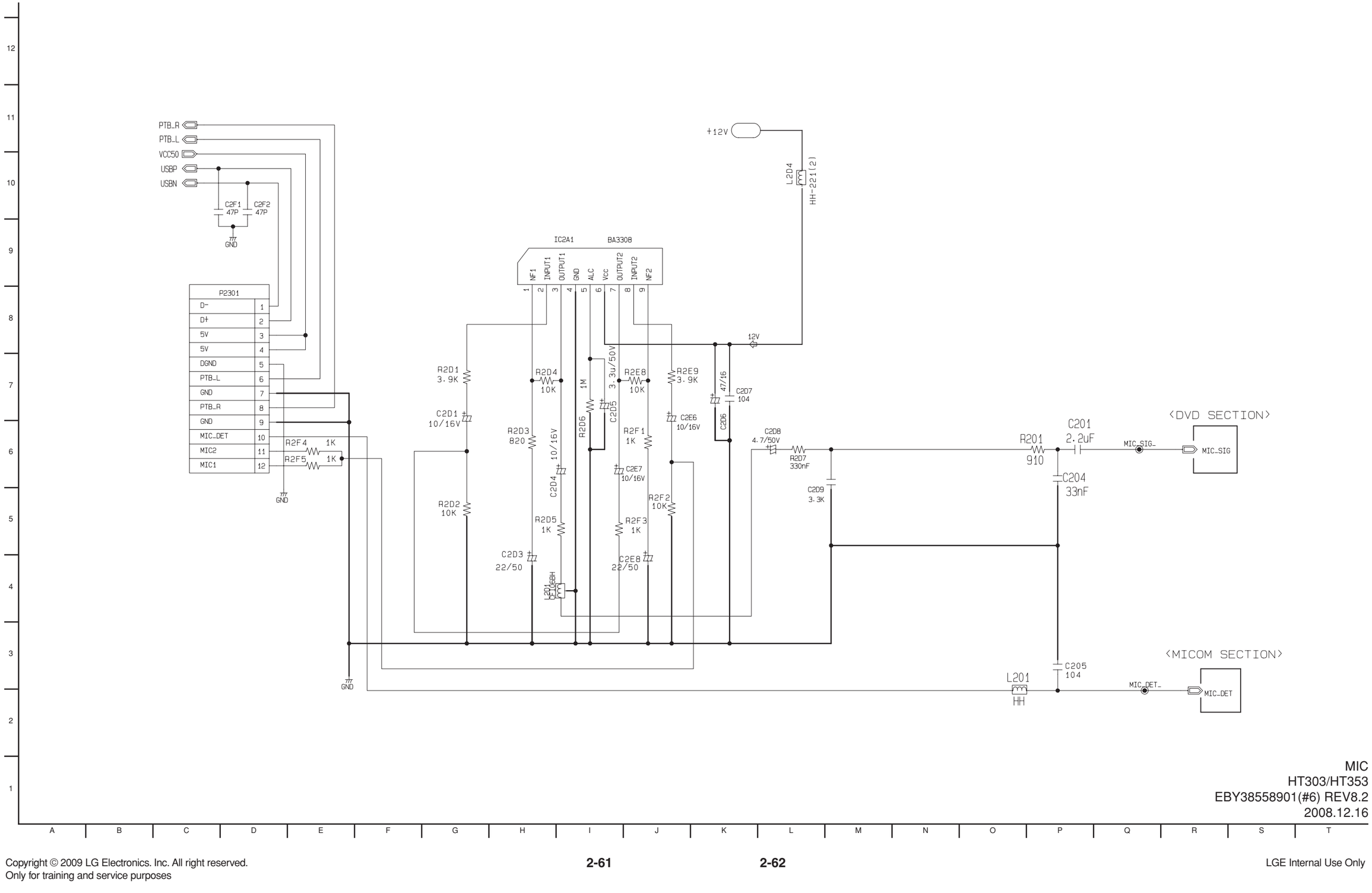


6. AMP CIRCUIT DIAGRAM



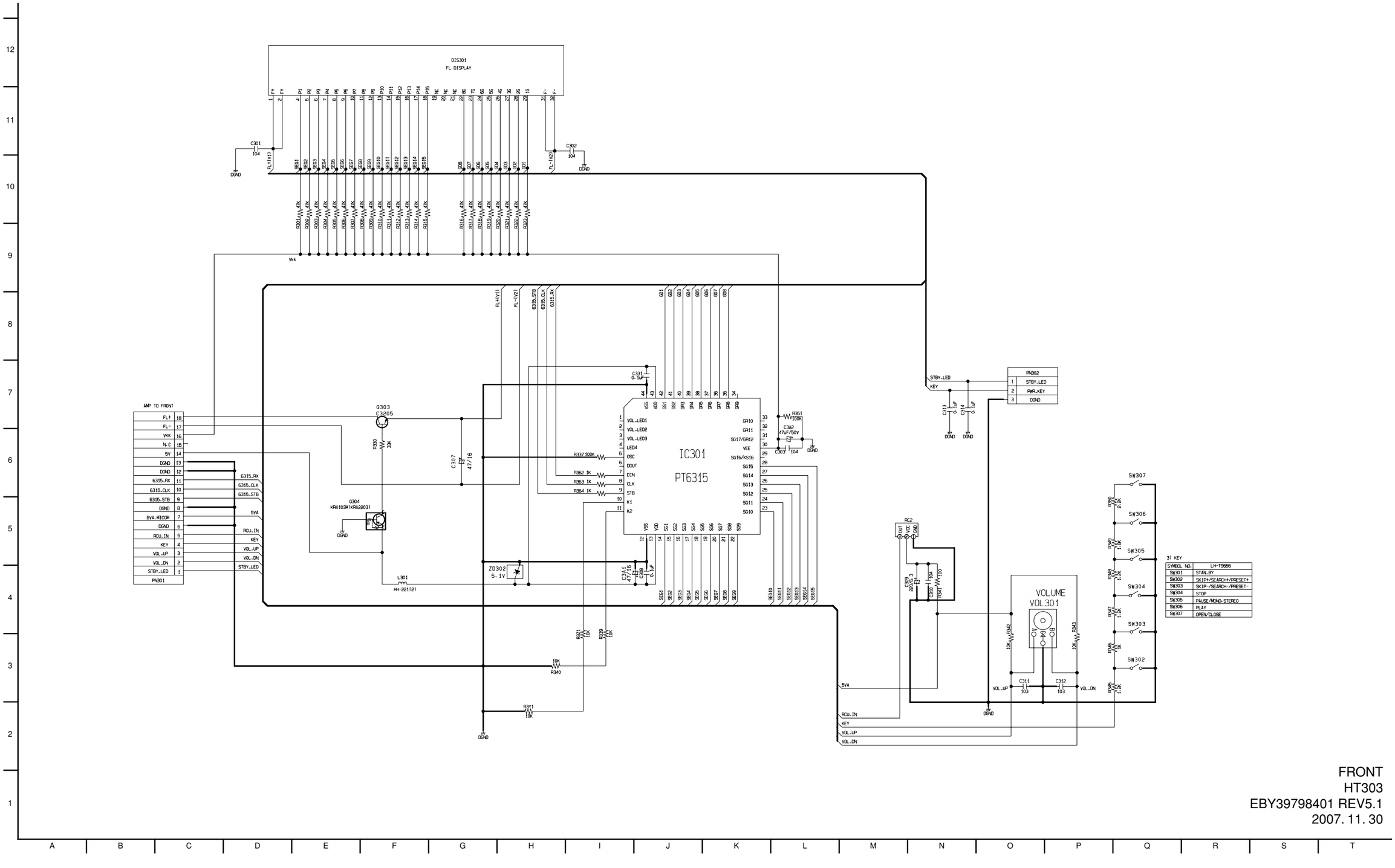
AMP
HT303/HT353
EBY38558901(#5) REV 8.2
2008.12.16

7. MIC CIRCUIT DIAGRAM



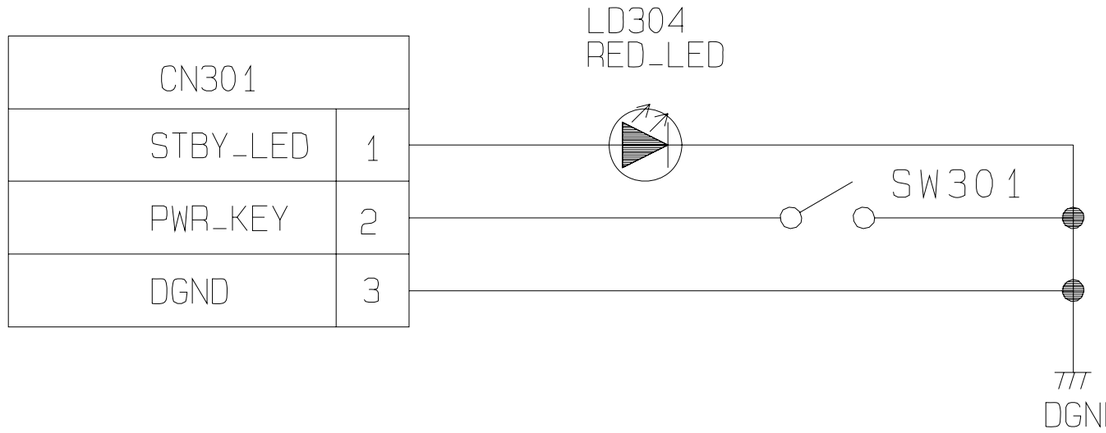
MIC
HT303/HT353
EBY38558901(#6) REV8.2
2008.12.16

8. FRONT CIRCUIT DIAGRAM



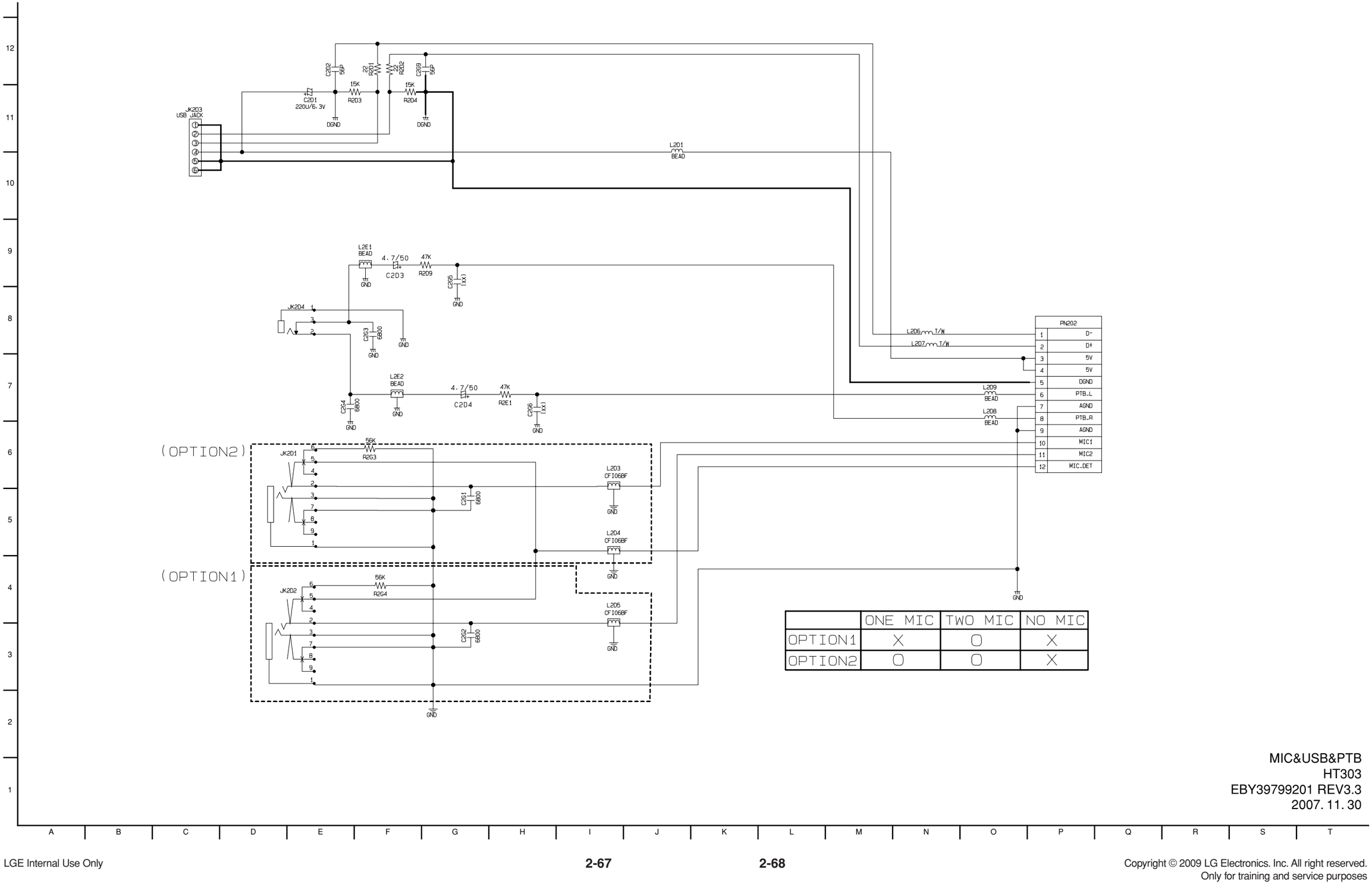
FRONT
HT303
EBY39798401 REV5.1
2007. 11. 30

9. PWR KEY CIRCUIT DIAGRAM



PWR KEY
HT303
EBY39799101(#1) REV2.1
2007. 11. 30

10. MIC & USB & PTB CIRCUIT DIAGRAM

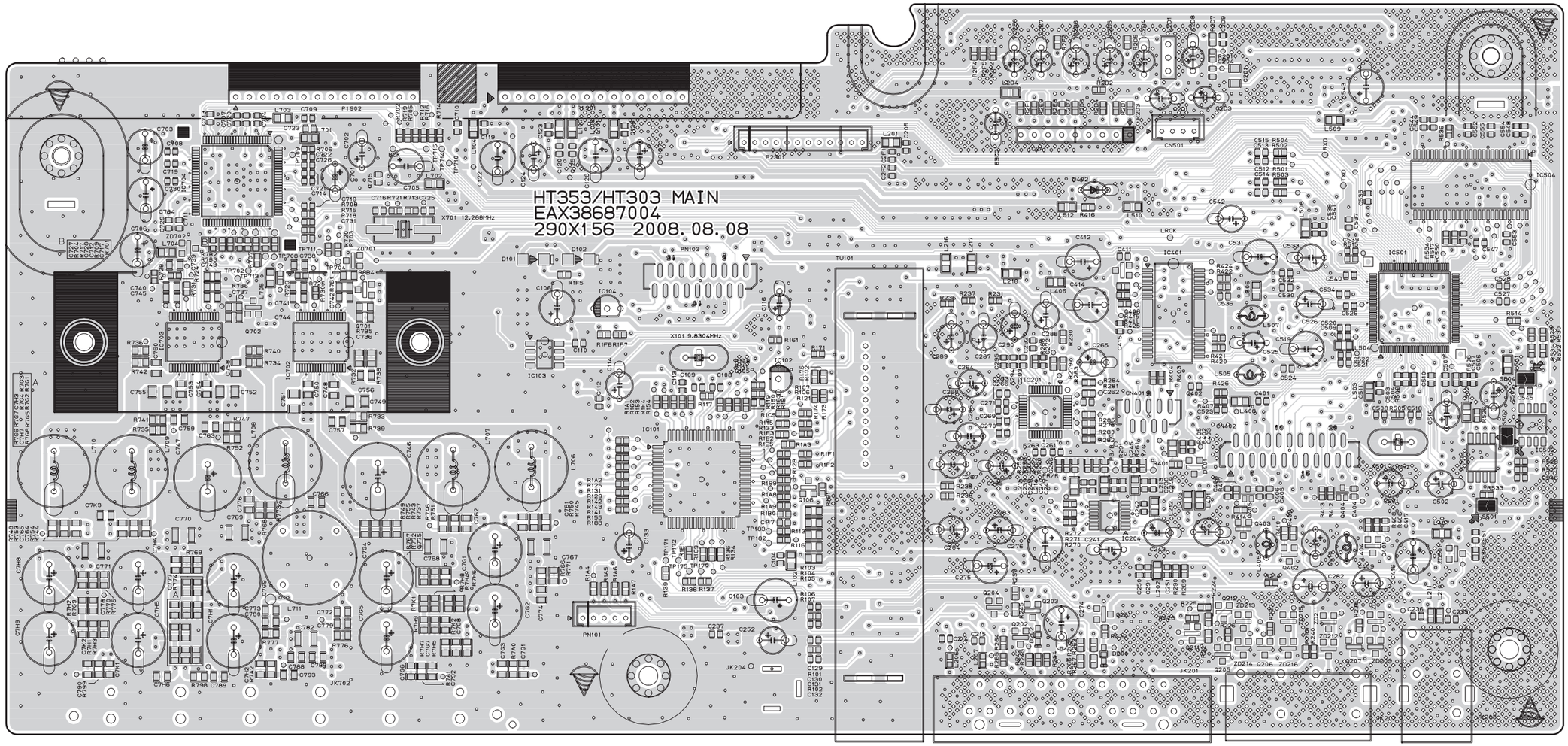


	ONE MIC	TWO MIC	NO MIC
OPTION1	X	O	X
OPTION2	O	O	X

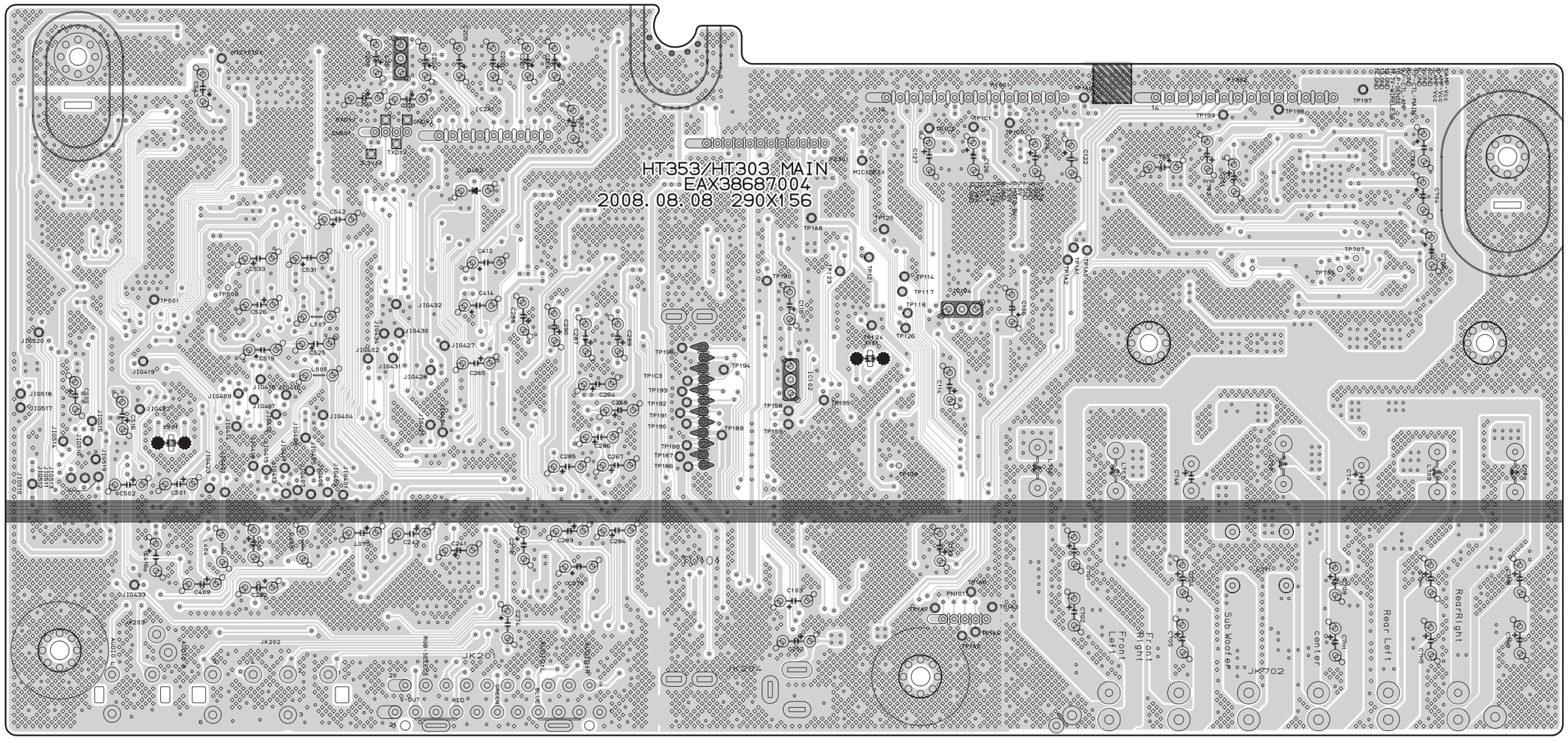
MIC&USB&PTB
HT303
EBY39799201 REV3.3
2007. 11. 30

PRINTED CIRCUIT BOARD DIAGRAMS

1. MAIN P.C. BOARD DIAGRAM (TOP VIEW)

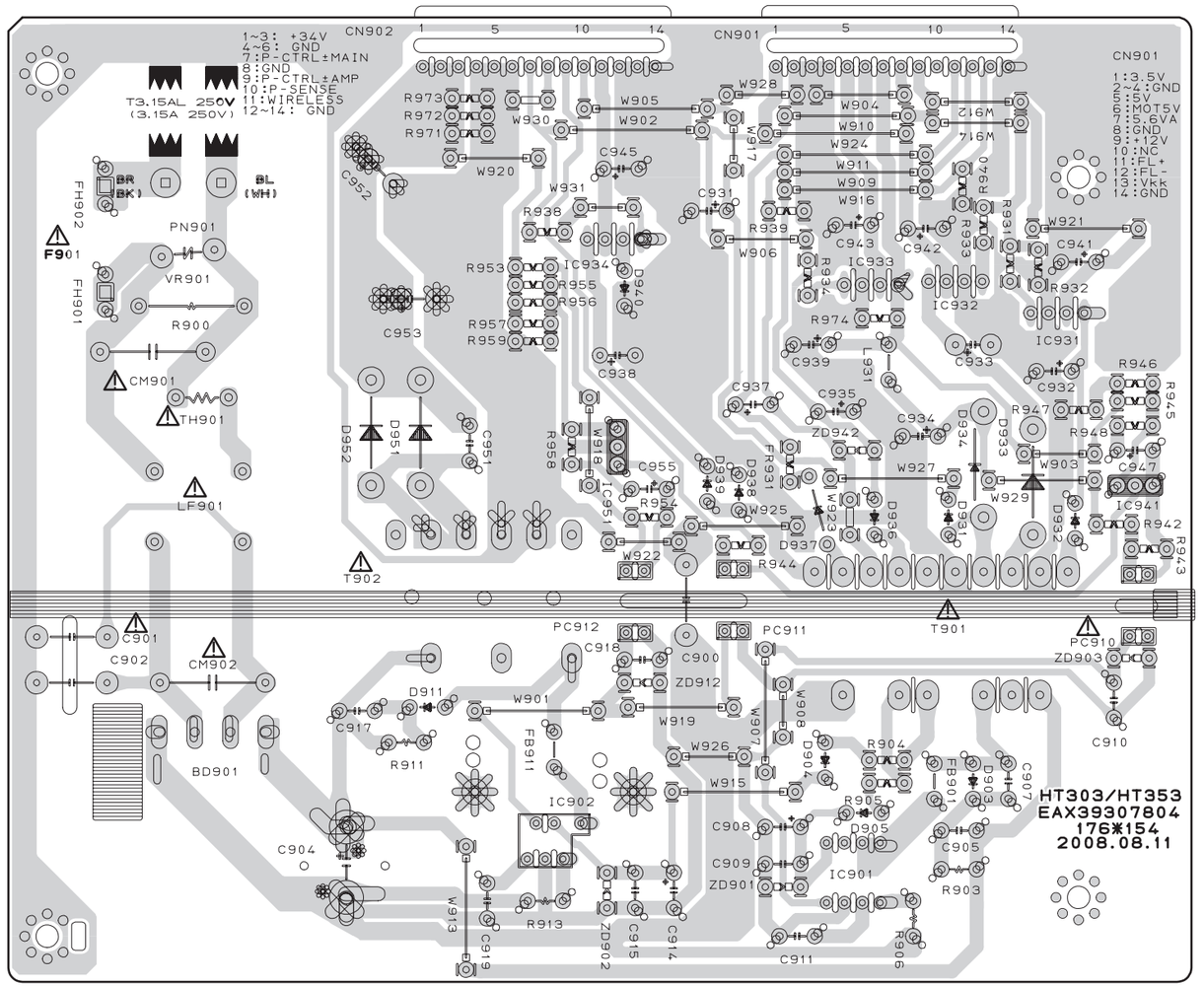


MAIN P.C. BOARD DIAGRAM (BOTTOM VIEW)

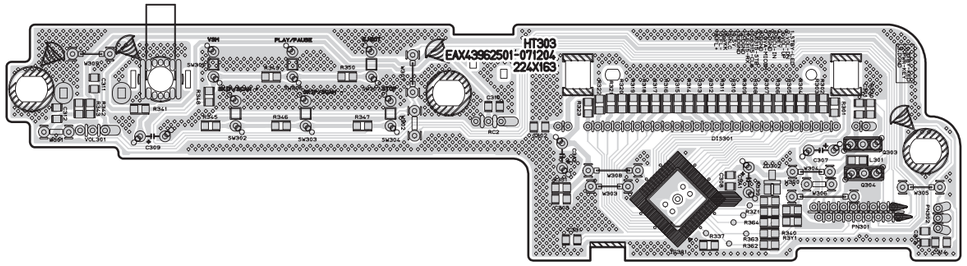


2. SMPS P.C. BOARD DIAGRAM

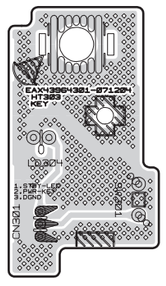
NOTE: Warning
⚠ Parts that are shaded are critical With respect to risk of fire or electrical shock.



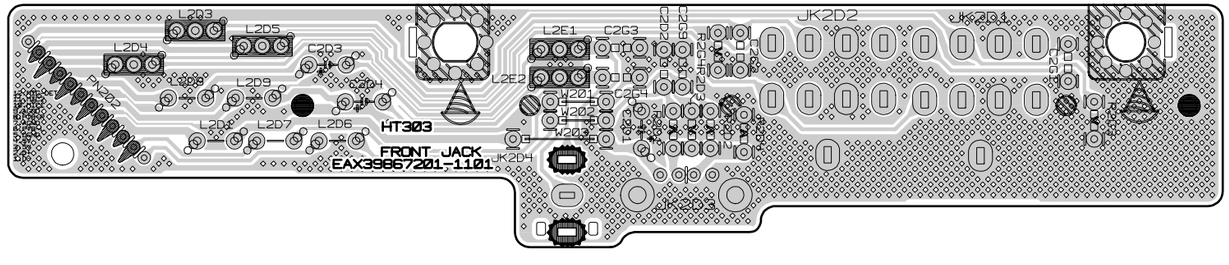
3. TIMER P.C BOARD DIAGRAM



4. KEY P.C. BOARD DIAGRAM



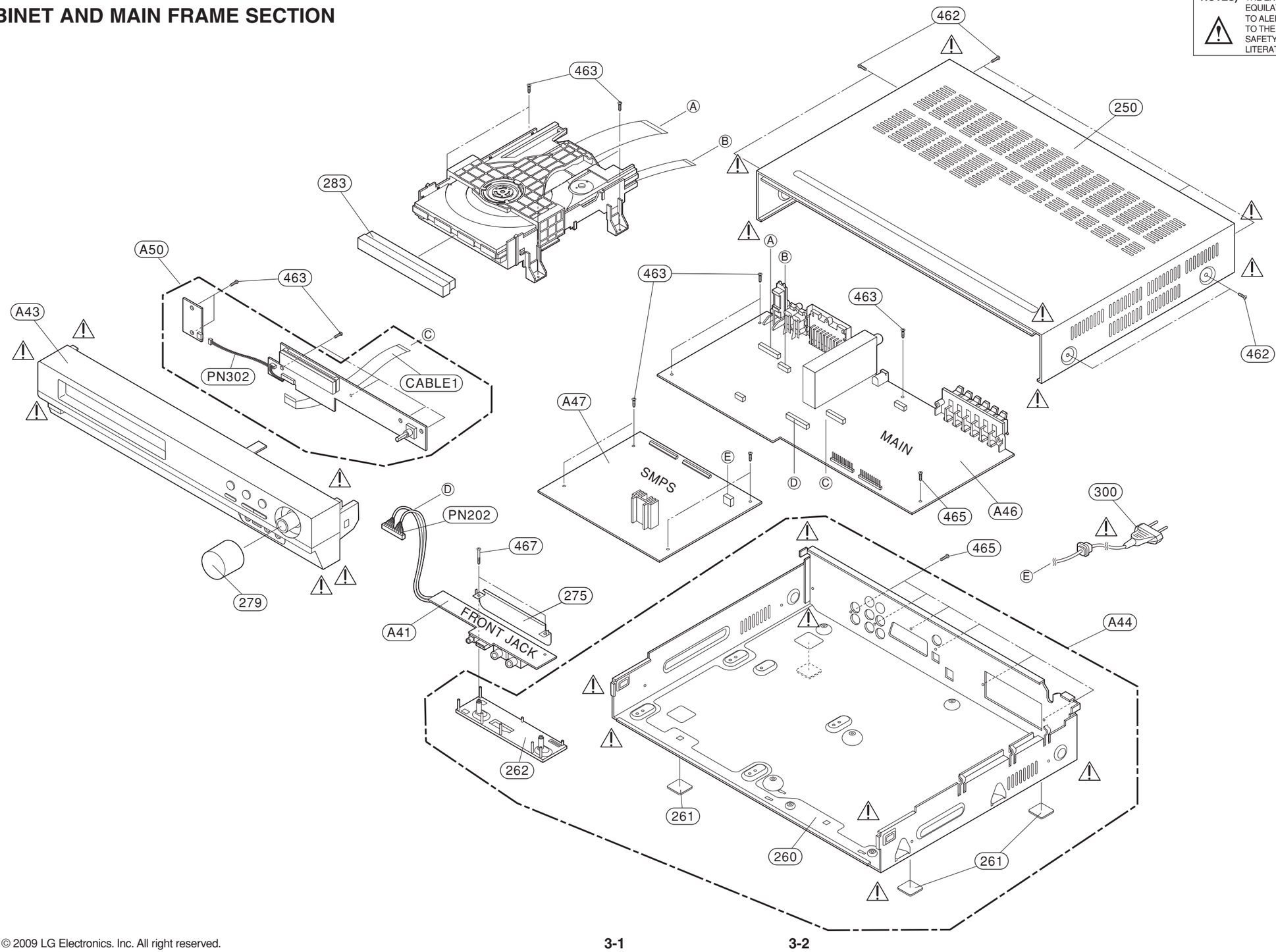
5. FRONT JACK P.C. BOARD DIAGRAM



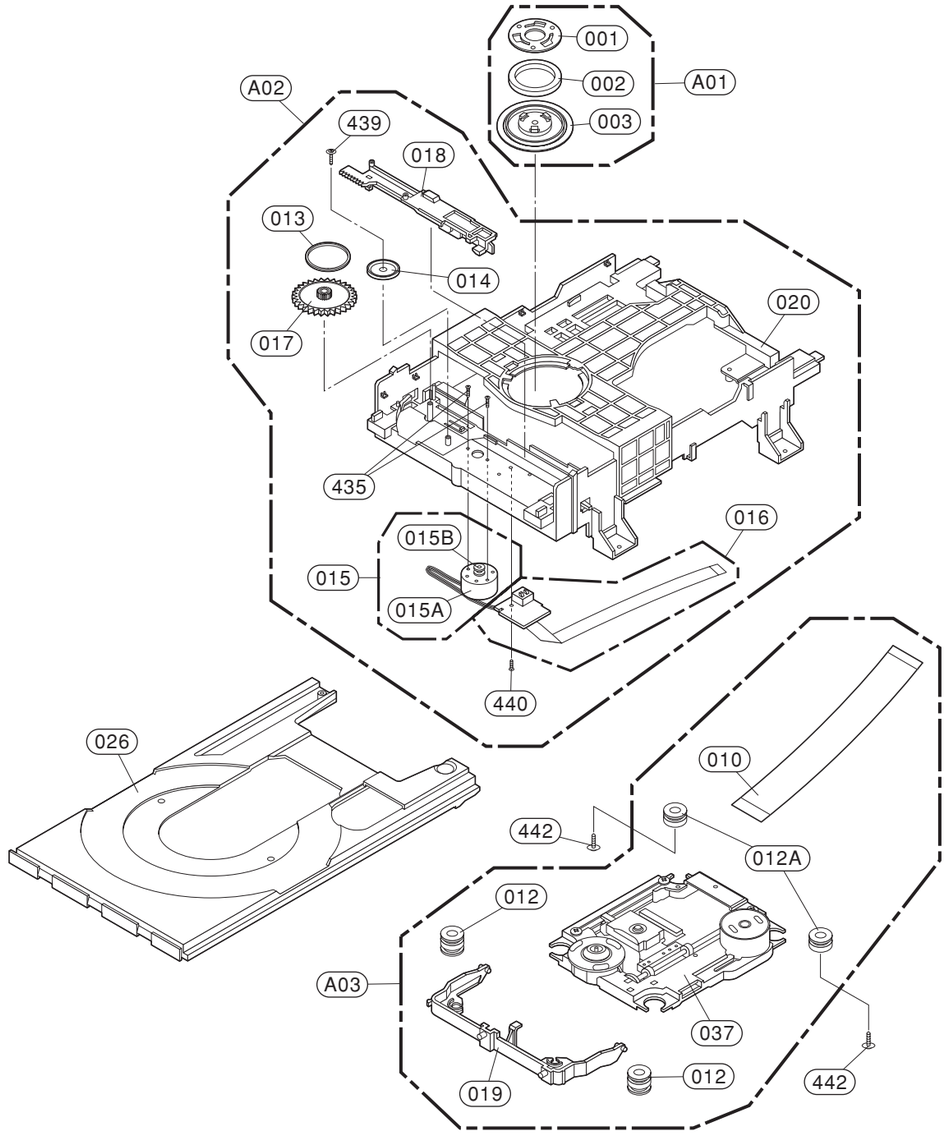
SECTION 3. EXPLODED VIEWS

• CABINET AND MAIN FRAME SECTION

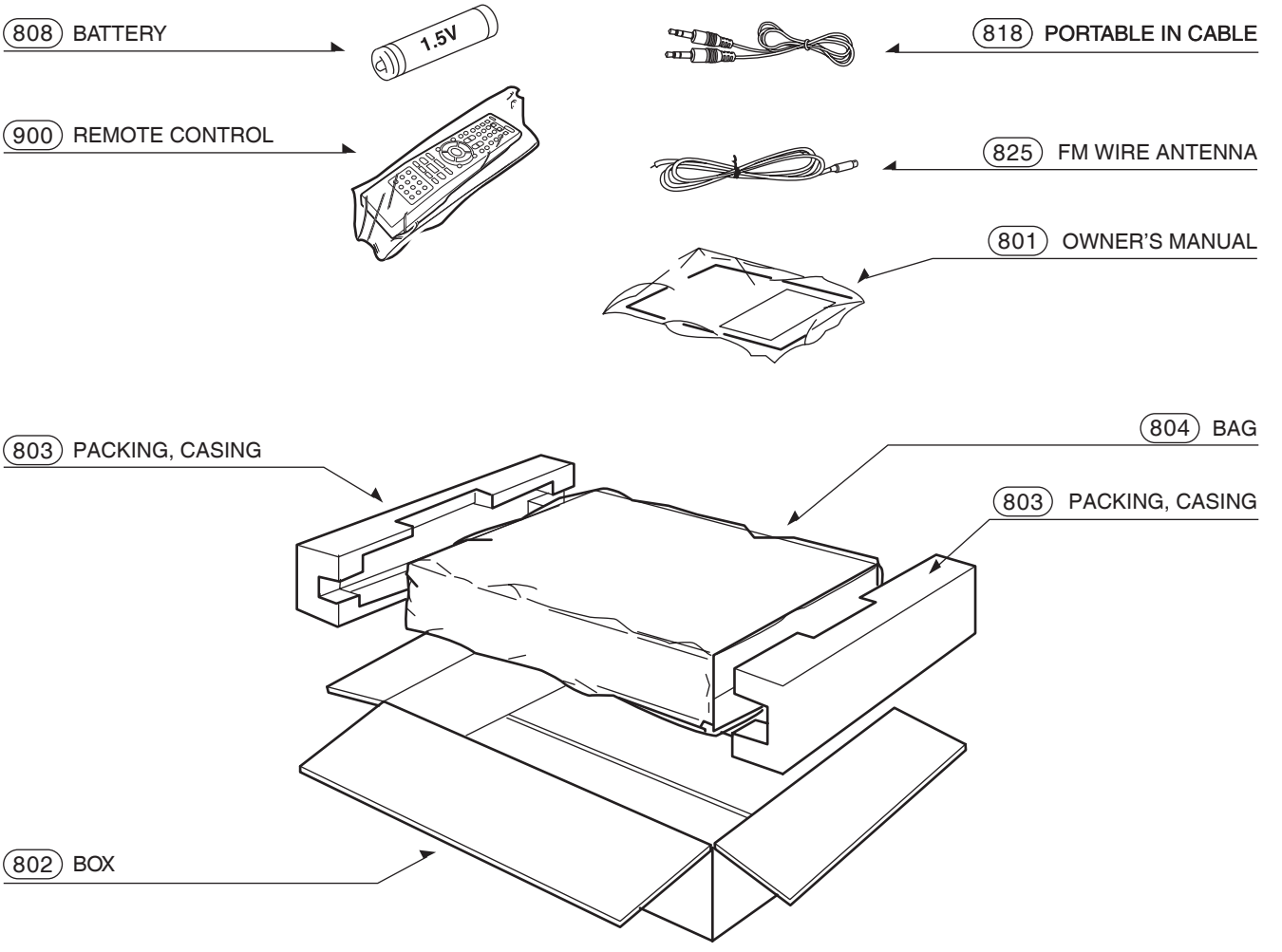
NOTES) THE EXCLAMATION POINT WITHIN AN EQUILATERAL TRIANGLE IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF IMPORTANT SAFETY INFORMATION IN SERVICE LITERATURE.



• DECK MECHANISM EXPLODED VIEW(DP-12TV)

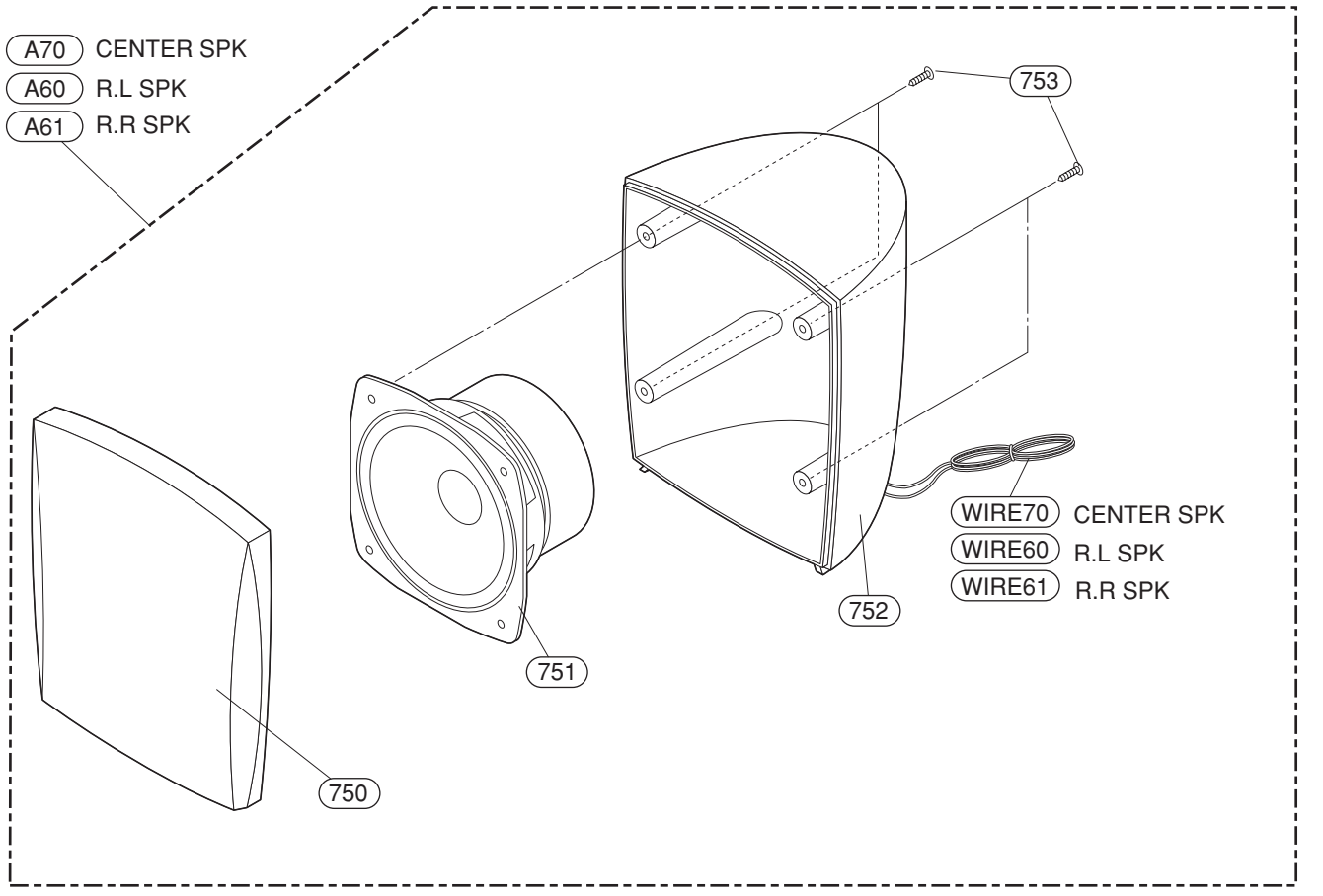


• PACKING ACCESSORY SECTION

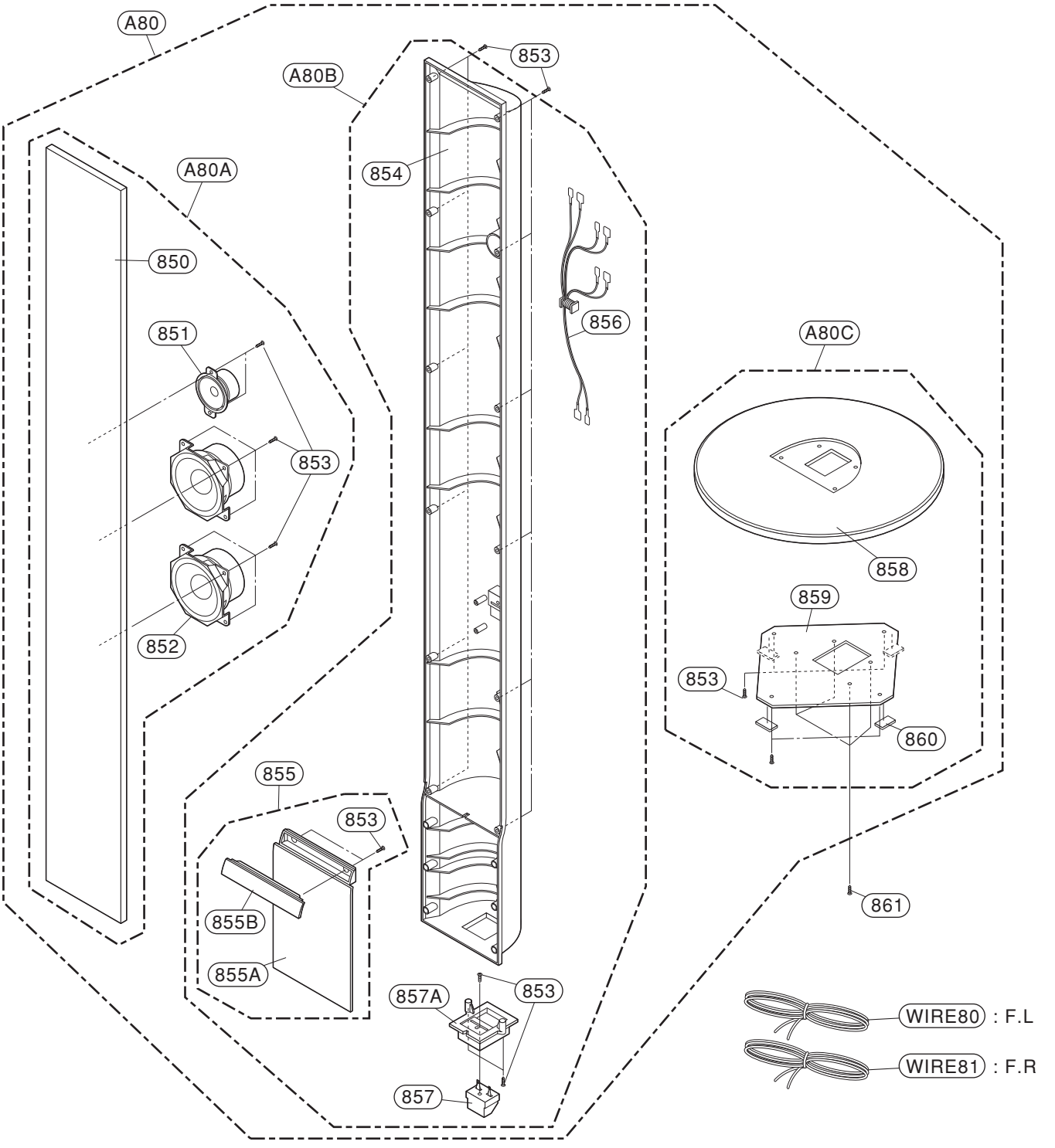


• SPEAKER SECTION

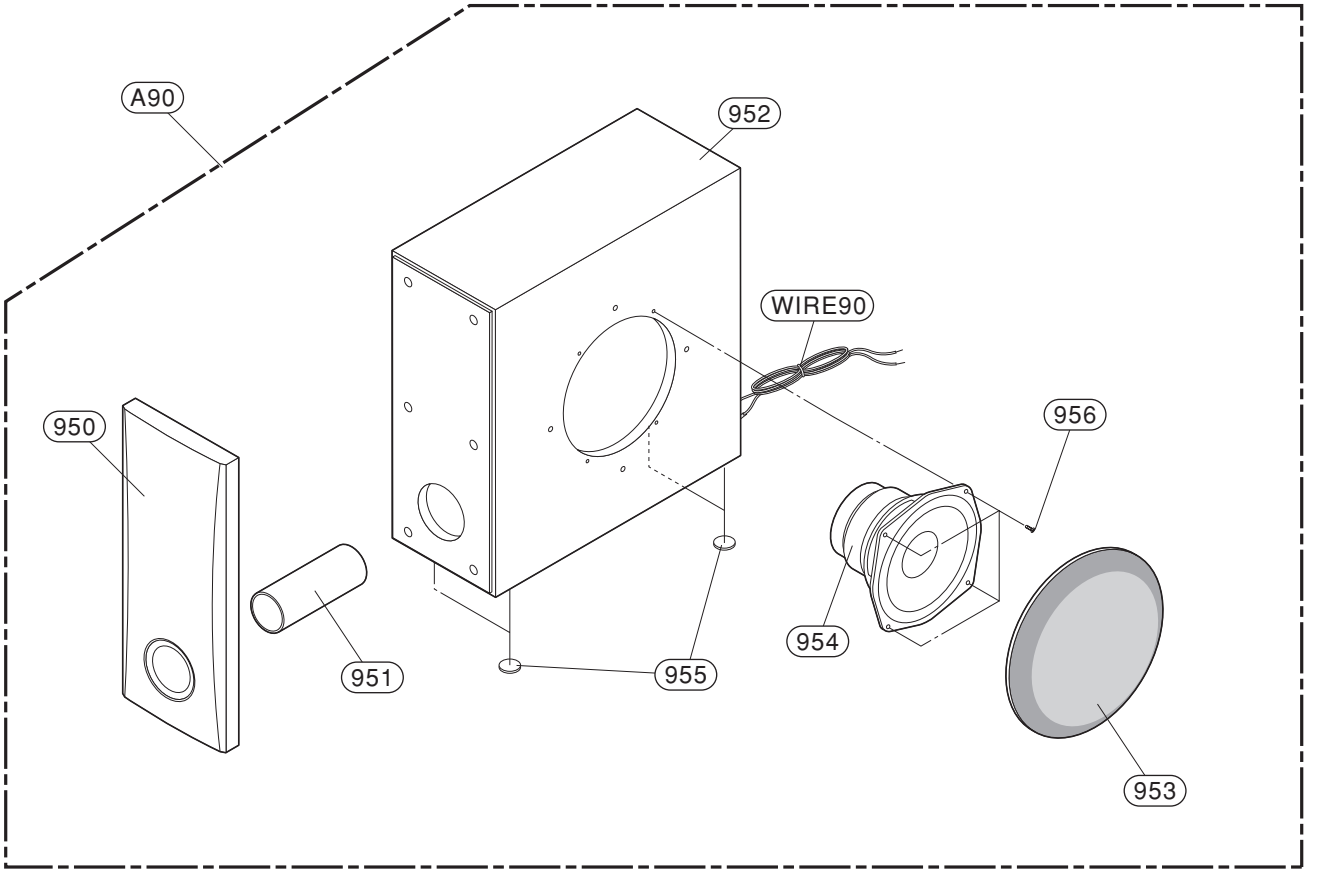
1. CENTER/REAR SPEAKER (SH33PD-S)



2. FRONT SPEAKER (SH33PD-F)



3. PASSIVE SUBWOOFER (SH33PD-W)



MEMO

SECTION 4. MECHANISM (DP-12TV)

[CONTENTS]

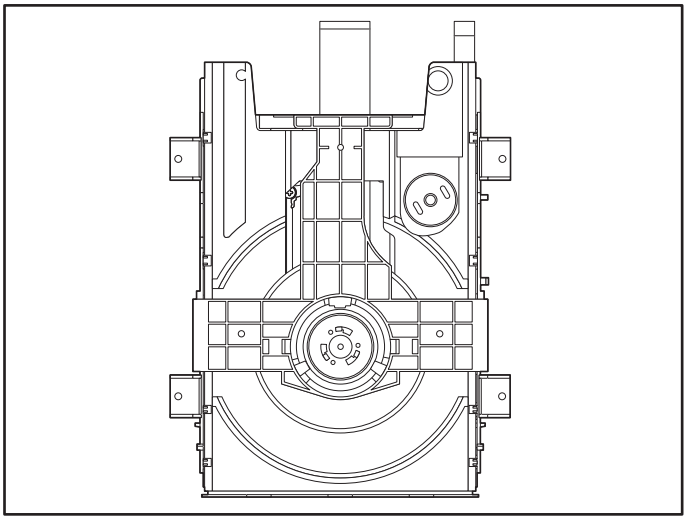
DECK MECHANISM PARTS LOCATIONS

DECK MECHANISM DISASSEMBLY

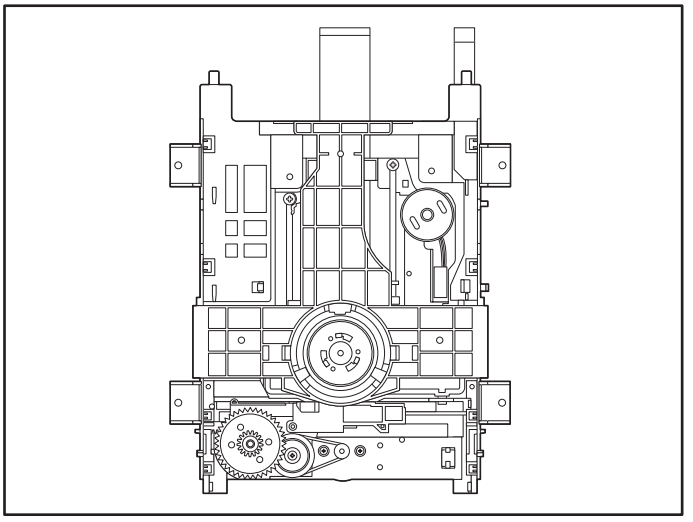
EXPLODED VIEW

DECK MECHANISM PARTS LOCATIONS

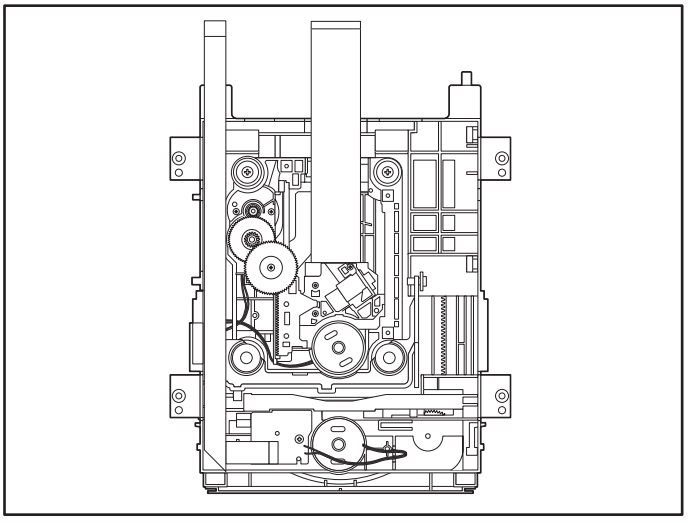
• Top View



• Top View(without Tray Disc)



• Bottom View



Procedure Starting No.		Parts	Fixing Type	Disassembly	Figure
	1	Main Base			4-1
1	2	Clamp Assembly Disc			4-1
1, 2	3	Plate Clamp			4-1
1, 2, 3	4	Magnet Clamp			4-1
1, 2, 3, 4	5	Clamp Upper			4-1
1	6	Tray Disc			4-2
1, 6	7	Base Assembly Sled			4-3
1, 2, 6	8	Gear Feed	4 Screws, 1 Connector 1 Locking Tabs		4-3
1, 2, 6, 8	9	Gear Middle			4-3
1, 2, 6, 8, 9	10	Gear Rack	1 Screw		4-3
1, 2, 7	11	Rubber Rear			4-3
1, 2, 7	12	Frame Assembly Up/Down	1 Screw	Bottom	4-4
1, 2	13	Belt Loading	1 Locking Tab		4-4
1, 2 ,13	14	Gear Pulley			4-4
1, 2, 13, 14	15	Gear Loading	1 Locking Tab		4-4
1, 2, 7, 12, 13, 14	16	Guide Up/Down			4-4
1, 2, 13	17	PWB Assembly Loading	1 Locking Tab 1 Hook 2Screw	Bottom	4-4
1, 2, 7, 12, 13, 14, 15, 16, 17	18	Base Main	2 Locking Tabs		4-4

Note
When reassembling, perform the procedure in reverse order.
The “Bottom” on Disassembly column of above Table indicates the part should be disassembled at the Bottom side.

DECK MECHANISM DISASSEMBLY

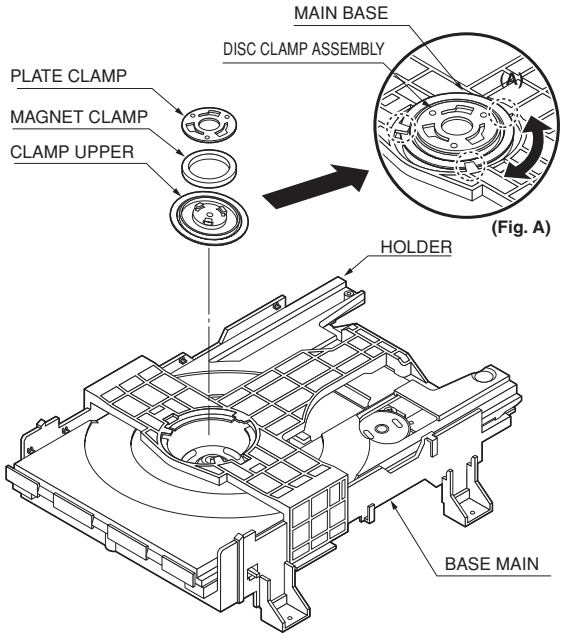


Fig. 4-1

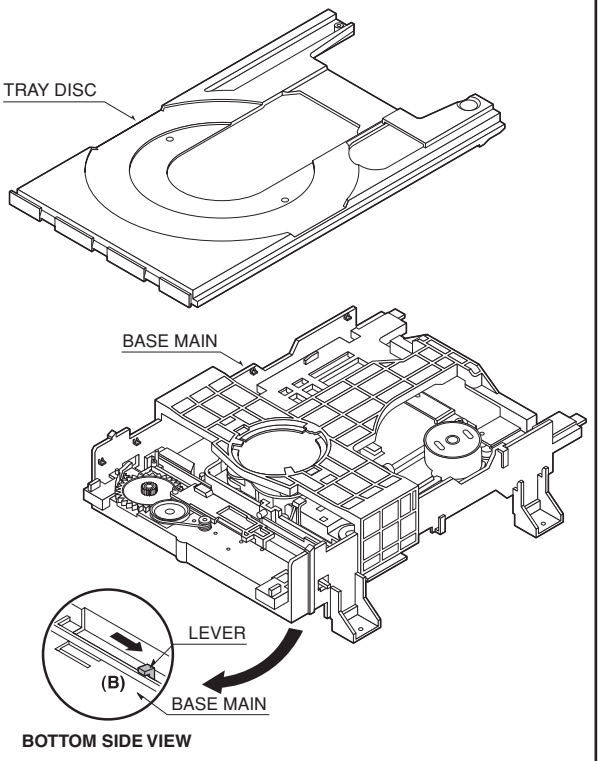


Fig. 4-2

1. Main Base (Fig. 4-1)

1-1. Clamp Assembly Disc

1) Place the Clamp Assembly Disc as Fig. (A)
2) Lift up the Clamp Assembly Disc in direction of arrow(A).
3) Separate the Clamp Assembly Disc from the Holder Clamp.

1-1-1. Plate Clamp

1) Turn the Plate Clamp to counterclockwise direction and then lift up the Plate Clamp.

1-1-2. Magnet Clamp

1-1-3. Clamp Upper

2. Tray Disc (Fig. 4-2)

1) Insert and push a Driver in the emergency eject hole(A) at the right side, or put the Driver on the Lever(B) of the Gear Emergency and pull the Lever(B) in direction of arrow so that the Tray Disc is ejected about 15~20mm.
2) Pull the Tray Disc until it is separated from the Base Main completely.

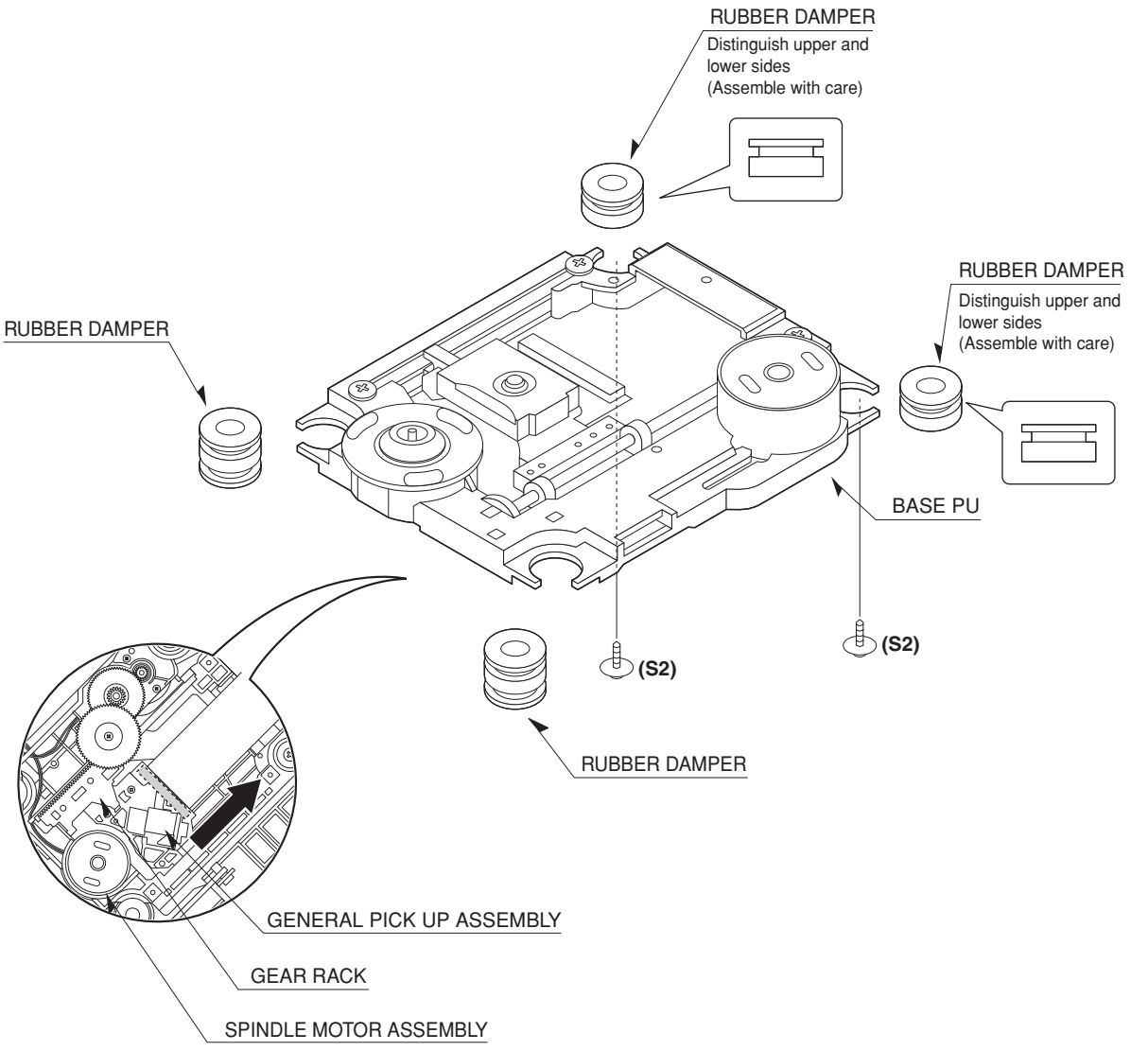


Fig. 4-3

3. Base Assembly Sled (Fig. 4-3)

1) Release 4 Screw(S2).
2) Disconnect the FFC Connector(C1)

3-1. Gear Feed

3-2. Gear Middle

3-3. Gear Rack

1) Release the Scerw(S3)

4. Rubber Rear (Fig. 4-3)

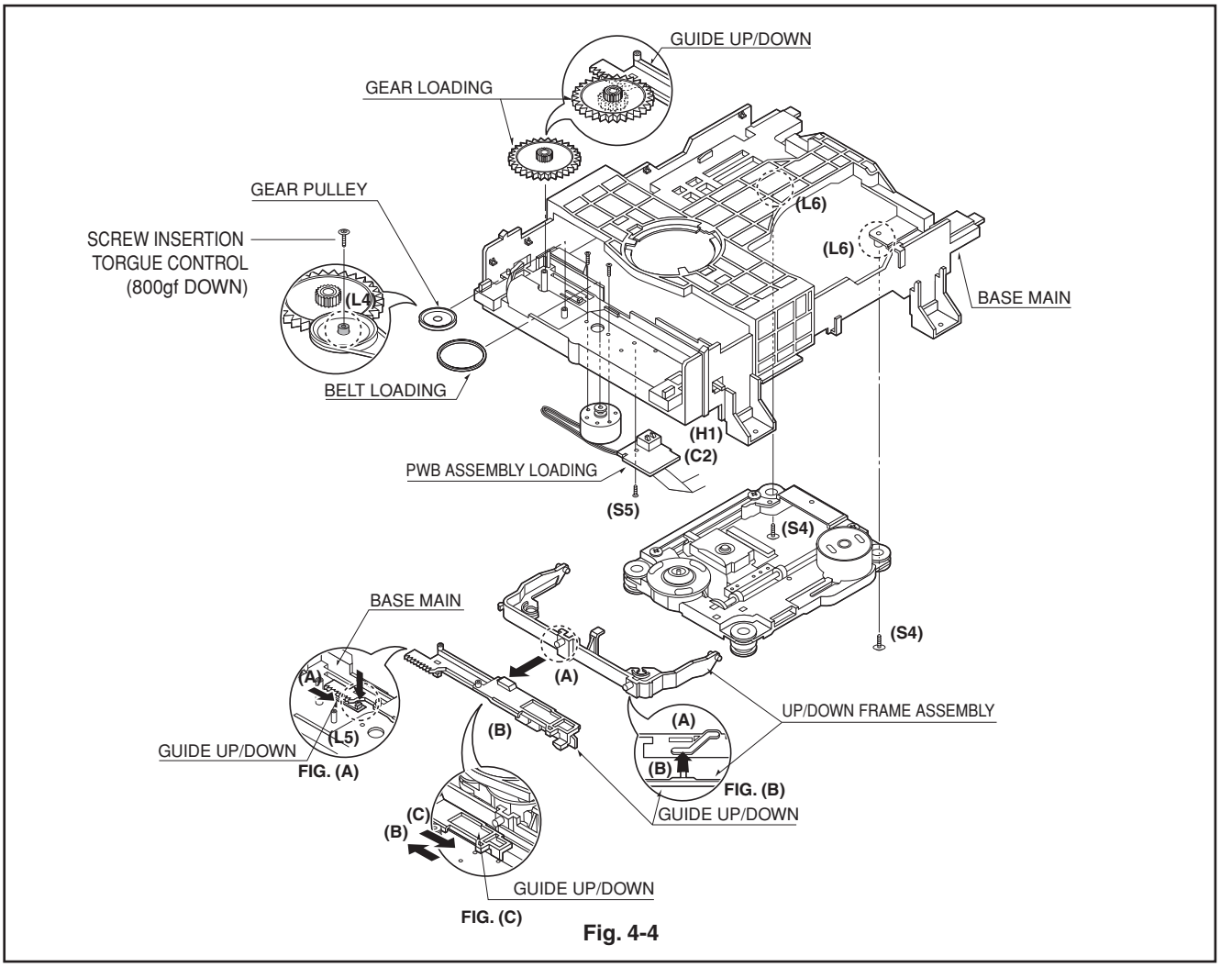


Fig. 4-4

5. Frame Assembly Up/Down (Fig. 4-4)

Note

Put the Base Main face down(Bottom Side)

1) Release the screw(S4)
2) Unlock the Locking Tab(L3) in direction of arrow and then lift up the Frame Assembly Up/Down to separate it from the Base Main.

Note

- When reassembling move the Guide Up/Down in direction of arrow(C) until it is positioned as Fig.(C).
- When reassembling insert (A) portion of the Frame Assembly Up/Down in the (B) portion of the Guide Up/Down as Fig.(B)

6. Belt Loading(Fig. 4-4)

Note

Put the Base Main on original position(Top Side)

7. Gear pulley (Fig. 4-4)

1) Unlock the Locking Tab(L4) in direction of arrow(B) and then separate the Gear Pulley from the Base Main.

8. Gear Loading (Fig. 4-4)

9. Guide Up/Down (Fig. 4-4)

1) Move the Guide Up/Down in direction of arrow(A) as Fig.(A)
2) Push the Locking Tab(L5) down and then lift up the Guide Up/Down to separate it from the Base Main.

Note

When reassembling place the Guide Up/Down as Fig.(C) and move it in direction arrow(B) until it is locked by the Locking Tab(L5). And confirm the Guide Up/Down as Fig.(A)

10. PWB Assembly Loading (Fig. 4-4)

Note

Put the Base Main face down(Bottom Side)

1) Release 1 Screws(S5)
2) Unlock the Loading Motor (C2) from the Hook (H1) on the Base Main.
3) Unlock 2 Locking Tabs(L6) and separate the PWB Assembly Loading from the Base Main.

11. Base Main(Fig. 4-4)

DECK MECHANISM EXPLODED VIEW (DP-12TV)