HT32F52344/HT32F52354
Datasheet

32-Bit Arm® Cortex®-M0+ Microcontroller,
up to 128 KB Flash and 8 KB SRAM with 1 Msps ADC,
CMP, DIV, UART, SPI, I²C, MCTM, GPTM, SCTM, BFTM,
CRC, RTC, WDT, PDMA, EBI and USB2.0 FS

Revision: V1.20 Date: August 28, 2025

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1 General Description

The Holtek HT32F52344/52354 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The devices operate at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 128 KB of embedded Flash memory for code/data storage and 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, ADC, CMP, I^2C, UART, SPI, MCTM, GPTM, SCTM, BFTM, CRC-16/32, RTC, WDT, PDMA, EBI, USB2.0 FS, SW-DP (Serial Wire Debug Port), etc., are also implemented in the devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application controllers, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor controllers and so on.

arm CORTEX

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- Up to 128 KB on-chip Flash memory for instruction/data and option byte storage
- 8 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the HT32F52344/52354 series devices, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power on Reset / Power down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated clock PLL and USB PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE, LSI, LSE or system PLL. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- Single V_{DD} power supply: 1.65 V to 3.6 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- Two power domains: V_{DD}, V_{CORE}
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel ADC is integrated in these devices. There are multiplexed channels, which include 12 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

The internal voltage reference (VREF) provides a stable reference voltage output for the ADC and Comparators. VREF is internally connected to the ADC_IN15 input channel. The precise voltage of VREF is individually measured for each part by Holtek in during production test.

Comparator – CMP

- Two Rail-to-rail comparators
- Each comparator has configurable negative input used for flexible voltage selection
  - Dedicated I/O pin
  - Internal voltage reference provided by 8-bit scaler
- Programmable hysteresis
- Programmable speed and consumption
- Comparator output can be routed to I/O or to multiple timer or ADC trigger inputs
- 8-bit Scaler can be configurable to dedicated I/O for voltage reference
- Comparator has interrupt generation capability with wakeup from Sleep or Deep Sleep modes through the EXTI controller

The two general purpose comparators (CMP) are implemented within the devices. They can be configured either as standalone comparators or combined with the different kinds of peripheral IP. Each comparator is capable of asserting interrupts to the NVIC or waking up the CPU from Deep Sleep mode through EXTI wakeup event management unit.

I/O Ports – GPIO

- Up to 54 GPIOs
- Port A, B, C, D are mapped to 16-line EXTI interrupts
- Almost all I/O pins have configurable output driving current

There are up to 54 General Purpose I/O pins, GPIO, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15 and PD0 ~ PD5 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR), one 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse width of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and break input.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single-Channel Timer – SCTM

- 16-bit up and auto-reload counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM output.

Basic Function Timer – BFTM

- 32-bit compare match count-up counter – no I/O control features
- One shot mode – stops counting when compare match occurs
- Repetitive mode – restarts counter when compare match occurs

The Basic Function Timer is a simple 32-bit up-counting counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive and one shot modes. In the repetitive mode, the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real-Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} power domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated by the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume or interrupt signal from the MCU power saving modes.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with address mask function

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides a SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16}+X^{15}+X^{2}+1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16}+X^{12}+X^{5}+1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source:

  ADC, SPI, UART, I²C, MCTM, GPTM and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Operation in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and needs a software triggered start signal by controlling the "START" bit in the control register. The divider calculation complete flag will be set to 1 after 8 clock cycles, however, if the divisor register data is zero during the calculation, the division by zero error flag will be set to 1.

External Bus Interface – EBI

- Programmable interface for various memory types
- Translate the AHB transactions into the appropriate external device protocol
- Individual chip select signal for each memory bank
- Programmable timing to support a wide range of devices
- Automatic translation when AHB transaction width and external memory interface width are different
- Write buffer to decrease stalling of the AHB write burst transaction
- Multiplexed and non-multiplexed address and data line configurations
  - Up to 21 address lines
  - Up to 16-bit data bus width

The external bus interface is able to access external parallel interface devices such as SRAM, Flash and LCD modules. The interface is memory mapped into the CPU internal address map. The data and address lines are multiplexed in order to reduce the number of pins required to connect to the external devices. The read/write timing of the bus can be adjusted to meet the timing specification of the external devices. Note the interface only supports asynchronous 8-bit or 16-bit bus interface.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 full-speed (12 Mbps) specification
- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 byte EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte EP_SRAM is used as the endpoint buffer. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize overall system complexity and cost. The USB also contains suspend and resume features to meet low-power consumption requirement.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 33-pin QFN and 48/64-pin LQFP packages
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F52344	HT32F52354
Main Flash (KB)		64	127
Option Bytes Flash (KB)		1	1
SRAM (KB)		8	8
Timers	MCTM	1	
	GPTM	1	
	SCTM	2	
	BFTM	2	
	WDT	1	
	RTC	1	
Communication	USB	1	
	SPI	2	
	UART	2	
	I^2C	1	
PDMA		6 channels	
Hardware Divider		1	
EBI		1	
CRC-16/32		1	
EXTI		16	
12-bit ADC		1	
Number of channels		12 external channels	
Comparator		2	
GPIO		Up to 54	
CPU frequency		Up to 60 MHz	
Operating voltage		1.65 V ~ 3.6 V	
Operating temperature		-40 °C ~ 85 °C	
Package		33-pin QFN and 48/64-pin LQFP	

Block Diagram

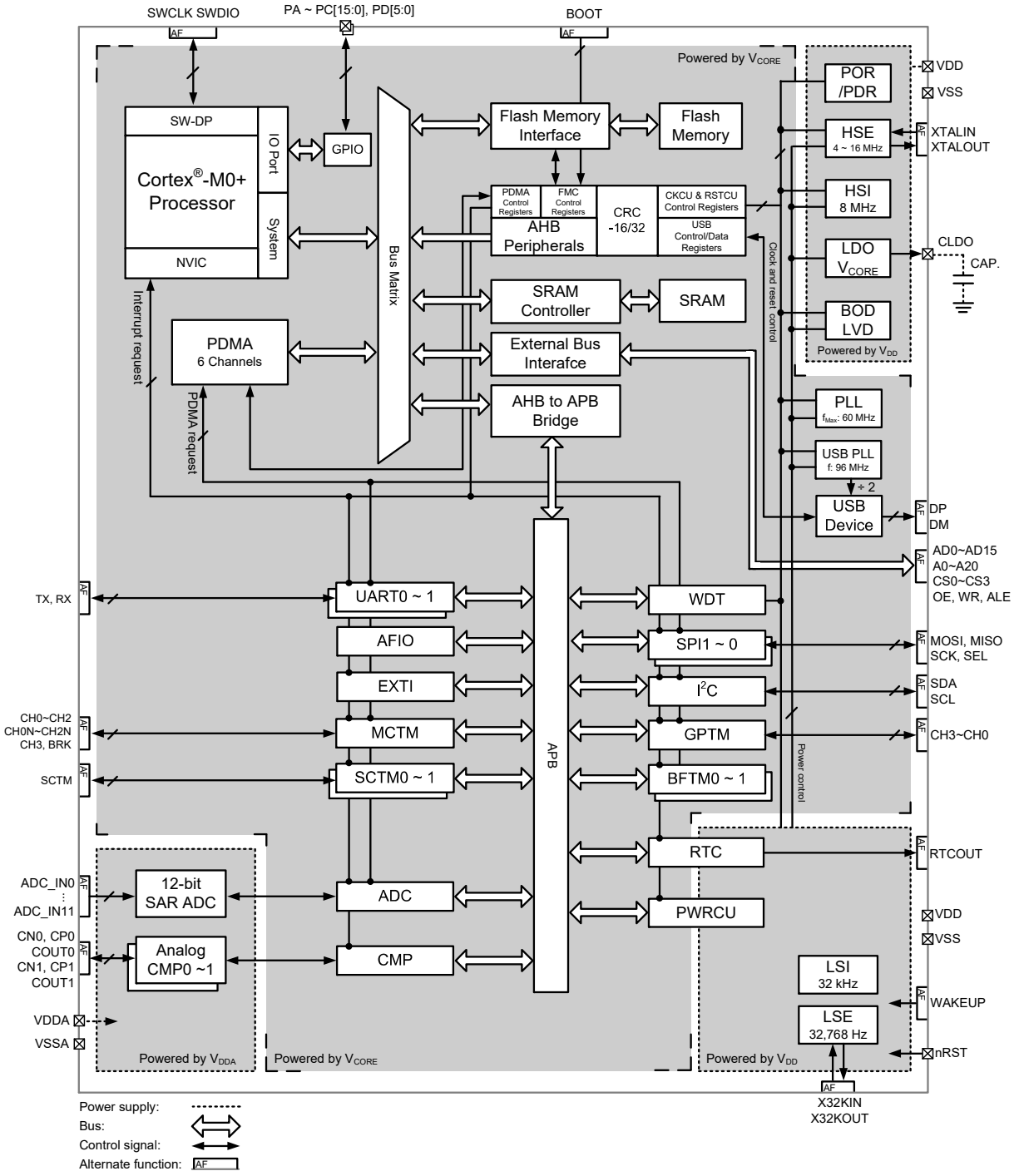


Figure 1. Block Diagram

Memory Map

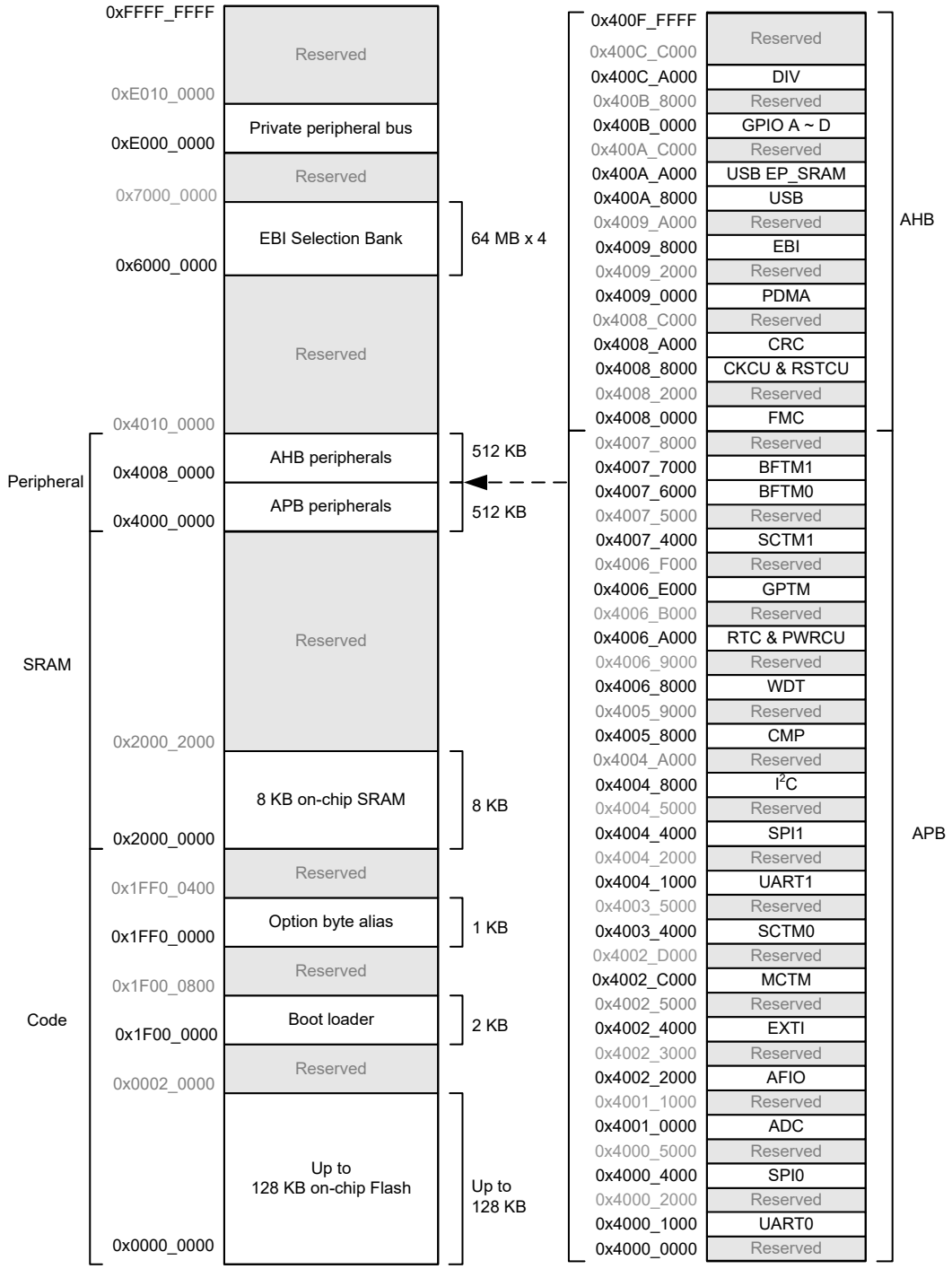


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	Reserved	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	CMP	
0x4005_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA Control Registers	
0x4009_2000	0x4009_7FFF	Reserved	
0x4009_8000	0x4009_9FFF	EBI Control Registers	
0x4009_A000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_9FFF	USB Control Register	
0x400A_A000	0x400A_BFFF	USB EP_SRAM	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400B_7FFF	GPIO D	
0x400B_8000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure

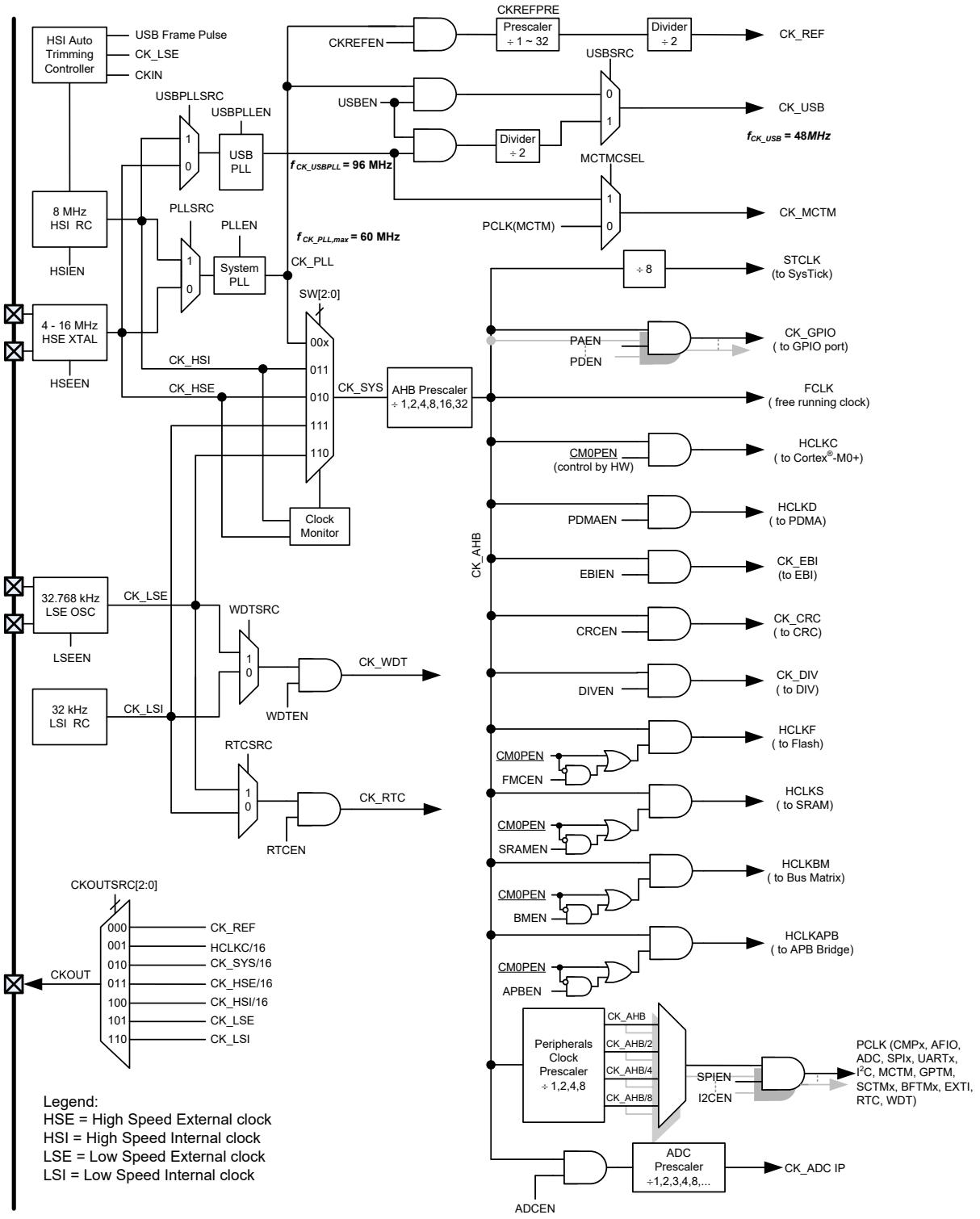


Figure 3. Clock Structure

4 Pin Assignment

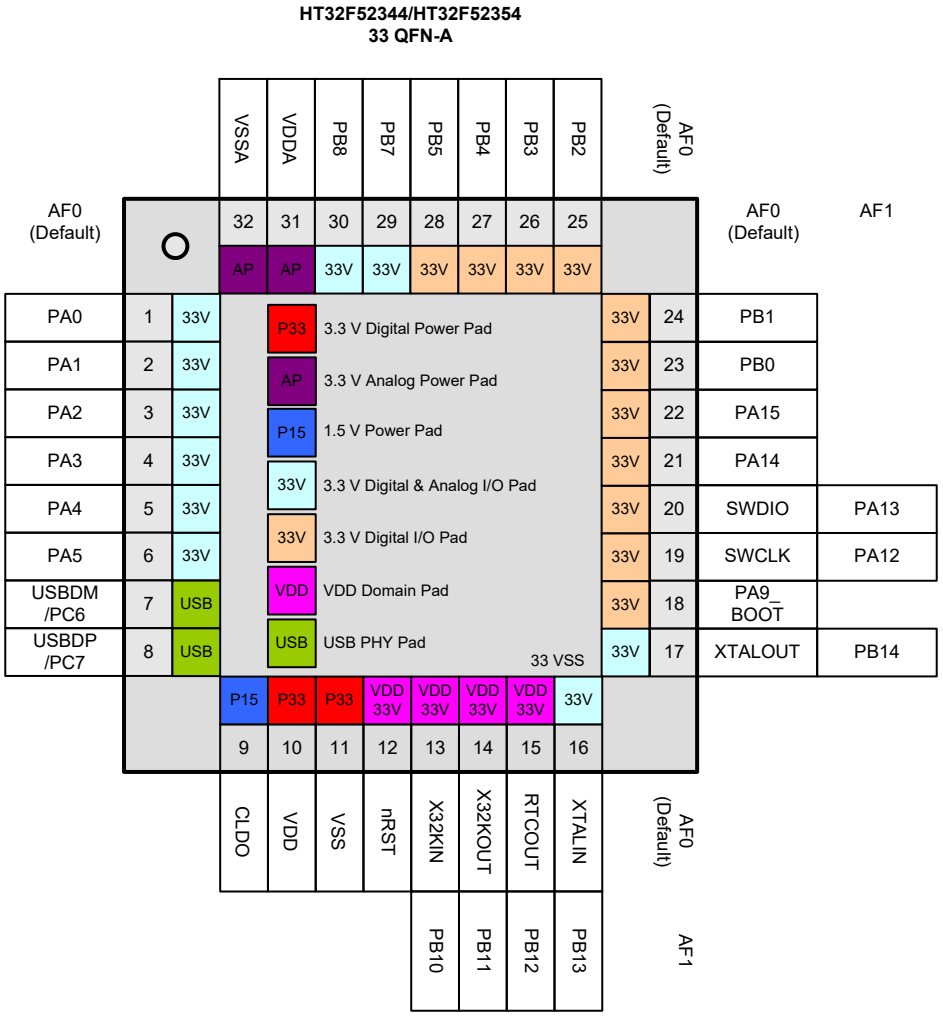


Figure 4. 33-pin QFN Pin Assignment

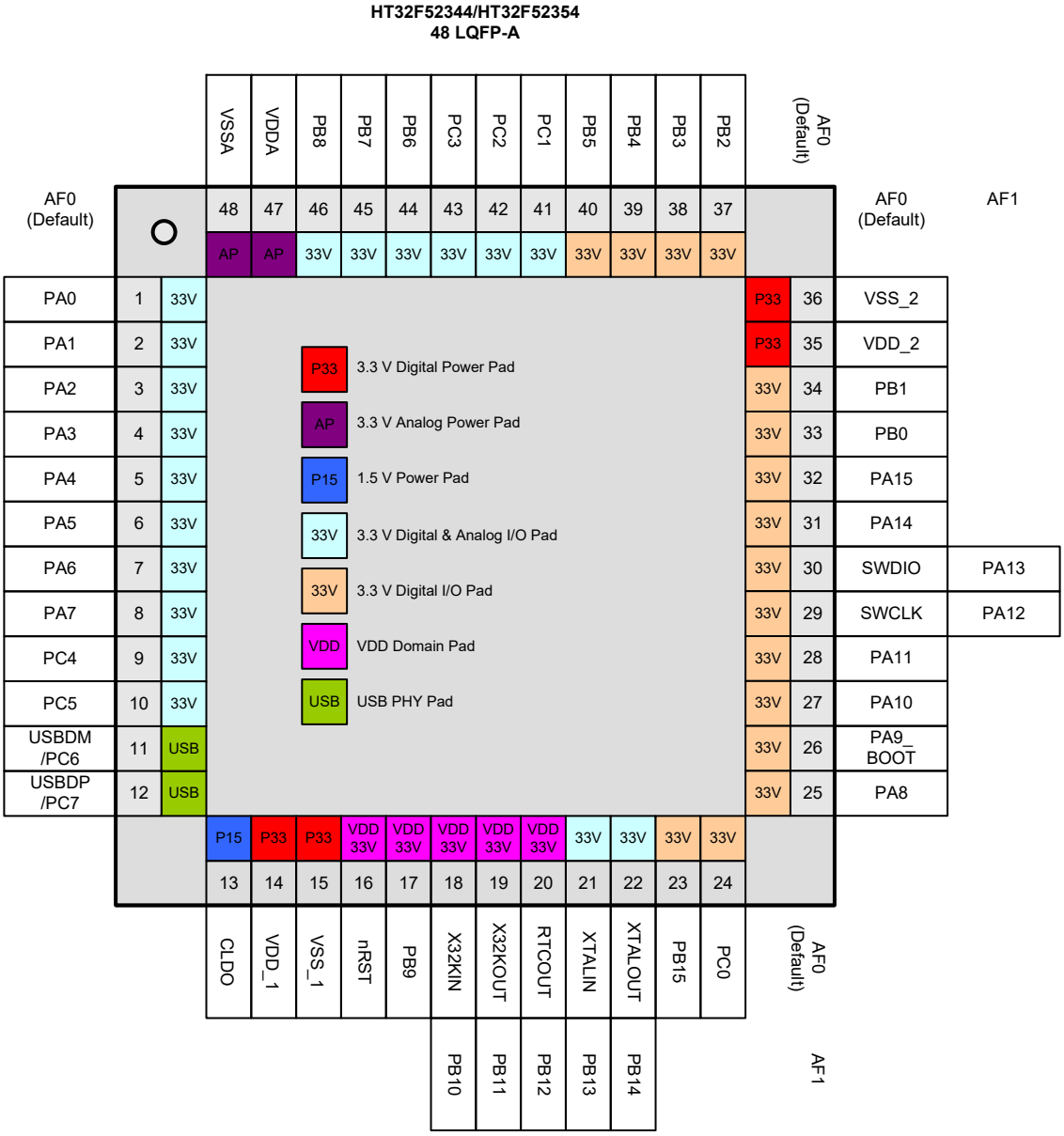


Figure 5. 48-pin LQFP Pin Assignment

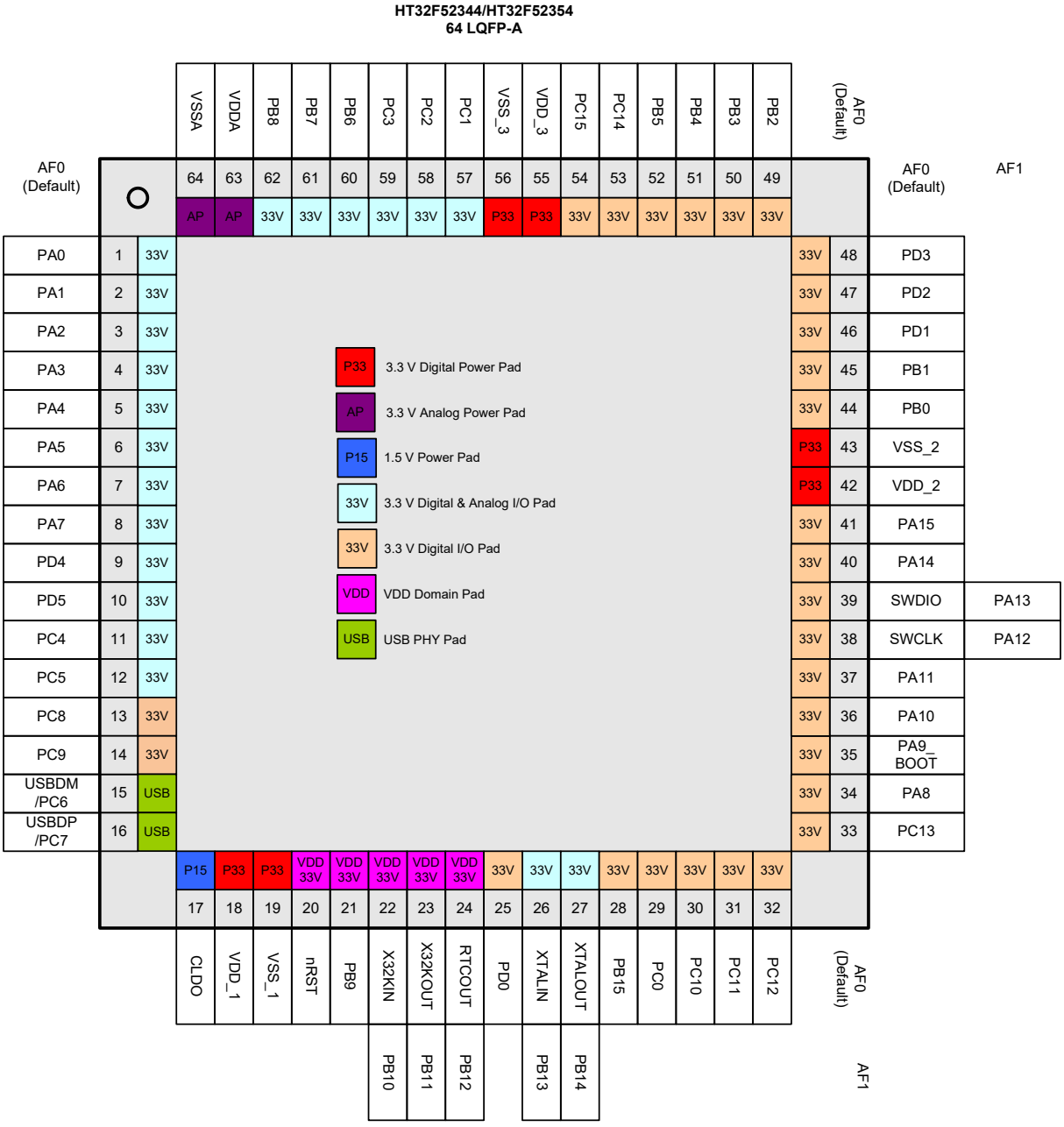


Figure 6. 64-pin LQFP Pin Assignment

Table 3. Pin Assignment

Packages			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	33 QFN	System Default	GPIO	ADC	CMP	GPTM /MCTM	SPI	UART	I²C	N/A	EBI	N/A	N/A	N/A	SCTM	N/A	System Other
1	1	1	PA0		ADC_IN0		GT_CH0	SPI1_SCK	UR1_TX	I2C_SCL								VREF
2	2	2	PA1		ADC_IN1		GT_CH1	SPI1_MOSI	UR1_RX	I2C_SDA								
3	3	3	PA2		ADC_IN2		GT_CH2	SPI1_MISO	UR0_TX									
4	4	4	PA3		ADC_IN3		GT_CH3	SPI1_SEL	UR0_RX									
5	5	5	PA4		ADC_IN4		GT_CH0	SPI0_SCK	UR1_TX	I2C_SCL								
6	6	6	PA5		ADC_IN5		GT_CH1	SPI0_MOSI	UR1_RX	I2C_SDA								
7	7		PA6		ADC_IN6		GT_CH2	SPI0_MISO										
8	8		PA7		ADC_IN7		GT_CH3	SPI0_SEL										
9			PD4		ADC_IN8				UR1_TX							SCTM0		
10			PD5		ADC_IN9				UR1_RX							SCTM1		
11	9		PC4		ADC_IN10		GT_CH0	SPI1_SEL	UR0_TX	I2C_SCL		EBI_A19				SCTM0		
12	10		PC5		ADC_IN11		GT_CH1	SPI1_SCK	UR0_RX	I2C_SDA		EBI_A20				SCTM1		
13			PC8				GT_CH2	SPI1_MOSI				EBI_A0						
14			PC9				GT_CH3	SPI1_MISO				EBI_A1						
15	11	7	PC6				MT_CH2		UR0_TX	I2C_SCL								
15	11	7	USBDM															
16	12	8	USBDP															
16	12	8	PC7				MT_CH2N		UR0_RX	I2C_SDA								
17	13	9	CLDO															
18	14	10	VDD_1															
19	15	11	VSS_1															
20	16	12	nRST															
21	17		PB9				MT_CH3											
22	18	13	X32KIN	PB10			GT_CH0	SPI1_SEL	UR1_TX							SCTM0		
23	19	14	X32KOUT	PB11			GT_CH1	SPI1_SCK	UR1_RX							SCTM1		
24	20	15	RTCOUT	PB12				SPI0_MISO	UR0_RX							SCTM0		WAKEUP
25			PD0									EBI_A18						
26	21	16	XTALIN	PB13					UR0_TX	I2C_SCL								
27	22	17	XTALOUT	PB14					UR0_RX	I2C_SDA								
28	23		PB15				MT_CH0	SPI0_SEL		I2C_SCL		EBI_A16						
29	24		PC0				MT_CH0N	SPI0_SCK		I2C_SDA		EBI_A17				SCTM1		
30			PC10				GT_CH0	SPI1_SEL				EBI_AD13						
31			PC11				GT_CH1	SPI1_SCK				EBI_AD14						
32			PC12				GT_CH2	SPI1_MOSI	UR1_TX	I2C_SCL		EBI_AD15						
33			PC13				GT_CH3	SPI1_MISO	UR1_RX	I2C_SDA		EBI_CS3						

Packages			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	33 QFN	System Default	GPIO	ADC	CMP	GPTM /MCTM	SPI	UART	I²C	N/A	EBI	N/A	N/A	N/A	SCTM	N/A	System Other
34	25		PA8						UR1_TX							SCTM0		
35	26	18	PA9_BOOT					SPI0_MOSI				EBI_A1				SCTM1		CKOUT
36	27		PA10				MT_CH1	SPI0_MOSI	UR1_RX									
37	28		PA11				MT_CH1N	SPI0_MISO				EBI_A0				SCTM0		
38	29	19	SWCLK	PA12														
39	30	20	SWDIO	PA13														
40	31	21	PA14				MT_CH0	SPI1_SEL		I2C_SCL		EBI_AD0						
41	32	22	PA15				MT_CH0N	SPI1_SCK		I2C_SDA		EBI_AD1				SCTM1		
42			VDD_2															
43			VSS_2															
44	33	23	PB0				MT_CH1	SPI1_MOSI	UR0_TX	I2C_SCL		EBI_AD2						
45	34	24	PB1				MT_CH1N	SPI1_MISO	UR0_RX	I2C_SDA		EBI_AD3				SCTM0		
46			PD1				MT_CH2					EBI_AD10						
47			PD2				MT_CH2N					EBI_AD11						
48			PD3				MT_CH3					EBI_AD12						
	35		VDD_2															
	36	33	VSS_2															
49	37	25	PB2				MT_CH2	SPI0_SEL	UR1_TX			EBI_AD4						CKIN
50	38	26	PB3				MT_CH2N	SPI0_SCK	UR1_RX			EBI_AD5				SCTM1		
51	39	27	PB4				MT_BRK	SPI0_MOSI	UR1_TX			EBI_AD6				SCTM0		
52	40	28	PB5				GT_CH2	SPI0_MISO	UR1_RX			EBI_AD7						
53			PC14				MT_CH3			I2C_SCL		EBI_AD8						
54			PC15							I2C_SDA		EBI_AD9				SCTM1		
55			VDD_3															
56			VSS_3															
57	41		PC1			CN0	MT_CH0	SPI1_SEL	UR1_TX			EBI_OE						
58	42		PC2			CP0	MT_CH0N	SPI1_SCK				EBI_CS0						
59	43		PC3			COUT0	MT_BRK	SPI1_MOSI	UR1_RX			EBI_WE						
60	44		PB6			CN1	GT_CH3	SPI1_MISO	UR0_TX			EBI_ALE						
61	45	29	PB7			CP1	MT_CH1	SPI0_MISO	UR0_TX	I2C_SCL		EBI_CS1						
62	46	30	PB8			COUT1	MT_CH1N	SPI0_SEL	UR0_RX	I2C_SDA		EBI_CS2						
63	47	31	VDDA															
64	48	32	VSSA															

Note: The pin number 33 of the 33QFN package is located at the exposed pad of the QFN package.

Table 4. Pin Description

Pin Number			Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64 LQFP	48 LQFP	33 QFN					Default Function (AF0)
1	1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2
4	4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3
5	5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4
6	6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5
7	7		PA6	AI/O	33V	4/8/12/16 mA	PA6
8	8		PA7	AI/O	33V	4/8/12/16 mA	PA7
9			PD4	AI/O	33V	4/8/12/16 mA	PD4
10			PD5	AI/O	33V	4/8/12/16 mA	PD5
11	9		PC4	AI/O	33V	4/8/12/16 mA	PC4
12	10		PC5	AI/O	33V	4/8/12/16 mA	PC5
13			PC8	I/O	33V	4/8/12/16 mA	PC8
14			PC9	I/O	33V	4/8/12/16 mA	PC9
15	11	7	PC6	I/O	33V	4/8/12/16 mA	PC6
15	11	7	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard
16	12	8	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard
16	12	8	PC7	I/O	33V	4/8/12/16 mA	PC7
17	13	9	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connected with an external capacitor as close as possible between this pin and VSS_1
18	14	10	VDD_1	P	—	—	Voltage for digital I/O
19	15	11	VSS_1	P	—	—	Ground reference for digital I/O
20	16	12	nRST(3)	I	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
21	17		PB9(3)	I/O (V_{DD})	33V	4/8/12/16 mA	PB9
22	18	13	PB10(3)	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KIN
23	19	14	PB11(3)	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KOUT
24	20	15	PB12(3)	I/O (V_{DD})	33V	4/8/12/16 mA	RTCOUT
25			PD0	I/O	33V	4/8/12/16 mA	PD0
26	21	16	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
27	22	17	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
28	23		PB15	I/O	33V	4/8/12/16 mA	PB15
29	24		PC0	I/O	33V	4/8/12/16 mA	PC0
30			PC10	I/O	33V	4/8/12/16 mA	PC10
31			PC11	I/O	33V	4/8/12/16 mA	PC11
32			PC12	I/O	33V	4/8/12/16 mA	PC12
33			PC13	I/O	33V	4/8/12/16 mA	PC13
34	25		PA8	I/O	33V	4/8/12/16 mA	PA8
35	26	18	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
36	27		PA10	I/O	33V	4/8/12/16 mA	PA10
37	28		PA11	I/O	33V	4/8/12/16 mA	PA11
38	29	19	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
39	30	20	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
40	31	21	PA14	I/O	33V	4/8/12/16 mA	PA14
41	32	22	PA15	I/O	33V	4/8/12/16 mA	PA15
42	35		VDD_2	P	—	—	Voltage for digital I/O
43	36	33	VSS_2	P	—	—	Ground reference for digital I/O

Pin Number			Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64 LQFP	48 LQFP	33 QFN					Default Function (AF0)
44	33	23	PB0	I/O	33V	4/8/12/16 mA	PB0
45	34	24	PB1	I/O	33V	4/8/12/16 mA	PB1
46			PD1	I/O	33V	4/8/12/16 mA	PD1
47			PD2	I/O	33V	4/8/12/16 mA	PD2
48			PD3	I/O	33V	4/8/12/16 mA	PD3
49	37	25	PB2	I/O	33V	4/8/12/16 mA	PB2
50	38	26	PB3	I/O	33V	4/8/12/16 mA	PB3
51	39	27	PB4	I/O	33V	4/8/12/16 mA	PB4
52	40	28	PB5	I/O	33V	4/8/12/16 mA	PB5
53			PC14	I/O	33V	4/8/12/16 mA	PC14
54			PC15	I/O	33V	4/8/12/16 mA	PC15
55			VDD_3	P	—	—	Voltage for digital I/O
56			VSS_3	P	—	—	Ground reference for digital I/O
57	41		PC1	AI/O	33V	4/8/12/16 mA	PC1
58	42		PC2	AI/O	33V	4/8/12/16 mA	PC2
59	43		PC3	AI/O	33V	4/8/12/16 mA	PC3
60	44		PB6	AI/O	33V	4/8/12/16 mA	PB6
61	45	29	PB7	AI/O	33V	4/8/12/16 mA	PB7
62	46	30	PB8	AI/O	33V	4/8/12/16 mA	PB8
63	47	31	VDDA	P	—	—	Analog voltage for ADC and Comparator
64	48	32	VSSA	P	—	—	Ground reference for ADC and Comparator

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 33V = 3.3 V tolerant, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, only the USB interface can be used for communication.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	+85	°C
T_{STG}	Storage Temperature Range	-60	+150	°C
T_J	Maximum Junction Temperature	—	+125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	1.65	3.3	3.6	V
V_{DDA}	Analog Operating Voltage	—	2.5	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{LDO} = 10 mA and voltage variant = ±5 %, After trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0 ~ 3.6 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
		V_{DD} = 1.65 ~ 2.0 V Regulator input @ V_{LDO} = 1.5 V	—	20	25	
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

The current consumption is influenced by several parameters and factors, including the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is configured under the following conditions for current consumption measured:

- All I/O pins are set to a high-impedance (floating) state.
- All peripherals are disabled unless specifically stated otherwise.
- The Flash memory access time is optimized using the minimum wait states number, depending on the f_{HCLK} frequency.
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$.

Table 8. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Run Mode)	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, all peripherals enabled	—	16.7	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, all peripherals disabled	—	7.9	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, all peripherals enabled	—	13.7	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, all peripherals disabled	—	7.7	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, all peripherals enabled	—	6.7	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, all peripherals disabled	—	3.4	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, all peripherals enabled	—	2.7	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, all peripherals disabled	—	1.48	—	mA
		V_{DD} = 3.3 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, all peripherals enabled	—	25	—	µA
		V_{DD} = 3.3 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, all peripherals disabled	—	20	—	µA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Sleep Mode)	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, all peripherals enabled	—	11	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, all peripherals disabled	—	1.3	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, all peripherals enabled	—	7.5	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, all peripherals disabled	—	1.1	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, all peripherals enabled	—	4.4	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, all peripherals disabled	—	0.85	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, all peripherals enabled	—	1.7	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, all peripherals disabled	—	0.45	—	mA
	Supply Current (Deep-Sleep1 Mode)	V_{DD} = 3.3 V, all clock off (HSE/HSI/LSE), LDO in low power mode, LSI on, RTC on	—	15.5	—	μA
	Supply Current (Deep-Sleep2 Mode)	V_{DD} = 3.3 V, all clock off (HSE/HSI/LSE), LDO off, DMOS on, LSI on, RTC on	—	3.7	—	μA
	Supply Current (Power-Down Mode)	V_{DD} = 3.3 V, LDO off, DMOS off, LSE on, RTC on, LSI on	—	2.7	—	μA
		V_{DD} = 3.3 V, LDO off, DMOS off, LSE off, RTC off, LSI on	—	1.3	—	

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 9. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	0.6	—	3.6	V
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.40	1.55	1.65	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.27	1.45	1.57	V
$V_{PORHYST}$	POR Hysteresis	—	—	100	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 10. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed	V_{DD} Falling edge	1.62	1.68	1.74	V
			V_{DD} Rising edge	1.68	1.74	1.8	
$V_{BODHTST}$	BOD Hysteresis	V_{DD} = 2.0 V	—	—	60	—	mV
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	1.67	1.75	1.83	V
			LVDS = 001	1.87	1.95	2.03	V
			LVDS = 010	2.07	2.15	2.23	V
			LVDS = 011	2.27	2.35	2.43	V
			LVDS = 100	2.47	2.55	2.63	V
			LVDS = 101	2.67	2.75	2.83	V
			LVDS = 110	2.87	2.95	3.03	V
			LVDS = 111	3.07	3.15	3.23	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	200	—	μs
I_{DDLVD}	Operation Current (2)	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register

External Clock Characteristics

Table 11. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	1.65	—	3.6	V
f_{HSE}	HSE Frequency	—	4	—	16	MHz
C_{LHSE}	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 0	—	—	160	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3 V	—	—	4	ms

Table 12. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	1.65	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 1.65 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{DD} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L \geq$ 7 pF, V_{DD} = 1.65 V ~ 2.7 V, T_A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L <$ 7 pF, V_{DD} = 1.65 V ~ 3.6 V, T_A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 1.65 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 13. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	1.65	—	3.6	V
f_{HSI}	HSI Frequency	V_{DD} = 3.3 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 3.6 V T_A = -40 °C ~ 85 °C	-3	—	3	%
		V_{DD} = 1.65 V ~ 3.6 V T_A = -40 °C ~ 85 °C	-6	—	6	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	μA
	Power Down Current		—	—	0.05	μA
t_{SUHSI}	HSI Oscillator Startup Time	f_{HSI} = 8 MHz	—	—	10	μs

Table 14. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	1.65	—	3.6	V
f_{LSI}	LSI Frequency	V_{DD} = 3.3 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V, T_A = 25 °C	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V, T_A = 25 °C	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V, T_A = 25 °C	—	—	100	μs

System PLL Characteristics

Table 15. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	60	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	μs

USB PLL Characteristics

Table 16. USB PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	USB PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	USB PLL Output Clock	—	64	—	96	MHz
t_{LOCK}	USB PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 17. Flash Memory Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program/Erase Cycles before failure (Endurance)	T_A = -40 °C ~ 85 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 18. I/O Port Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V I/O	$V_I = V_{SS}$, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin		—	—	3	
I_{IH}	High Level Input Current	3.3 V I/O	$V_I = V_{DD}$, On-chip pull-down resister disabled	—	—	3	μA
		Reset pin		—	—	3	
V_{IL}	Low Level Input Voltage	3.3 V I/O		-0.4	—	V_{DD} × 0.35	V
		Reset pin		-0.4	—	V_{DD} × 0.35	
V_{IH}	High Level Input Voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.4	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.4	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V_{OL} = 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OL} = 0.4 V		8	—	—	mA
		3.3 V I/O 12 mA drive, V_{OL} = 0.4 V		12	—	—	mA
		3.3 V I/O 16 mA drive, V_{OL} = 0.4 V		16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		8	—	—	mA
		3.3 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		12	—	—	mA
		3.3 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		16	—	—	mA
V_{OL}	Low Level Output Voltage	3.3 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.4	V
		3.3 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.4	
		3.3 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.4	
		3.3 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.4	
V_{OH}	High Level Output Voltage	3.3 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.4	—	—	
		3.3 V 12 mA drive I/O, I_{OH} = 12 mA		V_{DD} - 0.4	—	—	
		3.3 V 16 mA drive I/O, I_{OH} = 16 mA		V_{DD} - 0.4	—	—	
R_{PU}	Internal Pull-up Resistor	3.3 V I/O, V_{DD} = 3.3 V		—	60	—	kΩ
R_{PD}	Internal Pull-down Resistor	3.3 V I/O, V_{DD} = 3.3 V		—	60	—	kΩ

ADC Characteristics

Table 19. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	A/D Converter Operating Voltage	—	2.5	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V	—	1	TBD	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	Msps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.

3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

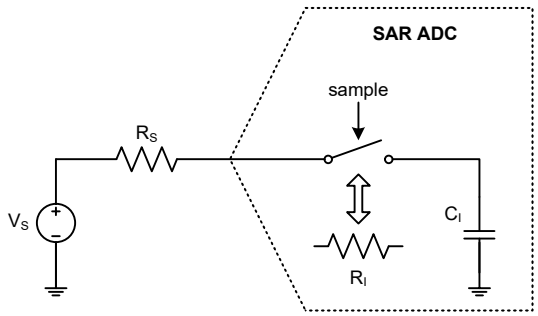


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below 1/4 LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Internal Reference Voltage Characteristics

Table 20. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		1.65	—	3.6	V
V_{REF}	Internal Reference Voltage after Factory Trimming at 25 °C Temperature	V_{DDA} ≥ 1.65 V	1.215 V VREFSEL [1:0] = 00	1.19	1.215	1.24	V
		V_{DDA} ≥ 2.3 V	2.0 V VREFSEL [1:0] = 01	1.96	2.0	2.04	
		V_{DDA} ≥ 2.8 V	2.5 V VREFSEL [1:0] = 10	2.45	2.5	2.55	
		V_{DDA} ≥ 3.0 V	2.7 V VREFSEL [1:0] = 11	2.65	2.7	2.75	
V_{REFACC}	Reference Voltage Accuracy after Trimming	V_{DDA} = 1.65 V ~ 3.6 V, V_{REF} = 1.215 V, T_A = -40 °C ~ 85 °C		-3.0	—	+3.0	%
t_{STABLE}	Stable Time	—		—	—	100	ms
t_{SREFV}	ADC Sampling Time when Reading Reference Voltage	—		10	—	—	μs
I_{DD}	Operating Current	—		—	30	50	μA
I_{DDPWD}	Power Down Current	—		—	—	0.01	μA

Comparator Characteristics

Table 21. Comparator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating Voltage	Comparator mode		2.0	3.3	3.6	V
V_{IN}	Input Common Mode Voltage Range	CP or CN		V_{SSA}	—	V_{DDA}	V
V_{IOS}	Input Offset Voltage (1)	T_A = 25 °C		-15	—	15	mV
V_{HYS}	Input Hysteresis V_{DDA} = 3.3 V	No hysteresis, CMPHM [1:0] = 00		—	0	—	mV
		Low hysteresis, CMPHM [1:0] = 01		—	30	—	mV
		Middle hysteresis, CMPHM [1:0] = 10		—	70	—	mV
		High hysteresis, CMPHM [1:0] = 11		—	100	—	mV
t_{RT}	Response Time Input Overdrive = ±100 mV	High Speed Mode	V_{DDA} ≥ 2.7 V	—	50	100	ns
			V_{DDA} < 2.7 V	—	100	250	
		Low Speed Mode		—	2	5	μs
I_{CMP}	Current Consumption V_{DDA} = 3.3 V	High Speed Mode		—	180	—	μA
		Low Speed Mode		—	30	—	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CMPST}	Comparator Startup Time	Comparator enabled to output valid	—	—	50	μs
I_{CMP_DN}	Power Down Supply Current	CMPEN = 0, CVREN = 0, CVROE = 0	—	—	0.1	μA
Comparator Voltage Reference (CVR)						
V_{CVR}	Output Range	—	V_{SSA}	—	V_{DDA}	V
N_{Bits}	CVR Scaler Resolution	—	—	8	—	bits
t_{CVRST}	Setting Time	CVR Scaler Setting Time from CVREF = “00000000” to “11111111”	—	—	100	μs
I_{CVR}	Current Consumption V_{DDA} = 3.3 V	CVREN=1, CMPREFOE=0	—	65	—	μA
		CVREN=1, CVROE=1	—	80	110	μA

Note: Data based on characterization results only, not tested in production.

MCTM/GPTM/SCTM Characteristics

Table 22. MCTM/GPTM/SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for MCTM, GPTM and PWM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	f_{TM}
f_{EXT}	External Single Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 23. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	us
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.

2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 0 and SEQ_FILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 1 and SEQ_FILTER = 00.

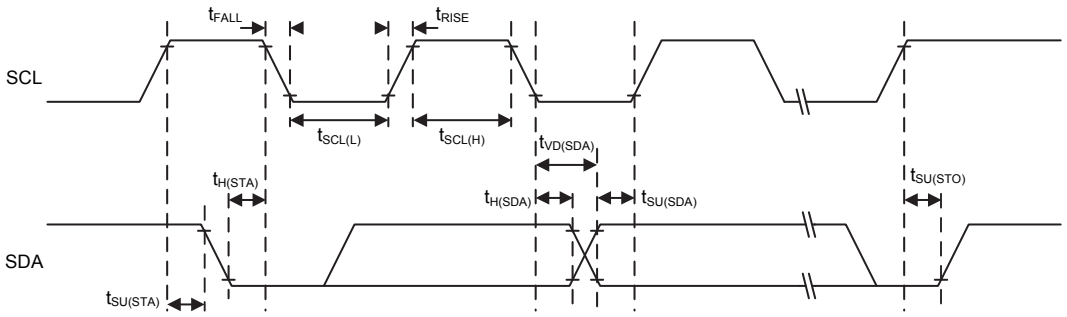


Figure 8. I²C Timing Diagram

SPI Characteristics

Table 24. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

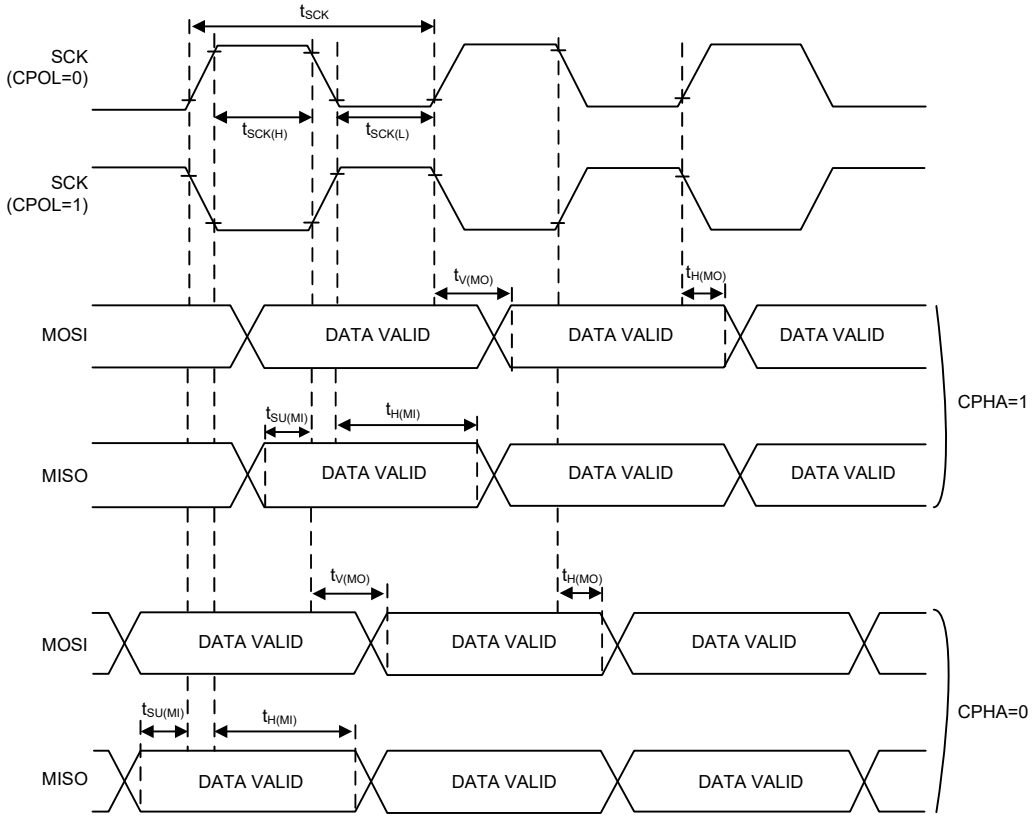


Figure 9. SPI Timing Diagram – SPI Master Mode

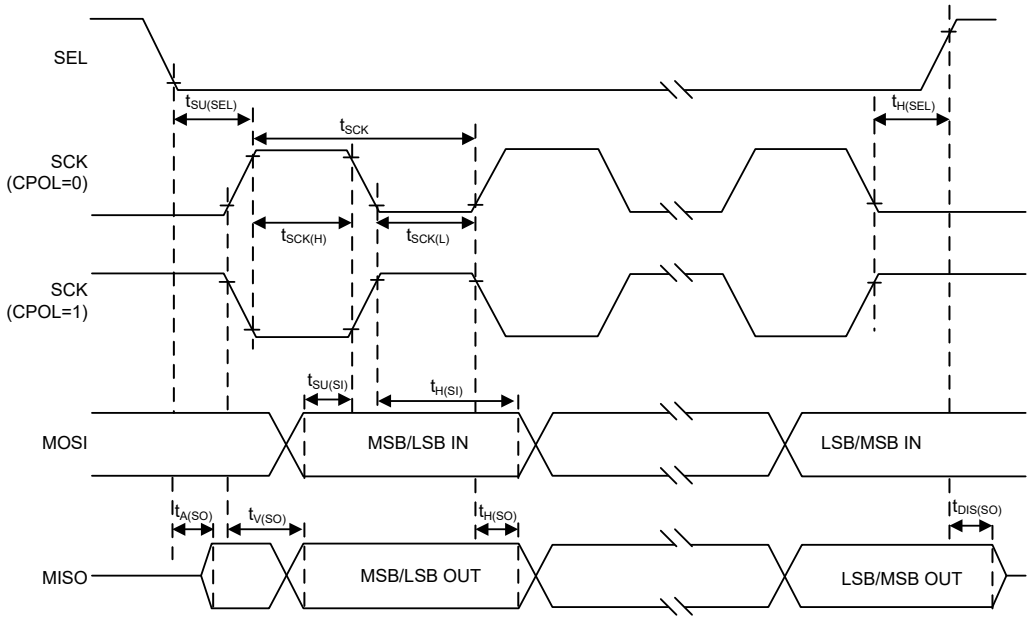


Figure 10. SPI Timing Diagram – SPI Slave Mode with CPHA=1

USB Characteristics

The USB interface is USB-IF certified - Full Speed.

Table 25. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	USB Operating Voltage	—	3.0	—	3.6	V
V_{DI}	Differential Input Sensitivity	|USBDP – USBDM|	0.2	—	—	V
V_{CM}	Common Mode Voltage Range	—	0.8	—	2.5	V
V_{SE}	Single-ended Receiver Threshold	—	0.8	—	2.0	V
V_{OL}	Pad Output Low Voltage	1.5 kΩ R_L to V_{DD}	0	—	0.3	V
V_{OH}	Pad Output High Voltage		2.8	—	3.6	V
V_{CRS}	Differential Output Signal Cross-point Voltage		1.3	—	2.0	V
Z_{DRV}	Driver Output Resistance	—	—	10	—	Ω
C_{IN}	Transceiver Pad Capacitance	—	—	—	20	pF

Note: 1. Data based on characterization results only, not tested in production.

2. The USB functionality is ensured down to 2.7 V but not for the full USB electrical characteristics which will experience degradation in the V_{DD} voltage range of 2.7 to 3.0 V.

3. R_L is the resistor load connected to the USB driver USBDP.

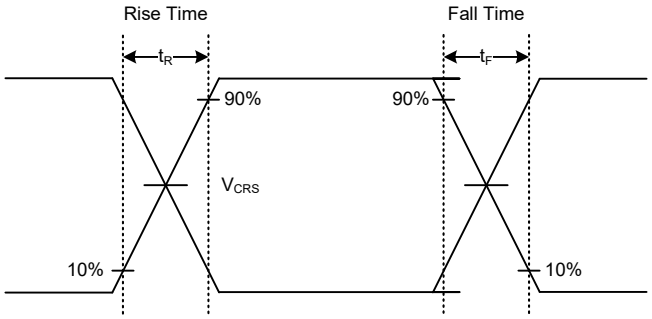


Figure 11. USB Signal Rise Time and Fall Time and Cross-Point Voltage (V_{CRS}) Definition

Table 26. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_R	Rise Time	C_L = 50 pF	4	—	20	ns
t_F	Fall Time	C_L = 50 pF	4	—	20	ns
$t_{R/F}$	Rise Time / Fall Time Matching	$t_{R/F} = t_R / t_F$	90	—	110	%

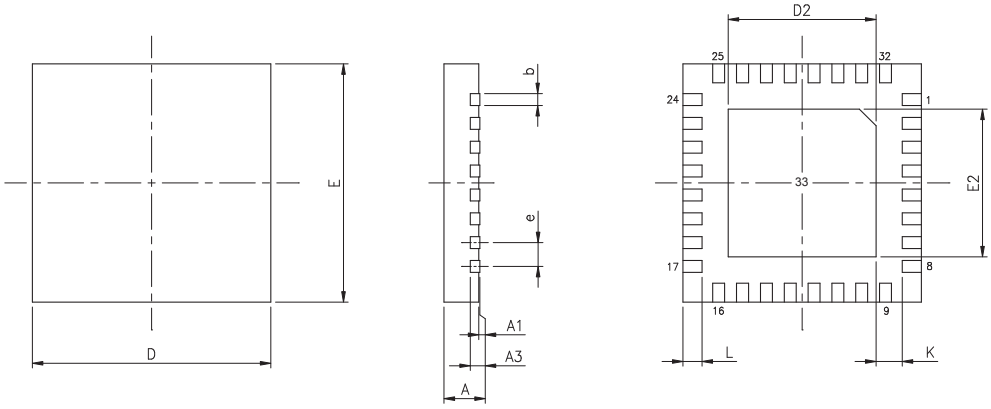
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

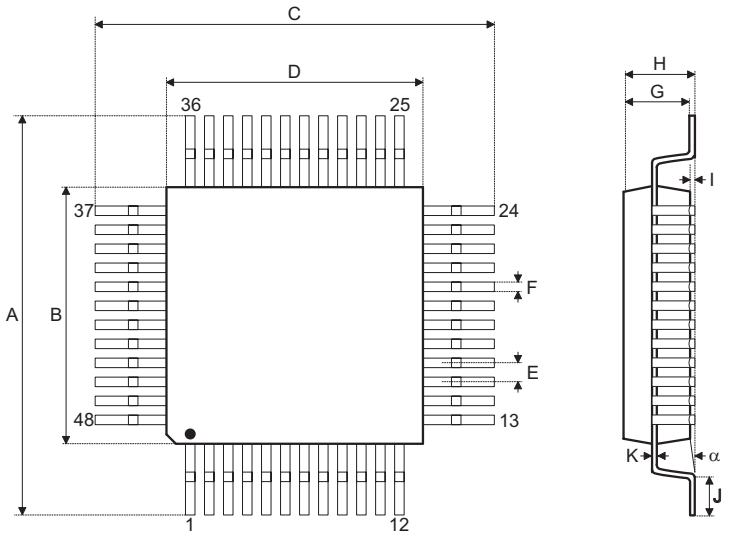
SAW Type 33-pin QFN (4mm×4mm×.075mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 BSC	
b	0.006	0.008	0.010
D		0.157 BSC	
E		0.157 BSC	
e		0.016 BSC	
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 BSC	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
K	0.20	—	—

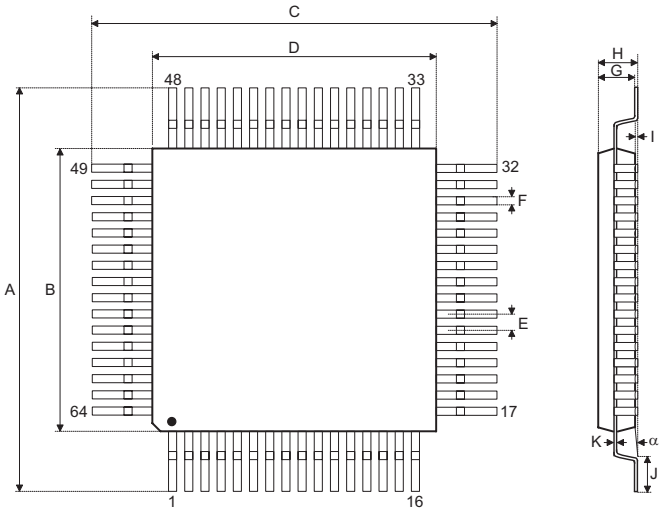
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.020 BSC	
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.50 BSC	
F	0.17	0.22	0.27
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.016 BSC	
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.40 BSC	
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°