HT32F61141
Datasheet

32-Bit Arm® Cortex®-M0+ 5V USB Smart Card Reader Microcontroller, 64 KB Flash and 16 KB SRAM with USB, UART, SPI, I^2C, GPTM, SCTM, BFTM, SCI, CRC, UID, RTC and WDT

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1 General Description

The Holtek HT32F61141 device is high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 48 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 64 KB of embedded Flash memory for code/data storage and 16 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as I^2C, UART, SPI, SCI, GPTM, SCTM, BFTM, CRC-16/32, 96-bit Unique ID, RTC, WDT, USB2.0 and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as Smart Card Reader, STB, POS and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 48 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- 64 KB on-chip Flash memory for instruction/data and option byte storage
- 16 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the HT32F61141 device, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power on Reset / Power down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 5 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillators and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M0+ are derived from the system clock (CK_SYS) which can source from the HSI, HSE, LSI, LSE or system PLL. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Control Unit – PWRCU

- Flexible power supply: V_{DD} power supply (2.5 V ~ 5.5 V), V_{DDIO} for I/Os (1.8 V ~ 5.5 V)
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- V_{REG} Power supply for USB
- V_{REGCRD} power supply for SCI0
- V_{DDIO} power supply for SCI1
- Five power domains: V_{DD}, V_{DDIO}, V_{REG}, V_{REGCRD} and V_{CORE}
- Three power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger sources and types
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line

- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

I/O Ports – GPIO

- Up to 36 GPIOs
- Port A, B, C are mapped to 16-line EXTI interrupts
- Almost all I/O pins have configurable output driving current

There are up to 36 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output

- PWM waveform generation with Edge-aligned

The Single Channel Timer, SCTM, consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter Counter-Reload (CRR) and several control / status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM outputs.

Basic Function Timer – BFTM

- 32-bit compare match up-counter – no I/O control features
- One shot mode – stops counting when compare match occurs
- Repetitive mode – restarts counter when compare match occurs

The Basic Function Timer, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals, generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes which are repetitive and one shot modes. In the repetitive mode, the counter will be restarted at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit down-counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real-Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, circuitry includes an APB interface, a 24-bit up-counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} power domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated by the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off. The RTC counter is used as a wakeup timer to generate a system resume signal from the MCU power saving modes.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detection and clock synchronization function to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master who controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud rate clock frequency of up to (f_{PCLK}/16) MHz
- Capability of full duplex communication
- Fully programmable serial communication characteristics including
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Smart Card Interface – SCI

- Supports ISO 7816-3 standard (EMVCo Certification for SCI0)
- SCI0 supports 5.0 V, 3.0 V, 1.8 V smart card (Class A, B, C)
- SCI0 supports card power over current protection
- Supports VDDIO pin to provide the SCI1 power supply
- Supports of both T = 0 and T = 1 protocols
- Character mode
- Single transmit buffer and single receive buffer
- 11-bit ETU (elementary time unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and checking
- Automatic character retry on parity error detection in transmission and reception modes

The Smart Card Interface SCI is compatible with the ISO 7816-3 standard. The Smart Card interface includes functions for Card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform the required Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 Full-Speed (12 Mbps) specification
- Fully integrated USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 5 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 bytes EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and nine configurable endpoints. A 1024-byte EP_SRAM is used as the endpoint buffers. Each endpoint buffer size is programmable using corresponding registers, thus providing maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize overall system complexity and cost. The USB also contains suspend and resume features to meet low-power consumption requirement.

Unique Identifier – UID

- Total 96-bit UID is unique and not duplicate with other HT32 MCU devices
- It is unchangeable and determined by MCU manufacturer

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoints or code / literal patches
- 2 comparators for hardware watch points

Package and Operation Temperature

- 32-pin QFN and 48-pin LQFP packages
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F61141
Main Flash (KB)		63
Option Bytes Flash (KB)		1
SRAM (KB)		16
Timers	GPTM	1
	SCTM	2
	BFTM	2
	WDT	1
	RTC	1
Communication	USB	1
	SPI	1
	UART	2
	I^2C	1
	SCI	2
CRC-16/32		1
EXTI		16
GPIO		Up to 36
CPU frequency		Up to 48 MHz
Operating voltage		2.5 V ~ 5.5 V
Operating temperature		-40 °C ~ 85 °C
Package		32-pin QFN and 48-pin LQFP

Block Diagram

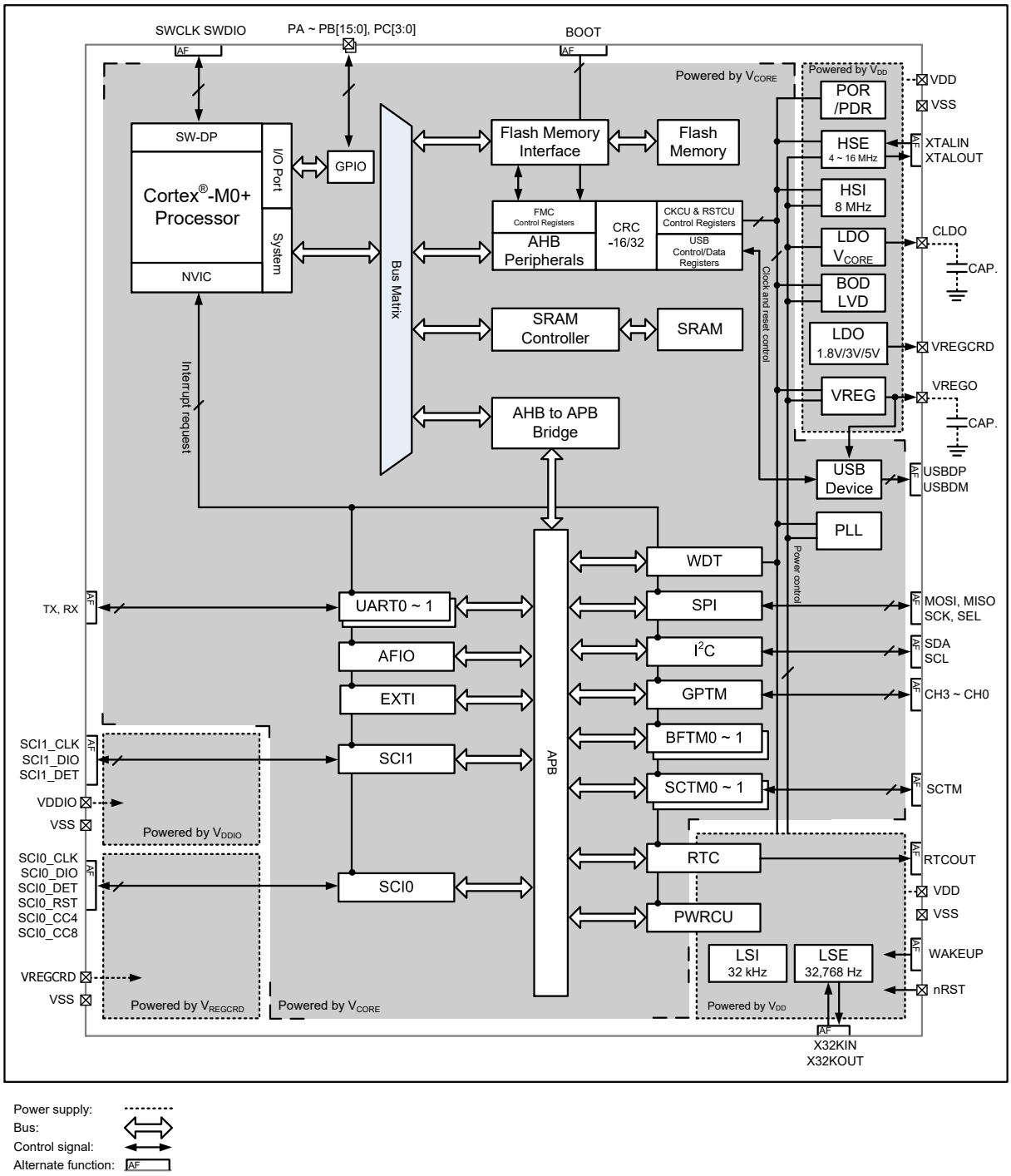


Figure 1. Block Diagram

Memory Map

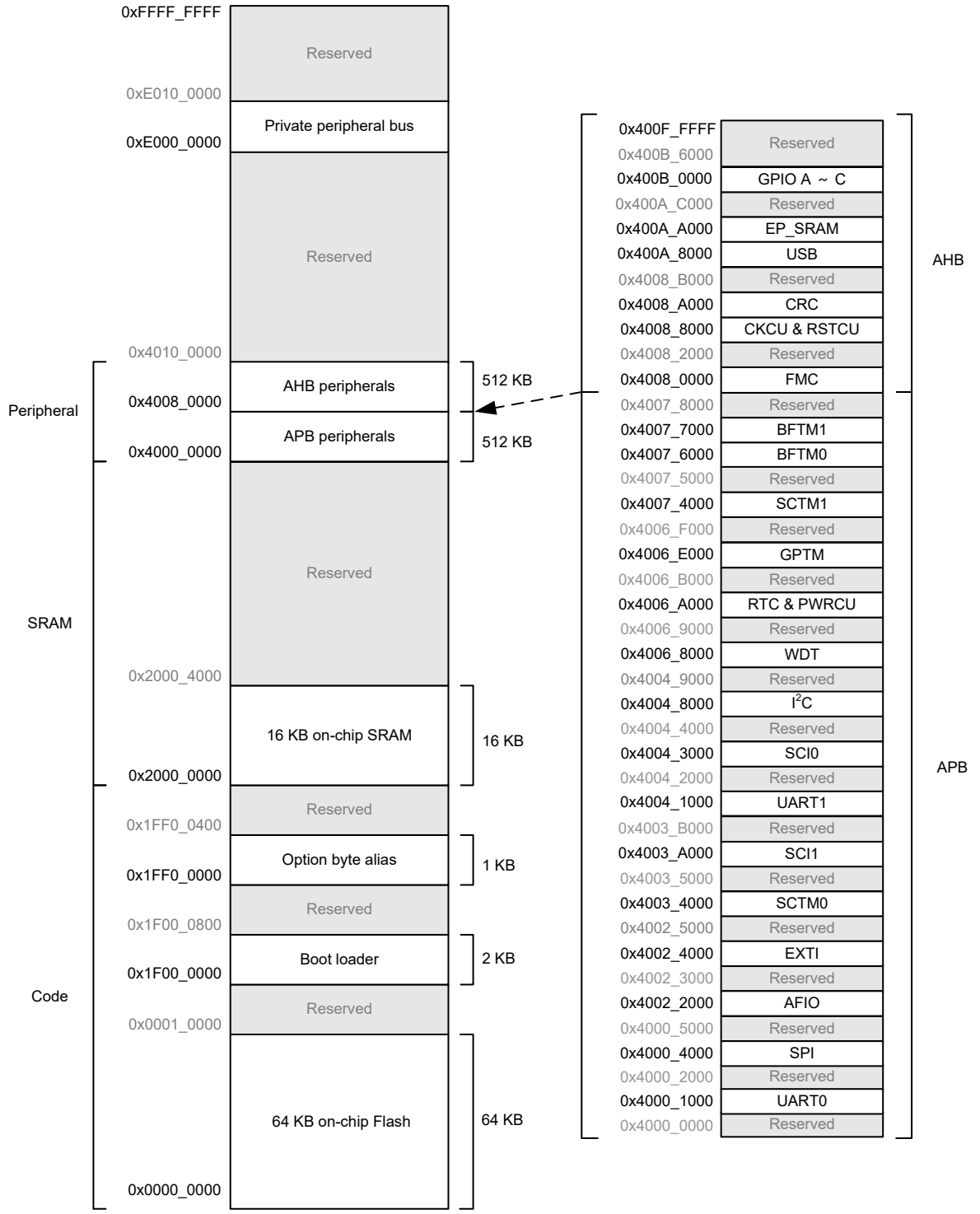
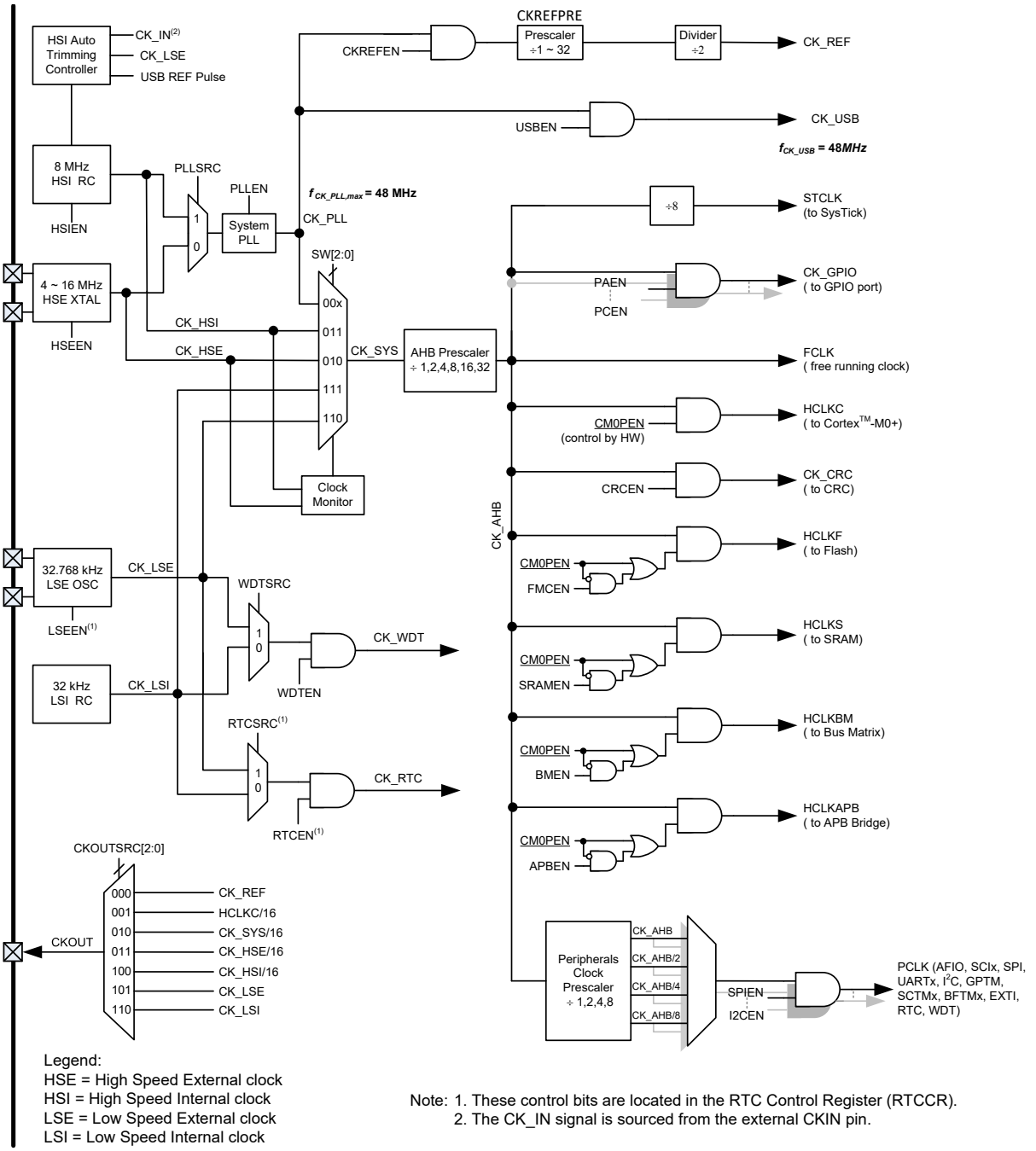


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	Reserved	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_9FFF	Reserved	
0x4003_A000	0x4003_AFFF	SCI1	
0x4003_B000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	Reserved	
0x4004_3000	0x4004_3FFF	SCI0	
0x4004_4000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_AFFF	CRC	
0x4008_B000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_9FFF	USB	
0x400A_A000	0x400A_BFFF	EP_SRAM	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400F_FFFF	Reserved	

Clock Structure



Legend:
HSE = High Speed External clock
HSI = High Speed Internal clock
LSE = Low Speed External clock
LSI = Low Speed Internal clock

Note: 1. These control bits are located in the RTC Control Register (RTCCR).
2. The CK_IN signal is sourced from the external CKIN pin.

Figure 3. Clock Structure

4 Pin Assignment

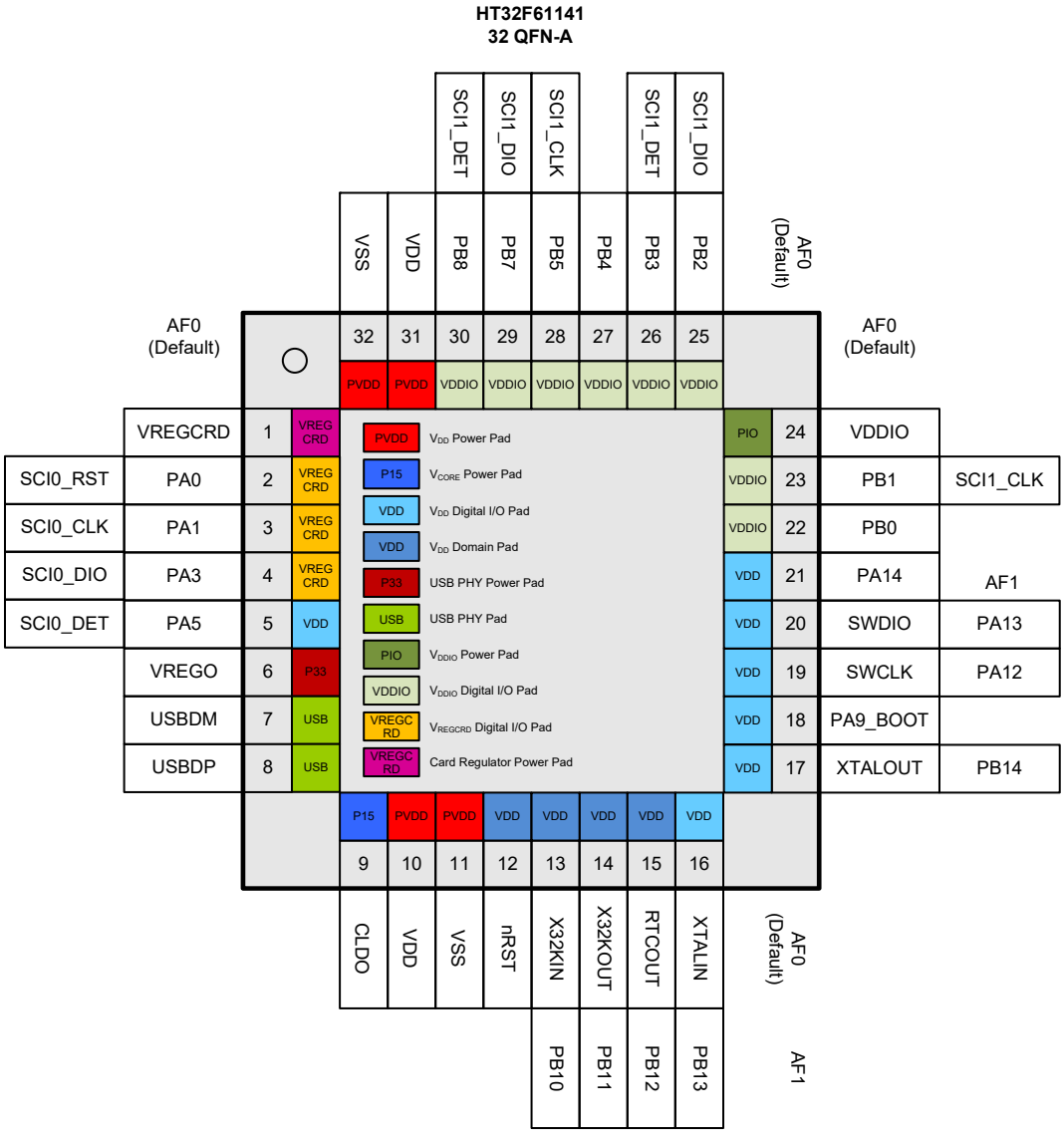


Figure 4. 32-pin QFN Pin Assignment

Note: The substrate is internally connected to VSS.

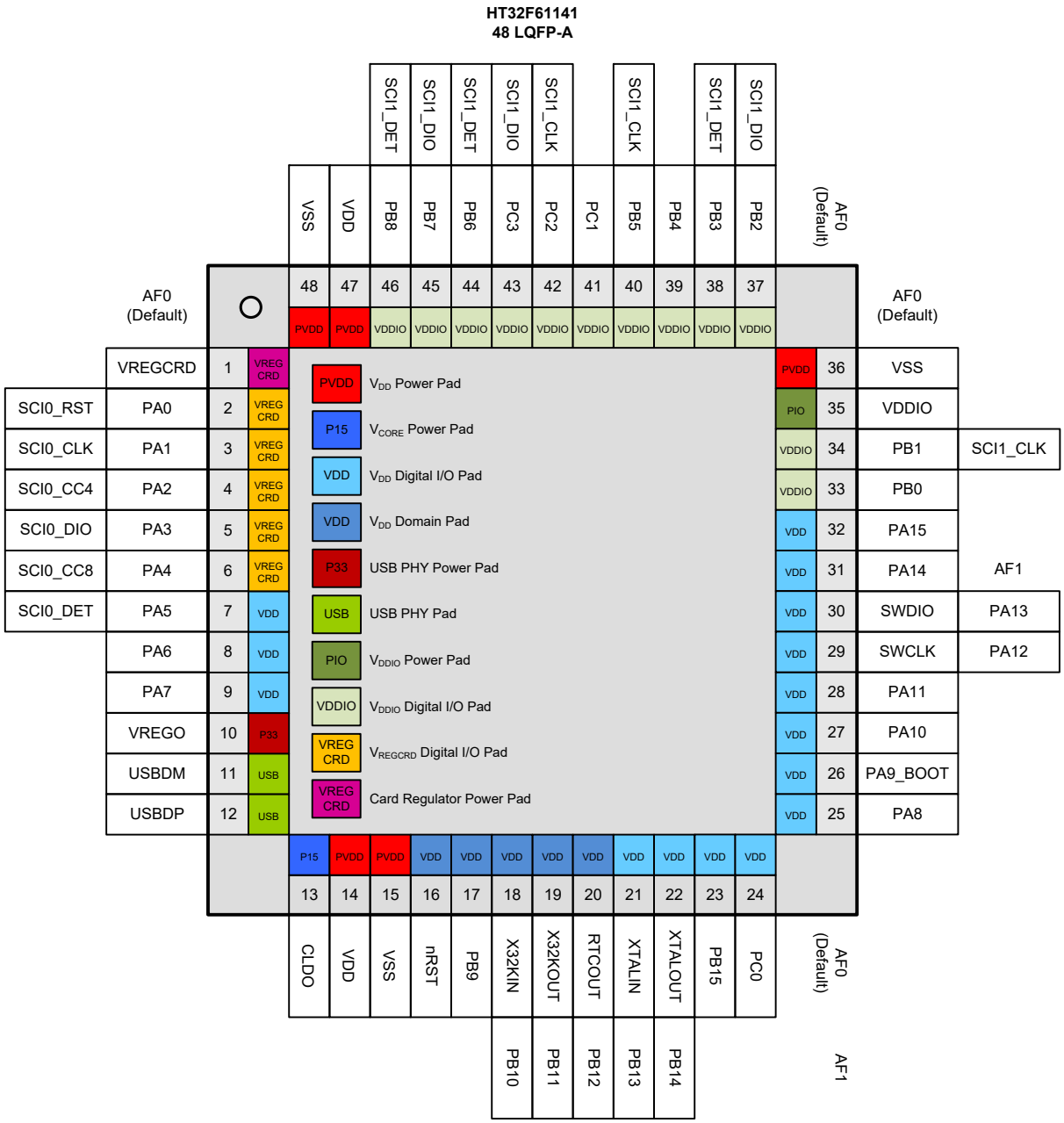


Figure 5. 48-pin LQFP Pin Assignment

Table 3. Pin Assignment

Package		Alternate Function Mapping															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	32 QFN	System Default	GPIO	N/A	N/A	GPTM	SPI	UART	I²C	SCI	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
1	1	VREGCRD															
2	2	PA0								SCI0_ RST							
3	3	PA1								SCI0_ CLK							
4		PA2								SCI0_ CC4							
5	4	PA3								SCI0_ DIO							
6		PA4								SCI0_ CC8							
7	5	PA5								SCI0_ DET							
8		PA6				GT_ CH0		UR0_ RX	I2C_ SCL						SCTM0		
9		PA7				GT_ CH1		UR0_ TX	I2C_ SDA						SCTM1		
10	6	VREGO															
11	7	USBDM															
12	8	USBDP															
13	9	CLDO															
14	10	VDD															
15	11	VSS															
16	12	nRST															
17		PB9													SCTM1		WAKEUP1
18	13	X32KIN	PB10					UR1_ TX									
19	14	X32KOUT	PB11					UR1_ RX									
20	15	RTCOUT	PB12												SCTM0		WAKEUP0
21	16	XTALIN	PB13			GT_ CH2											
22	17	XTALOUT	PB14			GT_ CH3											
23		PB15					SPI_ SEL		I2C_ SCL						SCTM0		
24		PC0					SPI_ SCK		I2C_ SDA						SCTM1		
25		PA8				GT_ CH0		UR0_ RX									
26	18	PA9_ BOOT				GT_ CH3	SPI_ MOSI	UR0_ TX									CKOUT
27		PA10				GT_ CH1											
28		PA11				GT_ CH2	SPI_ MISO								SCTM1		
29	19	SWCLK	PA12														
30	20	SWDIO	PA13														
31	21	PA14				GT_ CH3	SPI_ SEL		I2C_ SCL								
32		PA15				GT_ CH2	SPI_ SCK		I2C_ SDA						SCTM0		
33	22	PB0				GT_ CH1	SPI_ MOSI	UR1_ TX	I2C_ SCL						SCTM0		

Package		Alternate Function Mapping															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	32 QFN	System Default	GPIO	N/A	N/A	GPTM	SPI	UART	I²C	SCI	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
34	23	PB1				GT_ CH0	SPI_ MISO	UR1_ RX	I2C_ SDA	SCI1_ CLK					SCTM1		
35	24	VDDIO															
36	SUB	VSS															
37	25	PB2				GT_ CH0	SPI_ SEL	UR0_ TX		SCI1_ DIO							CKIN
38	26	PB3				GT_ CH1	SPI_ SCK	UR0_ RX		SCI1_ DET					SCTM0		
39	27	PB4				GT_ CH2	SPI_ MOSI	UR1_ TX							SCTM1		
40	28	PB5				GT_ CH3	SPI_ MISO	UR1_ RX		SCI1_ CLK							
41		PC1					SPI_ SEL		I2C_ SCL								
42		PC2					SPI_ SCK		I2C_ SDA	SCI1_ CLK							
43		PC3				GT_ CH3	SPI_ MOSI	UR0_ TX		SCI1_ DIO							
44		PB6				GT_ CH2	SPI_ MISO	UR0_ RX		SCI1_ DET							
45	29	PB7				GT_ CH1		UR0_ TX	I2C_ SCL	SCI1_ DIO					SCTM0		
46	30	PB8				GT_ CH0		UR0_ RX	I2C_ SDA	SCI1_ DET					SCTM1		
47	31	VDD															
48	32	VSS															

Table 4. Pin Description

Pin Number		Pin Name	Type(1)	I/O Structure(2)	OutputDriving	Description
48 LQFP	32 QFN					Default Function (AF0)
1	1	VREGCRD	P	—	—	On-chip voltage regulator 1.8 V / 3.0 V / 5.0 V outputIf using the internal SCI0 voltage regulator, it must be connected a 2.2 μF capacitor as close as possible between this pin and VSS.
2	2	PA0	I/O (V_{REGCRD})	5V	4/8/12/16 mA	PA0
3	3	PA1	I/O (V_{REGCRD})	5V	4/8/12/16 mA	PA1
4		PA2	I/O (V_{REGCRD})	5V	4/8/12/16 mA	PA2
5	4	PA3	I/O (V_{REGCRD})	5V	4/8/12/16 mA	PA3
6		PA4	I/O (V_{REGCRD})	5V	4/8/12/16 mA	PA4
7	5	PA5	I/O	5V	4/8/12/16 mA	PA5
8		PA6	I/O	5V	4/8/12/16 mA	PA6
9		PA7	I/O	5V	4/8/12/16 mA	PA7
10	6	VREGO	P	—	—	On-chip USB voltage regulator 3.3 V output If using the internal USB voltage regulator, it must be connected a 2.2 μF capacitor as close as possible between this pin and VSS.
11	7	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
12	8	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
13	9	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS.
14	10	VDD	P	—	—	Voltage for V_{DD} domain digital I/O
15	11	VSS	P	—	—	Ground reference for digital I/O
16	12	nRST(3)	I	5V_PU	—	External reset pin
17		PB9(3)	I/O (V_{DD})	5V	4/8/12/16 mA	PB9
18	13	PB10(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KIN
19	14	PB11(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KOUT
20	15	PB12(3)	I/O (V_{DD})	5V	4/8/12/16 mA	RTCOUT
21	16	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
22	17	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
23		PB15	I/O	5V	4/8/12/16 mA	PB15
24		PC0	I/O	5V	4/8/12/16 mA	PC0
25		PA8	I/O	5V	4/8/12/16 mA	PA8
26	18	PA9	I/O	5V_PU	4/8/12/16 mA	PA9_BOOT
27		PA10	I/O	5V	4/8/12/16 mA	PA10
28		PA11	I/O	5V	4/8/12/16 mA	PA11

Pin Number		Pin Name	Type(1)	I/O Structure(2)	OutputDriving	Description
48 LQFP	32 QFN					Default Function (AF0)
29	19	PA12	I/O	5V_PU	4/8/12/16 mA	SWCLK
30	20	PA13	I/O	5V_PU	4/8/12/16 mA	SWDIO
31	21	PA14	I/O	5V	4/8/12/16 mA	PA14
32		PA15	I/O	5V	4/8/12/16 mA	PA15
33	22	PB0	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB0
34	23	PB1	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB1
35	24	VDDIO	P	—	—	Voltage for digital V_{DDIO} domain I/O
36	SUB	VSS	P	—	—	Ground reference for digital I/O
37	25	PB2	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB2
38	26	PB3	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB3
39	27	PB4	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB4
40	28	PB5	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB5
41		PC1	I/O (V_{DDIO})	5V	4/8/12/16 mA	PC1
42		PC2	I/O (V_{DDIO})	5V	4/8/12/16 mA	PC2
43		PC3	I/O (V_{DDIO})	5V	4/8/12/16 mA	PC3
44		PB6	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB6
45	29	PB7	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB7
46	30	PB8	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB8
47	31	VDD	P	—	—	Voltage for regulator V_{REGCRD} domain I/O
48	32	VSS	P	—	—	Ground reference for the regulator

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, V_{DD} = V_{DD} Power, V_{DDIO} = V_{DDIO} Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, only the USB interface can be used for communication.
5. The SUB is the substrate and connected to VSS.

5 Electrical Characteristics

Power Supply Scheme

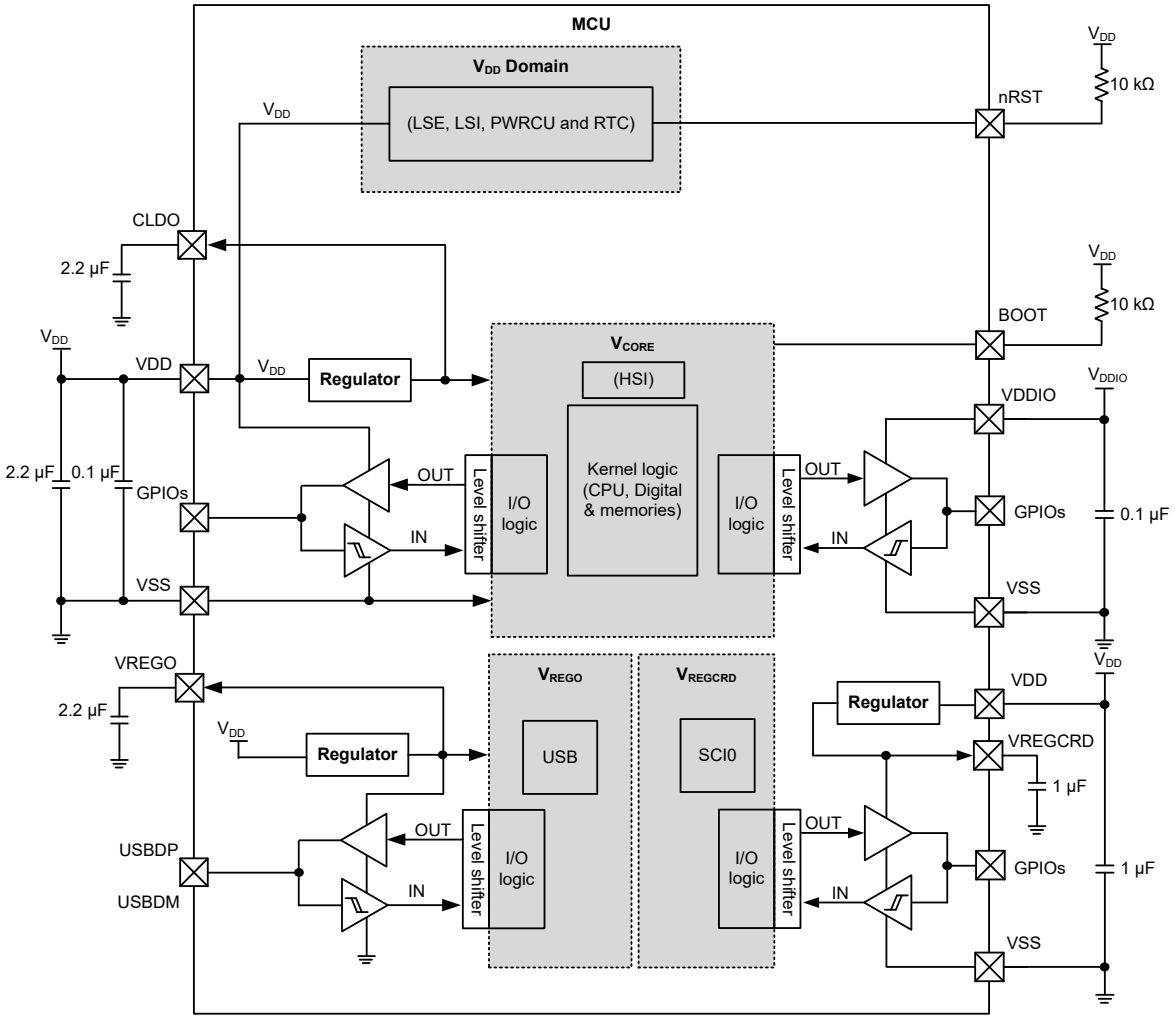


Figure 6. Power Supply Scheme

Note: 1. All regulator capacitors must be placed as close to the MCU as possible.
2. It is recommended that the pull-up resistor of the BOOT pin is 10 kΩ.
3. It is recommended that the pull-up resistor of the nRST pin is 10 kΩ.

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDIO}	External I/O Supply Voltage	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 5.5	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	+85	°C
T_{STG}	Storage Temperature Range	-60	+150	°C
T_J	Maximum Junction Temperature	—	+125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
V_{DDIO}	I/O Operating Voltage	—	1.8	5.0	5.5	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ± 5 %, after trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

On-Chip USB Voltage Regulator Characteristics

Table 8. USB Voltage Regulator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IN}	Operation Voltage Input Range	—		2.5	—	5.5	V
V_{VREGO}	On-chip USB Regulator Output Voltage after Trimming	V_{IN} ≥ 3.6 V	VREGVS [1:0] = 00	3.069	3.3	3.531	V
		V_{IN} ≥ 3.4 V	VREGVS [1:0] = 01	2.79	3.0	3.21	
		V_{IN} ≥ 4.5 V	VREGVS [1:0] = 10	3.72	4.0	4.28	
		V_{IN} ≥ 2.5 V	VREGVS [1:0] = 11	1.656	1.8	1.944	
I_{VREGO}	Output Current (Regulator Normal Mode)	V_{IN} = 3.6 V Regulator input @ V_{VREGO} = 3.3 V		—	30	50	mA
$V_{VREGOLR}$	Output Load Regulation (Regulator Normal Mode)	V_{IN} = 3.6 V Regulator input @ V_{VREGO} = 3.3 V		—	0.1	1	mV / mA
C_{VREGO}	External Capacitor Value for internal USB Regula- tor Output(1)	V_{IN} = 5.5 V Regulator input @ V_{VREGO} = 3.3 V; I_{VREGO} ≤ 50 mA		1	2.2	—	μF
I_{STATIC}	Static Current (Regulator Normal Mode)	V_{IN} = 5.5 V @ V_{VREGO} = 3.3 V, T_A = -40 °C ~ 85 °C, I_{VREGO} ≤ 50 mA		—	30	50	μA
I_{PWD}	Regulator Power Down Current	V_{IN} = 5.5 V Regulator input		—	—	0.01	μA
t_{SETUP}	Regulator Set Up Time	V_{IN} = 5.5 V, C_{VREGO} = 2.2 μF, T_A = -40 °C ~ 85 °C		—	—	500	μs

Note: 1. The Multi-layer Ceramic Capacitor (MLCC) is used for the external capacitor of the power regulator.
2. Owing to the on-chip USB voltage regulator output is internally connected to the USB driver, therefore, the on-chip USB voltage regulator has to be set to 3.3 V voltage output for the full USB electrical characteristics when the MCU USB functionality is active.
3. The reference voltage of the on-chip USB voltage regulator is from the on-chip V_{CORE} LDO Bandgap reference.

On-Chip Card Voltage Regulator Characteristics

Table 9. Card Voltage Regulator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IN}	Operation Voltage Input Range	—		2.5	—	5.5	V
$V_{VREGCRD}$	On-chip Card Regulator Output Voltage after Trimming	V_{IN} ≥ 2.5 V	VCD [1:0] = 01	1.66	1.8	1.94	V
		V_{IN} ≥ 3.3 V	VCD [1:0] = 10	2.76	3.0	3.24	
		V_{IN} ≥ 5.3 V	VCD [1:0] = 11	4.6	5.0	5.4	
$I_{VREGCRD}$	Output Current (Regulator Normal Mode)	V_{IN} = $V_{VREGCRD}$ + 0.5 V Regulator input, Δ $V_{VREGCRD}$ = 1.8 V - 3%		35	—	—	mA
		V_{IN} = $V_{VREGCRD}$ + 0.3 V Regulator input, Δ $V_{VREGCRD}$ = 3.0 V - 3%		55	—	—	mA
		V_{IN} = $V_{VREGCRD}$ + 0.3 V Regulator input, Δ $V_{VREGCRD}$ = 5.0 V - 3%		55	—	—	mA
$V_{VREGCRDLR}$	Output Load Regulation (Regulator Normal Mode)	V_{IN} = 3.6 V Regulator input @ V_{VREGO} = 3.3 V		—	0.1	1	mV / mA
$C_{VREGCRD}$	External Capacitor Value for internal Card Regula- tor Output(1)	V_{IN} = 5.5 V Regulator input @ $V_{VREGCRD}$ = 3.0 V; $I_{VREGCRD}$ ≤ 55 mA		1	2.2	—	μF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{STATIC}	Static Current (Regulator Normal Mode)	V_{IN} = 5.5 V @ $V_{VREGCRD}$ = 3.0 V, T_A = -40 °C ~ 85 °C, $I_{VREGCRD}$ ≤ 55 mA	—	30	50	μA
$V_{VREGCRD_VR}$	Output Voltage Ripple (Stable)	V_{IN} = 5.5 V @ $V_{VREGCRD}$ = 3.0 V, T_A = -40 °C ~ 85 °C, $I_{VREGCRD}$ ≤ 55 mA	—	—	200	mV
I_{OCDET}	Current Overload Detection (Regulator Normal Mode)	V_{IN} = 5.5 V @ $V_{VREGCRD}$ = 3.0 V, T_A = -40 °C ~ 85 °C, CRDMOC = 0	-10%	80	+10%	mA
		V_{IN} = 5.5 V @ $V_{VREGCRD}$ = 3.0 V, T_A = -40 °C ~ 85 °C, CRDMOC = 1	-10%	100	+10%	mA
t_{OCDET}	Detection Time On Current Overload	V_{IN} = 5 V, I_{OCDET} current up to 150 mA	—	—	1400	μs
$V_{PWRGOOD}$	Regulator Power Good Voltage	V_{IN} = 5 V, No load	$V_{VREGCRD}$ × 90%	—	—	V
I_{PWD}	Regulator Power Down Current	V_{IN} = 5 V Regulator input	—	—	0.01	μA
t_{OFF}	Regulator Output Turn Off Time	V_{IN} = 5 V, $C_{VREGCRD}$ = 2.2 μF $V_{VREGCRD}$ down to 0.4 V	—	—	1000	μs
t_{SETUP}	Regulator Set Up Time	V_{IN} = 5 V, $C_{VREGCRD}$ = 2.2 μF, T_A = -40 °C ~ 85 °C	—	—	1000	μs

Note: 1. The Multi-layer Ceramic Capacitor (MLCC) is used for the external capacitor of the power regulator.
2. Owing to the on-chip Card voltage regulator output is internally connected to the SCI0 driver, therefore, the on-chip Card voltage regulator has to be set to 1.8 V / 3.0 V / 5.0 V voltage output for the Smart Card Interface electrical characteristics when the MCU SCI0 functionality is active.
3. The reference voltage of the on-chip Card voltage regulator is from the on-chip V_{CORE} LDO Bandgap reference.

Power Consumption

The current consumption is influenced by several parameters and factors, including the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is configured under the following conditions for current consumption measured:

- All I/O pins are set to a high-impedance (floating) state.
- All peripherals are disabled unless specifically stated otherwise.
- The Flash memory access time is optimized using the minimum wait states number, depending on the f_{HCLK} frequency.
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$.

Table 10. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max @ T_A		Unit
						25 °C	85 °C	
I_{DD}	Run Mode	48 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 48 MHz	All peripherals enabled	9.75	11.0	—	mA
				All peripherals disabled	4.85	5.31	—	
		40 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 40 MHz	All peripherals enabled	9.81	11.1	—	
				All peripherals disabled	5.76	6.34	—	
		20 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 20 MHz	All peripherals enabled	5.12	5.58	—	
				All peripherals disabled	2.81	3.04	—	
		8 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = off	All peripherals enabled	1.94	2.09	—	
				All peripherals disabled	1.16	1.25	—	
		32 kHz	V_{DD} = 5.0 V LSI = 32 kHz LDO in low power mode	All peripherals enabled	28.4	40.5	—	μA
				All peripherals disabled	25.3	36.6	—	
	Sleep Mode	48 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 48 MHz MCU core sleep	All peripherals enabled	6.23	6.86	—	mA
				All peripherals disabled	0.86	0.95	—	
		40 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 40 MHz MCU core sleep	All peripherals enabled	5.27	5.82	—	
				All peripherals disabled	0.79	0.86	—	
		20 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 20 MHz MCU core sleep	All peripherals enabled	3.20	3.46	—	
				All peripherals disabled	0.66	0.73	—	
		8 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = off MCU core sleep	All peripherals enabled	1.15	1.24	—	
				All peripherals disabled	0.29	0.32	—	
	Deep-Sleep1 Mode	—	V_{DD} = 5.0 V, All clock off (HSI / HSE / PLL / LSE), LDO in low power mode, LSI on, RTC on		21.6	29.3	—	μA
	Deep-Sleep2 Mode	—	V_{DD} = 5.0 V, All clock off (HSI / HSE / PLL / LSE), LDO off, DMOS on, LSI on, RTC on		5.0	6.67	—	μA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real-time clock.
4. Code = while (1) {208 NOP} executed in Flash.

Reset and Supply Monitor Characteristics

Table 11. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	2.22	2.35	2.48	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	2.12	2.20	2.33	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 12. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	T_A = -40 °C ~ 85 °C, After factory-trimmed, V_{DD} Falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	T_A = -40 °C ~ 85 °C V_{DD} Falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3.53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHYST}$	LVD Hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 5.0 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 5.0V	—	—	200	—	μs
I_{DDLVD}	Operation Current (2)	V_{DD} = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 13. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_HSE}	HSE Frequency	V_{DD} = 2.5 V ~ 5.0 V	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 5.0 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	12	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	V_{DD} = 5.0 V	—	0.5	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 0	—	—	110	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 5.0 V, R_{ESR} = 100 Ω, C_L = 12 pF @ 8 MHz, HSEGAIN = 0	—	0.85	—	mA
		V_{DD} = 5.0 V, R_{ESR} = 25 Ω, C_L = 12 pF @ 16 MHz, HSEGAIN = 1	—	3.0	—	
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 5.0 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 5.0 V	—	—	4	ms

Table 14. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 2.5 V ~ 5.5 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{DD} = 5.0 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz R_{ESR} = 50 kΩ, C_L ≥ 7 pF V_{DD} = 2.5 V ~ 5.5 V T_A = -40 °C ~ 85 °C	—	4.0	5.6	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz R_{ESR} = 50 kΩ, C_L < 7 pF V_{DD} = 2.5 V ~ 5.5 V T_A = -40 °C ~ 85 °C	—	3.6	4.5	μA
	LSE Oscillator Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 2.5 V ~ 5.5 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 15. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_HSI}	HSI Frequency	V_{DD} = 5.0 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 5.0 V, T_A = 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ 85 °C	-3	—	3	%
Duty	Duty Cycle	f_{CK_HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{CK_HSI} = 8 MHz @ V_{DD} = 2.5 V ~ 5.5 V	—	—	140	μA
	HSI Oscillator Power Down Current		—	—	0.01	μA
t_{SUHSI}	HSI Oscillator Startup Time	f_{CK_HSI} = 8 MHz	—	—	20	μs

Table 16. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_LSI}	LSI Frequency	V_{DD} = 5.0 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 5.0 V	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 5.0 V	—	0.5	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 5.0 V	—	—	100	μs

System PLL Characteristics

Table 17. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	48	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 18. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before Failure (Endurance)	T_A = -40 °C ~ 85 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 19. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	5.0 V I/O	$V_I = V_{SS}$, On-chip pull-up resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
I_{IH}	High Level Input Current	5.0 V I/O	$V_I = V_{DD}$, On-chip pull-down resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
V_{IL}	Low Level Input Voltage	5.0 V I/O		- 0.5	—	V_{DD} × 0.35	V
		Reset pin		- 0.5	—	V_{DD} × 0.35	
V_{IH}	High Level Input Voltage	5.0 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	
I_{OL}	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V_{OL} = 0.6 V		4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.6 V		8	—	—	
		5.0 V I/O 12 mA drive, V_{OL} = 0.6 V		12	—	—	
		5.0 V I/O 16 mA drive, V_{OL} = 0.6 V		16	—	—	
I_{OH}	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	4	—	mA
		5.0 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	8	—	
		5.0 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	12	—	
		5.0 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	16	—	
V_{OL}	Low Level Output Voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.6	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.6	
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.6	
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.6	
V_{OH}	High Level Output Voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.6	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.6	—	—	
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA		V_{DD} - 0.6	—	—	
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA		V_{DD} - 0.6	—	—	
R_{PU}	Internal Pull-up Resistor	V_{DD} = 5.0 V		—	50	—	kΩ
		V_{DD} = 3.3 V		—	76	—	
		V_{DD} = 5.0 V, On SCI0_DIO pin		7.5	15	22.5	
R_{PD}	Internal Pull-down Resistor	V_{DD} = 5.0 V		—	50	—	kΩ
		V_{DD} = 3.3 V		—	76	—	

GPTM / SCTM Characteristics

Table 20. GPTM / SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM / SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 21. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

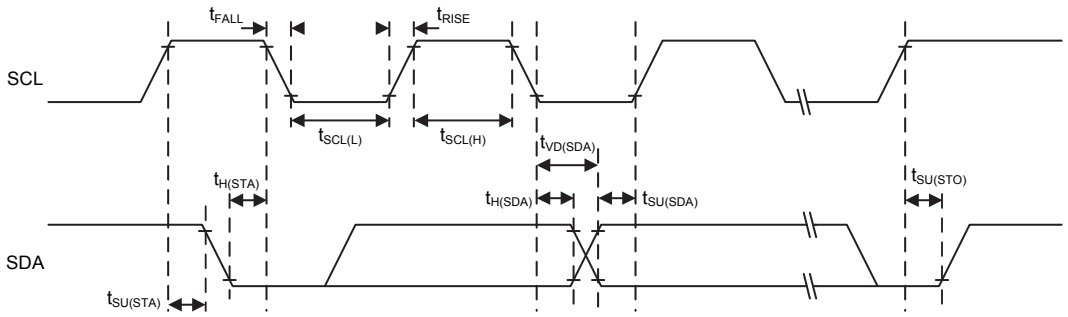


Figure 7. I²C Timing Diagram

SPI Characteristics

Table 22. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High / Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3 \times t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2 \times t_{PCLK}$	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3 \times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

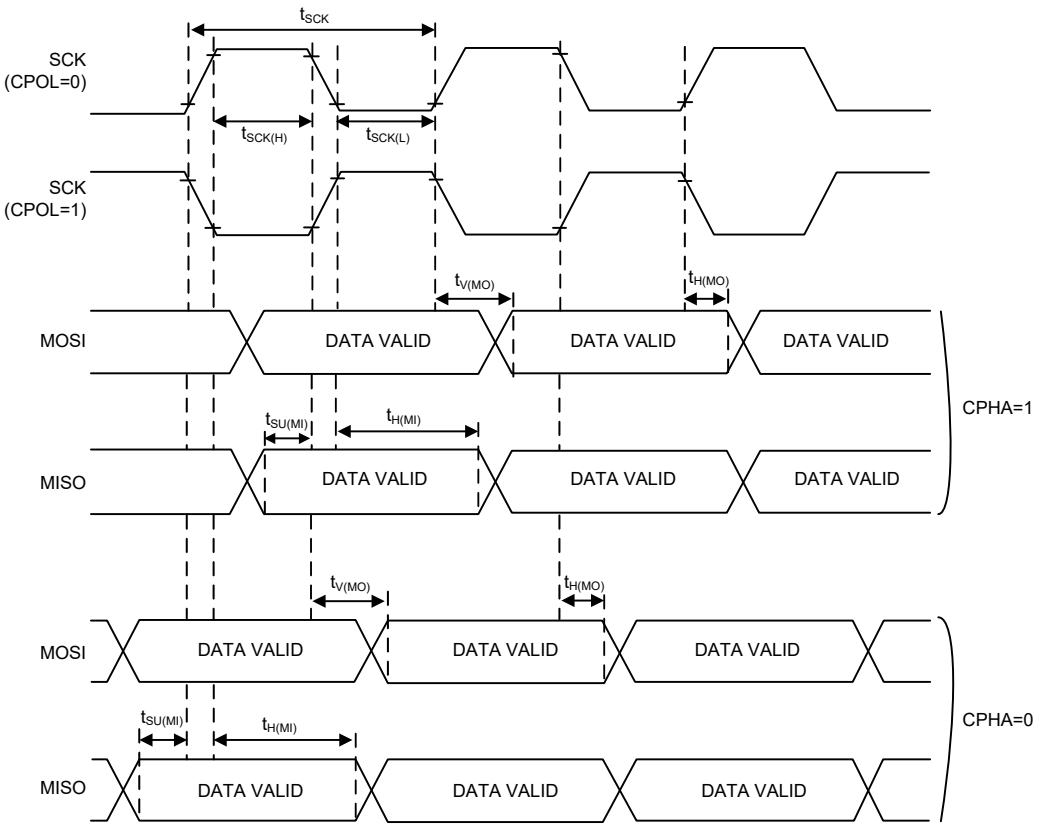


Figure 8. SPI Timing Diagram – SPI Master Mode

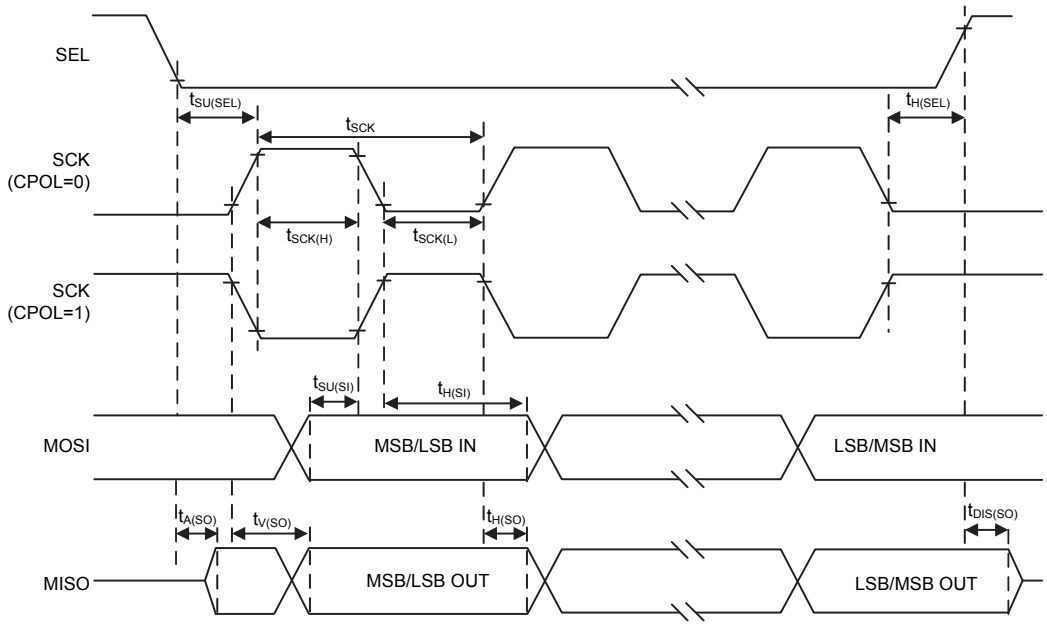


Figure 9. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

USB Characteristics

The USB interface is USB-IF certified – Full Speed.

Table 23. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{USB}	USB Operating Voltage	—	3.0	—	3.6	V
V_{DI}	Differential Input Sensitivity	|USBDP-USBDM|	0.2	—	—	V
V_{CM}	Common Mode Voltage Range	—	0.8	—	2.5	V
V_{SE}	Single-ended Receiver Threshold	—	0.8	—	2.0	V
V_{OL}	Pad Output Low Voltage	1.5 kΩ R_L to V_{REGO}	0	—	0.3	V
V_{OH}	Pad Output High Voltage		2.8	—	3.6	V
V_{CRS}	Differential Output Signal Cross-point Voltage		1.3	—	2.0	V
Z_{DRV}	Driver Output Resistance	—	—	10	—	Ω
C_{IN}	Transceiver Pad Capacitance	—	—	—	20	pF

Note: 1. Data based on characterization results only, not tested in production.
2. Owing to the on-chip USB voltage regulator output is internally connected to the USB driver, the on-chip USB voltage regulator has to be set to 3.3 V voltage output for the full USB electrical characteristics when the MCU USB functionality is active.
3. R_L is the resistor load connected to the USB driver USBDP.

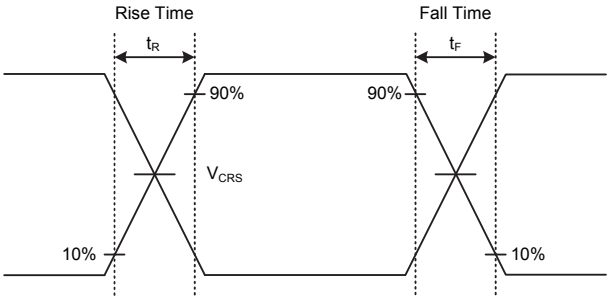


Figure 10. USB Signal Rise Time, Fall Time and Cross-Point Voltage (V_{CRS}) Definition

Table 24. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_R	Rise Time	C_L = 50 pF	4	—	20	ns
t_F	Fall Time	C_L = 50 pF	4	—	20	ns
$t_{R/F}$	Rise Time / Fall Time Matching	$t_{R/F} = t_R / t_F$	90	—	110	%

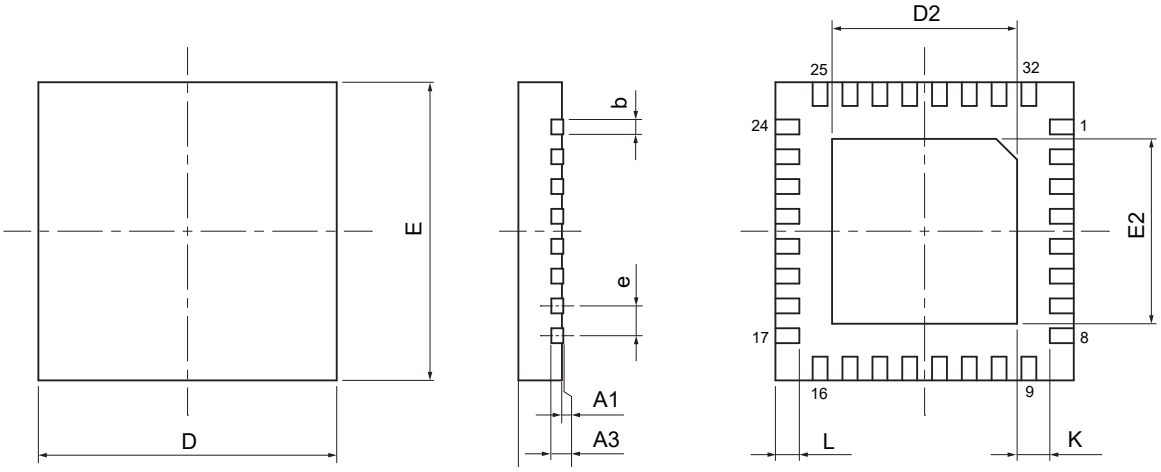
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

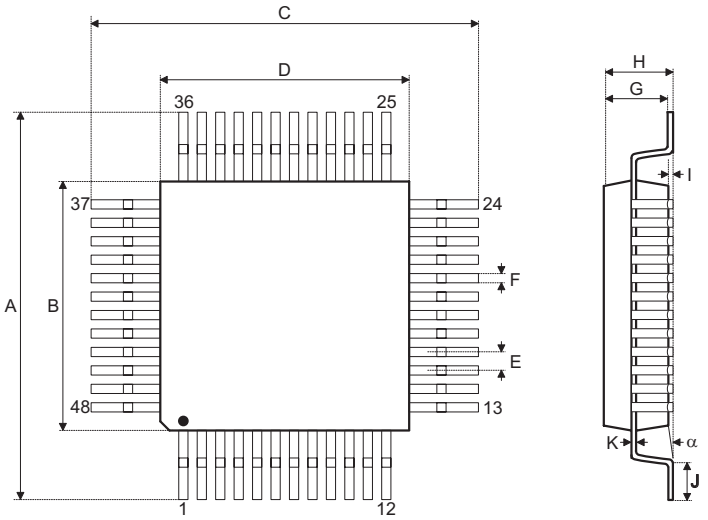
SAW Type 32-pin QFN (4mm × 4mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.006	0.008	0.010
D		0.157 BSC	
E		0.157 BSC	
e		0.016 BSC	
D2	0.100	—	0.108
E2	0.100	—	0.108
L	0.010	—	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.55	—	2.75
E2	2.55	—	2.75
L	0.25	—	0.45
K	0.20	—	—

48-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.020 BSC	
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.50 BSC	
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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