HT32F61355/HT32F61356/HT32F61357 Datasheet

32-Bit Arm® Cortex®-M0+ Microcontroller
with 32-channel Music Synthesizer
up to 128 KB Flash, 16 KB SRAM and 32/64/128 Mbits
Flash Data Memory with Music Synthesis Engine (MIDI Engine)
DAC, 1 Msps ADC, USART, UART, SPI, QSPI, I²C, I²S
GPTM, SCTM, BFTM, CRC, RTC, WDT, PDMA and USB2.0 FS

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1 General Description

These devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The devices operate at a frequency of up to 48 MHz with a Flash accelerator to obtain maximum efficiency. They provide up to 128 KB of embedded Flash memory for code/data storage and 16 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, 2-channel DAC, I^{2}C, I^{2}S, USART, UART, SPI, QSPI, GPTM, SCTM, CRC-16/32, RTC, WDT, PDMA, USB2.0 FS, 32-channel music synthesizer, SW-DP (Serial Wire Debug Port), etc., are also implemented in the devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The devices integrate Wave Table synthesis function. They can operate up to 32 channels of Wave Table synthesis at one time and control the MIDI Engine to generate melody by setting the special registers. The Wave Table synthesis waveform data including instrument tone, MIDI scores, voice, sound effect,etc., are strored in the internal SPI Flash Data Memory. With these features, the devices provide enhanced functions and higher performance.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as electronic organs, digital pianos, electronic drums, electric guitars, electric accordions and so on.

arm CORTEX

2 Development Tools

For rapid product development and to simplify device parameter setting, Holtek has provided relevant development tools which users can download from the following link:

https://www.holtek.com/page/tool-detail/dev_plat/voice/audio_workshop

3 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 48 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontrollers and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the Armv6-M architecture and supports Thumb® instruction sets; single-cycle I/O port; hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- Up to 128 KB on-chip Flash memory for instruction/data and option byte storage
- 16 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripheral. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash

Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power on Reset / Power down Reset – POR/PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), an HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the LSI, LSE, HSI, HSE or PLL. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- Single V_{DD} power supply: 2.0 V to 3.6 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- Two power domains: V_{DD}, V_{CORE}
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 16 external analog input channels

A 12-bit multi-channel ADC is integrated in the devices. There are multiplexed channels, which include 16 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

I/O Ports – GPIO

- Up to 43 GPIOs
- Port A, B, C, D are mapped to 16-line EXTI interrupts
- Almost all I/O pins have a configurable output driving current.

There are up to 43 General Purpose I/O pins, GPIO for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the devices have related control and configuration registers in the External Interrupt Control Unit, EXTI.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer Module, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single-Channel Timer – SCTM

- 16-bit up and auto-reload counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single-Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM output.

Basic Function Timer – BFTM

- One 32-bit compare match count-up counter – no I/O control features
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Digital to Analog Converter – DAC

- Two 16-bit high resolution D/A converters with excellent frequency response characteristics and good power consumption for stereo audio output.

Music Synthesis Engine (MIDI Engine) – MSE

- Up to 32 simultaneous sounds @ CPU Frequency = 48 MHz / Up to 16 simultaneous sounds @ CPU Frequency = 24 MHz
- 10-bit Volume Control
- Output sampling frequency up to 50 kHz
- Waveform data lengths of 8, 12 or 16 bits
- Stereo output
- Supports Repeat loop Play
- Supports PDMA interface

Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real-Time Clock – RTC

- 32-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, includes an APB interface, a 32-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} Domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I^2C is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I^2C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Inter-IC Sound – I^{2}S

- Master or slave mode
- Mono and stereo
- I^{2}S-justified, Left-justified and Right-justified mode
- 8 / 16 / 24 / 32-bit sample size with 32-bit channel extended
- 8 × 32-bit TX & RX FIFO with PDMA supported
- 8-bit Fractional Clock Divider with rate control

The I^{2}S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADCs or DACs. The I^{2}S supports a variety of data formats. In addition to the stereo I^{2}S-justified, Left-justified and Right-justified modes, there are mono PCM modes with 8 / 16 / 24 / 32-bit sample size. When the I^{2}S operates in the master mode, then when using the fractional divider, it can provide an accurate sampling frequency output and support the rate control function and fine-tuning of the output frequency to avoid system problems caused by the cumulative frequency error between different devices.

Operation Divider – DIV

- Signed/unsigned 32-bit divider
- Operation in 8 clock cycles, Load in 1 clock cycle
- Division by zero error flag

In order to enhance MCU performance, a Divider is implemented within the devices. The division and modulus functions of the truncated division are related in the following way:

$$A / B = Q \ldots R$$

Where “A” is Dividend, “B” is Divisor, “Q” is Quotient and “R” is Remainder. Divider needs software trigger start signal by using the control register “START” bit , after 8 clock cycles, the divider calculate complete flag will be set to 1, but if divisor register data is zero, divide 0 error flag will be set to 1.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Quad Serial Peripheral Interface – QSPI

- Master or slave mode
- Master mode speed up to $f_{HCLK}/2$
- Slave mode speed up to $f_{HCLK}/3$
- Programmable data frame length up to 16 bits
- FIFO Depth: 8 levels
- MSB or LSB first shift selection
- Programmable slave select high or low active polarity
- Multi-master and multi-slave operation
- Master mode supports the dual/quad output read mode of QSPI series NOR Flash
- Four error flags with individual interrupt
  - Read overrun
  - Write collision
  - Mode fault
  - Slave abort
- Supports PDMA interface

The Quad Serial Peripheral Interface, QSPI, provides a QSPI protocol data transmit and receive functions in both master or slave mode. The QSPI interface uses 6 pins for Dual/Quad SPI, among which are serial data input and output lines SIO3, SIO2, MISO/SIO1 and MOSI/SIO0, the clock line SCK, and the slave select line SEL.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to ($f_{PCLK}/16$) MHz for Asynchronous mode and ($f_{PCLK}/8$) MHz for synchronous mode
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, TX FIFO, and receiver FIFO, RX FIFO. The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud rate clock frequency up to $f_{PCLK}/16$ MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, then this means that the data stream contains a data error.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 full-speed (12 Mbps) specification
- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints (EP1 ~ EP3) for bulk and interrupt transfer
- 4 double-buffered endpoints (EP4 ~ EP7) for bulk, interrupt and isochronous transfer
- 1,024 bytes EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte EP_SRAM is used as the endpoint buffer. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize the overall system complexity and cost. The USB functional block also contains the resume and suspend feature to meet the requirements of low-power consumption.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8 / 16 / 32-bit width data transfer
- Supports Linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source: ADC, SPI, QSPI, USART, UART, I^2C, I^2S, GPTM, MIDI Engine and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to join each data movement operation.

SPI Flash Data Memory

- Full voltage range: 2.3 V ~ 3.6 V
- Serial Interface Architecture
- SPI compatible: Mode 0 and Mode 3
- 256 bytes per programmable page
- Standard, Dual or Quad SPI modes
- Low power consumption
- Uniform Sector Architecture
- Any sector or block can be erased individually
- Software and Hardware Reset
- Read Unique ID Number

The Flash data memory is a 32 / 64 / 128 Mbits Serial Flash memory, with advanced write protection mechanisms. The devices support the single bit and four bits serial input and output commands via standard Serial Peripheral Interface (SPI) pins: Serial Clock, Chip Select, Serial DQ0 (DI) and DQ1(DO), DQ2 and DQ3. The memory can be programmed 1 to 256 bytes each time, using the Page Program instruction.

The devices also offer a sophisticated method for protecting individual blocks against erroneous or malicious program and erase operations. By providing the ability to individually protect and unprotect blocks, a system can unprotect a specific block to modify its contents while keeping the remaining blocks of the memory array securely protected.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 48/64-pin LQFP packages
- Operation temperature range: -40 °C to 85 °C

4 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F61355	HT32F61356	HT32F61357
Main Flash (KB)		127.5		
Option Bytes Flash (KB)		0.5		
SRAM (KB)		16		
Timers	GPTM	1		
	SCTM	4		
	BFTM	2		
	RTC	1		
	WDT	1		
Communication	USB	1		
	SPI	1		
	QSPI	1		
	USART	1		
	UART	1		
	I^{2}C	1		
	I^{2}S	1		
PDMA		6 Channels		
Hardware Divider		1		
CRC-16 / 32		1		
EXTI		16		
12-bit ADC		1		
Number of channels		16 External Channels		
Music Synthesis Engine		32 Channels		
16-bit DAC		2 Channels		
SPI Flash Data Memory		32 Mbits	64 Mbits	128 Mbits
GPIO		Up to 43		
CPU frequency		Up to 48 MHz		
Operating voltage		2.0 V ~ 3.6 V		
Operating temperature		-40 °C ~ 85 °C		
Package		48 / 64-pin LQFP		

Note: The functions listed here, except the SPI Flash Data Memory, are compatible with the HT32F0006 device. Refer to the HT32F0006 user manual for detailed functional description.

Block Diagram

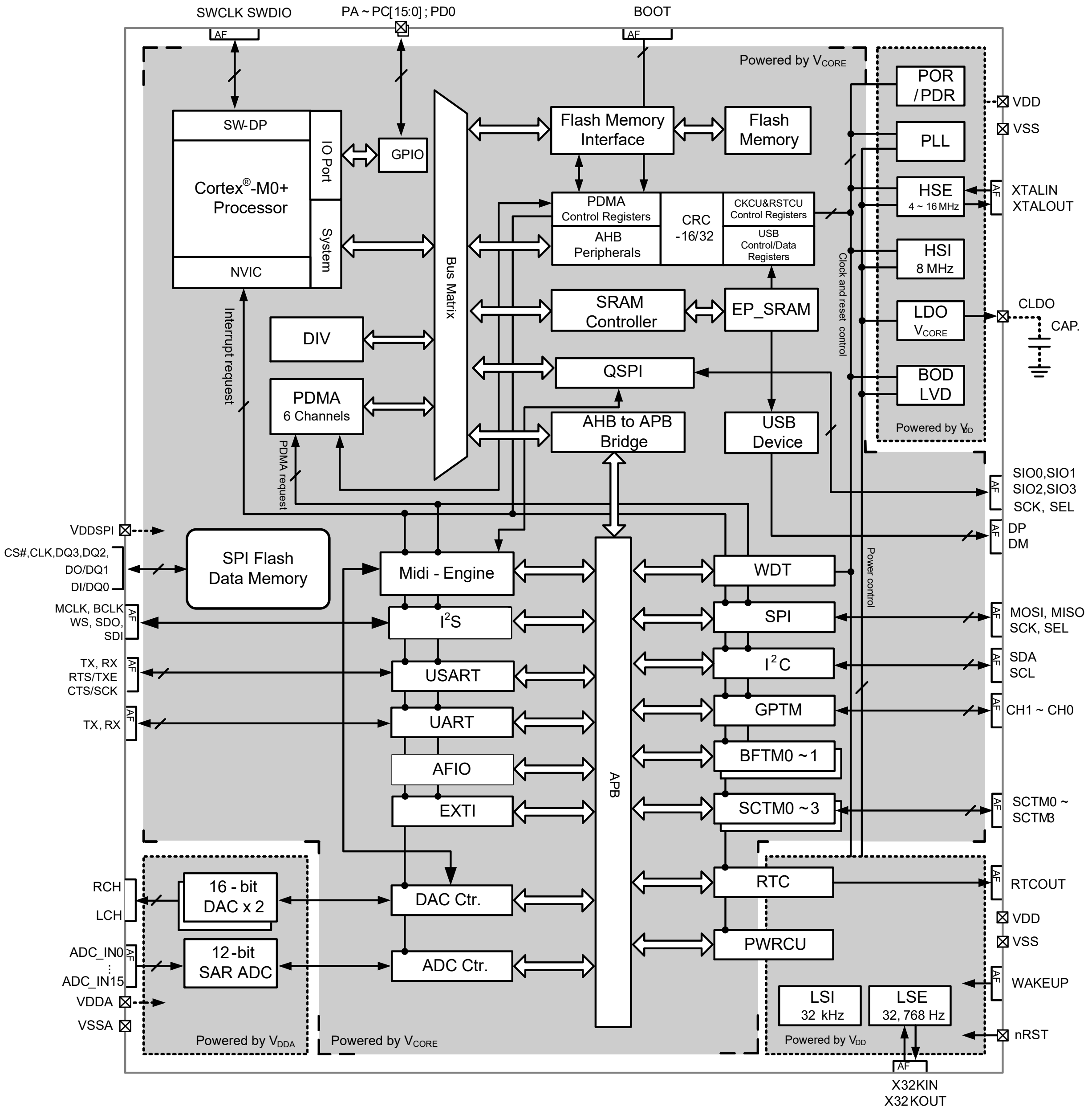


Figure 1. Block Diagram

Memory Map

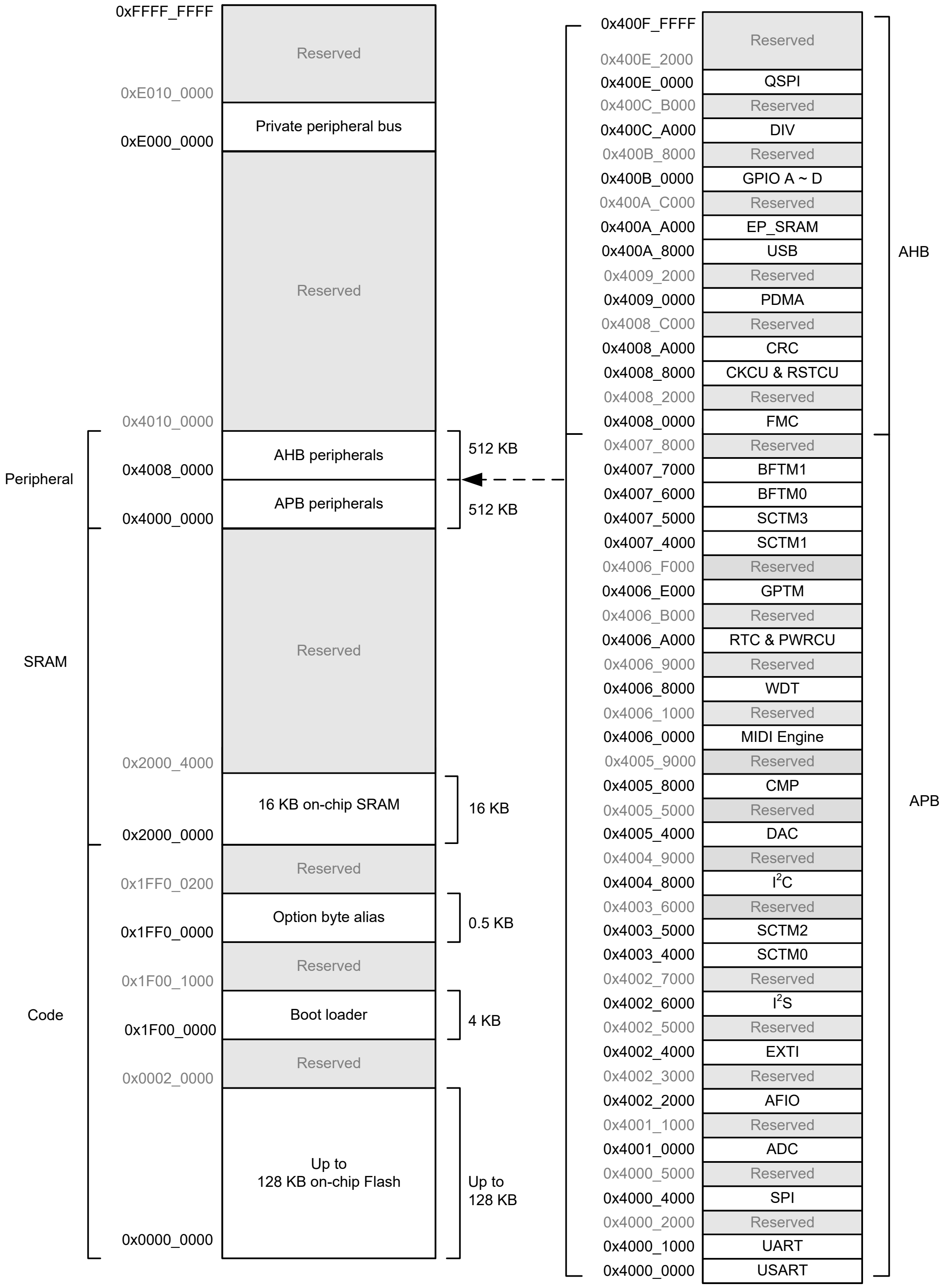


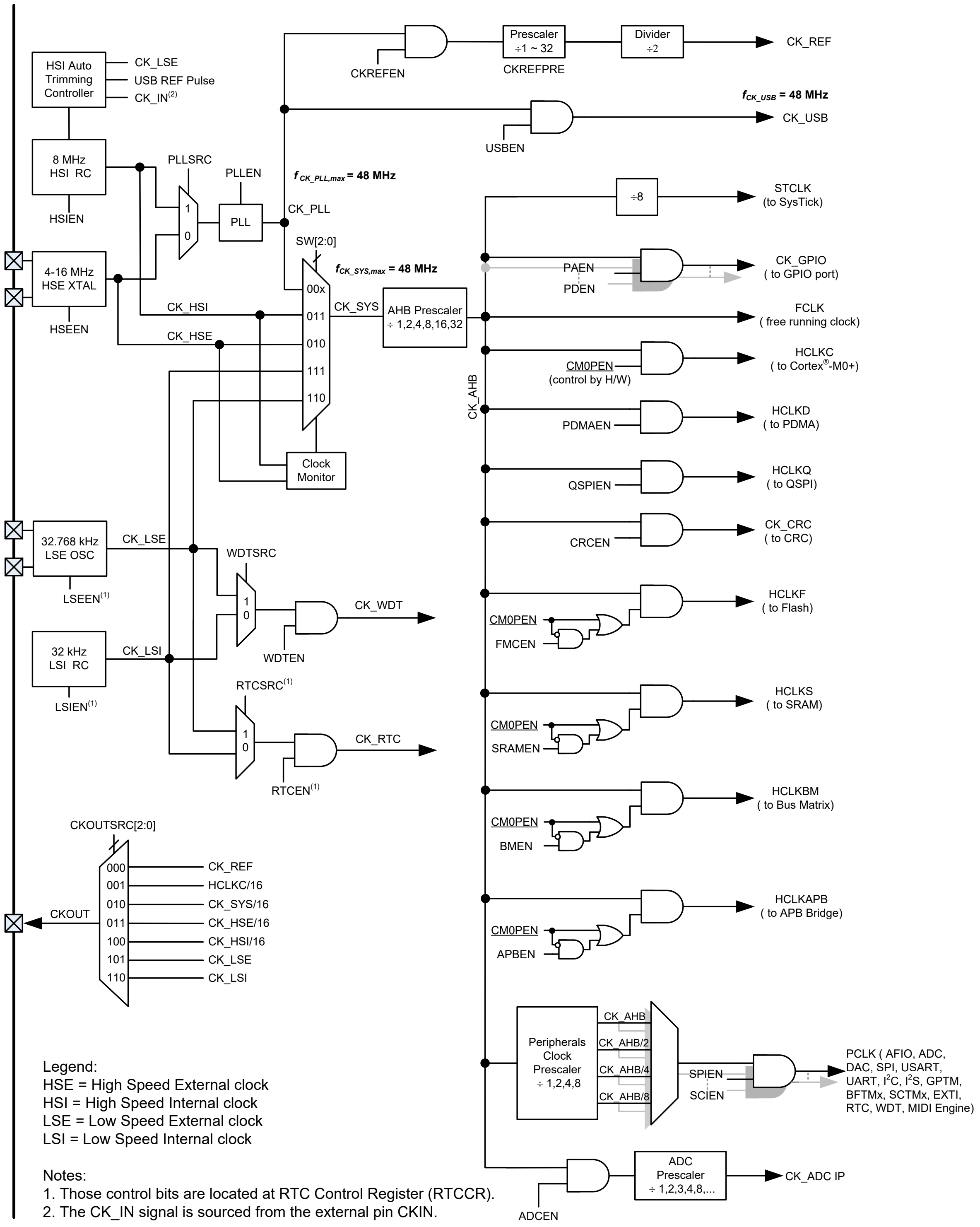
Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_5FFF	Reserved	
0x4002_6000	0x4002_6FFF	I^{2}S	
0x4002_7000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^{2}C	
0x4004_9000	0x4005_3FFF	Reserved	
0x4005_4000	0x4005_4FFF	DAC	
0x4005_5000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	Comparator	
0x4005_9000	0x4005_FFFF	Reserved	
0x4006_0000	0x4006_0FFF	MIDI Engine	
0x4006_1000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC&PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	SCTM3	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA Control Registers	
0x4009_2000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_BFFF	USB	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400B_7FFF	GPIO D	
0x400B_8000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_AFFF	DIV	
0x400C_B000	0x400D_FFFF	Reserved	
0x400E_0000	0x400E_1FFF	QSPI	
0x400E_2000	0x400F_FFFF	Reserved	

Clock Structure



Legend:
HSE = High Speed External clock
HSI = High Speed Internal clock
LSE = Low Speed External clock
LSI = Low Speed Internal clock

Notes:
1. Those control bits are located at RTC Control Register (RTCCR).
2. The CK_IN signal is sourced from the external pin CKIN.

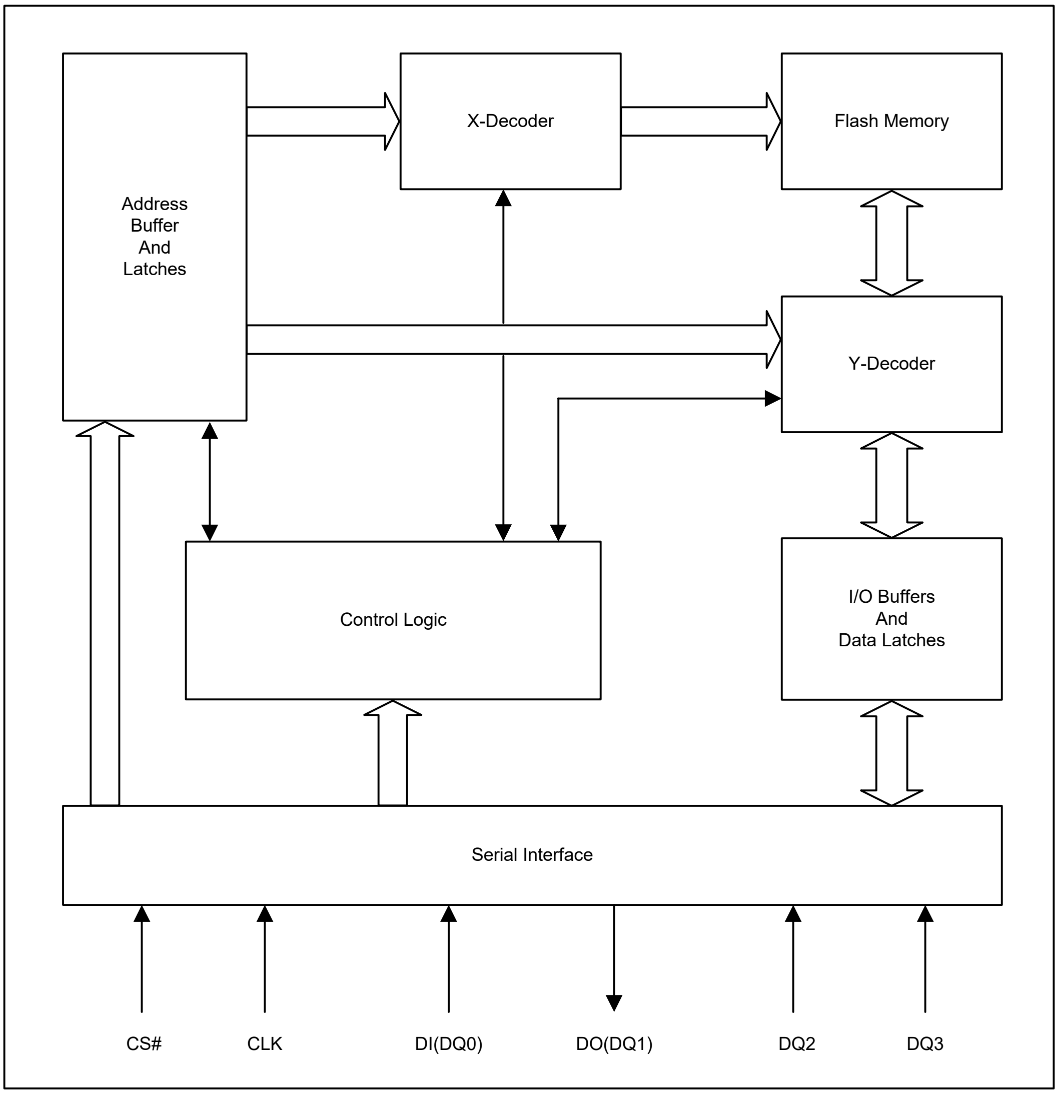
Figure 3. Clock Structure

5 SPI Flash Data Memory

The SPI Flash Data Memory is the location where the user's music data is stored. By using the Holtek Audio Workshop tool, these devices offer users the flexibility to conveniently change and develop their applications while also offering a means of field programming.

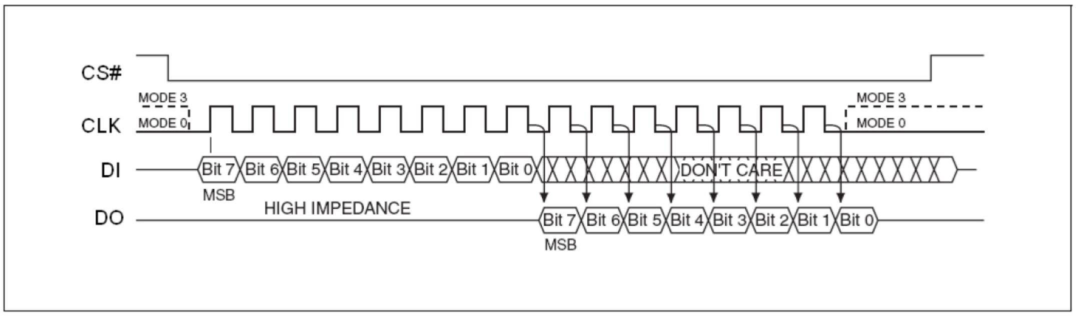
The Flash data memory supports the single bit and four bits serial input and output commands via standard Serial Peripheral Interface (SPI) pins: Serial Clock, Chip Select, Serial DQ0 (DI) and DQ1(DO), DQ2 and DQ3.

The internal Flash Data Memory within the devices has a capacity of 32 / 64 / 128 Mbits respectively and can be programmed 1 to 256 bytes each time, using the Page Program instruction.



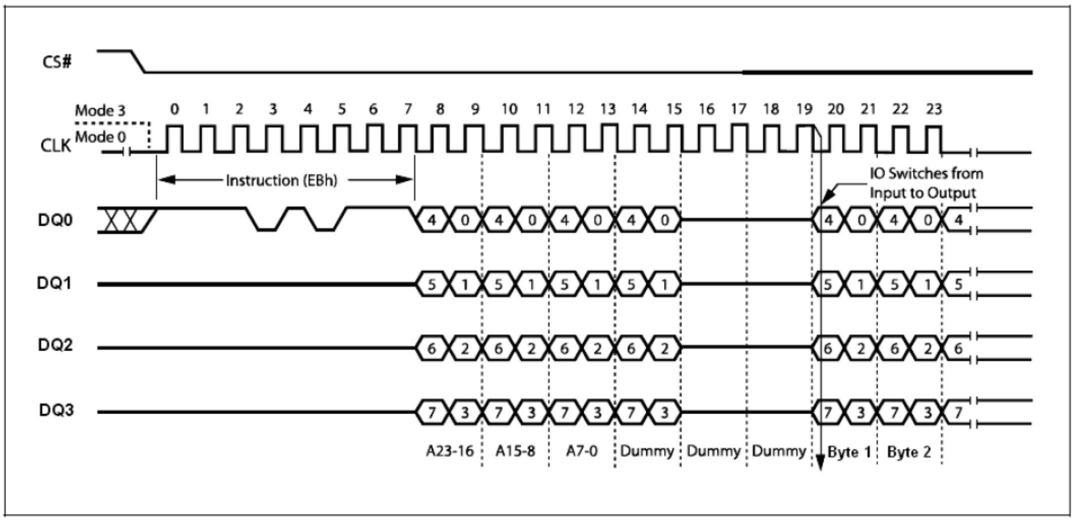
Standard SPI Modes

The Flash data memory is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3, as shown in the following figure, concerns the normal state of the CLK signal when the SPI bus master is in standby state and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of CLK. Data output on the DO pin is clocked out on the falling edge of CLK.



Quad I/O SPI Modes

The Flash Memory supports Quad input/output operation when using the Quad I/O Fast Read (EBh) instruction. This instruction allows data to be transferred to or from the Serial Flash memory at four to six times the rate possible with the standard SPI. When using Quad SPI instruction the DI and DO pins become bidirectional I/O pins DQ0 and DQ1, and DQ2 and DQ3 are also used.

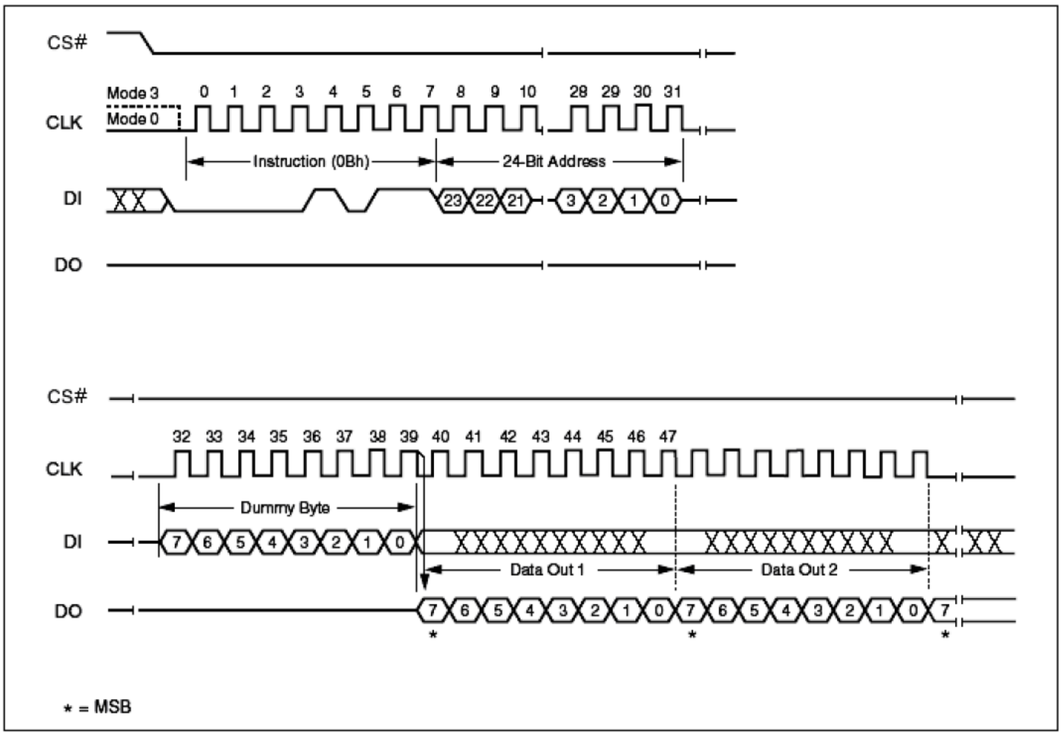


Read Data Bytes at Higher Speed (FAST_READ) (0Bh)

The Flash data Memory is first selected by driving Chip Select (CS#) to Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out at the falling edge of Serial Clock (CLK).

The instruction sequence is shown in following figure. The first byte to be addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (CS#) to High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

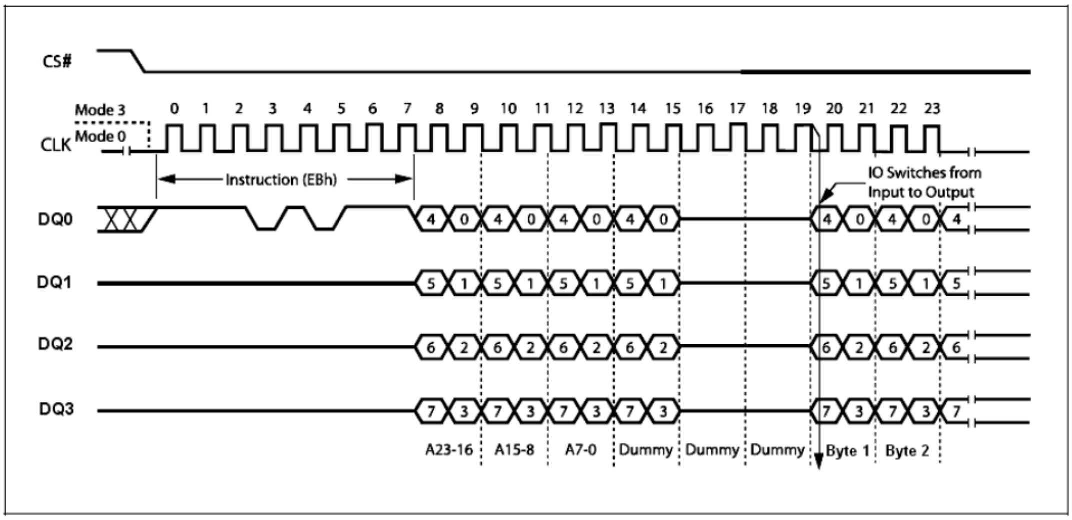


Quad Input / Output FAST_READ (EBh)

For the Quad Input/Output FAST_READ (EBh) instruction, the address and data bits are input and output through four pins, DQ0, DQ1, DQ2 and DQ3 and six dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Quad Input/Output FAST_READ (EBh) instruction enables quad throughput of Serial Flash in read mode. The address is latched on the rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) is shifted out on the falling edge of CLK. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out with a single Quad Input/Output FAST_READ instruction. The address counter rolls over to 000000h when the highest address has been reached. Once writing Quad Input/Output FAST_READ instruction, the following address/dummy/data out will be performed as 4-bit instead of previous 1-bit.

The sequence of issuing Quad Input/Output FAST_READ (EBh) instruction is: CS# goes low ⇒ send Quad Input/Output FAST_READ (EBh) instruction ⇒ 24-bit address interleave on DQ3, DQ2, DQ1 and DQ0 ⇒ 6 dummy clocks ⇒ data out interleave on DQ3, DQ2, DQ1 and DQ0 ⇒ drive CS# to High at any time during data out to end Quad Input/Output FAST_READ (EBh) operation, as shown in the following figure.



6 Pin Assignment

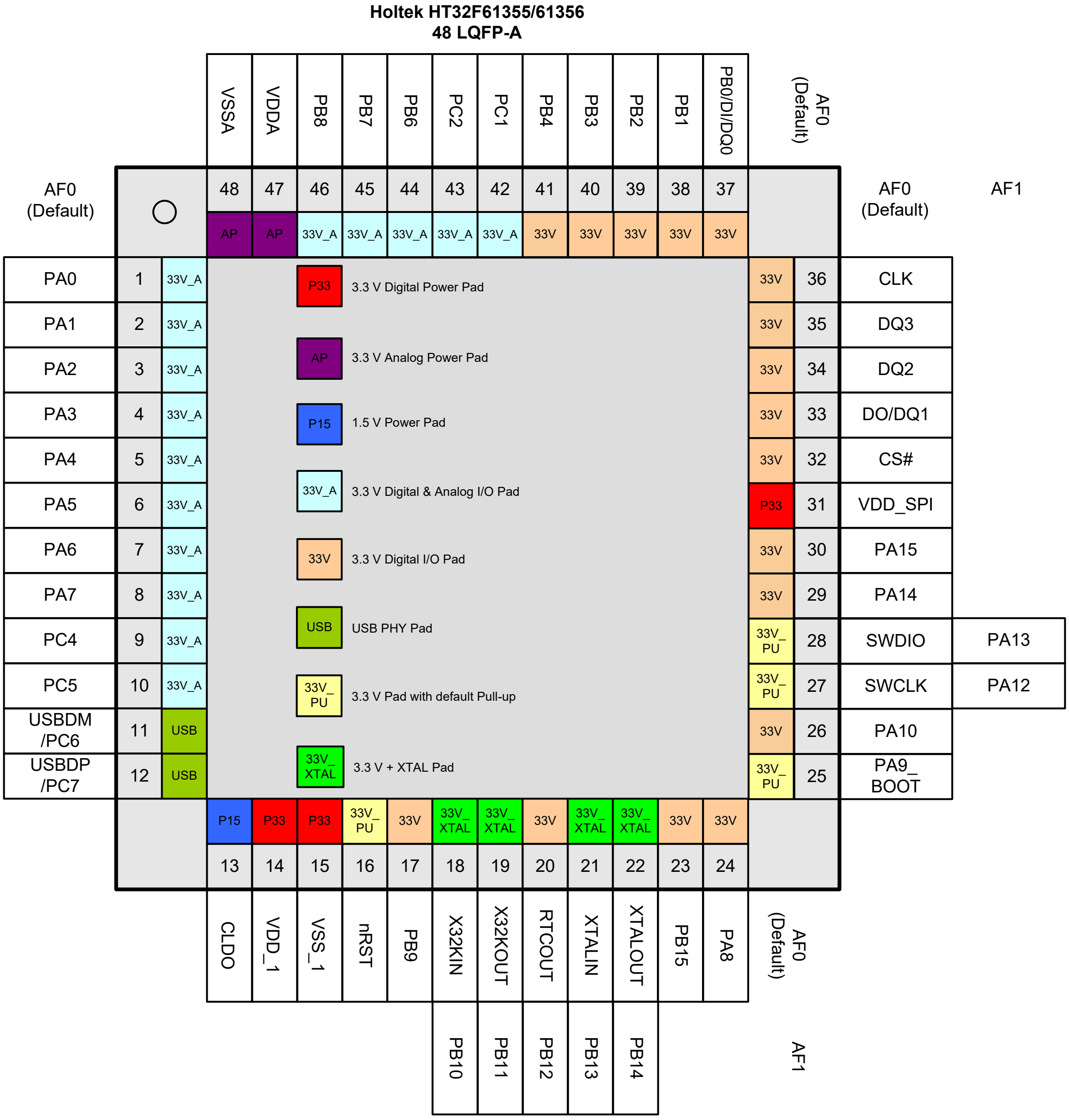


Figure 4. HT32F61355/61356 48-pin LQFP Pin Assignment

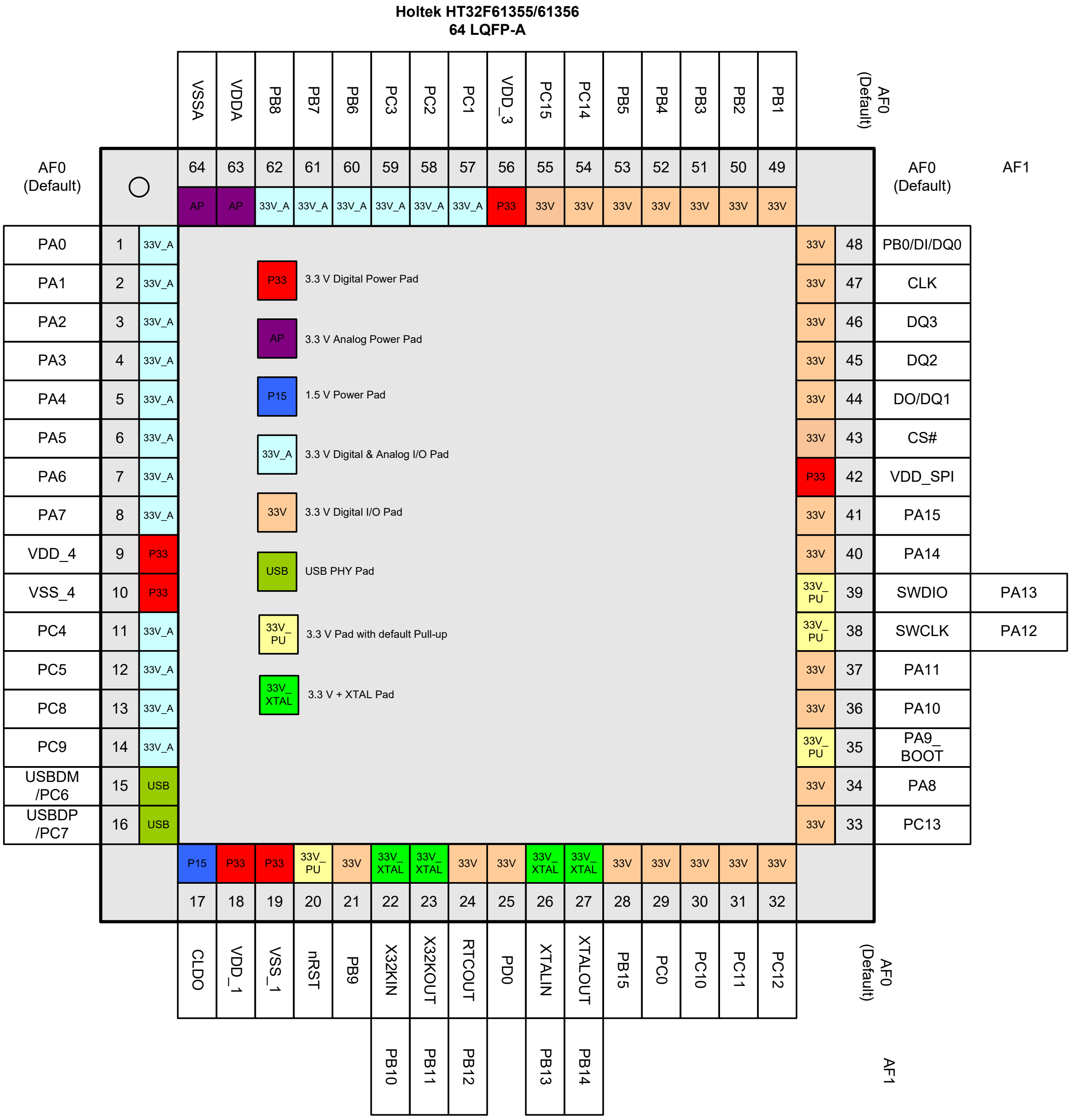


Figure 5. HT32F61355/61356 64-pin LQFP Pin Assignment

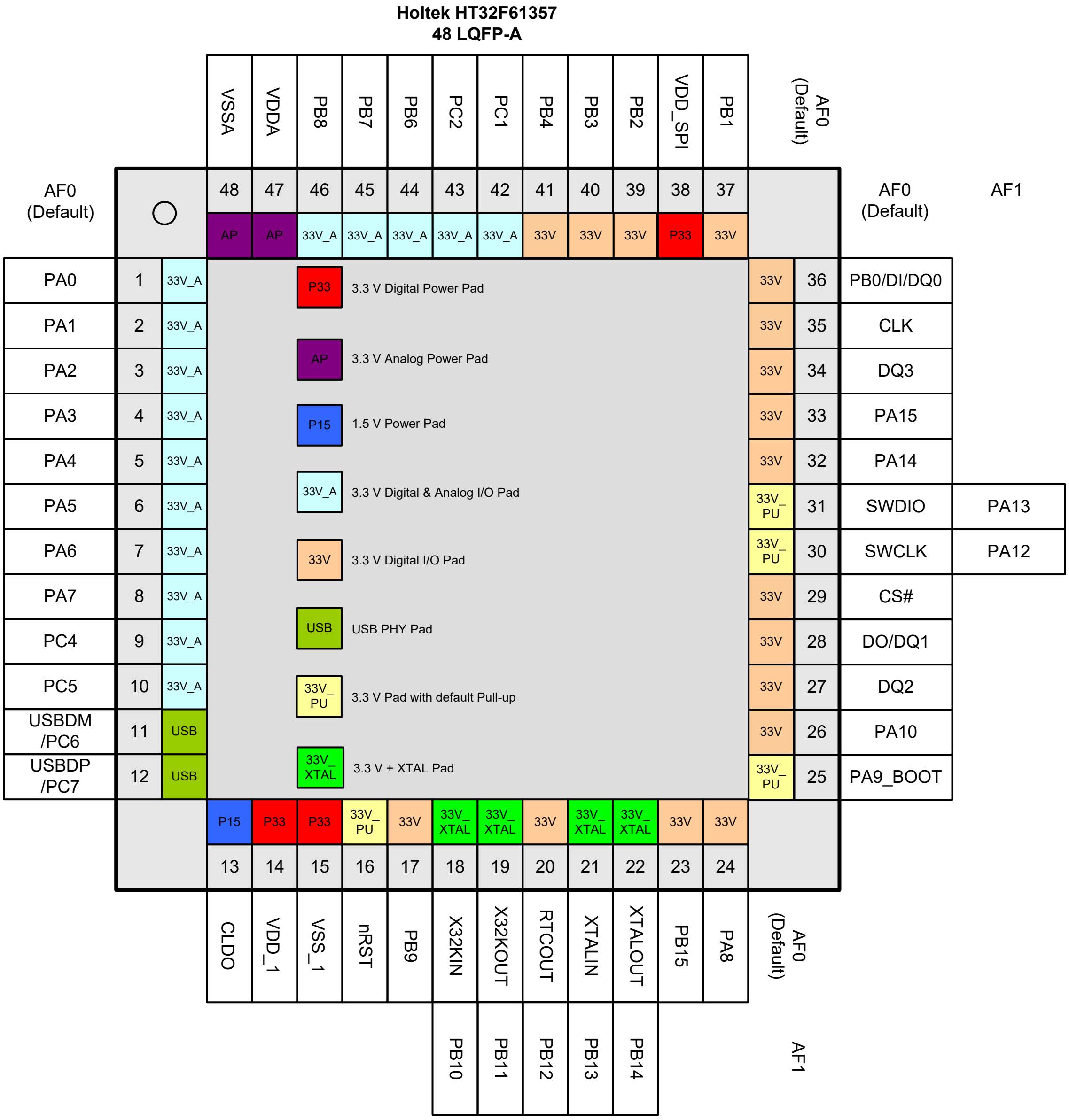


Figure 6. HT32F61357 48-pin LQFP Pin Assignment

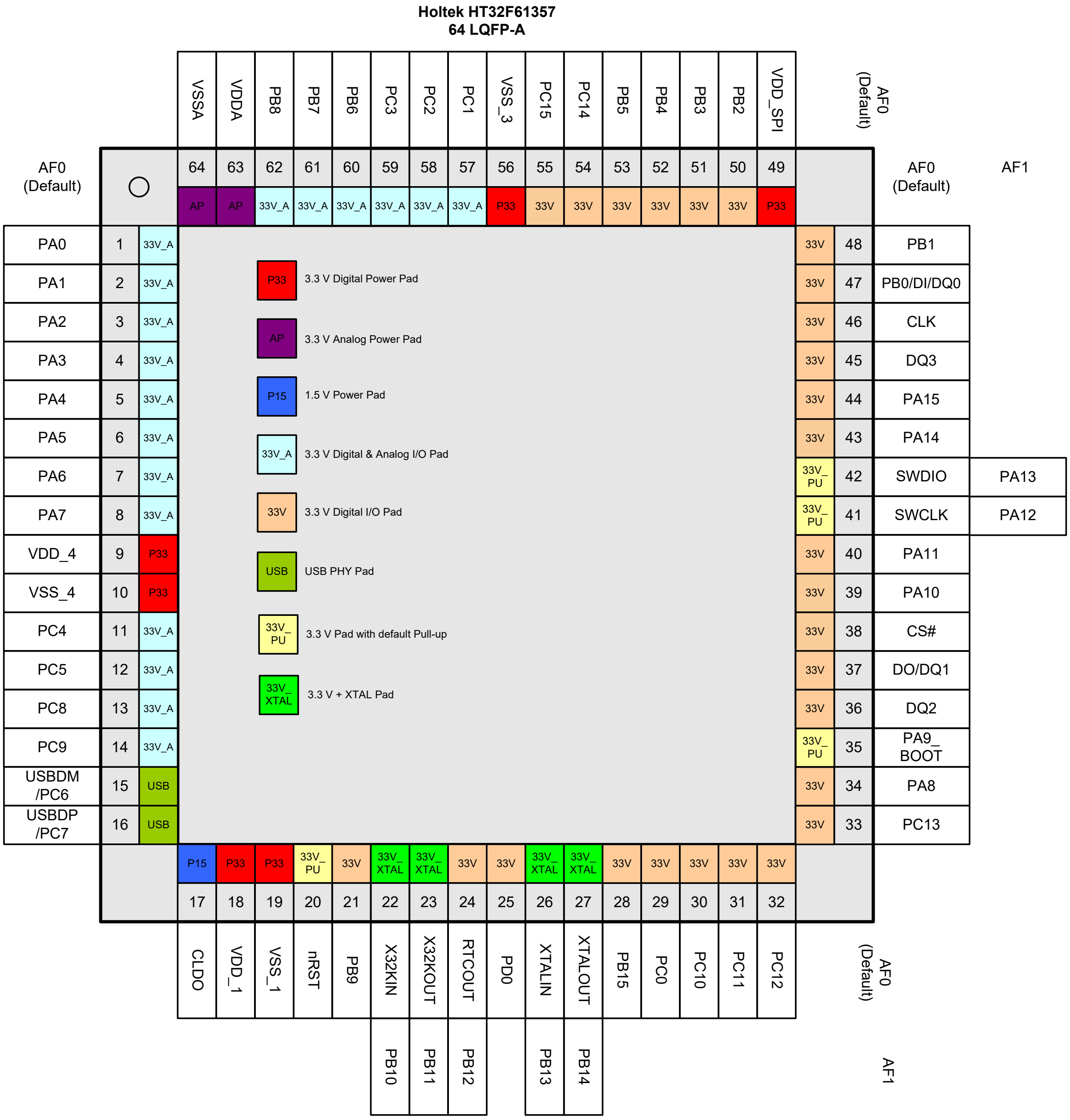


Figure 7. HT32F61357 64-pin LQFP Pin Assignment

Table 3. HT32F61355/HT32F61356 Pin Assignment

Package		Alternate Function Number															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	System Default	GPIO	ADC/ DAC	N/A	GPTM	SPI/ QSPI	USART /UART	I²C	N/A	N/A	I²S	N/A	N/A	SCTM	N/A	System Other
1	1	PA0		ADC_IN4			QSPI_SCK	USR_RTS				I2S_WS					
2	2	PA1		ADC_IN5			QSPI_SIO0	USR_CTS				I2S_BCLK					
3	3	PA2		ADC_IN6			QSPI_SIO1	USR_TX				I2S_SDO					
4	4	PA3		ADC_IN7			QSPI_SEL	USR_RX				I2S_SDI					
5	5	PA4		ADC_IN8		GT_CH0	SPI_SCK		I2C_SCL								
6	6	PA5		ADC_IN9		GT_CH1	SPI_MOSI		I2C_SDA								
7	7	PA6		ADC_IN10		GT_CH2	SPI_MISO	USR_RTS									
8	8	PA7		ADC_IN11		GT_CH3	SPI_SEL	USR_CTS				I2S_MCLK					
9		VDD_4															
10		VSS_4															
11	9	PC4		ADC_IN12		GT_CH0	QSPI_SIO2	UR_TX							SCTM0		
12	10	PC5		ADC_IN13		GT_CH1	QSPI_SIO3	UR_RX							SCTM1		
13		PC8		ADC_IN14		GT_CH2											
14		PC9		ADC_IN15		GT_CH3											
15	11	PC6						USR_TX	I2C_SCL								
15	11	USBDM															
16	12	USBDP															
16	12	PC7						USR_RX	I2C_SDA								
17	13	CLDO															
18	14	VDD_1															
19	15	VSS_1															
20	16	nRST															
21	17	PB9					QSPI_SIO2										
22	18	X32KIN	PB10												SCTM2		
23	19	X32KOUT	PB11												SCTM3		
24	20	RTCOUT	PB12												SCTM0		WAKEUP
25		PD0					QSPI_SIO3		I2C_SDA			I2S_SDI					
26	21	XTALIN	PB13														
27	22	XTALOUT	PB14														
28	23	PB15					SPI_SEL					I2S_MCLK					
29		PC0					SPI_SCK								SCTM3		
30		PC10					QSPI_SEL					I2S_WS					
31		PC11					QSPI_SCK					I2S_BCLK					

Package		Alternate Function Number															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	System Default	GPIO	ADC/ DAC	N/A	GPTM	SPI/ QSPI	USART /UART	I^{2}C	N/A	N/A	I^{2}S	N/A	N/A	SCTM	N/A	System Other
32		PC12					QSPI_SIO0		I2C_SCL			I2S_SDO					
33		PC13					QSPI_SIO1		I2C_SDA			I2S_SDI					
34	24	PA8					QSPI_SIO2	USR_TX				I2S_MCLK			SCTM2		
35	25	PA9_BOOT					SPI_MOSI					I2S_WS			SCTM3		CKOUT
36	26	PA10					QSPI_SIO3	USR_RX									
37		PA11					SPI_MISO					I2S_MCLK			SCTM0		
38	27	SWCLK	PA12														
39	28	SWDIO	PA13														
40	29	PA14					QSPI_SEL										
41	30	PA15					QSPI_SCK								SCTM1		
42	31	VDD_SPI															
43	32	CS#															
44	33	DO/DQ1															
45	34	DQ2															
46	35	DQ3															
47	36	CLK															
48	37	PB0					QSPI_SIO0	USR_TX	I2C_SCL								
48	37	DI/DQ0															
49	38	PB1					QSPI_SIO1	USR_RX	I2C_SDA						SCTM2		
50	39	PB2					SPI_SEL	UR_TX									CKIN (Auto-trim)
51	40	PB3					SPI_SCK	UR_RX							SCTM1		
52	41	PB4					SPI_MOSI								SCTM0		
53		PB5					SPI_MISO										
54		PC14							I2C_SCL								
55		PC15							I2C_SDA								
56		VDD_3															
57	42	PC1		DAC_RCH			QSPI_SEL					I2S_MCLK					
58	43	PC2		DAC_LCH			QSPI_SCK										
59		PC3		ADC_IN0			QSPI_SIO0										
60	44	PB6		ADC_IN1			QSPI_SIO1	UR_TX				I2S_BCLK					
61	45	PB7		ADC_IN2			QSPI_SIO2					I2S_SDO					
62	46	PB8		ADC_IN3			QSPI_SIO3	UR_RX				I2S_SDI					
63	47	VDDA															
64	48	VSSA															

Table 4. HT32F61357 Pin Assignment

Package		Alternate Function Number															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	System Default	GPIO	ADC /DAC	N/A	GPTM	SPI/ QSPI	USART /UART	I²C	N/A	N/A	I²S	N/A	N/A	SCTM	N/A	System Other
1	1	PA0		ADC_IN4			QSPI_SCK	USR_RTS				I2S_WS					
2	2	PA1		ADC_IN5			QSPI_SIO0	USR_CTS				I2S_BCLK					
3	3	PA2		ADC_IN6			QSPI_SIO1	USR_TX				I2S_SDO					
4	4	PA3		ADC_IN7			QSPI_SEL	USR_RX				I2S_SDI					
5	5	PA4		ADC_IN8		GT_CH0	SPI_SCK		I2C_SCL								
6	6	PA5		ADC_IN9		GT_CH1	SPI_MOSI		I2C_SDA								
7	7	PA6		ADC_IN10		GT_CH2	SPI_MISO	USR_RTS									
8	8	PA7		ADC_IN11		GT_CH3	SPI_SEL	USR_CTS				I2S_MCLK					
9		VDD_4															
10		VSS_4															
11	9	PC4		ADC_IN12		GT_CH0	QSPI_SIO2	UR_TX							SCTM0		
12	10	PC5		ADC_IN13		GT_CH1	QSPI_SIO3	UR_RX							SCTM1		
13		PC8		ADC_IN14		GT_CH2											
14		PC9		ADC_IN15		GT_CH3											
15	11	PC6						USR_TX	I2C_SCL								
15	11	USBDM															
16	12	USBDP															
16	12	PC7						USR_RX	I2C_SDA								
17	13	CLDO															
18	14	VDD_1															
19	15	VSS_1															
20	16	nRST															
21	17	PB9					QSPI_SIO2										
22	18	X32KIN	PB10												SCTM2		
23	19	X32KOUT	PB11												SCTM3		
24	20	RTCOUT	PB12												SCTM0		WAKEUP
25		PD0					QSPI_SIO3		I2C_SDA			I2S_SDI					
26	21	XTALIN	PB13														
27	22	XTALOUT	PB14														
28	23	PB15					SPI_SEL					I2S_MCLK					
29		PC0					SPI_SCK								SCTM3		
30		PC10					QSPI_SEL					I2S_WS					
31		PC11					QSPI_SCK					I2S_BCLK					

Package		Alternate Function Number															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	System Default	GPIO	ADC /DAC	N/A	GPTM	SPI/ QSPI	USART /UART	I^2C	N/A	N/A	I^2S	N/A	N/A	SCTM	N/A	System Other
32		PC12					QSPI_SIO0		I2C_SCL			I2S_SDO					
33		PC13					QSPI_SIO1		I2C_SDA			I2S_SDI					
34	24	PA8					QSPI_SIO2	USR_TX				I2S_MCLK			SCTM2		
35	25	PA9_BOOT					SPI_MOSI					I2S_WS			SCTM3		CKOUT
36	27	DQ2															
37	28	DO/DQ1															
38	29	CS#															
39	26	PA10					QSPI_SIO3	USR_RX									
40		PA11					SPI_MISO					I2S_MCLK			SCTM0		
41	30	SWCLK	PA12														
42	31	SWDIO	PA13														
43	32	PA14					QSPI_SEL										
44	33	PA15					QSPI_SCK								SCTM1		
45	34	DQ3															
46	35	CLK															
47	36	PB0					QSPI_SIO0	USR_TX	I2C_SCL								
47	36	DI/DQ0															
48	37	PB1					QSPI_SIO1	USR_RX	I2C_SDA						SCTM2		
49	38	VDD_SPI															
50	39	PB2					SPI_SEL	UR_TX									CKIN (Auto-trim)
51	40	PB3					SPI_SCK	UR_RX							SCTM1		
52	41	PB4					SPI_MOSI								SCTM0		
53		PB5					SPI_MISO										
54		PC14							I2C_SCL								
55		PC15							I2C_SDA								
56		VSS_3															
57	42	PC1		DAC_RCH			QSPI_SEL					I2S_MCLK					
58	43	PC2		DAC_LCH			QSPI_SCK										
59		PC3		ADC_IN0			QSPI_SIO0										
60	44	PB6		ADC_IN1			QSPI_SIO1	UR_TX				I2S_BCLK					
61	45	PB7		ADC_IN2			QSPI_SIO2					I2S_SDO					
62	46	PB8		ADC_IN3			QSPI_SIO3	UR_RX				I2S_SDI					
63	47	VDDA															
64	48	VSSA															

Table 5. HT32F61355/HT32F61356 Pin Description

Pin Number		Pin Name	Type[(1)]	I/O Structure[(2)]	Output Driving	Description
64LQFP	48LQFP					Default Function (AF0)
1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2, this pin provides a USART_TX function in the Boot loader mode.
4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3, this pin provides a USART_RX function in the Boot loader mode.
5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4
6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5
7	7	PA6	AI/O	33V	4/8/12/16 mA	PA6
8	8	PA7	AI/O	33V	4/8/12/16 mA	PA7
9	—	VDD_4	P	—	—	Voltage for digital I/O
10	—	VSS_4	P	—	—	Ground reference for digital I/O
11	9	PC4	AI/O	33V	4/8/12/16 mA	PC4
12	10	PC5	AI/O	33V	4/8/12/16 mA	PC5
13	—	PC8	AI/O	33V	4/8/12/16 mA	PC8
14	—	PC9	AI/O	33V	4/8/12/16 mA	PC9
15	11	PC6	I/O	33V	4/8/12/16 mA	PC6
15	11	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	PC7	I/O	33V	4/8/12/16 mA	PC7
17	13	CLDO	P	—	—	Core power LDO V_{CORE} output. It is must to connect a 1 μF capacitor as close as possible between this pin and VSS_1.
18	14	VDD_1	P	—	—	Voltage for digital I/O
19	15	VSS_1	P	—	—	Ground reference for digital I/O
20	16	nRST	I	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
21	17	PB9	I/O	33V	4/8/12/16 mA	PB9
22	18	PB10	AI/O	33V	< 2 mA	X32KIN
23	19	PB11	AI/O	33V	< 2 mA	X32KOUT
24	20	PB12	I/O	33V	< 2 mA	RTCOUT
25	—	PD0	I/O	33V	4/8/12/16 mA	PD0
26	21	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
27	22	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
28	23	PB15	I/O	33V	4/8/12/16 mA	PB15
29	—	PC0	I/O	33V	4/8/12/16 mA	PC0
30	—	PC10	I/O	33V	4/8/12/16 mA	PC10
31	—	PC11	I/O	33V	4/8/12/16 mA	PC11
32	—	PC12	I/O	33V	4/8/12/16 mA	PC12
33	—	PC13	I/O	33V	4/8/12/16 mA	PC13
34	24	PA8	I/O	33V	4/8/12/16 mA	PA8
35	25	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT

Pin Number		Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64LQFP	48LQFP					Default Function (AF0)
36	26	PA10	I/O	33V	4/8/12/16 mA	PA10
37	—	PA11	I/O	33V	4/8/12/16 mA	PA11
38	27	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
39	28	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
40	29	PA14	I/O	33V	4/8/12/16 mA	PA14
41	30	PA15	I/O	33V	4/8/12/16 mA	PA15
42	31	VDD_SPI	P	—	—	SPI Flash Data Memory Power
43	32	CS#	I/O	33V	—	SPI Flash Data Memory Chip Select
44	33	DO/DQ1	I/O	33V	—	SPI Flash Data Memory Serial Data Output or Data Input / Output 1
45	34	DQ2	I/O	33V	—	SPI Flash Data Memory Serial Data Input / Output 2
46	35	DQ3	I/O	33V	—	SPI Flash Data Memory Serial Data Input / Output 3
47	36	CLK	I/O	33V	—	SPI Flash Data Memory Serial Clock Input
48	37	PB0	I/O	33V	4/8/12/16 mA	PB0
48	37	DI/DQ0	I/O	33V	—	SPI Flash Data Memory Serial Data Input or Data Input / Output 0
49	38	PB1	I/O	33V	4/8/12/16 mA	PB1
50	39	PB2	I/O	33V	4/8/12/16 mA	PB2
51	40	PB3	I/O	33V	4/8/12/16 mA	PB3
52	41	PB4	I/O	33V	4/8/12/16 mA	PB4
53	—	PB5	I/O	33V	4/8/12/16 mA	PB5
54	—	PC14	I/O	33V	4/8/12/16 mA	PC14
55	—	PC15	I/O	33V	4/8/12/16 mA	PC15
56	—	VDD_3	P	—	—	Voltage for digital I/O
57	42	PC1	AI/O	33V	4/8/12/16 mA	PC1
58	43	PC2	AI/O	33V	4/8/12/16 mA	PC2
59	—	PC3	AI/O	33V	4/8/12/16 mA	PC3
60	44	PB6	AI/O	33V	4/8/12/16 mA	PB6
61	45	PB7	AI/O	33V	4/8/12/16 mA	PB7
62	46	PB8	AI/O	33V	4/8/12/16 mA	PB8
63	47	VDDA	P	—	—	Analog voltage for ADC and DAC
64	48	VSSA	P	—	—	Ground reference for the ADC and DAC

Notes: 1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up.
2. 33V = 3.3 V operation I/O type.
3. The GPIOs are in an AF0 state after a V_{CORE} power on reset (POR) except for the RTCOUT pin.
4. In the Boot loader mode, the USART and USB interfaces are available for communication.

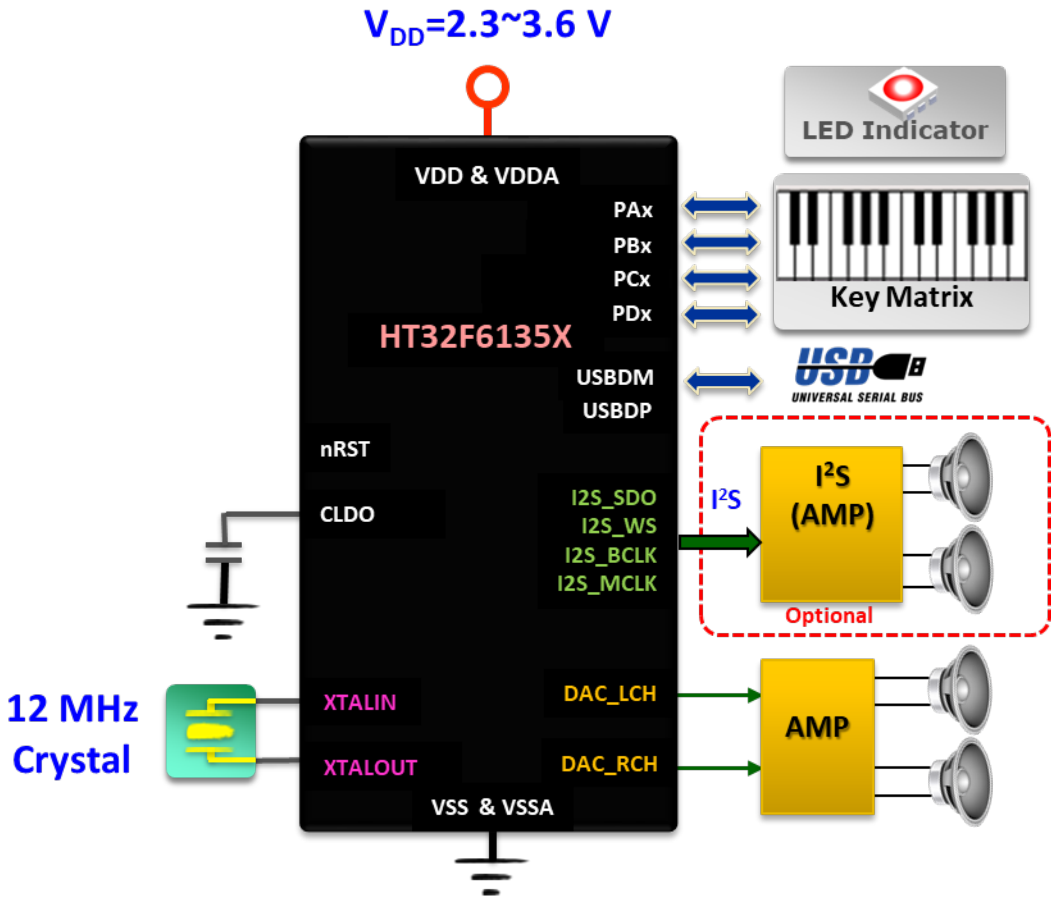
Table 6. HT32F61357 Pin Description

Pin Number		Pin Name	Type[(1)]	I/O Structure[(2)]	Output Driving	Description
64LQFP	48LQFP					Default Function (AF0)
1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2, this pin provides a UART_TX function in the Boot loader mode.
4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3, this pin provides a UART_RX function in the Boot loader mode.
5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4
6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5
7	7	PA6	AI/O	33V	4/8/12/16 mA	PA6
8	8	PA7	AI/O	33V	4/8/12/16 mA	PA7
9	—	VDD_4	P	—	—	Voltage for digital I/O
10	—	VSS_4	P	—	—	Ground reference for digital I/O
11	9	PC4	AI/O	33V	4/8/12/16 mA	PC4
12	10	PC5	AI/O	33V	4/8/12/16 mA	PC5
13	—	PC8	AI/O	33V	4/8/12/16 mA	PC8
14	—	PC9	AI/O	33V	4/8/12/16 mA	PC9
15	11	PC6	I/O	33V	4/8/12/16 mA	PC6
15	11	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	PC7	I/O	33V	4/8/12/16 mA	PC7
17	13	CLDO	P	—	—	Core power LDO V_{CORE} output. It is must to connect a 1 μF capacitor as close as possible between this pin and VSS_1.
18	14	VDD_1	P	—	—	Voltage for digital I/O
19	15	VSS_1	P	—	—	Ground reference for digital I/O
20	16	nRST	I	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
21	17	PB9	I/O	33V	4/8/12/16 mA	PB9
22	18	PB10	AI/O	33V	< 2 mA	X32KIN
23	19	PB11	AI/O	33V	< 2 mA	X32KOUT
24	20	PB12	I/O	33V	< 2 mA	RTCOUT
25	—	PD0	I/O	33V	4/8/12/16 mA	PD0
26	21	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
27	22	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
28	23	PB15	I/O	33V	4/8/12/16 mA	PB15
29	—	PC0	I/O	33V	4/8/12/16 mA	PC0
30	—	PC10	I/O	33V	4/8/12/16 mA	PC10
31	—	PC11	I/O	33V	4/8/12/16 mA	PC11
32	—	PC12	I/O	33V	4/8/12/16 mA	PC12
33	—	PC13	I/O	33V	4/8/12/16 mA	PC13
34	24	PA8	I/O	33V	4/8/12/16 mA	PA8
35	25	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT

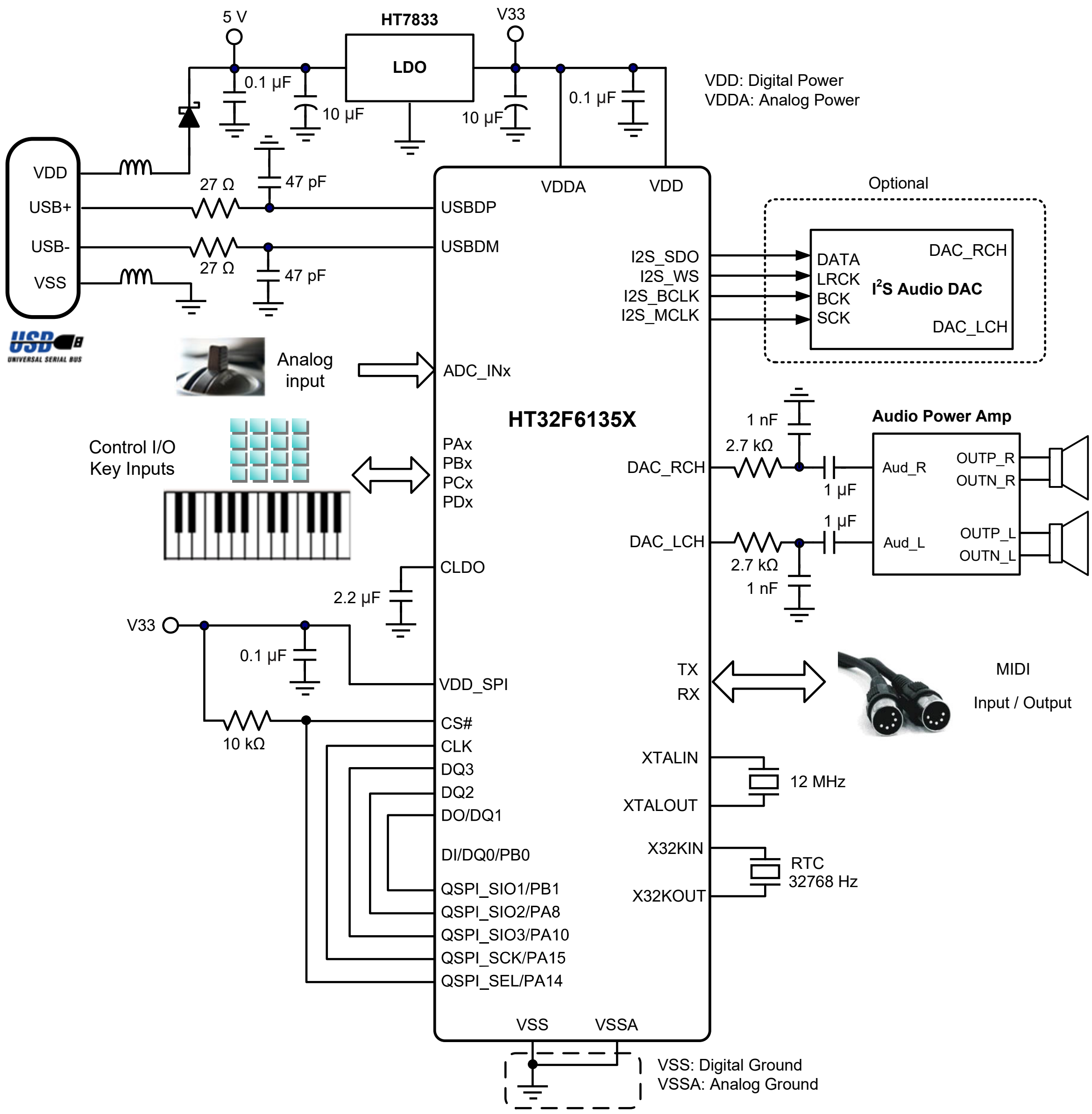
Pin Number		Pin Name	Type[1]	I/O Structure[2]	Output Driving	Description
64LQFP	48LQFP					Default Function (AF0)
36	27	DQ2	I/O	33V	—	SPI Flash Data Memory Serial Data Input / Output 2
37	28	DO/ DQ1	I/O	33V	—	SPI Flash Data Memory Serial Data Output or Data Input / Output 1
38	29	CS#	I/O	33V	—	SPI Flash Data Memory Chip Select
39	26	PA10	I/O	33V	4/8/12/16 mA	PA10
40	—	PA11	I/O	33V	4/8/12/16 mA	PA11
41	30	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
42	31	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
43	32	PA14	I/O	33V	4/8/12/16 mA	PA14
44	33	PA15	I/O	33V	4/8/12/16 mA	PA15
45	34	DQ3	I/O	33V	—	SPI Flash Data Memory Serial Data Input / Output 3
46	35	CLK	I/O	33V	—	SPI Flash Data Memory Serial Clock Input
47	36	PB0	I/O	33V	4/8/12/16 mA	PB0
47	36	DI/DQ0	I/O	33V	—	SPI Flash Data Memory Serial Data Input or Data Input / Output 0
48	37	PB1	I/O	33V	4/8/12/16 mA	PB1
49	38	VDD_SPI	P	—	—	SPI Flash Data Memory Power
50	39	PB2	I/O	33V	4/8/12/16 mA	PB2
51	40	PB3	I/O	33V	4/8/12/16 mA	PB3
52	41	PB4	I/O	33V	4/8/12/16 mA	PB4
53	—	PB5	I/O	33V	4/8/12/16 mA	PB5
54	—	PC14	I/O	33V	4/8/12/16 mA	PC14
55	—	PC15	I/O	33V	4/8/12/16 mA	PC15
56	—	VSS_3	P	—	—	Ground reference for digital I/O
57	42	PC1	AI/O	33V	4/8/12/16 mA	PC1
58	43	PC2	AI/O	33V	4/8/12/16 mA	PC2
59	—	PC3	AI/O	33V	4/8/12/16 mA	PC3
60	44	PB6	AI/O	33V	4/8/12/16 mA	PB6
61	45	PB7	AI/O	33V	4/8/12/16 mA	PB7
62	46	PB8	AI/O	33V	4/8/12/16 mA	PB8
63	47	VDDA	P	—	—	Analog voltage for ADC and DAC
64	48	VSSA	P	—	—	Ground reference for the ADC and DAC

Note: 1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up.
2. 33V = 3.3 V operation I/O type.
3. The GPIOs are in an AF0 state after a V_{CORE} power on reset (POR) except for the RTCOUT pin.
4. In the Boot loader mode, the USART and USB interfaces are available for communication.

7 Application Block



8 Application Circuits



9 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the devices. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the devices. Note that the devices are not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{SS} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	+85	°C
T_{STG}	Storage Temperature Range	-60	+150	°C
T_J	Maximum Junction Temperature	—	+125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 8. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	I/O Operating Voltage	—	2.0	3.3	3.6	V
V_{DDA}	Analog Operating Voltage	—	2.5	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 9. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	$V_{DD} \geq 2.0$ V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, After trimming.	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	—	1	—	μF

Power Consumption

Table 10. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Run Mode)	V_{DD} = 3.3 V, HSE = 8 MHz, PLL = 48 MHz, f_{HCLK} = 48 MHz, f_{PCLK} = 48 MHz	All peripherals enabled	—	18.84	—	mA
			All peripherals disabled	—	9.55	—	
		V_{DD} = 3.3 V, HSE off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz	All peripherals enabled	—	2.383	—	mA
			All peripherals disabled	—	22.0	—	μA
	Supply Current (Sleep Mode)	V_{DD} = 3.3 V, HSE = 8 MHz, PLL = 48 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 48 MHz	All peripherals enabled	—	11.914	—	mA
			All peripherals disabled	—	1.856	—	
	Supply Current (Deep-Sleep1 Mode)	V_{DD} = 3.3 V, All clock off (HSE/PLL/f_{HCLK}), LDO in low power mode, LSI on, RTC on		—	16.44	—	μA
	Supply Current (Deep-Sleep2 Mode)	V_{DD} = 3.3 V, All clock off (HSE/PLL/f_{HCLK}), LDO off, DMOS on, LSI on, RTC on		—	4.686	—	μA
	Supply Current (Power-Down Mode)	V_{DD} = 3.3 V, LDO off, DMOS off, LSE on, LSI on, RTC on		—	2.636	—	μA
		V_{DD} = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC off		—	1.236	—	

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real-time clock.
4. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 11. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power-on Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ +85 °C	1.66	1.79	1.90	V
V_{PDR}	Power-down Reset Threshold (Falling Voltage on V_{DD})		1.49	1.64	1.78	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 12. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	T_A = -40 °C ~ 85 °C, After factory-trimmed V_{DD} Falling edge)		2.02	2.1	2.18	V
V_{LVD}	Voltage of Low Voltage Detection	T_A = -40 °C ~ 85 °C (V_{DD} Falling edge)	LVDS = 000	2.17	2.25	2.33	V
			LVDS = 001	2.32	2.4	2.48	
			LVDS = 010	2.47	2.55	2.63	
			LVDS = 011	2.62	2.7	2.78	
			LVDS = 100	2.77	2.85	2.93	
			LVDS = 101	2.92	3.0	3.08	
			LVDS = 110	3.07	3.15	3.23	
			LVDS = 111	3.22	3.3	3.38	
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	—	—	μs
I_{DDLVD}	Operation Current[2]	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register

External Clock Characteristics

Table 13. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	2.0	—	3.6	V
f_{HSE}	High Speed External Oscillator Frequency (HSE)	—	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT Pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 0	—	—	160	Ω
		V_{DD} = 2.4 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 1				
D_{HSE}	HSE Oscillator Duty cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3 V	—	—	4	ms

Table 14. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{BAK}	Operation Range	—	2.0	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{BAK} = 2.0 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{BAK} = 3.3 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{BAK} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L ≥ 7 pF, V_{BAK} = 2.0 V ~ 2.7 V, T_A = -40 °C ~ +85 °C	—	3.3	6.3	µA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L < 7 pF, V_{BAK} = 2.0 V ~ 3.6 V, T_A = -40 °C ~ +85 °C	—	1.8	3.3	µA
	Power Down Current	—	—	—	0.01	µA
t_{suLSE}	Startup Time (Low Current Mode)	f_{CK_LSI} = 32.768 kHz, V_{BAK} = 2.0 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout:

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Table 15. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	2.0	—	3.6	V
f_{HSI}	HSI Frequency	V_{DD} = 3.3 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 3.6 V, T_A = -40 °C ~ +85 °C	-3	—	3	%
		V_{DD} = 2.0 V ~ 3.6 V T_A = -40 °C ~ +85 °C	-4	—	4	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	µA
	Power Down Current		—	—	0.05	µA
t_{suHSI}	Startup Time	f_{HSI} = 8 MHz	—	—	10	µs

Table 16. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	V_{DD} = 3.3 V, T_A = -40 °C ~ +85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V, T_A = 25 °C	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V, T_A = 25 °C	—	0.4	0.8	µA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V, T_A = 25 °C	—	—	100	µs

PLL Characteristics

Table 17. PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	PLL Output Clock	—	16	—	48	MHz
t_{LOCK}	PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 18. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before Failure. (Endurance)	T_A = -40 °C ~ +85 °C	10	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ +85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ +85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ +85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ +85 °C	10	—	—	ms

I/O Port Characteristics

Table 19. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V I/O	V_I = V_{SS}, On-chip pull-up resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	3.3 V I/O	V_I = V_{DD}, On-chip pull-down resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	3.3 V I/O		- 0.5	—	V_{DD} × 0.35	V
		Reset pin		- 0.5	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V_{OL} = 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OL} = 0.4 V		8	—	—	
		3.3 V I/O 12 mA drive, V_{OL} = 0.4 V		12	—	—	
		3.3 V I/O 16 mA drive, V_{OL} = 0.4 V		16	—	—	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.4 V	4	—	—	mA
		3.3 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.4 V	8	—	—	
		3.3 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.4 V	12	—	—	
		3.3 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.4 V	16	—	—	
V_{OL}	Low Level Output Voltage	3.3 V 4 mA drive I/O, I_{OL} = 4 mA	—	—	0.4	V
		3.3 V 8 mA drive I/O, I_{OL} = 8 mA	—	—	0.4	
		3.3 V 12 mA drive I/O, I_{OL} = 12 mA	—	—	0.4	
		3.3 V 16 mA drive I/O, I_{OL} = 16 mA	—	—	0.4	
V_{OH}	High Level Output Voltage	3.3 V 4 mA drive I/O, I_{OH} = 4 mA	V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive I/O, I_{OH} = 8 mA	V_{DD} - 0.4	—	—	
		3.3 V 12 mA drive I/O, I_{OH}= 12 mA	V_{DD} - 0.4	—	—	
		3.3 V 16 mA drive I/O, I_{OH} = 16 mA	V_{DD} - 0.4	—	—	
R_{PU}	Internal Pull-up Resistor	3.3 V I/O	—	46	—	kΩ
R_{PD}	Internal Pull-down Resistor	3.3 V I/O	—	46	—	kΩ

ADC Characteristics

Table 20. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.7	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V, 1 Msps	—	0.9	1.0	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.1	µA
f_{ADC}	A/D Converter Clock	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	Msps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup up Time	—	—	—	1	µs
N	Resolution	—	—	12	—	bit
INL	Integral Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.
3. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the VDDA supply power of the A/D Converter has to be equal to the VDD supply power of the MCU in the application circuit.

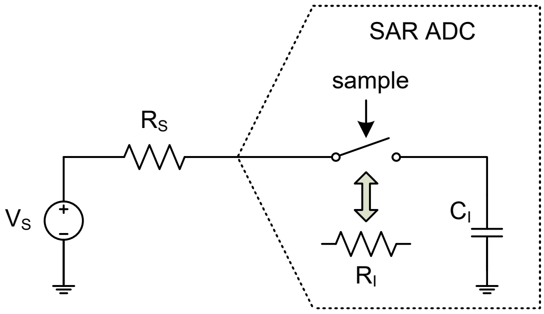


Figure 8. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

SCTM/GPTM Characteristics

Table 21. SCTM/GPTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM / SCTM	—	—	—	48	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency On Channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bit

I²C Characteristics

Table 22. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time	0	—	0	—	0	—	ns
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: SEQFILTER = 01 and COMBFILTEREN is disabled.

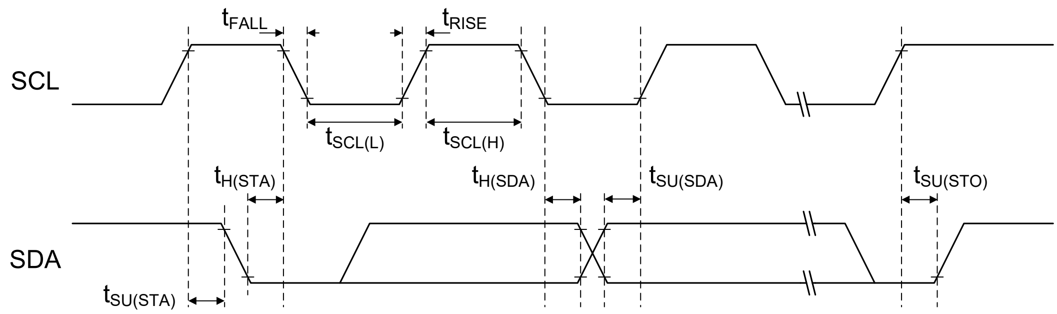


Figure 9. I²C Timing Diagrams

I²S Characteristics

Table 23. I²S Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I²S Master Mode						
$t_{WSD(MO)}$	WS Output to BCLK Delay	—	—	TBD	—	ns
$t_{DOD(MO)}$	Data Output to BCLK Delay	—	—	TBD	—	ns
$t_{DIS(MI)}$	Data Input Setup Time	—	—	TBD	—	ns
$t_{DIH(MI)}$	Data Input Hold Time	—	—	TBD	—	ns
I²S Slave Mode						
$t_{BCH(SI)}$	BCLK High Pulse Width	—	—	TBD	—	ns
$t_{BCL(SI)}$	BCLK Low Pulse Width	—	—	TBD	—	ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{WSS(SI)}$	WS Input Setup Time	—	—	TBD	—	ns
$t_{DOD(SO)}$	Data Output to BCLK Delay	—	—	TBD	—	ns
$t_{DIS(SI)}$	Data Input Setup Time	—	—	TBD	—	ns
$t_{DIH(SI)}$	Data Input Hold Time	—	—	TBD	—	ns

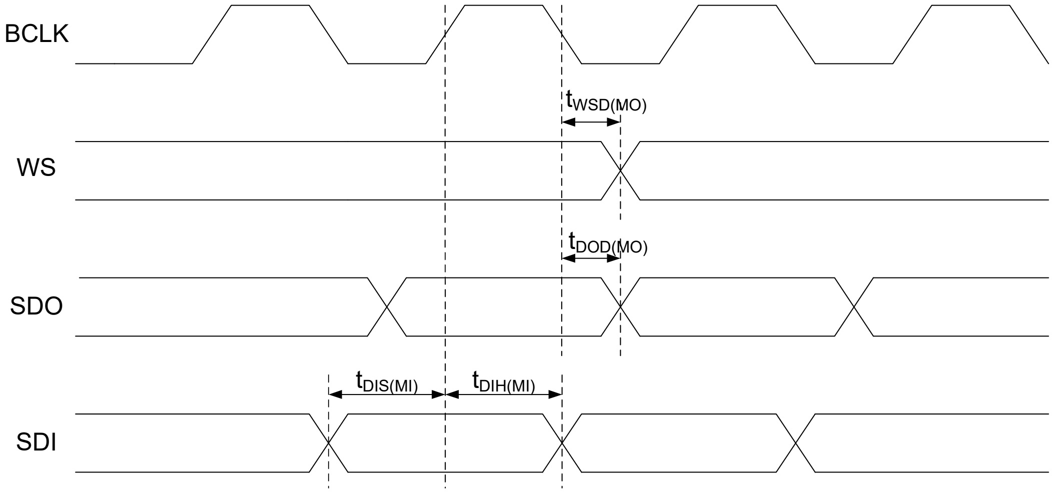


Figure 10. Timing of I²S Master Mode

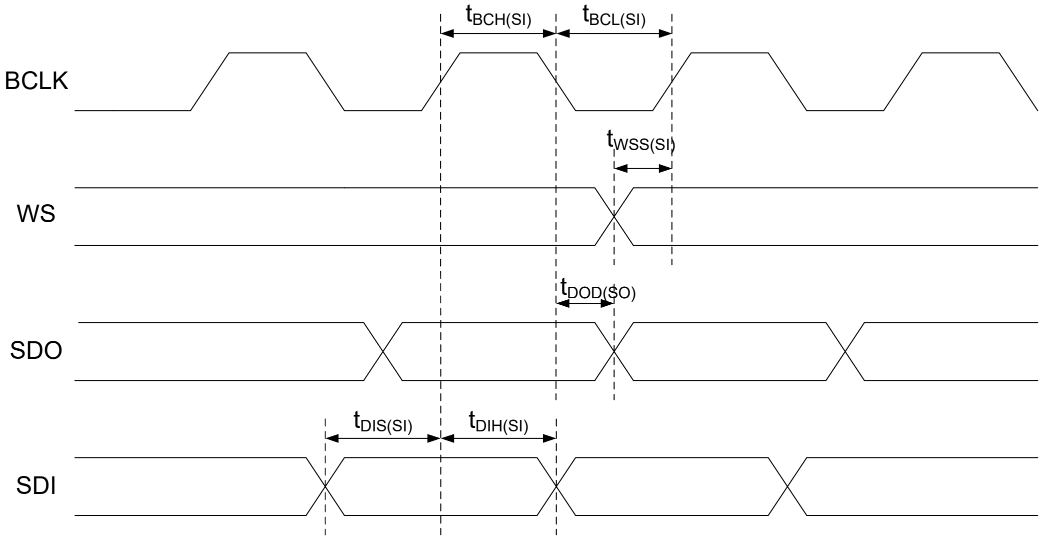


Figure 11. Timing of I²S Slave Mode

SPI Characteristics

Table 24. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK} ($1/t_{SCK}$)	SPI Master Output SCK Clock Frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK} ($1/t_{SCK}$)	SPI Slave Input SCK Clock Frequency	Slave Mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3 \times t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2 \times t_{PCLK}$	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3 \times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: $t_{SCK} = 1/f_{SCK}$; $t_{PCLK} = 1/f_{PCLK}$. SPI output (input) clock frequency f_{SCK}; SPI peripheral clock frequency f_{PCLK}.

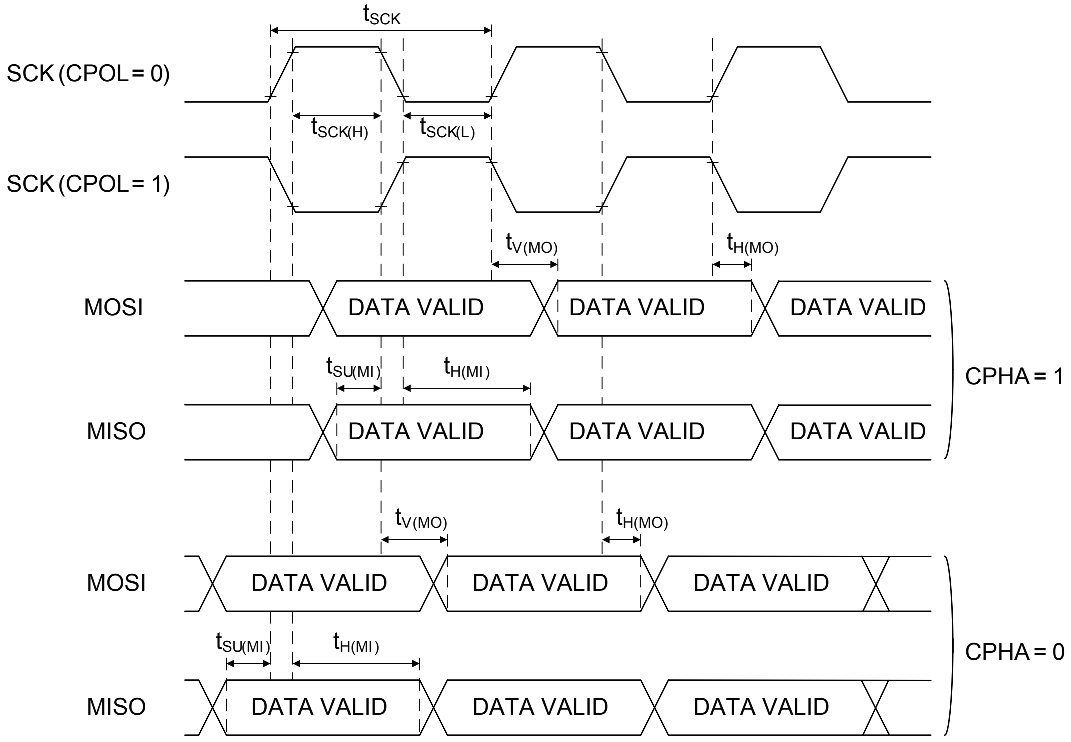


Figure 12. SPI Timing Diagrams – SPI Master Mode

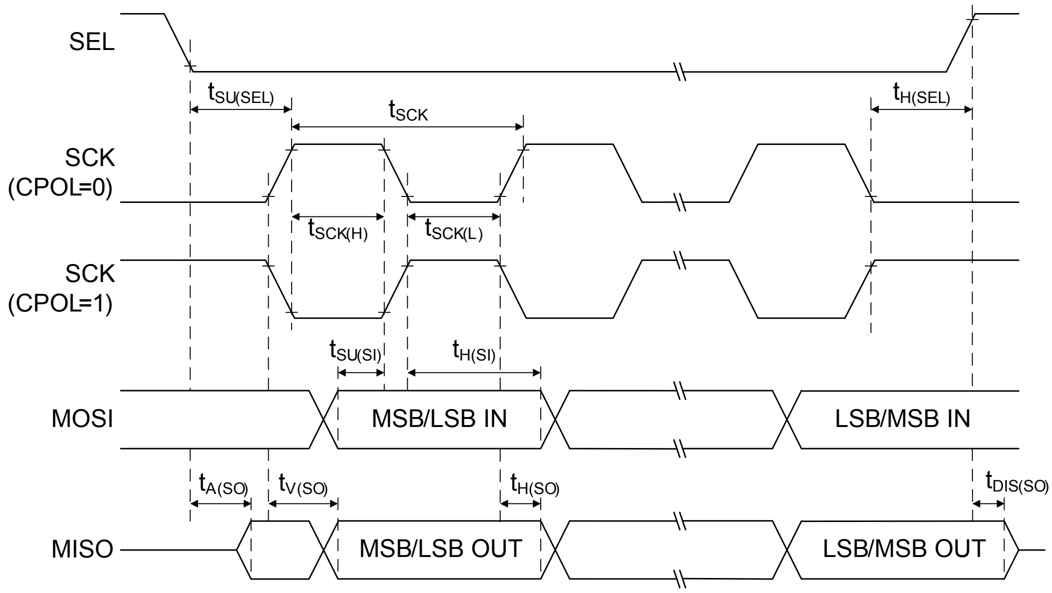


Figure 13. SPI Timing Diagrams – SPI Slave Mode with CPHA = 1

QSPI Characteristics

Table 25. QSPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
QSPI Master Mode						
f_{SCK} $(1/t_{SCK})$	QSPI Master Output SCK Clock Frequency	Master mode QSPI peripheral clock frequency f_{HCLK}	—	—	$f_{HCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
QSPI Slave Mode (1-bit Serial Mode Only)						
f_{SCK} $(1/t_{SCK})$	QSPI Slave Input SCK Clock Frequency	Slave mode QSPI peripheral clock frequency f_{HCLK}	—	—	$f_{HCLK}/3$	MHz
$Duty_{SCK}$	QSPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3 \times t_{HCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2 \times t_{HCLK}$	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3 \times t_{HCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: $t_{SCK} = 1/f_{SCK}$; $t_{HCLK} = 1/f_{HCLK}$. QSPI output (input) clock frequency f_{SCK}; QSPI peripheral clock frequency f_{HCLK}.

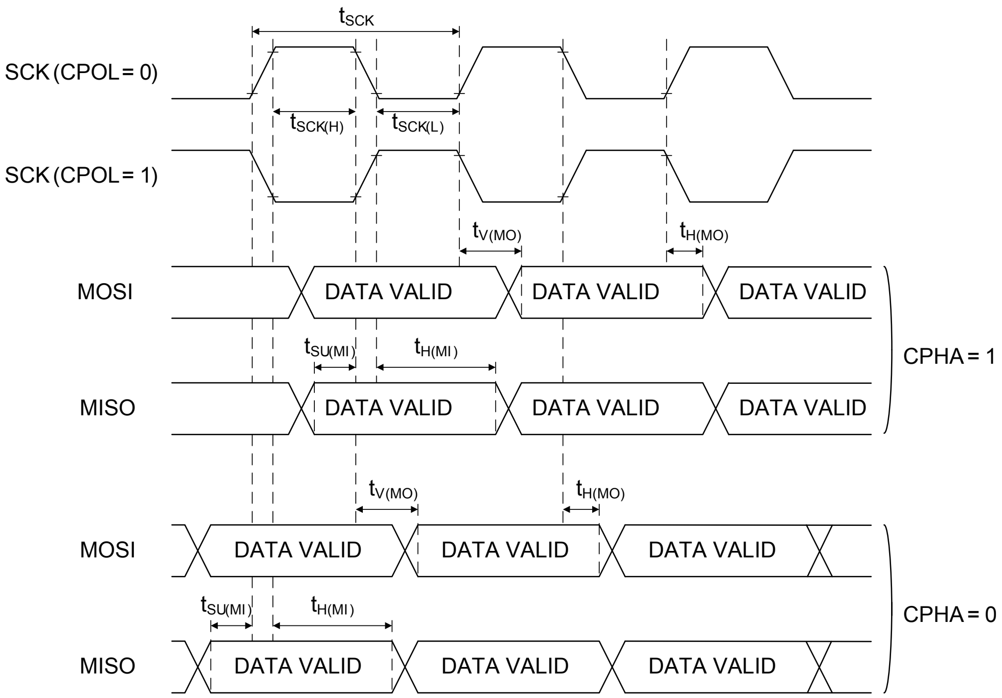


Figure 14. QSPI Timing Diagrams – QSPI Master Mode (1-bit Serial Mode, DUALEN = 0, QUADEN = 0)

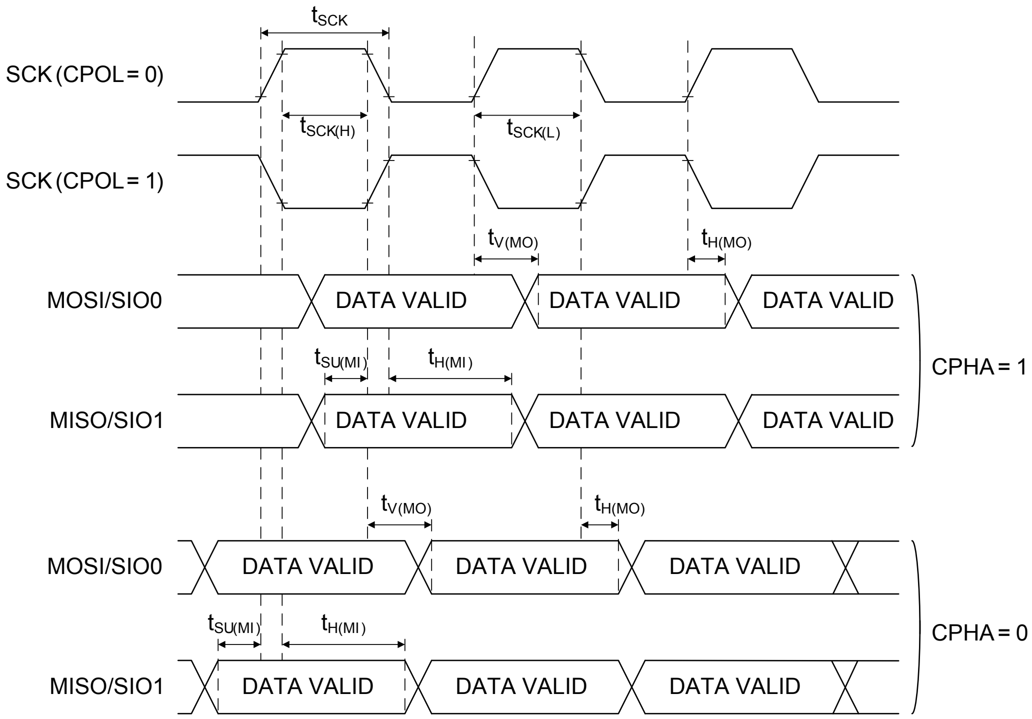


Figure 15. QSPI Timing Diagrams – QSPI Master Mode (Dual Mode, DUALEN = 1)

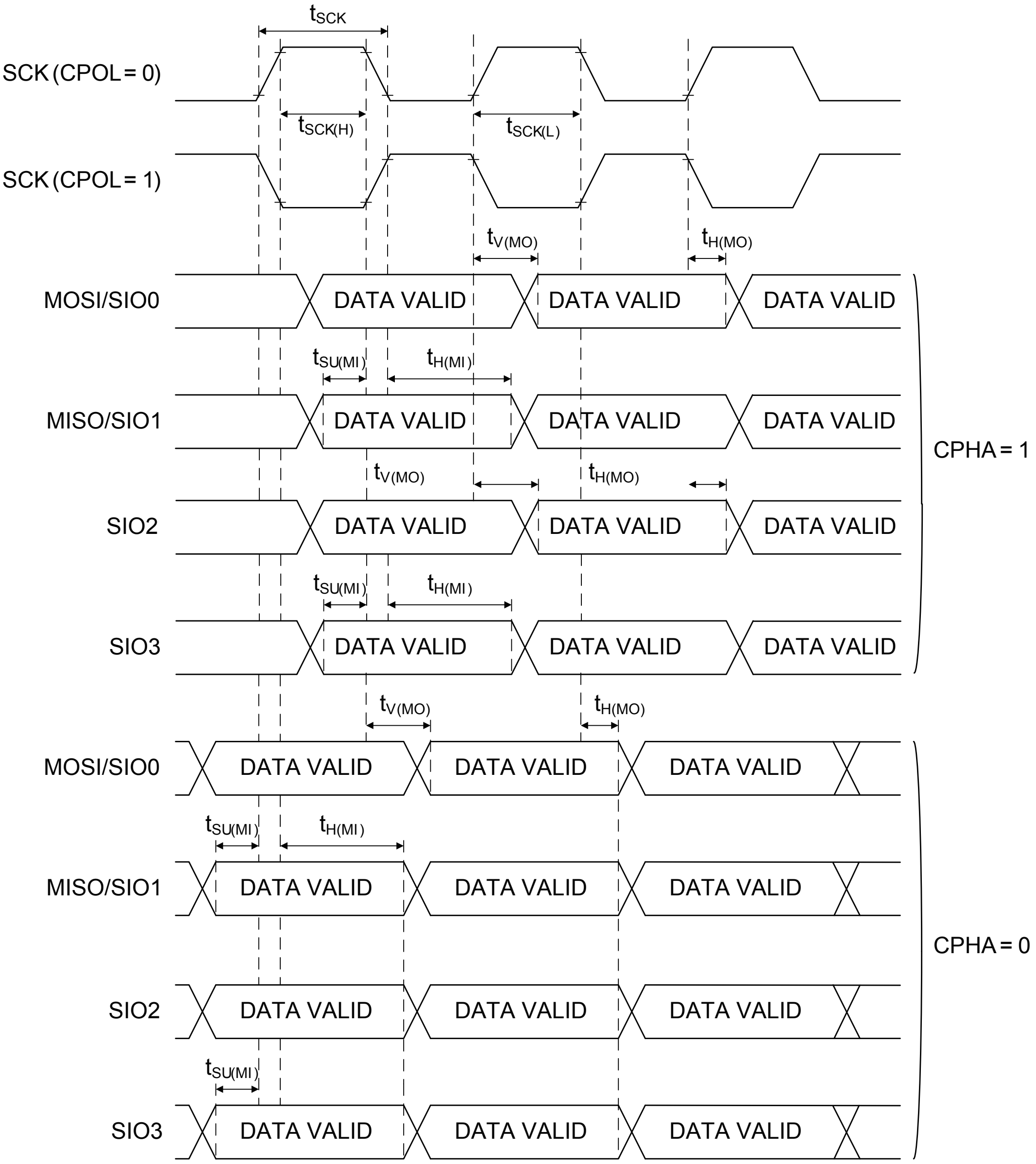


Figure 16. QSPI Timing Diagrams – QSPI Master Mode (Quad Mode, QUADEN = 1)

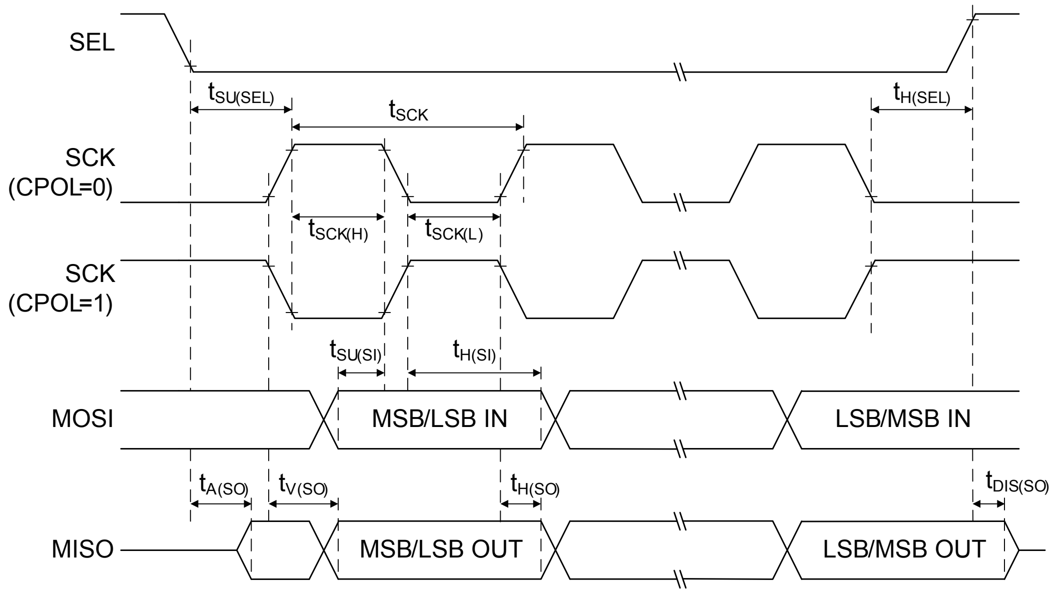


Figure 17. QSPI Timing Diagrams – QSPI Slave Mode with CPHA = 1 (1-bit Serial Mode)

USB Characteristics

The USB interface is USB-IF certified – Full Speed.

Table 26. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	USB Operating Voltage	—	3.0	—	3.6	V
V_{DI}	Differential Input Sensitivity	|USBDP - USBDM|	0.2	—	—	V
V_{CM}	Common Mode Voltage Range	—	0.8	—	2.5	V
V_{SE}	Single-ended Receiver Threshold	—	0.8	—	2.0	V
V_{OL}	Pad Output Low Voltage	R_L of 1.5 kΩ to V_{DD}	0	—	0.3	V
V_{OH}	Pad Output High Voltage		2.8	—	3.6	V
V_{CRS}	Differential Output Signal Cross-point Voltage		1.3	—	2.0	V
Z_{DRV}	Driver Output Resistance	—	—	10	—	Ω
C_{IN}	Transceiver Pad Capacitance	—	—	—	20	pF

Note: 1. Data based on characterization results only, not tested in production.

2. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which will experience degradation in the 2.7-to-3.0 V V_{DD} voltage range.

3. R_L is the load connected to the USB driver USBDP.

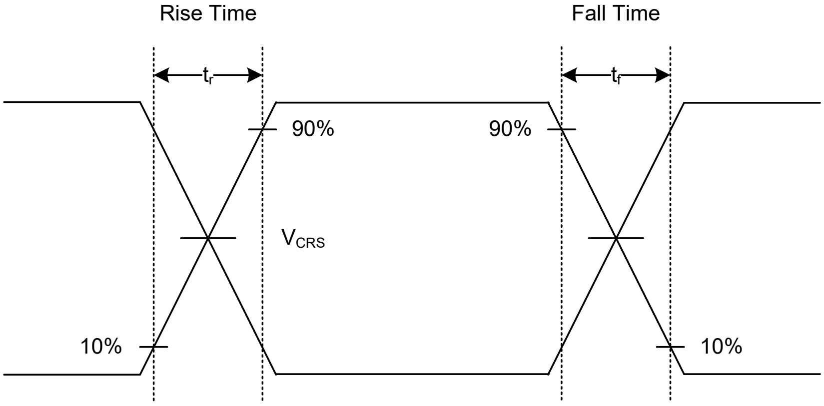


Figure 18. USB Signal Rise Time and Fall Time and Cross-Point Voltage (V_{CRS}) Definition

Table 27. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_r	Rise Time	C_L = 50 pF	4	—	20	ns
t_f	Fall Time	C_L = 50 pF	4	—	20	ns
$t_{r/f}$	Rise Time / Fall Time Matching	$t_{r/f} = t_r / t_f$	90	—	110	%

Audio D/A Converter Characteristics

Table 28. Audio D/A Converter Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.2	—	3.6	V
I_{DD}	Operating Current	V_{DD} = 3 V	—	3	—	mA
THD+N	Total Harmonic Distortion + Noise (Note)	V_{DD} = 3 V, 10 kΩ load	—	-50	—	dB

Note: Sine wave input @1 kHz, –6 dB.

SPI Flash Data Memory DC Characteristics

Table 29. SPI Flash Data Memory DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	—	2.3	—	3.6	V
I_{LI}	Input Leakage Current	—	—	1	±2	μA
I_{LO}	Output Leakage Current	—	—	1	±2	μA
I_{STB}	Standby Current	CS# = V_{CC}, V_{IN} = V_{DD} or V_{CC}	—	—	2	μA
I_{CC1}	Operating Current (Read)	CLK = 0.1 V_{CC} / 0.9 V_{DD} at 48 MHz, DQ = open	—	6	14	mA
		CLK = 0.1 V_{CC} / 0.9 V_{DD} at 48 MHz, Quad Output Read, DQ = open	—	8.5	20	mA
I_{CC2}	Operating Current (Page Program)	CS# = V_{DD}	—	9	30	mA
V_{IL}	Input Low Voltage	—	-0.5	—	0.2 × V_{DD}	V
V_{IH}	Input High Voltage	—	0.7 × V_{DD}	—	V_{DD} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 μA, V_{DD} = V_{DD} Min.	—	—	0.3	V
V_{OL}	Output High Voltage	I_{OH} = -100 μA, V_{DD} = V_{DD} Min.	V_{DD} - 0.2	—	—	V

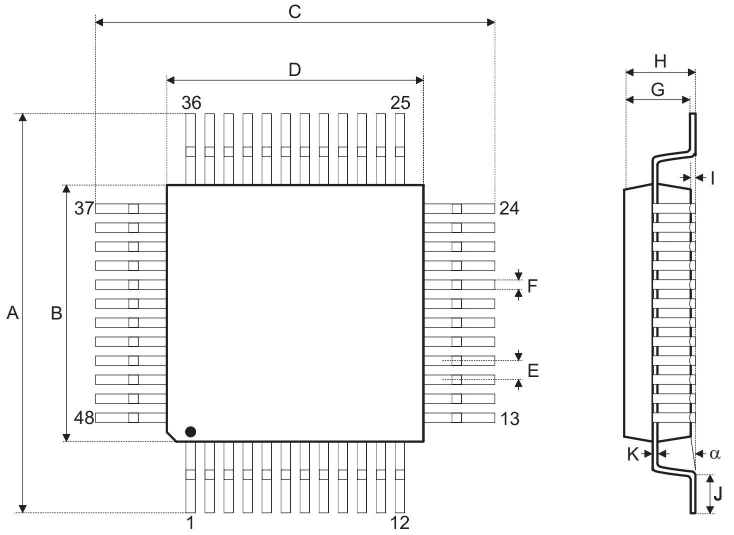
10 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

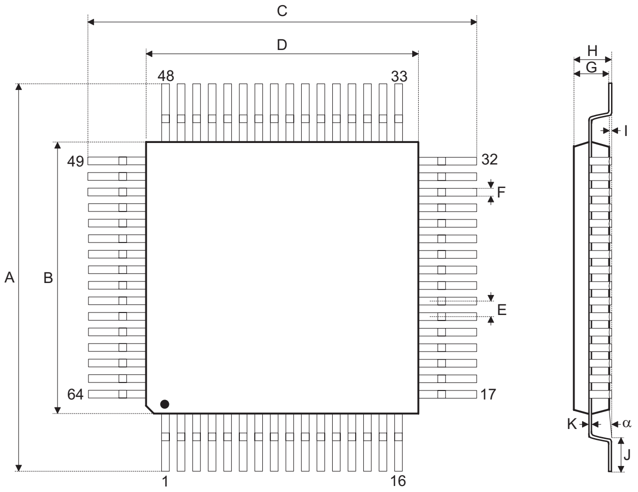
48-pin LQFP (7 mm × 7 mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.020 BSC	
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.50 BSC	
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

64-pin LQFP (7 mm × 7 mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.016 BSC	
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.40 BSC	
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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