HT32F61730
Datasheet

32-Bit Arm® Cortex®-M0+ BMS Microcontroller,
32 KB Flash and 2 KB SRAM with
Individual Cell Voltage Monitor, 500 ksps ADC,
UART, SPI, I²C, SCTM, BFTM, LEDC, RTC and WDT

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1 General Description

The Holtek HT32F61730 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The device operates at a frequency of 16 MHz to obtain maximum efficiency. It provides 32 KB of embedded Flash memory for code/data storage and 2 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, UART, SPI, SCTM, BFTM, LEDC, RTC, WDT and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The device also has an individual cell voltage monitor module, a high accuracy voltage regulator, two discharge N-type MOSFET gate drivers and a charge N-type MOSFET gate driver, which is suitable for 3 to 8 rechargeable lithium batteries. The cell voltage monitor is designed to monitor each battery cell voltage individually and outputs the divide-by-2 voltage to the analog multiplexer with ±7.5 mV accuracy when analog output is 2.1 V. After being selected by an analog multiplexer, the output voltage is directly connected to the internal A/D converter for measurement. The integrated high accuracy V_{REFO} is 2.5 V (maximum drift ±15 mV). The internal gate drivers can directly drive external power N-type MOSFETs to control charge and discharge. It also has functions of differential amplifier to detect charge/discharge current, hardware discharge short-current protection and overtemperature protection and so on. The integrated battery balance circuitry provides a cell balance current without the need of external transistors.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as handheld measurement instruments, electric power tools, handheld hair dryers, handheld vacuum cleaners in addition to many others.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 16 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- 32 KB on-chip Flash memory for instruction/data and option byte storage
- 2 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions for the embedded on-chip Flash Memory. The word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power On Reset / Power Down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 16 MHz RC oscillator trimmed to ±1 % accuracy at 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE, LSI or LSE. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- Single V_{DD} power supply: 2.5 V ~ 5.5 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- Two power domains: V_{DD} and V_{CORE} power domains
- Three power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt / Event Controller – EXTI

- Up to 8 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 8 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 500 ksps conversion rate
- Up to 7 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are multiplexed channels, which include 7 external analog signal channels and 2 internal channels which can be measured. There are two conversion modes to convert an analog signal to digital data. The A/D conversion can be operated in one shot and continuous conversion mode.

The internal voltage reference generator (VREF) which can provide a stable ADC reference positive voltage (ADCREFP) and the Band gap of VREF is internally connected to the ADC internal input channel. The precise voltage of the V_{REF} is individually measured for each part by Holtek during production test.

I/O Ports – GPIO

- Up to 23 GPIOs
- Port A, B, C are mapped to 8-line EXTI interrupts
- Almost all I/O pins have configurable output driving current

There are up to 23 General Purpose I/O pins, which for the implementation of logic input / output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Single-Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 8-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 256 to generate the counter clock frequency
- One input Capture function
- Two compare Match Output
- PWM waveform generation with Edge-aligned counting Mode
- Single Pulse Mode Output

The Single Channel Timer Module, SCTM, consists of one 16-bit up-counter, one 16-bit Capture / Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM outputs.

Basic Function Timer – BFTM

- 16-bit compare match up-counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 16-bit up-counting counter designed to measure time intervals and generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes, repetitive and one shot modes. In the repetitive mode, the counter will restart at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit down-counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog Timer configuration.

Real-Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, circuitry includes the APB interface, a 24-bit up-counter, a control register, a prescaler, a compare register and a status register. The RTC circuits are located in the V_{CORE} power domain. The RTC counter is used as a wakeup timer to generate a system resume or interrupt signal from the MCU power saving mode.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Supports 7-bit addressing mode and general call addressing
- Supports two 7-bit slave addresses

The I²C module is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- Programmable data frame length up to 8 bits
- FIFO Depth: 4 levels

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamlined data

bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

LED Controller – LEDC

- Supports 8-segment digital displays up to 4
- Supports 8-segment digital displays with common anode or common cathode
- Support frame interrupt
- Three clock sources: LSI, LSE and PCLK
- The LED light on/off times can be controlled using the dead time setting

The LED controller is used to drive 8-segment digital displays. This device can driver 8-segment digital displays up to 4. Users can flexibly configure the pin position and number of the COMs according to the digital displays in the application. In a complete frame period, the enabled COMs will be scanned from the lower to the higher. Taking an example of where four 8-segment LEDs are used and where COM0, COM1, COM2 and COM3 are enabled. Here COM0, COM1, COM2 and the COM3 will be scanned successively in this sequence within a complete frame period. The scanning time of each COM port is equal to 1/4 frame, which is subdivided into the dead time duty and the COM duty. Users can adjust the dead time duty to change the LED brightness.

Individual Cell Voltage Monitor

- Integrated voltage regulator with 5 V / 50 mA and ±1 % accuracy
- Individual cell voltage monitor outputs 1/2 of battery cell voltage, when the analog output is 2.1 V, it has an accuracy of ±7.5 mV
- At T_A = -40 °C ~ 85 °C, 2.5 V reference voltage output with a maximum variation of 15 mV in temperature drift
- Internal cell balance switches
- Two Discharge N-type MOSFET gate drivers
- Single Charge N-type MOSFET gate driver
- Charge/Discharge differential OPA current monitor
  - IMON outputs amplified ISP-ISN differential voltage
  - Voltage amplifying rate selection: 10 / 50

- Discharge short-current detection
  - Detection threshold voltage selection: 50 mV / 100 mV / 150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV
  - Detection debounce time selection: 0 μs ~ 992 μs, 32 sections, 32 μs per section
- Integrated Over-temperature protection selection: 85 °C / 100 °C / 125 °C / 150 °C
- Sleep mode with 0.1 μA ultra-low standby current
- Two High-voltage wake-up functions

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 64-pin LQFP package
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F61730
Main Flash (KB)		31
Option Bytes Flash (KB)		1
SRAM (KB)		2
Timers	SCTM	3
	BFTM	1
	WDT	1
	RTC	1
Communication	SPI	1
	UART	2
	I^2C	1
EXTI		8
12-bit ADC		1
Number of channels		7 Externa Channels
GPIO		Up to 23
LEDC		4 × 8-segment
Individual Cell Voltage Monitor		1
CPU frequency		Up to 16 MHz
Operating voltage		2.5 V ~ 5.5 V
Operating temperature		-40 °C ~ 85 °C
Package		64-pin LQFP

Note: The functions listed here, except the Individual Cell Voltage Monitor, are compatible with the HT32F50030 device. Refer to the HT32F50020 / HT32F50030 user manual for detailed functional description.

Block Diagram

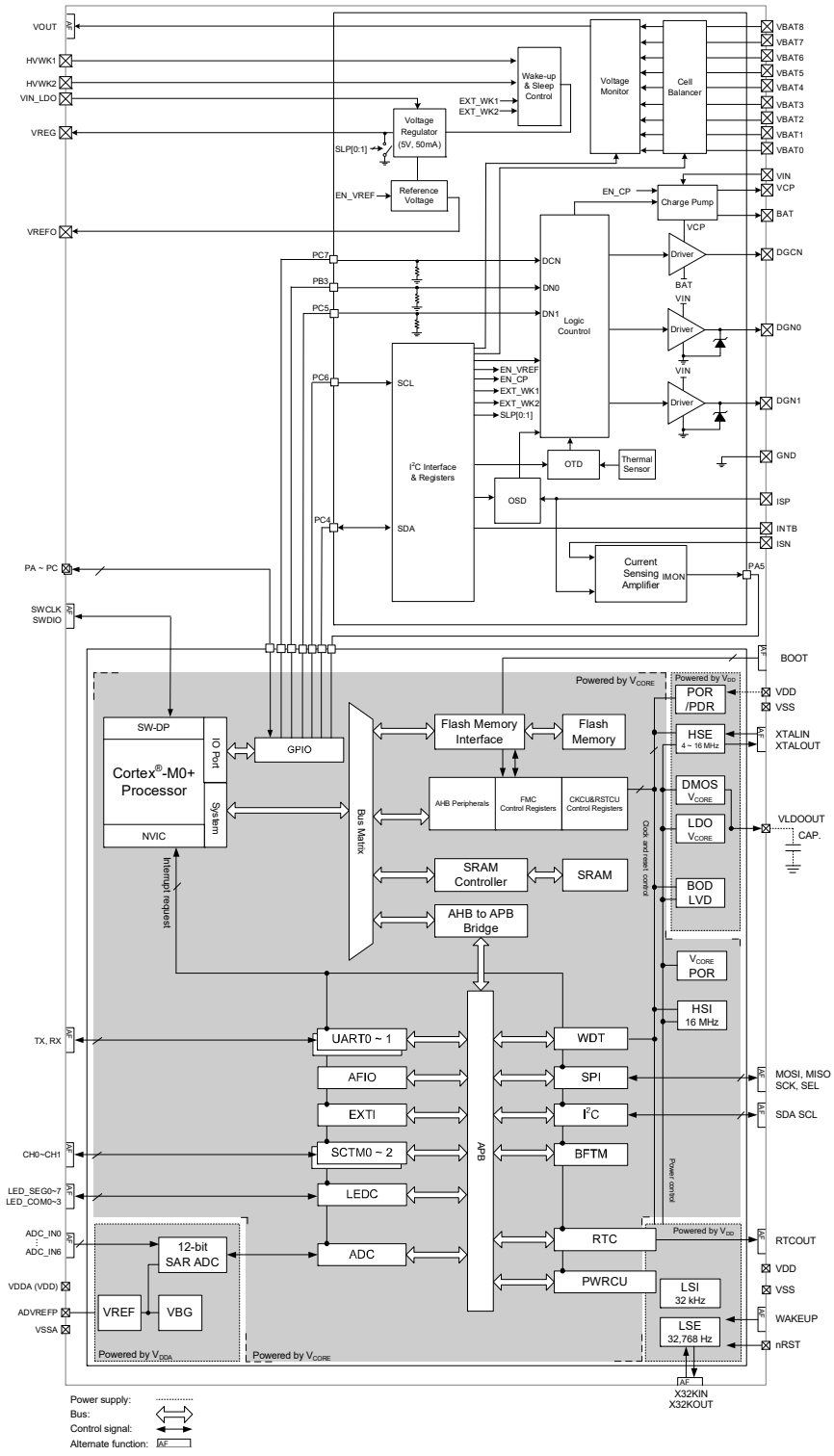


Figure 1. Block Diagram

Memory Map

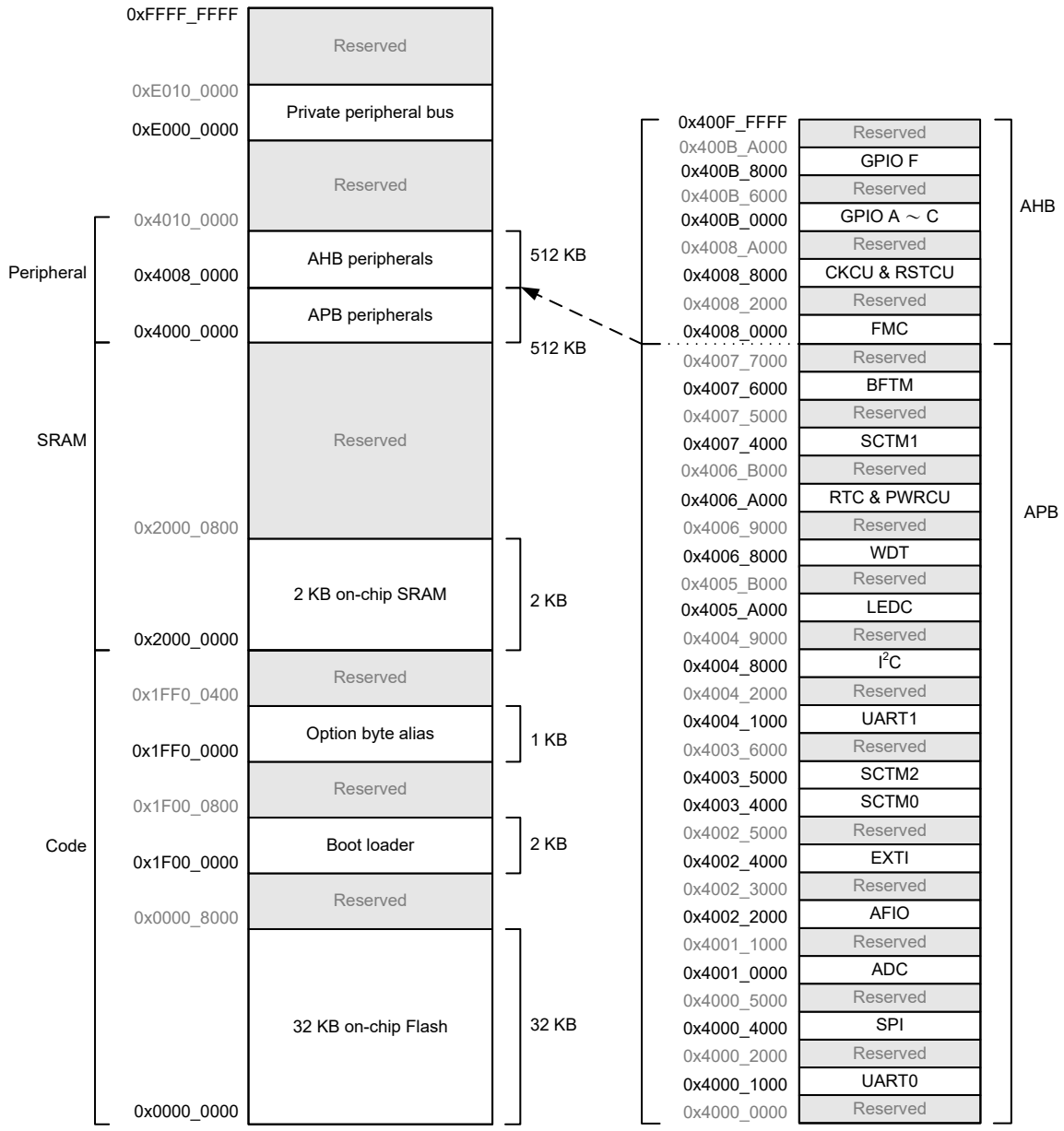


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	Reserved	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4005_9FFF	Reserved	
0x4005_A000	0x4005_AFFF	LEDC	
0x4005_B000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM	
0x4007_7000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400B_7FFF	Reserved	
0x400B_8000	0x400B_9FFF	GPIO F	
0x400B_A000	0x400F_FFFF	Reserved	

Clock Structure

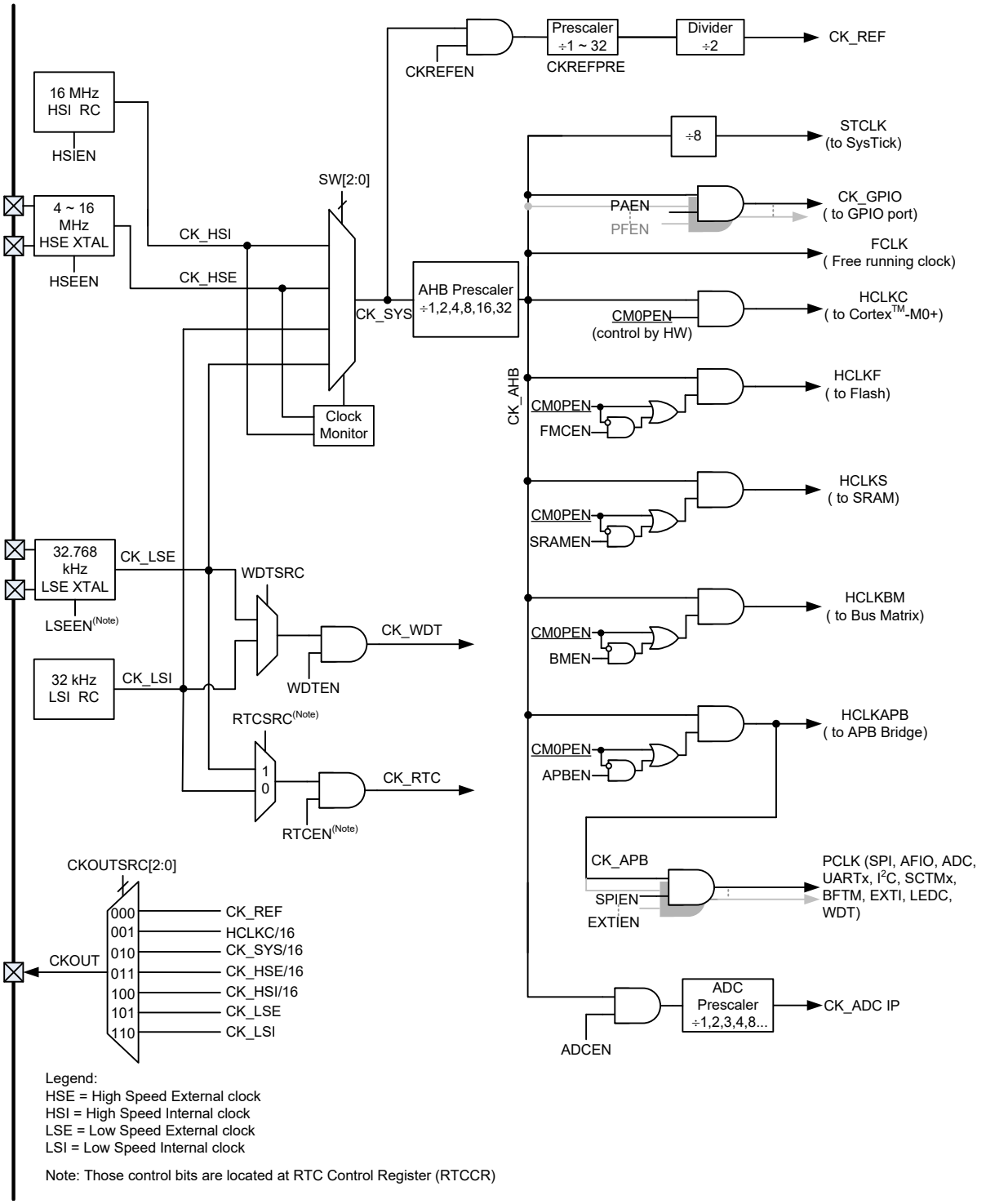


Figure 3. Clock Structure

4 Individual Cell Voltage Monitor

The cell voltage monitor is designed to monitor each battery cell voltage individually and outputs the divide-by-2 voltage to the analog multiplexer. When the analog output is 2.1 V, it has an accuracy of ±7.5 mV. When the analog output is 4.2 V, it has an accuracy of ±15 mV. Each monitor cell voltage from pin VBAT1 ~ VBAT8 can be observed sequentially and measured by using the internal A/D converter, which is only required to internal connect the VOUT pin to the A/D converter channels. The device has a 2.5 V reference voltage output, V_{REFO}, which provides the reference voltage V_{REF} for the A/D converter.

The current monitor channel provide charge and discharge current monitoring and short-current protection. The device can directly drive external N-type MOSFETs to control charge and discharge by charge and discharge gate drivers. The internal battery balance circuitry provides a cell balance current without the need of external transistors.

An integrated 5 V regulator provides a 5 V supply to the device with a 50 mA driving current capability and which has ±1 % accuracy. The voltage regulator, cell voltage monitor, current monitors, and gate drivers are shut down with an ultra-low standby current 0.1 μA when the monitor is in the Sleep mode. When the HVWK1 or HVWK2 pin is triggered by a voltage greater than its threshold, the device will return to the normal operating status.

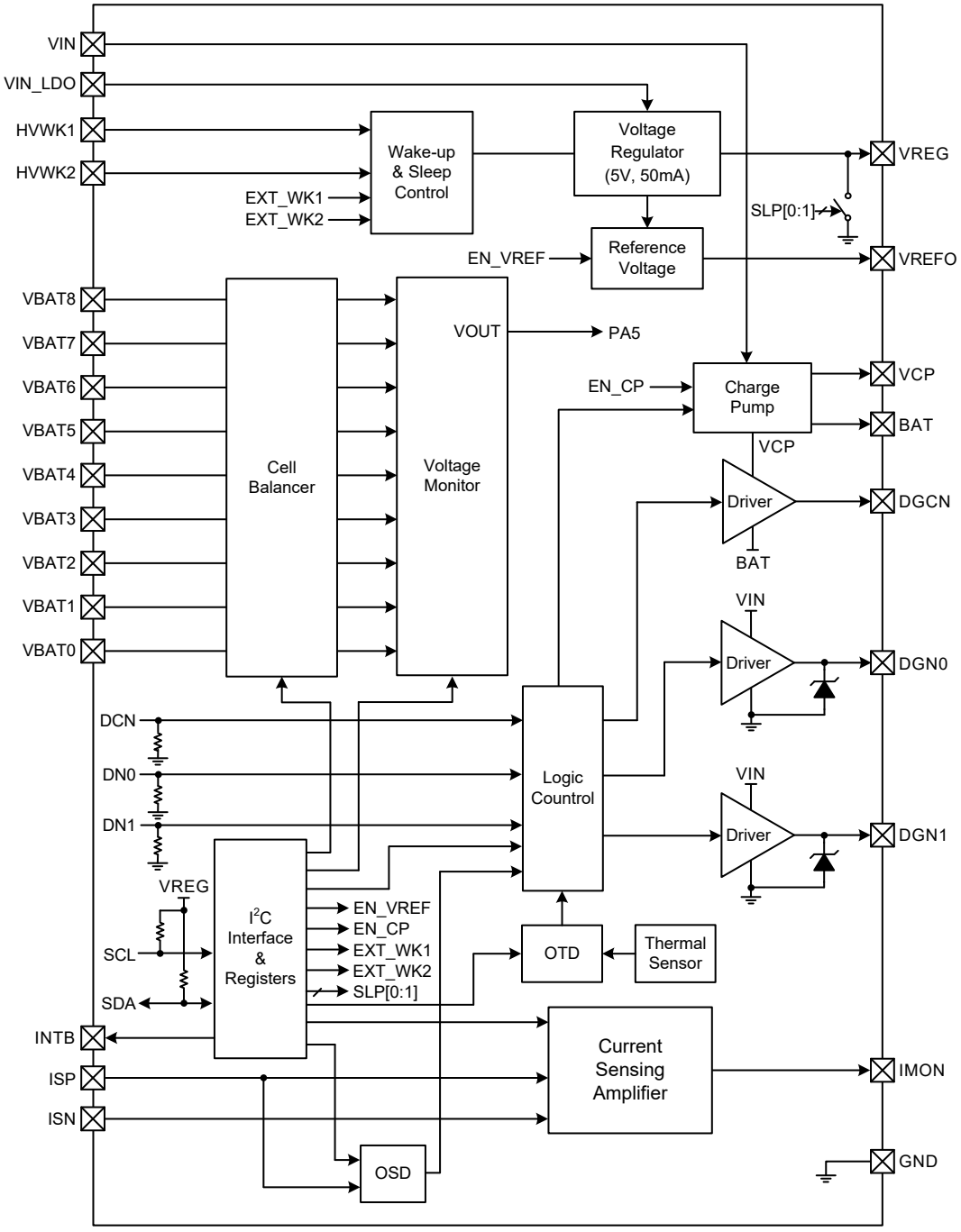


Figure 4. Individual Cell Voltage Monitor Block Diagram

I²C Serial Interface

The Individual Cell Voltage Monitor supports I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines are open-drain structure and two pull-high resistors are required. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the Wired-AND function. Data transfer is initiated only when the bus is not busy.

Data Validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low.

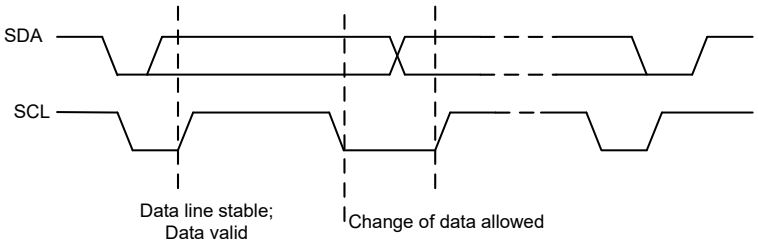


Figure 5. Data Validity

START and STOP

(1) A high to low signal transition on the SDA data line while SCL is high defines a START (S)

(2) A low to high signal transition on the SDA data line while SCL is high defines a STOP (P)

(3) START and STOP are always generated by the master. The bus is considered to be busy after the START. The bus is considered to be free again a certain time after the STOP.

(4) The bus stays busy if a REPEATED START (Sr) is generated instead of a STOP. In the respect, the START and REPEATED START are functionally identical.

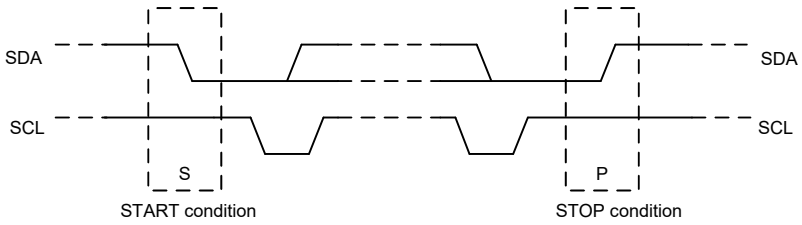


Figure 6. START and STOP

Byte Format

Every byte put on the SDA data line signal must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

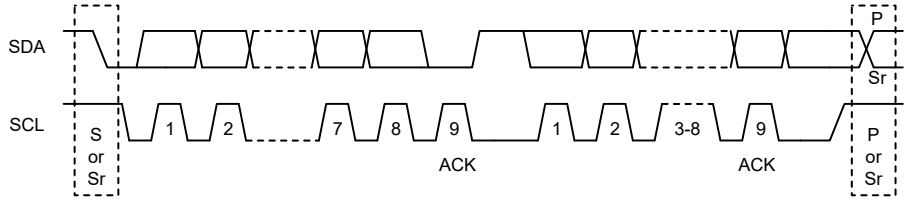


Figure 7. Byte Format

Acknowledge

(1) Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, the master generates an extra acknowledge related clock pulse.

(2) A slave receiver which is addressed must generate an Acknowledge response signal after the reception of each byte.

(3) The device that provides an acknowledge must pull down the SDA data line signal during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

(4) A master receiver must signal an end of data to the slave by generating a NOT Acknowledge response signal on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or Repeated START.

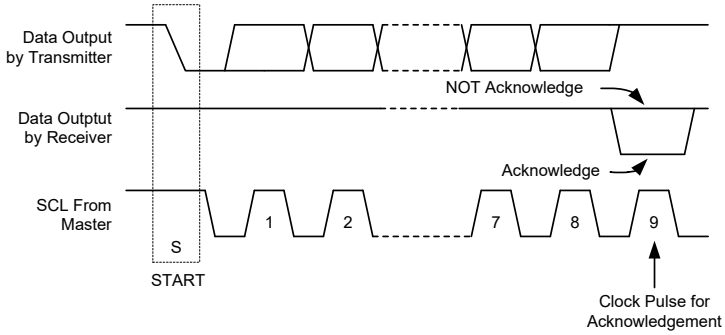


Figure 8. Acknowledge

I²C Time-out Control

In order to reduce the I²C lockup problem due to reception of erroneous clock sources, a time-out function is provided. The I²C time-out function starts timing for the specified I²C time-out period (t_{OUT}) when receiving START (S) from I²C bus. The timer is reset by every falling edge of SCL data line signal and gets interrupted when receiving STOP (P). If the next falling edge of SCL data line signal or STOP (P) does not appear throughout the I²C time-out period (t_{OUT}), SDA and SCL data line signals are set to default states at the end of timing and meanwhile the registers remains unchanged. The I²C time-out is 32 ms.

Slave Address

(1) The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When R/W bit is '1', then a READ operation is selected. When R/W bit is '0', it selects WRITE operation.

(2) The slave address is "1011101". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA data line signal.

Figure 9. Slave Address

Write Operation

An I²C write operation combines a START bit, a Slave address byte with a Write bit, a Register address byte, single or multiple Data bytes, and a STOP bit.

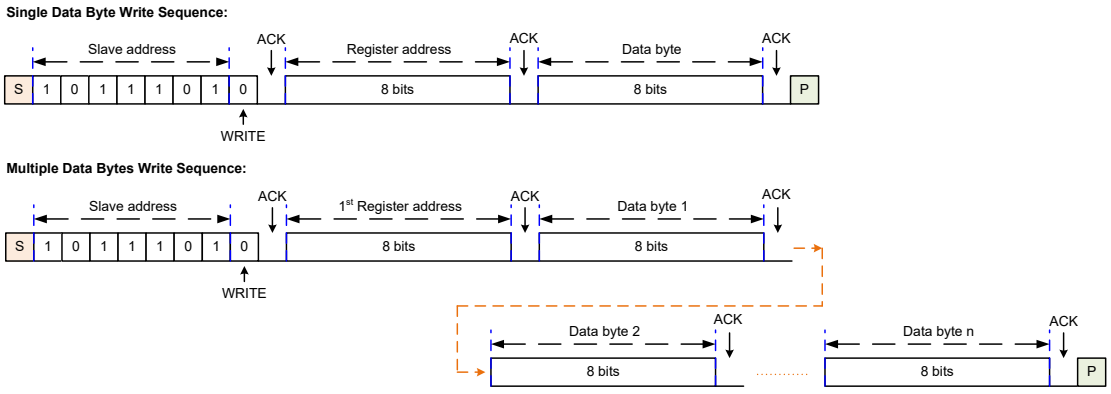


Figure 10. Write Operation

Read Sequence

The complete read mode consists of two stages. 1st stage: writes in the Register Address Byte to the slave. 2nd state: reads out the single or multiple Data Bytes from the slave.

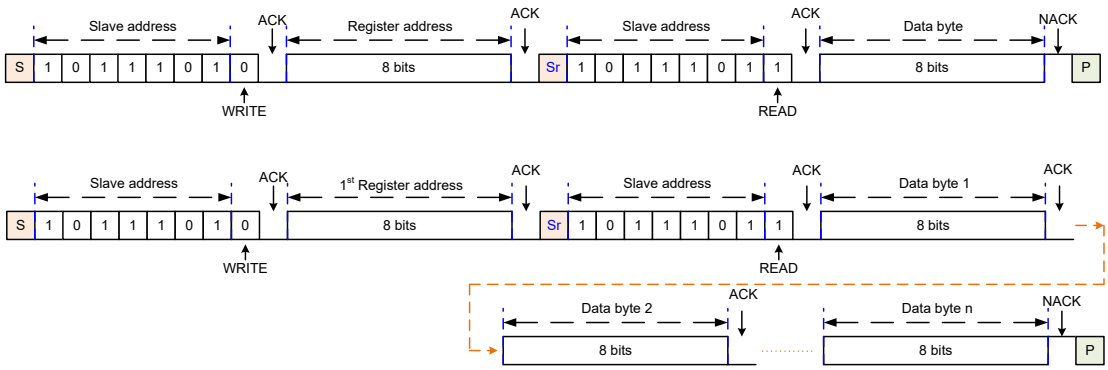


Figure 11. Read Sequence

Individual Cell Voltage Monitor I²C Register Map

The Individual Cell Voltage Monitor I²C register bit map is listed below.

Table 3. Individual Cell Voltage Monitor I²C Register Map

Address	Acronym	Access Type	Value after POR	Register Description
00H	REG00	R/W	1000 0000	Sleep, Reference Voltage, Charge Pump and Voltage Monitor Control
01H	REG01	R/W	0000 0000	Cell Balance Control
02H	REG02	R/W	0000 0000	Current Monitor Setting
03H	REG03	R/W	1000 0001	Short-Current Detection Setting 1
04H	REG04	R/W	0000 0001	Short-Current Detection Setting 2
05H	REG05	R/W	0000 0011	Short-Current Detection Control
06H	REG06	R/W	1001 0010	Over-temperature Detection and Thermal Sensor
07H	REG07	R	0000 0000	Chip Status
08H	REG08	R/W	0000 0000	Interrupt Mask
09H	REG09	R	0000 0000	Interrupt Flag

- **Sleep, Reference Voltage, Charge Pump and Voltage Monitor Control Register (00H)**

Bit	7	6	5	4	3	2	1	0
Name	SLP1	SLP0	EN_VREF	EN_S	EN_CP	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	0	0	0	0	0	0	0

Bit 7 ~ 6 **SLP1 ~ SLP0**: Sleep mode enable control

SLP1	SLP0	Action
0	0	Normal operation
0	1	Enter sleep mode
1	0	Normal operation
1	1	Normal operation

Bit 5 **EN_VREF**: Reference voltage output function enable control
0: Reference voltage output function is disabled, VREFO pin output = 0 V
1: Reference voltage output function is enabled, VREFO pin output = 2.5 V

Bit 4 **EN_S**: Voltage monitor function enable control
0: Voltage monitor function is disabled, VOUT pin output = 0 V
1: Voltage monitor function is enabled, VOUT pin output = ($V_{BAT1\sim8}$ - $V_{BAT0\sim7}$) × 1/2

Bit 3 **EN_CP**: Charge pump function enable control
0: Charge pump function is disabled
1: Charge pump function is enabled, VCP pin = V_{CP}

Bit 2 ~ 0 **B2 ~ B0**: 8-to-1 analog multiplexer selection bits (MSB: B2, LSB: B0)
Control B2 ~ B0 to select which cell voltage to be outputted to VOUT.

EN_S	B2	B1	B0	V_{OUT} (V)
0	—	—	—	0
1	0	0	0	(V_{BAT1} - V_{BAT0}) × 1/2
1	0	0	1	(V_{BAT2} - V_{BAT1}) × 1/2
1	0	1	0	(V_{BAT3} - V_{BAT2}) × 1/2
1	0	1	1	(V_{BAT4} - V_{BAT3}) × 1/2
1	1	0	0	(V_{BAT5} - V_{BAT4}) × 1/2
1	1	0	1	(V_{BAT6} - V_{BAT5}) × 1/2
1	1	1	0	(V_{BAT7} - V_{BAT6}) × 1/2
1	1	1	1	(V_{BAT8} - V_{BAT7}) × 1/2

*To avoid voltage drop caused by balance current, the cell balance function must be turned off during the voltage monitoring.

- **Cell Balance Control Register (01H)**

Bit	7	6	5	4	3	2	1	0
Name	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **CB8**: Enable control of the cell balance switch between VBAT8 and VBAT7
0: Balance switch Off
1: Balance switch On

Bit 6 **CB7**: Enable control of the cell balance switch between VBAT7 and VBAT6
0: Balance switch Off
1: Balance switch On

Bit 5 **CB6**: Enable control of the cell balance switch between VBAT6 and VBAT5
0: Balance switch Off
1: Balance switch On

Bit 4 **CB5**: Enable control of the cell balance switch between VBAT5 and VBAT4
0: Balance switch Off
1: Balance switch On

Bit 3 **CB4**: Enable control of the cell balance switch between VBAT4 and VBAT3
0: Balance switch Off
1: Balance switch On

Bit 2 **CB3**: Enable control of the cell balance switch between VBAT3 and VBAT2
0: Balance switch Off
1: Balance switch On

Bit 1 **CB2**: Enable control of the cell balance switch between VBAT2 and VBAT1
0: Balance switch Off
1: Balance switch On

Bit 0 **CB1**: Enable control of the cell balance switch between VBAT1 and VBAT0
0: Balance switch Off
1: Balance switch On

- **Current Monitor Setting Register (02H)**

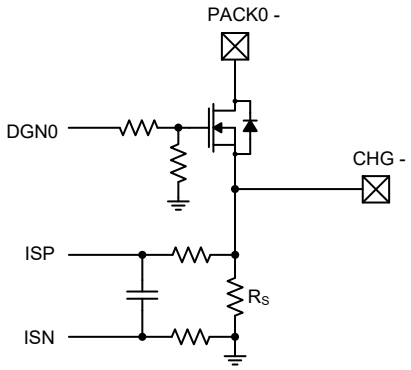
Bit	7	6	5	4	3	2	1	0
Name	IMCE	ZERO	IAR	Reserved	Reserved	Reserved	Reserved	Reserved
R/W	R/W	R/W	R/W	—	—	—	—	—
POR	0	0	0	0	0	0	0	0

Bit 7 **IMCE**: Enable current monitor
0: Disable current monitor
1: Enable current monitor

Bit 6 **ZERO**: Execute zero correction of current monitor
0: The input of internal differential voltage amplifier circuit are connected to ISP and ISN pin
1: Both input of internal differential voltage amplifier circuit are connected to GND

Bit 5 **IAR**: Select the voltage amplifying rate of current monitor
0: Voltage amplifying rate = 10
1: Voltage amplifying rate = 50

R_S	IAR	Maximum Discharge Current (A)	Maximum Charge Current (A)
2 mΩ	0	195	15
	1	38	2
5 mΩ	0	78	6
	1	15	0.8



Bit 4 ~ 0 Reserved bits, these bits should be kept unchanged after power-on

• Short-Current Detection Setting 1 Register (03H)

Bit	7	6	5	4	3	2	1	0
Name	ISCE1	ISCE0	Reserved	Reserved	Reserved	SC_2	SC_1	SC_0
R/W	R/W	R/W	—	—	—	R/W	R/W	R/W
POR	1	0	0	0	0	0	0	1

Bit 7 ~ 6 **ISCE1 ~ ISCE0**: Enable short-current detection

ISCE1	ISCE0	Action
0	0	Short current detection is off
0	1	Short current detection is activated
1	0	Short current detection is off
1	1	Short current detection is off

Bit 5 ~ 3 Reserved bits, these bits should be kept unchanged after power-on

Bit 2 ~ 0 **SC_2 ~ SC_0**: Select the short-current detection threshold voltage (V_{SCTH}) of short-current detection

If the voltage of V_{ISP} is greater than the threshold voltage, INTB is pulled low by internal switch.

SC_2	SC_1	SC_0	Threshold Voltage
0	0	0	50 mV
0	0	1	100 mV
0	1	0	150 mV
0	1	1	200 mV
1	0	0	250 mV
1	0	1	300 mV
1	1	0	350 mV
1	1	1	400 mV

• Short-Current Detection Setting 2 Register (04H)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	TD_4	TD_3	TD_2	TD_1	TD_0
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	1

Bit 7 ~ 5 Reserved bits, these bits should be kept unchanged after power-on

Bit 4 ~ 0 **TD_4 ~ TD_0**: Select the debounce time of short-current detection

TD_4	TD_3	TD_2	TD_1	TD_0	Debounce Time
0	0	0	0	0	0 μs
0	0	0	0	1	32 μs
0	0	0	1	0	64 μs
0	0	0	1	1	96 μs
0	0	1	0	0	128 μs
0	0	1	0	1	160 μs
0	0	1	1	0	192 μs
0	0	1	1	1	224 μs

TD_4	TD_3	TD_2	TD_1	TD_0	Debounce Time
0	1	0	0	0	256 μs
0	1	0	0	1	288 μs
0	1	0	1	0	320 μs
0	1	0	1	1	352 μs
0	1	1	0	0	384 μs
0	1	1	0	1	416 μs
0	1	1	1	0	448 μs
0	1	1	1	1	480 μs
1	0	0	0	0	512 μs
1	0	0	0	1	544 μs
1	0	0	1	0	576 μs
1	0	0	1	1	608 μs
1	0	1	0	0	640 μs
1	0	1	0	1	672 μs
1	0	1	1	0	704 μs
1	0	1	1	1	736 μs
1	1	0	0	0	768 μs
1	1	0	0	1	800 μs
1	1	0	1	0	832 μs
1	1	0	1	1	864 μs
1	1	1	0	0	896 μs
1	1	1	0	1	928 μs
1	1	1	1	0	960 μs
1	1	1	1	1	992 μs

- **Short-Current Detection Control Register (05H)**

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	IS_ACT_DGCN	IS_ACT_DGN1	IS_ACT_DGN0
R/W	—	—	—	—	—	R/W	R/W	R/W
POR	0	0	0	0	0	0	1	1

Bit 7 ~ 3 Reserved bits, these bits should be kept unchanged after power-on

Bit 2 **IS_ACT_DGCN**: Control actions of DGCN when short-current event is detected
IS_ACT_DGCN can be written only when V_{DCN} = 0 V.
0: Remain present output status of DGCN when short-current event is detected
1: Shut down and lock the output of DGCN when short-current event is detected
The locked output of DGCN is released by the falling edge of DCN input signal.

Bit 1 **IS_ACT_DGN1**: Control actions of DGN1 when short-current event is detected
IS_ACT_DGN1 can be written only when V_{DN1} = 0 V.
0: Remain present output status of DGN1 when short-current event is detected
1: Shut down and lock the output of DGN1 when short-current event is detected
The locked output of DGN1 is released by the falling edge of DN1 input signal.

Bit 0 **IS_ACT_DGN0**: Control actions of DGN0 when short-current event is detected
IS_ACT_DGN0 can be written only when V_{DN0} = 0 V.
0: Remain present output status of DGN0 when short-current event is detected
1: Shut down and lock the output of DGN0 when short-current event is detected
The locked output of DGN0 is released by the falling edge of DN0 input signal.

• Over-temperature Detection and Thermal Sensor Register (06H)

Bit	7	6	5	4	3	2	1	0
Name	EN_OTD	Reserved	Reserved	OTD_ACT	Reserved	Reserved	OTDTH1	OTDTH0
R/W	R/W	—	—	R/W	—	—	R/W	R/W
POR	1	0	0	1	0	0	1	0

Bit 7 **EN_OTD**: Enable Over-temperature detection
0: Disable Over-temperature detection
1: Enable Over-temperature detection

Bit 6 ~ 5 Reserved bits, these bits should be kept unchanged after power-on

Bit 4 **OTD_ACT**: Control action of cell balance when internal over-temperature event is detected
0: Remain present turn-on status of cell balance when internal over-temperature event is detected
1: Turn off and lock all cell balance switches when internal over-temperature event is detected
The locked switches of cell balance can only turn on the cell balance function again after resetting the cell balance control register CB[8:1] = 0x00.

Bit 3 ~ 2 Reserved bits, these bits should be kept unchanged after power-on

Bit 1 ~ 0 **OTDTH1 ~ OTDTH0**: Select the over-temperature detection threshold

Symbol	OTDTH1	OTDTH0	OTD Threshold
T_{OTD1}	0	0	85 °C
T_{OTD2}	0	1	100 °C
T_{OTD3}	1	0	125 °C
T_{OTD4}	1	1	150 °C

• Chip Status Register (07H)

Bit	7	6	5	4	3	2	1	0
Name	DGCN_OUT	DGN1_OUT	DGN0_OUT	OTD_ST	EXT_WK2	EXT_WK1	Reserved	IS_SC_ST
R/W	R	R	R	R	R	R	—	R
POR	0	0	0	0	0	0	0	0

Bit 7 **DGCN_OUT**: DGCN output status
0: DGCN output status is off ($V_{DGCN} = V_{BAT}$)
1: DGCN output status is on ($V_{DGCN} = V_{CP}$)

Bit 6 **DGN1_OUT**: DGN1 output status
0: DGN1 output status is off (V_{DGN1} = 0 V)
1: DGN1 output status is on ($V_{DGN1} = V_Z$)

Bit 5 **DGN0_OUT**: DGN0 output status
0: DGN0 output status is off (V_{DGN0} = 0 V)
1: DGN0 output status is on ($V_{DGN0} = V_Z$)

Bit 4 **OTD_ST**: OTD event status
0: Junction temperature is under T_{OTD}
1: Present junction temperature is higher than T_{OTD}
OTD_ST goes to '0' when internal junction temperature drops under (T_{OTD} - T_{HYS}).

Bit 3 **EXT_WK2**: HVWK2 wake-up event status
0: Denotes that external wake-up event does not exist at HVWK2 pin
1: Denotes that external wake-up event exists at HVWK2 pin
When V_{HVWK2} remains higher than V_{WKTH} over 1 ms, EXT_WK2 will be set to '1', meanwhile SLP1 and SLP0 are reset to their POR values.
EXT_WK2 is cleared to '0' immediately when V_{HVWK2} drops under 1.5 V.

Bit 2 **EXT_WK1**: HVWK1 wake-up event status
0: Denotes that external wake-up event does not exist at HVWK1 pin
1: Denotes that external wake-up event exists at HVWK1 pin or is written by MCU
(1) When V_{HVWK1} remains higher than V_{WKTH} over 1ms, EXT_WK1 will be set to '1', meanwhile SLP1 and SLP0 are reset to their POR values.
EXT_WK1 is cleared to '0' immediately when V_{HVWK1} drops under 1.5 V.
(2) EXT_WK1 can be written as '1' by MCU for the purpose of sending a wake-up signal. EXT_WK1 have to be written as '0' and SLP[1:0] have to be written as 0b10 through I^2C interface after EXT_WK1 is set as '1' by MCU, otherwise external wake-up event on HVWK1 pin cannot be recognized and the follow-up Sleep command will be failed.
(3) Writing both EXT_WK1 and SLP[1:0] as '1' and 0b01 is NOT permitted for avoiding unpredictable status.
(4) Reading EXT_WK1 reveals the external wake-up even status of HVWK1 pin only.

Bit 1 Reserved bit, this bit should be kept unchanged after power-on

Bit 0 **IS_SC_ST**: Short-current protection detecting status
0: V_{ISP} is under V_{SCTH}
1: Short-current event is happening at Short-current detection ($V_{ISP} > V_{SCTH}$)

- **Interrupt Mask Register (08H)**

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	OTD_MSK	EXT_WK2_MSK	EXT_WK1_MSK	Reserved	IS_SC_MSK
R/W	—	—	—	R/W	R/W	R/W	—	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 5 Reserved bits, these bits should be kept unchanged after power-on

Bit 4 **OTD_MSK**: Over-temperature detection INTB mask
0: OTD_ST entry produces INTB pulse
1: OTD_ST entry does not produce INTB pulse but still trigger OTD_FLG

Bit 3 **EXT_WK2_MSK**: External wake-up event detection INTB mask
0: EXT_WK2 entry produces INTB pulse
1: EXT_WK2 entry does not produce INTB pulse but still trigger EXT_WK2_FLG

Bit 2 **EXT_WK1_MSK**: External wake-up event detection INTB mask
0: EXT_WK1 entry produces INTB pulse
1: EXT_WK1 entry does not produce INTB pulse but still trigger EXT_WK1_FLG

Bit 1 Reserved bit, this bit should be kept unchanged after power-on

Bit 0 **IS_SC_MSK**: Short-current detection INTB mask
0: IS_SC_ST entry produces INTB pulse
1: IS_SC_ST entry does not produce INTB pulse but still trigger IS_SC_FLG

● **Interrupt Flag Register (09H)**

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	OTD_FLG	EXT_WK2_FLG	EXT_WK1_FLG	Reserved	IS_SC_FLG
R/W	—	—	—	R	R	R	—	R
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 5 Reserved bits, these bits should be kept unchanged after power-on

Bit 4 **OTD_FLG**: Over-temperature detection INTB flag
0: Normal
1: OTD_ST rising edge detected
OTD_FLG is reset to '0' after I^2C master reads Interrupt Flag Register.

Bit 3 **EXT_WK2_FLG**: HVWK2 external wake-up event detection INTB flag
0: Normal
1: EXT_WK2 rising edge detected
EXT_WK2_FLG is reset to '0' after I^2C master reads Interrupt Flag Register.

Bit 2 **EXT_WK1_FLG**: HVWK1 external wake-up event detection INTB flag
0: Normal
1: EXT_WK1 rising edge detected
EXT_WK1_FLG is reset to '0' after I^2C master reads Interrupt Flag Register.

Bit 1 Reserved bit, this bit should be kept unchanged after power-on

Bit 0 **IS_SC_FLG**: Short-current detection INTB flag
0: Normal
1: IS_SC_ST rising edge detected
IS_SC_FLG is reset to '0' after I^2C master reads Interrupt Flag Register.

Cell Voltage Monitor

B2, B1 and B0 are used to control the switches SW1 ~ SW8 only if EN_S = '1'. The control truth table is shown below. It transfers 1/2 of each battery cell's voltage to VOUT. It's recommended that to keep EN_S = '0' when voltage scanning procedure is finish for power saving.

Table 4. Cell Voltage Monitor Truth Table

EN_S	B2	B1	B0	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	V_{OUT} (V)
0	X	X	X	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1	$(V_{BAT1} - V_{BAT0}) \times 1/2$
1	0	0	1	0	0	0	0	0	0	1	0	$(V_{BAT2} - V_{BAT1}) \times 1/2$
1	0	1	0	0	0	0	0	0	1	0	0	$(V_{BAT3} - V_{BAT2}) \times 1/2$
1	0	1	1	0	0	0	0	1	0	0	0	$(V_{BAT4} - V_{BAT3}) \times 1/2$
1	1	0	0	0	0	0	1	0	0	0	0	$(V_{BAT5} - V_{BAT4}) \times 1/2$
1	1	0	1	0	0	1	0	0	0	0	0	$(V_{BAT6} - V_{BAT5}) \times 1/2$
1	1	1	0	0	1	0	0	0	0	0	0	$(V_{BAT7} - V_{BAT6}) \times 1/2$
1	1	1	1	1	0	0	0	0	0	0	0	$(V_{BAT8} - V_{BAT7}) \times 1/2$

Cell Balance

Multiple channels of cell balance switch can be turned on via I²C interface. The register command byte of cell balance function is 01H, and the BIT7 ~ BIT0 of Data byte correspond to the cell balance switch of each channel from SW8 to SW1, respectively. More than one switch can be turned on in the same time, but side-by-side cell balance switches are recommended NOT to be turned on simultaneously to ensure equal balance current between each channel. After receiving turn on command, cell balance switch remains turned on until it is turned off by a '0' data or get a command of SLP0 = '1'. By setting OTD_ACT = '1', when internal junction temperature exceeds T_{OTD}, all balance switched are turned off and locked automatically and cannot be turned on again until the locked states are released. All locked switches are released by setting CB[8:1] = 0x00.

The typical cell balance current is 10 mA at battery cell voltage 4.2 V with series resistance 100 Ω, and the balance current can be adjusted by series resistors R0 ~ R8. Note that for the reason of keeping voltage monitor accuracy, do not proceed voltage monitor while cell balance is activated.

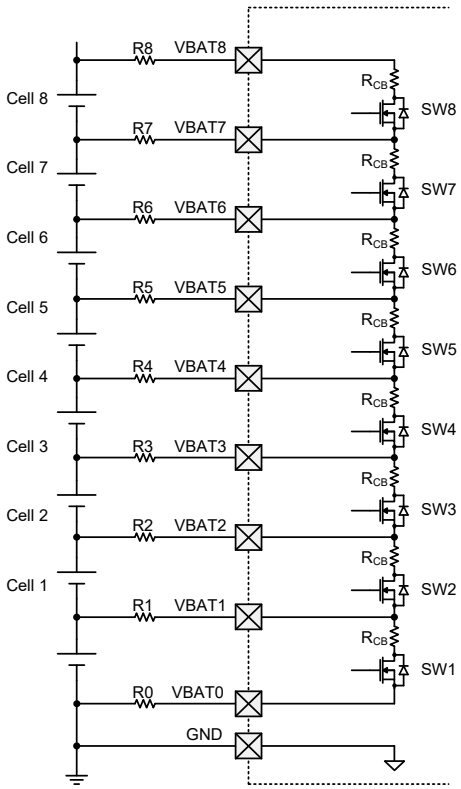


Figure 12. Cell Balance Application Schematic Diagram

Table 5. Cell Balance Switch Truth Table

CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	Balance Switch On/Off
1	0	0	0	0	0	0	0	SW1 On, others Off
0	1	0	0	0	0	0	0	SW2 On, others Off
0	0	1	0	0	0	0	0	SW3 On, others Off
0	0	0	1	0	0	0	0	SW4 On, others Off
0	0	0	0	1	0	0	0	SW5 On, others Off
0	0	0	0	0	1	0	0	SW6 On, others Off
0	0	0	0	0	0	1	0	SW7 On, others Off
0	0	0	0	0	0	0	1	SW8 On, others Off

Note: More than one switch can be turned On in the same time.

Current Monitor

A current monitor is fabricated for measuring battery discharge current. The current monitor with ISP and ISN input pins must be connected to the sense resistor on DGN0 or DGN1 pin discharge path. IMCE signal is the enable control of current monitor, and current monitors can be turned off by setting IMCE = '0' for power saving purpose.

Current measurement is accomplished with placing current sensing resistors connected between ISP and ISN pins, and measure input voltage difference of these pins. The ISP pin level should be higher than the ISN pin level in discharge state for a wide discharge current sensing range. While there is no current on sensing resistor or ZERO = '1', IMON outputs a center voltage of 0.5 V (typ.). When ZERO pin is set to '0', voltage difference of (V_{ISP} - V_{ISN}) is multiplied by the gain of amplifier which is denoted as $G_{IM(R10)}$ for a gain of 10 or $G_{IM(R50)}$ for a gain of 50 and outputted to IMON. The IMON output voltage amplify rate (G_{IM}) is selected by IAR.

The current monitor allows to use one sense resistor for charge and discharge current sensing. In discharge state, the voltage of ISP pin is greater than the ISN pin, and the output voltage of IMON is in the range of 0.5 V (typ.) to 2.5 V (VREF). In charge state, the voltage of ISP pin is smaller ISN pin, and the output voltage of IMON is in the range of 0 V to 0.5 V (typ.). IMON output voltage V_{IMON} is given by the following equation with the current sensing resistor R_S and its current I_S. The value of I_S is positive in discharge state and negative in charge state.

$$V_{IMON} = I_S \times R_S \times G_{IM} + 0.5$$

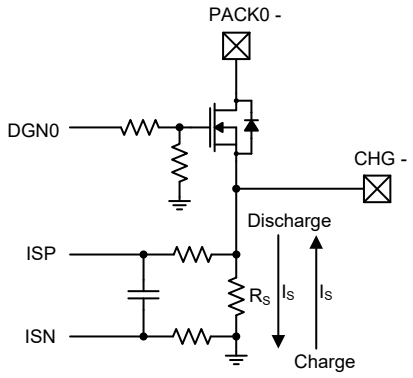


Figure 13. Current Monitor Schematic Diagram

Short-current Detection

A short-current detection and protection circuit are fabricated for detecting loading short event. Short current detection with ISP and ISN input pins must be connected to the sense resistor on DGN0 or DGN1 pin discharge path. The ISCE signal is the enable control of short current protection, and short-current protection can be turned off by setting ISCE = '0' for power saving purpose. By means of comparing V_{ISP} to short-current detection threshold voltage (V_{SCTH}), the exceeding current caused by loading shorted can be detected.

Sleep Mode

It is important not to confuse this Sleep mode with the SLEEP mode which is described in the "Power Management Control Unit" section of this datasheet.

When EXT_WK1 and EXT_WK2 signals are all '0' and receiving a sleep command from I^2C master, it indicates that high voltage applied on the HVWK1 or HVWK2 pin is not detected. The I^2C master will set the SLP1 and SLP0 signals according to register (00H) Bit 7 ~ 6 to make the Individual Cell Voltage Monitor to enter the Sleep mode. During the sleep mode, all outputs are shut down and the capacitor of VREG is discharged through internal discharge resistor. The pre-regulator and high voltage wake-up circuit are the only blocks that are still working in the sleep mode and operates with an ultra-low standby current of 0.1 μA (typical).

When either the EXT_WK or EXT_WK2 signal is '1', the I^2C master will set the SLP1 and SLP0 signals according to register (00H) Bit 7 ~ 6 and abandon the sleep command until the EXT_WK and EXT_WK2 are cleared to '0'.

Table 6. Sleep Mode Status Truth Table

EXT_WK1 Status	EXT_WK2 Status	Sleep Mode Status
0	0	According to I^2C master command or POR default value.
0	1	0
1	0	0
1	1	0

Wake up from Sleep Mode

The HVWK1 and HVWK2 pins can be used for detecting charger plugged-in, switch turned on, or load connected events. When the Individual Cell Voltage Monitor is under the Sleep mode and the EXT_WK1 and EXT_WK2 signals are all '0', it indicates that high voltage applied on the HVWK1 or HVWK2 pin is not detected. On the contrary, if either EXT_WK1 or EXT_WK2 signal is '1', it indicates that a wake-up event has occurred. If it is detected that the HVWK1 or HVWK2 pin is triggered by a pulse with requiring at least 5.5 V voltage and 1ms width, the output of VREG will resume and the whole Individual Cell Voltage Monitor is ready for normal operation. The reference timing diagram of entering sleep mode and waked up is listed below.

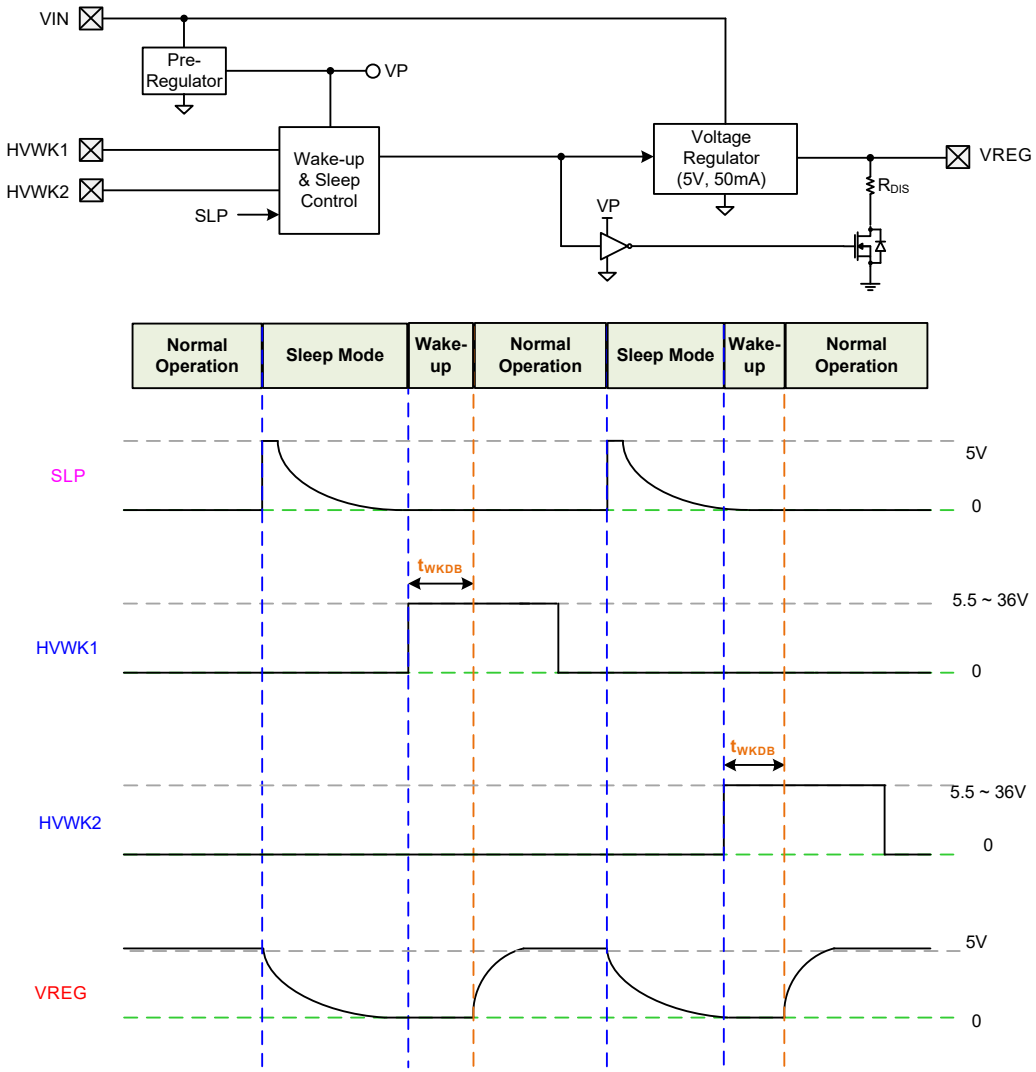


Figure 14. Sleep Mode Wake-up Sequence

Discharge Path, i.e., Low-side Power Switch Gate Driver

The DGN0 and DGN1 are fabricated in the chip as discharge switch controllers. The output voltage of DGN0 and DGN1 pins are both clamped at 12 V. A 370 kΩ pull-down resistor is integrated at discharge gate control input DN0 and DN1. While operating in Normal Operation or sleep mode, DGN0 and DGN1 are pulled down by 10 Ω resistors. The control logic and output status of DGN0 and DGN1 pins in each state are listed in the table below.

Table 7. DGN0 Control Logic and Output Status in Different Operating Modes

Operating Mode	DN0	V(DGN0)	Note
Normal Operation	0	0 V	DGN0 output low to 0 V
	1	12 V	DGN0 output high clamp to 12 V
Sleep Mode	X	0 V	Pulled-low to GND by 10 Ω

Table 8. DGN1 Control Logic and Output Status in Different Operating Modes

Operating Mode	DN1	V(DGN1)	Note
Normal Operation	0	0 V	DGN1 output low to 0 V
	1	12 V	DGN1 output high clamp to 12 V
Sleep Mode	X	0 V	Pulled-low to GND by 10 Ω

Charge Path, i.e., High-side Power Switch Gate Driver

A high-side power switch gate driver DGCN is provided as a charger switch controller. A charge pump circuit is fabricated to provide BAT or VCP voltage between the gate and source node of external charge power switch. When the DCN is‘0’, DGCN output low, the voltage level varies with the BAT pin. When the DCN is‘1’, DGCN output high, the voltage level varies with the VCP pin. A 370 kΩ pull-down resistor is integrated at the control input DCN.

Table 9. DCN Control Logic and DGCN Output Status

Input	Gate Driver Output	Note
DCN	V(DGCN)	
0	BAT	DGCN output low, the voltage level varies with the BAT pin
1	VCP	DGCN output high, the voltage level varies with the VCP pin

Over-temperature Detection

An over-temperature detection (OTD) is integrated in the Individual Cell Voltage Monitor to prevent from IC overheated while cell balance function is turned on. According to the setting of register (06 H), the over-temperature detection function is active when EN_OTD = ‘1’ and any of the Cell Balance switch is turned on. When internal junction temperature $T_J > T_{OTD}$, OTD_ST is set to ‘1’ and OTD_FLG is triggered as ‘1’ if OTD_MSK = ‘0’. OTD_ST goes to ‘0’ when internal junction temperature drops under (T_{OTD} - T_{HYS}).

By setting OTD_ACT = ‘1’, when internal junction temperature exceeds T_{OTD}, all balance switched are turned off and locked automatically. All locked switches cannot be turned on again until they are released by setting CB [8:1] = 0x00.

VIN, VREG Capacitors

The VIN input capacitor C1 and VREG output capacitor C2 are 4.7 µF for better input noise filtering and output load transient behavior.

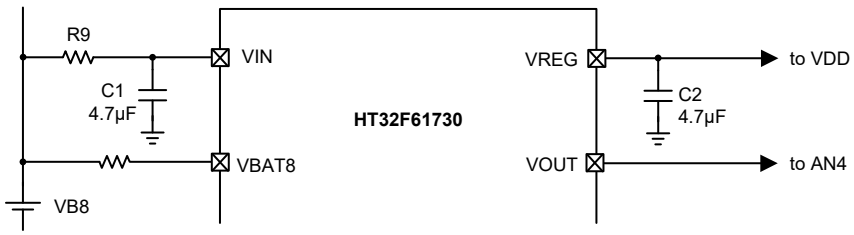


Figure 15. Input / output Capacitor Configuration

VIN_LDO Filter Recommendation

The input capacitor C1 for VIN_LDO is used for lowering the input voltage ripple while the battery is supplying a highly inductive load in PWM mode. The recommanded value of VIN_LDO input capacitor C1 is 4.7 μF. The input resistor R9 of VIN_LDO is able to reduce the inrush current during battery assembly, and also it shares the heat on chip while VREG outputs a large current in normal operation mode. The recommanded value for VIN_LDO input resistor R9 differs from different battery cell number applications. The recommended resistance values of VIN_LDO input resistor R9 with different battery cell numbers and the corresponding VREG maximum output current are listed in the table below.

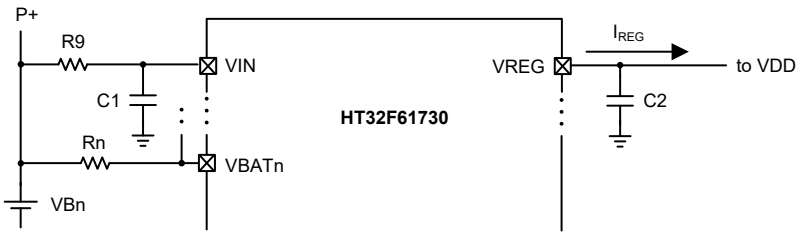


Figure 16. VIN R9 Configuration

Table 10. R9 Recommended Values for Different Cell Numbers

Battery Cell Number	Input Resistor (R9)	VREG Maximum Output Current
3S	15 Ω	50 mA
4S	43 Ω	50 mA
5S	110 Ω	40 mA
6S	220 Ω	35 mA
7S	330 Ω	30 mA
8S	430 Ω	30 mA

It is necessary to select an appropriate package for VIN_LDO input resistor (R9) in order to prevent it being damaged from overheated. The maximum power of the resistor is easily calculated by:

$$P_{R9.MAX} = (I_{REG})^2 \times R9, \text{ where } I_{REG} \text{ is the maximum VREG output current}$$

It is recommended to choose the resistor package that its maximum rated power is greater than twice the $P_{R9.MAX}$.

VBAT1 ~ VBAT8 Protection and Balance Resistor Selection

The VBAT1 ~ VBAT8 represents the VBAT1 ~ VBAT8 pins. Series resistors RBn includes R1 ~ R8, which not only suppress inrush and noise spikes applied to I/O pins, they affect cell balance current as well. Larger resistance of R1 ~ R8 provide better protection to VBAT1 ~ VBAT8 and other I/O pins, but they lower the cell balance current instead. The cell balance current of each channel is configured by internal balance resistors and external series resistors. Because the balance current of Cell 1 flows out through the GND pin while using the standard version product, the balance current of Cell 1 is greater than that of other cells. Considering inrush spike protection to I/O pins and noise reduction of voltage monitor, the recommended typical values of resistor R0 ~ R8 are 100 Ω, and the cell balance current I_{CB} is 10 mA while the voltage of battery cell is 4.2 V. If larger balance current is needed, the recommended minimum values of resistors R1 ~ R8 are 30 Ω which provide 23 mA while the voltage VBn of each cell is 4.2 V. To ensure the internal balance circuit works properly, the minimum battery cell voltage to start the balance function is 3 V. The recommended VBAT1 ~ VBAT8 series resistors and their related cell balance current are listed in the table below.

Table 11. R0 ~ R8 Recommended Values for Different Balance Current

Resistance of R0 ~ R8 (R_{Bn})	Typical Balance Current (@V_{Bn} = 4.2 V) (I_{CB})	Note
30 Ω	23.4 mA	Minimum value of resistor R0 ~ R8
51 Ω	19 mA	—
100 Ω	11.5 mA	—
150 Ω	8.5 mA	—

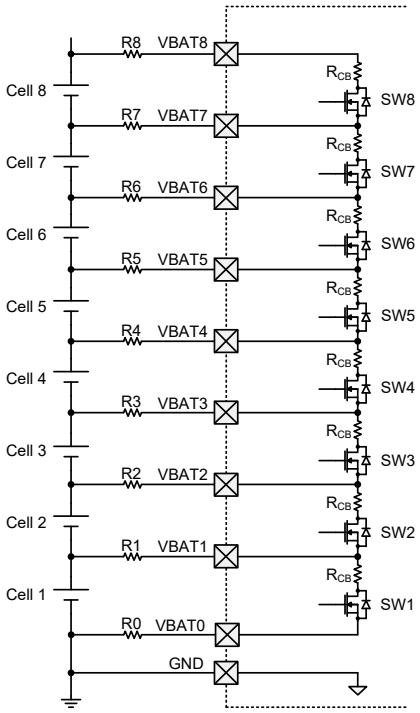


Figure 17. VBAT1 ~ VBAT8 Protection and Balance Resistors

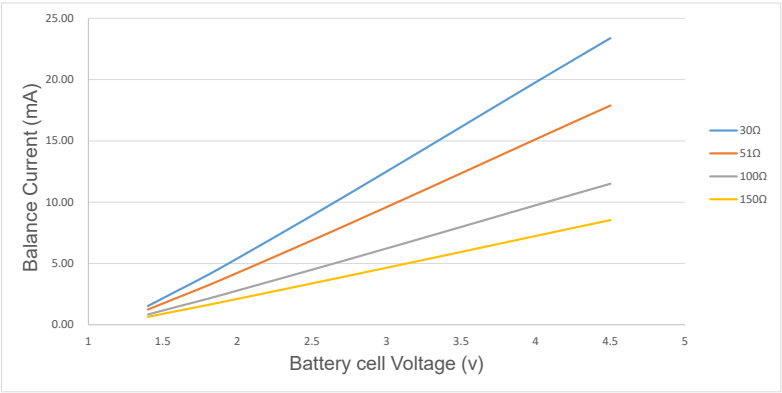


Figure 18. Balanced Current VS Balanced Voltage

Increase Cell Balance Current

Refer to the following application circuits, when cell balance is turned on internally, the R1 will generate a voltage drop to make transistor Q1 conductive. Set the V_{B1} = 4.2 V, R1 = R4 = R2 = 100 R, balanced current (I_{CB}) is 150 mA, it is recommended Q1 to choose NPN transient HFE ≥ 85, $V_{CE(sat)}$ ≤ 0.1 V, $V_{BE\ (sat)}$ ≈ 0.7 V, and calculate R3 according to the following formula:

1. $R3 = (V_{B1} - V_{CE(sat)}) / I_{CB}$
2. R3 selects resistance watts based on the calculation result

$P_D = ((V_{B1} - V_{CE(sat))})^2) / R_3$

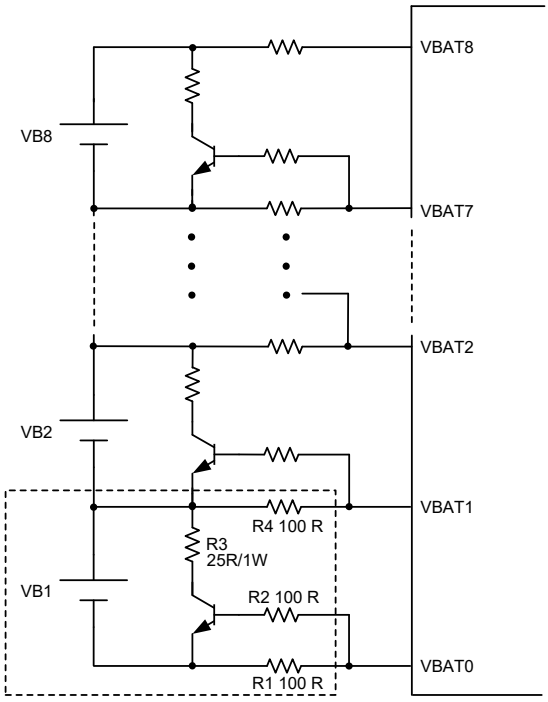


Figure 19. External Balanced Application Circuit

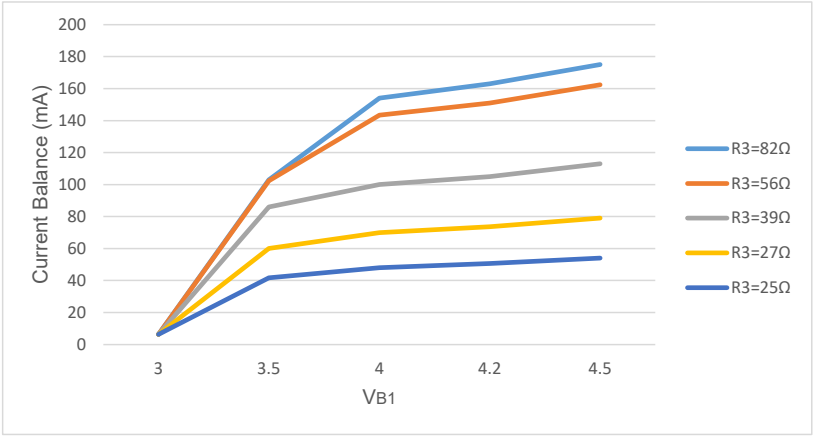


Figure 20. Alance Current VS V_{B1}

Charger and Switch Status Detection

The High-voltage wake-up (HVWK) function is capable of detecting charger plugged in or load switched on. Two recommended HVWK external circuits are listed below, the main distinction is between switch high-voltage wake-up and switch low-voltage wake-up, whereas the chargers are both high-voltage wake-up.

The first circuit is a typical application for charger or switch high-voltage wake-up function, switch active high detection, charger plugged-in detection and charger voltage detection.

When a charger is plugged in or load switch is on, the voltage of HVWK is triggered to be larger than V_{WKTH} and set the EXT_WK bit as "1". After the charger is removed or the switch is turned off, the EXT_WK bit is reset to "0". An MCU can acquire the charger or switch status by reading the EXT_WK bit through the I^2C interface. Therefore, by the means of reading the EXT_WK bit status, additional charger or switch detection circuits for MCU are not necessary.

When the MCU requires to directly detect the switch status, a clamp circuit R40, R41 and ZD1 should be added to prevent the high voltage generated by pressing SW from entering the SW_DET directly. The typical values of R40 and R41 are 100 kΩ and the ZD1 is 4.7 V. When the battery is at a low voltage (PACK0+ = 7.5 V), the voltage divided ratio of R40 and R41 should be adjusted according to the situation to ensure that the SW_DET voltage is higher than the MCU high level threshold.

In addition, the MCU can use its ADC to read the CHG_DET and then calculate the charger voltage using the voltage divided ratio of R42 and R43. The typical values of R42 and R43 are 100 kΩ and 5.1 kΩ respectively.

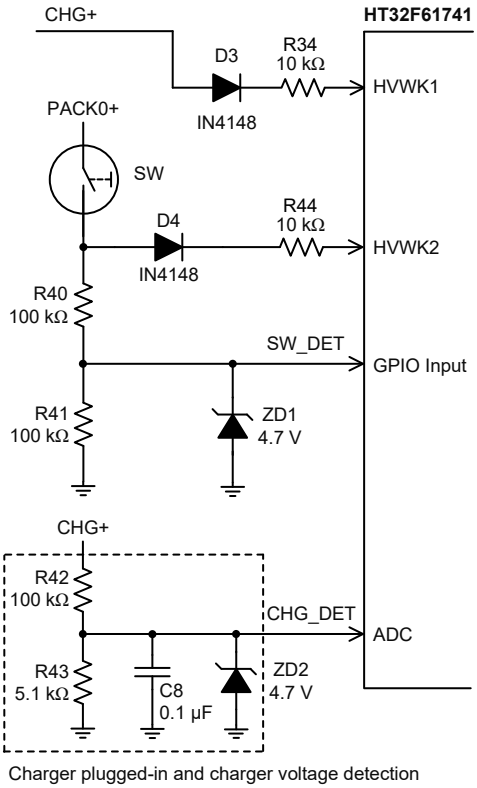


Figure 21. Charger and Switch Status Detection Circuit Diagram

The second circuit is a typical application for charger high-voltage wake-up function, switch low-voltage wake-up function, switch active low detection, charger plugged-in detection and charger voltage detection. The charger detection parts are the same as the diagram above.

For the switch low-voltage wake-up function, the switch detection circuit needs to be changed, which can be obtained from the following application circuit. When the switch is turned on, the Q1 is switched on and the voltage of HVWK is triggered to be larger than V_{WKTH} and set the EXT_WK bit as "1". After the switch is turned off, the Q1 is switched off and the EXT_WK bit is reset to "0".

When the MCU requires to directly detect the switch status, a reverse diode D5 should be connected in series between the SW and SW_DET to prevent the high voltage when the switch is off from entering the MCU pin. The typical value of diode D5 is 1N4148.

In the switch off state, when the MCU has no internal pull-up resistor function, it is recommended to add R45, with a typical value of 10 kΩ.

The resistance values of R41 and R40 should not be too small to avoid the current consumption after the switch is pressed. They must be matched with Q1. When Q1 is MMBT5401, the typical values of R41 and R40 are 100 kΩ.

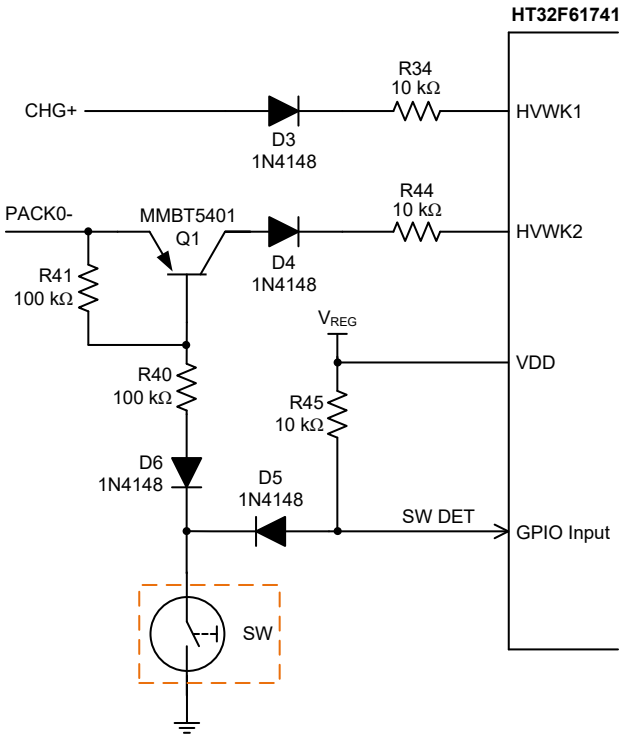


Figure 22. Charger and Switch Low-voltage Wake-up Detection Circuit Diagram

Voltage Spike Suppression Method

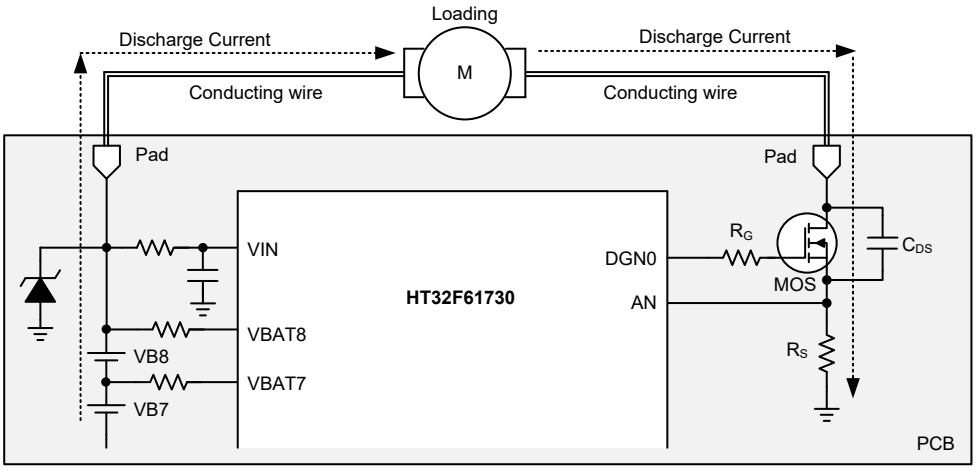


Figure 23. Simplified Typical BMS System Discharge Path Diagram

Most battery-management systems would monitor charge and discharge current to prevent over-current damage. Due to the parasitic inductance on conducting wires and PCB layout connections, large voltage spike may occurs while the controlled MOS rapidly shuts down the charge or discharge current, and this spike may damage the device VBAT1 ~ VBAT8 or VIN pins. Any voltage spike on VBAT1 ~ VBAT8 and VIN pins should not over the limitation in Absolute Maximum Ratings, which is 48 V. Four recommended measures listed below would help to reduce the voltage spike.

1. Make the external conducting wire and PCB layout connections as short as possible where large charge or discharge current flows.
2. Adjust the slew rate of MOS switch with the gate resistor R_G. Turn off the MOS with slower slew rate for lower voltage spike, and the tradeoff is a slower protection response time.
3. Add a capacitor (C_{DS}) between drain and source node of the MOS switch as shown above. The recommended capacitance is 0.1 μF to 0.22 μF.
4. Add a 39 V Zener diode between the highest voltage potential node of battery cells and GND.

System ESD / EFT Protection Circuit Description

Charge / Discharge Circuit

With reference to the following application circuit, connect pull-down resistors R12, R14 and R19 to the device DGCN, DGN0 and DGN1 pins respectively, with typical values of 10 MΩ. Connect resistors R10, R13 and R18 to the MOSFET gate nodes, with typical values of 20 Ω, 10 Ω and 10 Ω. The typical values of C2, C3 and C4 capacitors are 0.1 μF, which can reduce the external electrostatic energy of PACK+, CHG+, CHG- and PACK-. In the PCB layout, the above components should be placed close to the MOSFET pins.

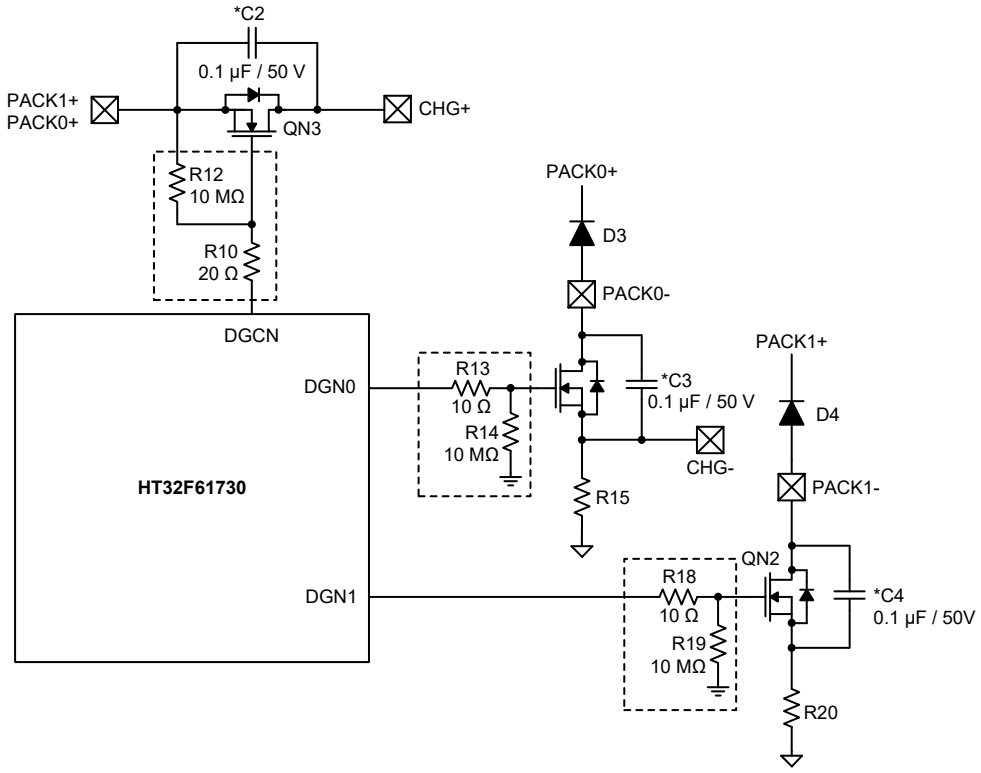


Figure 24. Charge / Discharge Switch Circuit Diagram

Power

The R5 and R7 resistors can reduce the external electrostatic energy of CHG+ and PACK+, which are typically 330 Ω. They should be placed close to the CHG+ and PACK+ terminals in the PCB layout. It should be noted that R5, R7 and R9 limit the VREG maximum current output, and the resistance values of these resistors require to be adjusted according to the actual applications.

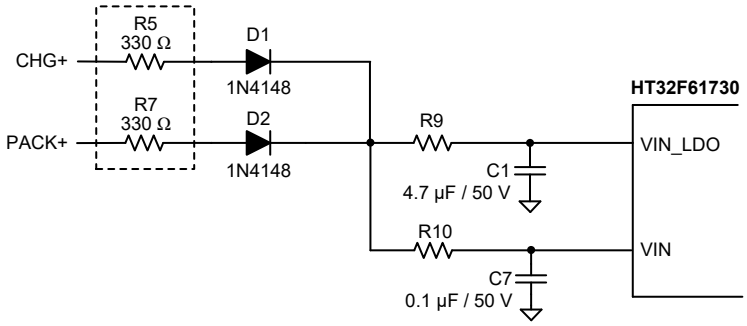


Figure 25. V_{IN} Power Supply Circuit Diagram

Battery Detection Circuit

Add an RBn resistor at each battery cell detection path and add a CBn capacitor to ground near the device VBAT pin, which can limit the reduced electrostatic energy. The typical value of the RBn resistor is 100 Ω, and the typical value of the CBn capacitor is 0.1 μF.

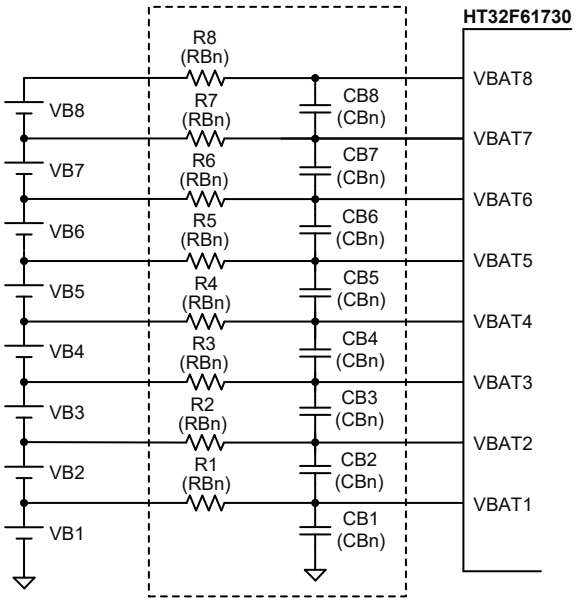


Figure 26. Battery Detection Circuit Diagram

Cell Balance Register Off Method

Time to execute "Cell Balance Register Off":

1. Execute the operation once after the MCU is powered on.
2. When each battery cell measurement procedure is executed, if the difference between the battery cell lowest and highest voltage is greater than 200 mV, it is necessary to execute the "cell balance register off" once and then perform the measurement procedure for each battery cell again to ensure the measurement accuracy. If the voltage difference still exceeds 200 mV, this indicates that the battery is unbalanced.

Considering that two adjacent cell balance registers cannot be on at the same time, it is necessary to turn off the cell balance register according to the following write logic:

1. Write 0x55 to the cell balance register (REG01)
2. Write 0xAA
3. Write 0x00

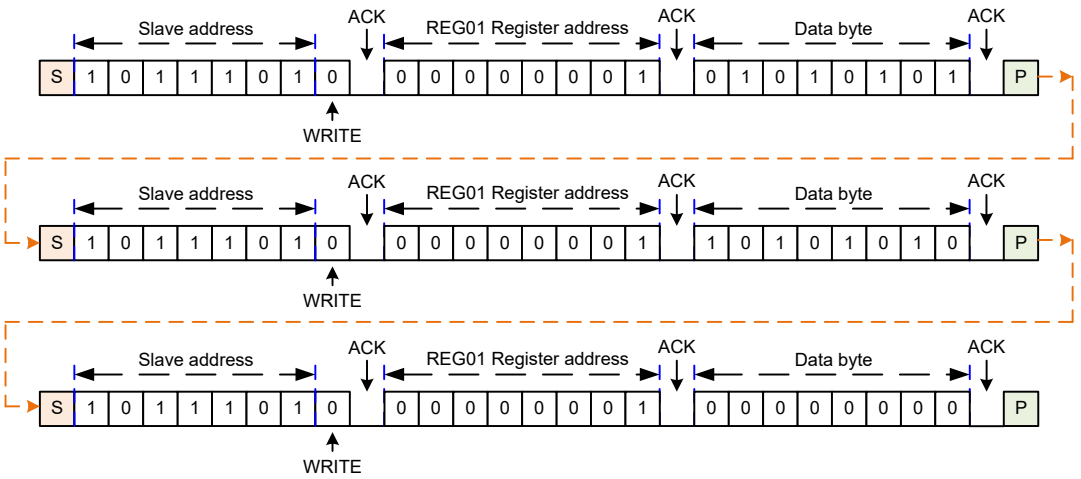


Figure 27. Cell Balance Turn off Timing Diagram

Cell Balance Register On Method

Considering that two adjacent cell balance registers cannot be on at the same time, it is necessary to turn on the cell balance register according to the following write logic:

1. Write 0x55 to the cell balance register (REG01)
2. Write 0xAA
3. Write 0x00
4. Write to the battery cell that needs to be turned on

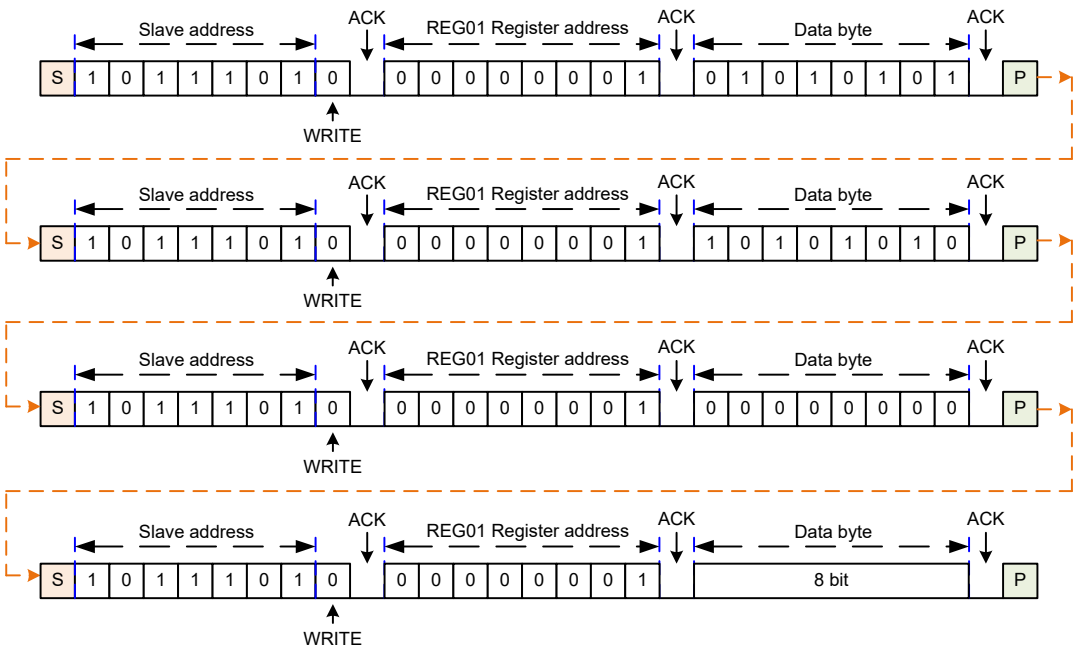


Figure 28. Cell Balance Turn on Timing Diagram

Thermal Considerations

The maximum power dissipation depends upon the thermal resistance of the product package, PCB layout, rate of surrounding airflow and difference between the junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA} (W)$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the product package.

For maximum operating rating conditions, the maximum junction temperature is 125 °C. However, it is recommended that the maximum junction temperature does not exceed 125 °C during normal operation to maintain high reliability. The de-rating curve of the maximum power dissipation is show below:

$$P_{D(MAX)} = (125\ ^\circ C - 25\ ^\circ C) / (58\ ^\circ C/W) = 1.724\ W$$

For a fixed $T_{J(MAX)}$ of 125 °C, the maximum power dissipation depends upon the operating ambient temperature and the package's thermal resistance, θ_{JA}. The de-rating curve below shows the effect of rising ambient temperature on the maximum recommended power dissipation.

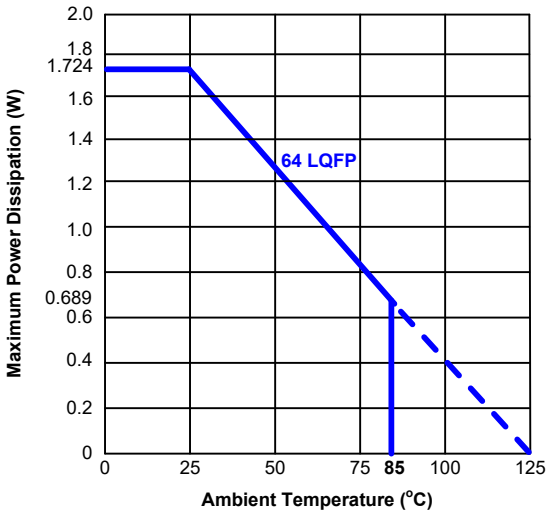


Figure 29. Derating Curve

5 Pin Assignment

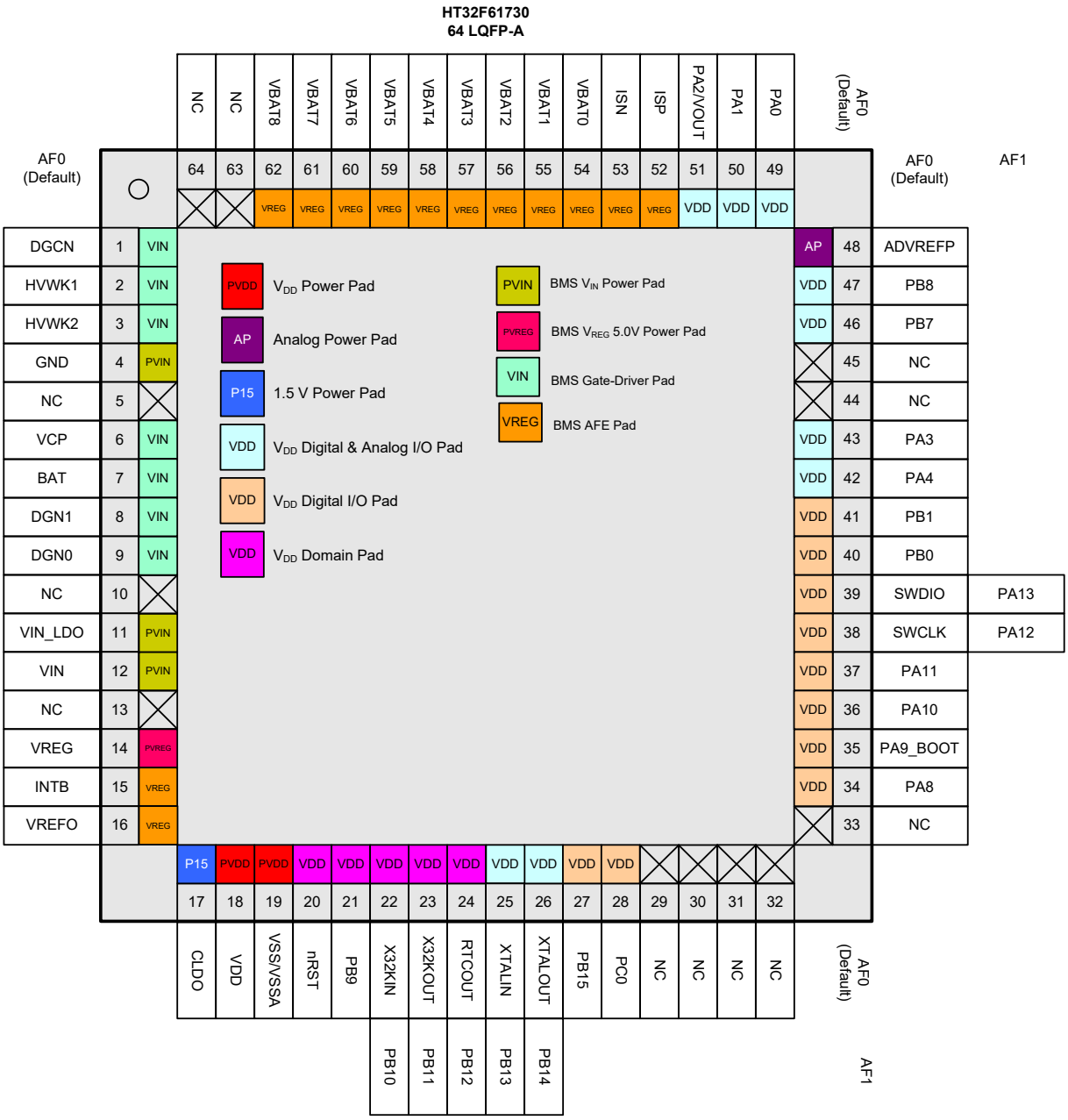


Figure 30. 64-pin LQFP Pin Assignment

Table 12. Pin Assignment

Package	Alternate Function Mapping							
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
64LQFP	System Default	System Other	ADC	LEDC	SCTM	SPI	UART	I²C
49	PA0	VBG	ADC_IN2	LED_SEG0	SCTM1_CH0	SPI_SCK		I2C_SCL
50	PA1		ADC_IN3	LED_SEG1	SCTM1_CH1	SPI_MOSI		I2C_SDA
51	PA2/VOUT(Note)		ADC_IN4	LED_SEG2		SPI_MISO	UR0_TX	
52	ISP							
53	ISN							
54	VBAT0							
55	VBAT1							
56	VBAT2							
57	VBAT3							
58	VBAT4							
59	VBAT5							
60	VBAT6							
61	VBAT7							
62	VBAT8							
1	DGCN							
2	HVWK1							
3	HVWK2							
4	GND							
6	VCP							
7	BAT							
8	DGN1							
9	DGN0							
11	VIN_LDO							
12	VIN							
14	VREG							
15	INTB							
16	VREFO							
17	CLDO							
18	VDD							
19	VSS/VSSA							
20	nRST							
21	PB9	PB9/ WAKEUP1			SCTM0_CH0			
22	X32KIN	PB10		LED_SEG4	SCTM1_CH1	SPI_SEL	UR1_TX	
23	X32KOUT	PB11		LED_SEG5	SCTM1_CH0	SPI_SCK	UR1_RX	
24	RTCOUT	PB12/ WAKEUP0			SCTM0_CH1	SPI_MISO		
25	XTALIN	PB13		LED_SEG6	SCTM2_CH0		UR0_TX	I2C_SCL
26	XTALOUT	PB14		LED_SEG7	SCTM2_CH1		UR0_RX	I2C_SDA

Package	Alternate Function Mapping							
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
64LQFP	System Default	System Other	ADC	LEDC	SCTM	SPI	UART	I²C
27	PB15					SPI_SEL		I2C_SCL
28	PC0			LED_COM0	SCTM1_CH1	SPI_SCK		I2C_SDA
34	PA8			LED_COM1	SCTM2_CH1		UR0_TX	
35	PA9_BOOT	CKOUT			SCTM1_CH0	SPI_MOSI		
36	PA10			LED_COM2	SCTM0_CH0	SPI_MOSI	UR0_RX	
37	PA11			LED_COM3	SCTM0_CH1	SPI_MISO		
38	SWCLK	PA12						
39	SWDIO	PA13						
40	PB0			LED_SEG0	SCTM2_CH0	SPI_MOSI	UR0_TX	I2C_SCL
41	PB1			LED_SEG1	SCTM2_CH1	SPI_MISO	UR0_RX	I2C_SDA
42	PA4		ADC_IN6	LED_SEG4		SPI_SCK	UR1_TX	I2C_SCL
43	PA3		ADC_IN5	LED_SEG3		SPI_SEL	UR0_RX	
46	PB7		ADC_IN0	LED_SEG4	SCTM0_CH0	SPI_MISO	UR0_TX	I2C_SCL
47	PB8		ADC_IN1	LED_SEG5	SCTM0_CH1	SPI_SEL	UR0_RX	I2C_SDA
48	ADVREFP							
5, 10, 13, 29~33, 44, 45, 63, 64	NC							

Note: The Individual Cell Voltage Monitor output VOUT is bonded together internally with PA2.

Table 13. Pin Description

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64LQFP					Default Function (AF0)
49	PA0	AI/O	5V	4/8/12/16 mA	PA0
50	PA1	AI/O	5V	4/8/12/16 mA	PA1
51	PA2/VOUT	AI/O	5V	4/8/12/16 mA	PA2, this pin provides a UART_TX function in the Boot loader mode
			5V	—	VOUT, Voltage monitor output
52	ISP	AI	—	—	AFE current monitor positive terminal voltage input pin. The voltage level of ISP pin should be higher than that of ISN in discharge state
53	ISN	AI	—	—	AFE current monitor negative terminal voltage input pin. Connected to the most negative terminal of battery cells
54	VBAT0	AI	—	—	Battery cell 1 negative terminal
55	VBAT1	AI	—	—	Battery cell 1 positive terminal and battery cell 2 negative terminal
56	VBAT2	AI	—	—	Battery cell 2 positive terminal and battery cell 3 negative terminal
57	VBAT3	AI	—	—	Battery cell 3 positive terminal and battery cell 4 negative terminal
58	VBAT4	AI	—	—	Battery cell 4 positive terminal and battery cell 5 negative terminal
59	VBAT5	AI	—	—	Battery cell 5 positive terminal and battery cell 6 negative terminal
60	VBAT6	AI	—	—	Battery cell 6 positive terminal and battery cell 7 negative terminal
61	VBAT7	AI	—	—	Battery cell 7 positive terminal and battery cell 8 negative terminal
62	VBAT8	AI	—	—	Battery cell 8 positive terminal
1	DGCN	AO	—	—	Gate driver output for driving charge n-MOSFET
2	HVWK1	AI	—	—	High voltage wake-up function sense and trigger pin 1
3	HVWK2	AI	—	—	High voltage wake-up function sense and trigger pin 2
4	GND	P	—	—	Ground terminal
6	VCP	AO	—	—	Charge pump capacitor for DGCN. Connect a capacitor between VCP and BAT
7	BAT	AO	—	—	Charge pump capacitor for DGCN. Connect a capacitor between VCP and BAT
8	DGN1	AO	—	—	Gate driver output 1 for driving discharge n-MOSFET. Recommended for applying on secondary loading path
9	DGN0	AO	—	—	Gate driver output 0 for driving discharge n-MOSFET. Recommended for applying on primary loading path
11	VIN_LDO	P	—	—	Input supply voltage for regulator

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64LQFP					Default Function (AF0)
12	VIN	P	—	—	AFE Gate-drive supply voltage. Connect to the top VBATn
14	VREG	P	—	—	Regulator 5 V / 50 mA output. Connect 4.7 μF capacitor typically
15	INTB	AO	—	—	Interrupt output pin of short-current detection for AFE. NMOS open drain output and output a low level pulse when short-current event is detected. Connect to the EXTIn generally
16	VREFO	AO	—	—	Reference voltage 2.5 V output pin. Connect to the VREF generally.
17	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS
18	VDD	P	—	—	Voltage for digital I/O
19	VSS/VSSA	P	—	—	Ground reference for digital I/O and A/D converter
20	nRST(3)	I	5V_PU	—	External reset
21	PB9(3)	I/O (V_{DD})	5V	4/8/12/16 mA	PB9
22	PB10(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KIN
23	PB11(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KOUT
24	PB12(3)	I/O (V_{DD})	5V	4/8/12/16 mA	RTCOUT
25	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
26	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
27	PB15	I/O	5V	4/8/12/16 mA	PB15
28	PC0	I/O (V_{DD})	5V	4/8/12/16 mA	PC0
34	PA8	I/O (V_{DD})	5V	4/8/12/16 mA	PA8
35	PA9	I/O (V_{DD})	5V_PU	4/8/12/16 mA	PA9_BOOT
36	PA10	I/O (V_{DD})	5V	4/8/12/16 mA	PA10
37	PA11	I/O (V_{DD})	5V	4/8/12/16 mA	PA11
38	PA12	I/O (V_{DD})	5V_PU	4/8/12/16 mA	SWCLK
39	PA13	I/O (V_{DD})	5V_PU	4/8/12/16 mA	SWDIO
40	PB0	I/O (V_{DD})	5V	4/8/12/16 mA	PB0
41	PB1	I/O (V_{DD})	5V	4/8/12/16 mA	PB1

Pin Number 64LQFP	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description Default Function (AF0)
42	PA4	AI/O	5V	4/8/12/16 mA	PA4
43	PA3	AI/O	5V	4/8/12/16 mA	PA3, this pin provides a UART_RX function in the Boot loader mode
46	PB7	AI/O	5V	4/8/12/16 mA	PB7
47	PB8	AI/O	5V	4/8/12/16 mA	PB8
48	ADVREFP	P	—	—	Positive reference voltage for the ADC
5, 10, 13, 29~33, 44, 45, 63, 64	NC	—	—	—	Not connected

Note: 1. I = input, O = output, A = Analog port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, the UART interface is available for communication.

Interconnection Signal Description

The MCU generated signals such as the SCTM0 channel output and SCTM2 channel output have been internally connected to the Individual Cell Voltage Monitor for control purpose. The connections are listed in the following table and the related control registers should be configured correctly using application program.

Table 14. Internal Connection Signal Lines

MCU Signal Name	Individual Cell Voltage Monitor Signal Name	Description
PC7	DCN	Gate-driver DGCN control input (Note). The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
PC5/SCTM2_CH1 (SCTM2)	DN1	Gate-driver DGN1 control input (Note). If the SCTM2_CH1 output is used, the MCU AFIO setting should be AF4 to select the SCTM pin function.
PC6	SCL	Individual Cell Voltage Monitor I^2C serial clock input line. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
PC4	SDA	Individual Cell Voltage Monitor I^2C serial data input / output line. The MCU AFIO setting should be AF0 to select the General Purpose Input / Output pin function.
PB3/SCTM0_CH0 (SCTM0)	DN0	Gate-driver DGN0 control input (Note). If the SCTM0_CH0 output is used, the MCU AFIO setting should be AF4 to select the SCTM pin function.
PA5/ADC_IN7 (ADC)	IMON	Current monitor output pin. Voltage of ISP-ISN multiplied by 10 or 50 is outputted. If the ADC_IN7 output is used, the MCU AFIO setting should be AF2 to select the ADC pin function.

Note: Internal pull down with 370 kΩ.

6 Electrical Characteristics

Power Supply Scheme

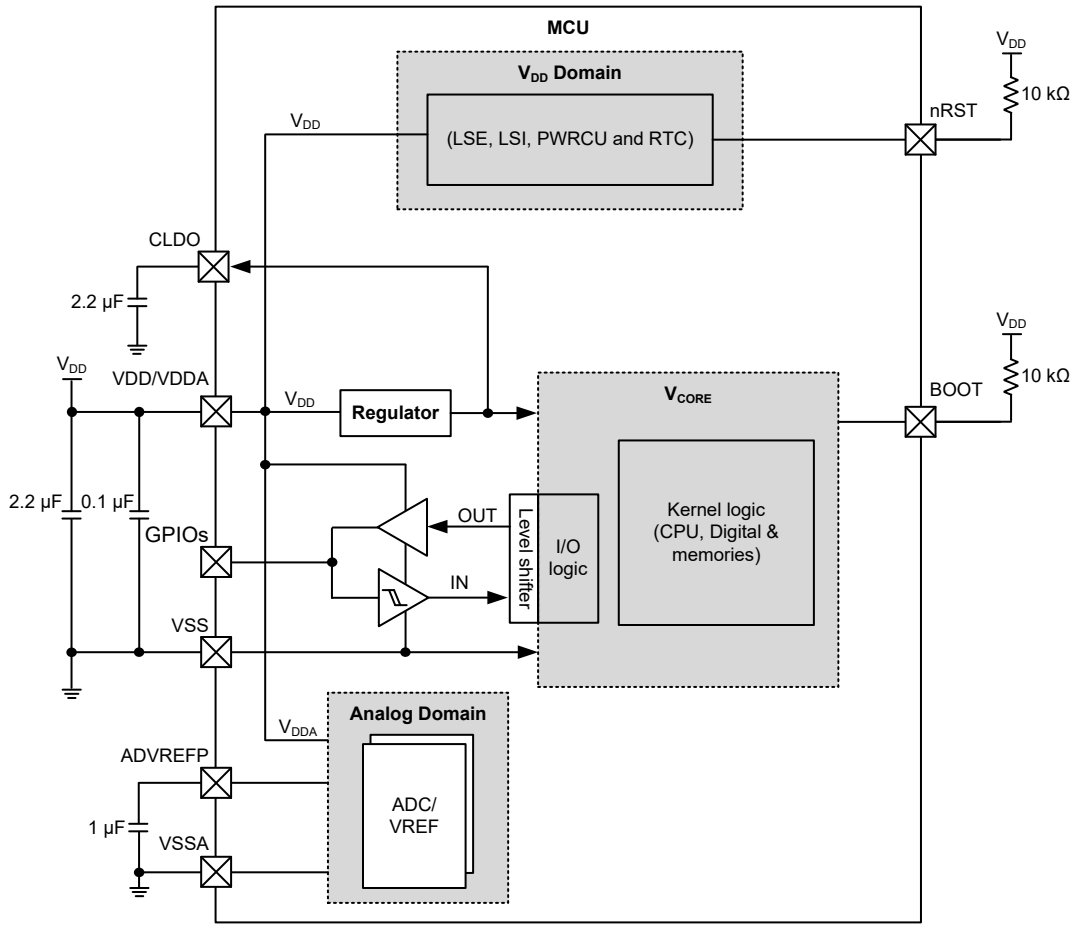


Figure 31. Power Supply Scheme

Note: 1. All regulator capacitors must be placed as close to the MCU as possible.
2. It is recommended that the pull-up resistor of the BOOT pin is 10 kΩ.
3. It is recommended that the pull-up resistor of the nRST pin is 10 kΩ.

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 15. Absolute Maximum Ratings

Symbol	Value	Unit
V_{DD}	(Vss-0.3) to (Vss+5.5)	V
Input Voltage	(Vss-0.3) to (V_{DD}+0.3)	V
T_A	-40 to 85	°C
T_{STG}	-60 to 150	°C
T_J	< 125	°C
P_D	< 500	mW
VIN, VIN_LDO,HVWK1,HVWK2, BAT	-0.3 to 48	V
DGCN, VCP	-0.3 to 60	V
DGN0, DGN1	-0.3 to 18	V
VREG, VOUT, ISP, ISN, IMON, INTB, VREFO	-0.3 to 5.5	V
Δ[VBATi ~ VBAT(i-1)], i=8~1	-0.3 to 5.5	V
Electrostatic Discharge Voltage (Human Body Model)	-2000 to 2000	V

Recommended DC Operating Conditions

Table 16. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
$V_{ADVREFP}$	ADC Positive Reference Voltage	—	2.5	5.0	5.5	V

Note: The $V_{ADVREFP}$ power voltage needs below or equal to the V_{DD} power voltage.

Recommended Operating Ratings

Table 17. Table xx. Recommended Operating Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input supply voltage for regulator	—	7.5	—	36	V
T_A	Operating Temperature Range	—	-40	—	85	°C

Note: Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specified performance limits.

On-Chip LDO Voltage Regulator Characteristics

Table 18. LDO Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{LDO} = 12 mA and voltage variant = ±5 %, After trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	12	15	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

The current consumption is influenced by several parameters and factors, including the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is configured under the following conditions for current consumption measured:

- All I/O pins are set to a high-impedance (floating) state.
- All peripherals are disabled unless specifically stated otherwise.
- The Flash memory access time is optimized using the minimum wait states number, depending on the f_{HCLK} frequency.
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$.

Table 19. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max @ T_A		Unit
						25 °C	85 °C	
I_{DD}	Supply Current (Run Mode)	16 MHz	V_{DD} = 5 V HSI = 16 MHz	All peripherals enabled	3.35	3.60	—	mA
				All peripherals disabled	2.75	2.95	—	
		8 MHz	V_{DD} = 5 V HSI = 16 MHz	All peripherals enabled	1.88	2.02	—	
				All peripherals disabled	1.57	1.69	—	
		32 kHz	V_{DD} = 5 V LSI = 32 kHz LDO in LCM Mode	All peripherals enabled	26.39	32.72	—	μA
				All peripherals disabled	25.13	31.42	—	
	Supply Current (Sleep Mode)	16 MHz	V_{DD} = 5 V HSI = 16 MHz	All peripherals enabled	1.16	1.24	—	mA
				All peripherals disabled	0.44	0.48	—	
		8 MHz	V_{DD} = 5 V HSI = 16 MHz	All peripherals enabled	0.77	0.83	—	
				All peripherals disabled	0.41	0.45	—	
	Supply Current (Deep-Sleep1 Mode)	—	V_{DD} = 5 V, HSI/HSE clock off, LDO in LCM Mode, LSE off, LSI on, RTC on		20.27	26.39	—	μA
	Supply Current (Deep-Sleep2 Mode)	—	V_{DD} = 5 V, HSI/HSE clock off, LDO off, DMOS on, LSE off, LSI on, RTC on		3.45	5.14	—	μA

Note: 1. HSE means high speed external oscillator. HSI means 16 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real-time clock.
4. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 20. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	2.22	2.35	2.48	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})		2.12	2.2	2.33	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.

2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 21. LVD / BOD Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed, V_{DD} falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3.53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 5.0 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 5.0 V	—	—	200	—	μs
I_{DDLVD}	Operation Current (2)	V_{DD} = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.

2. Bandgap current is not included.

3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 22. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSE}	HSE Frequency	V_{DD} = 2.5 V ~ 5.0 V	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 5.0 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	12	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	V_{DD} = 5.0 V	—	0.5	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 0	—	—	110	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 5.0 V, R_{ESR} = 100 Ω, C_L = 12 pF @ 8 MHz, HSEGAIN = 0	—	0.85	—	mA
		V_{DD} = 5.0 V, R_{ESR} = 25 Ω, C_L = 12 pF @ 16 MHz, HSEGAIN = 1	—	3.0	—	
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 5.0 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 5.0 V	—	—	4	ms

Table 23. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 2.5 V ~ 5.5 V	—	32.768	—	kHz
R_F	Internal feedback resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V	30	—	TBD	kΩ
C_L	Recommended load capacitances	V_{DD} = 5.0 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L ≥ 7 pF, V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L < 7 pF, V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 2.5 V ~ 5.5 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 24. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSI}	HSI Frequency	V_{DD} = 5 V @ 25 °C	—	16	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 2.5 V ~ 5.5 V, T_A = 25 °C	-1	—	1	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = -25 °C ~ 85 °C	-2.5	—	2	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = -40 °C ~ 85 °C	-4	—	3	%
Duty	Duty Cycle	f_{HSI} = 16 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 16 MHz @ V_{DD} = 2.5 V ~ 5.5 V	—	—	140	μA
	Power Down Current		—	—	0.01	μA
T_{SUHSI}	HSI Oscillator Startup Time	f_{HSI} = 16 MHz	—	—	20	μs

Table 25. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{LSI}	LSI Frequency	V_{DD} = 5.0 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	V_{DD} = 5.0 V, with factory-trimmed	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 5.0 V	—	0.5	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 5.0 V	—	—	100	μs

Memory Characteristics

Table 26. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before Failure (Endurance)	T_A = -40 °C ~ 85 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 27. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	5.0 V I/O	$V_I = V_{SS}$, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	5.0 V I/O	$V_I = V_{DD}$, On-chip pull-down resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	5.0 V I/O		-0.5	—	V_{DD} × 0.35	V
		Reset pin		-0.5	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	5.0 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	mV
I_{OL}	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V_{OL} = 0.6 V		4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.6 V		8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OL} = 0.6 V		12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OL} = 0.6 V		16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	4	—	mA
		5.0 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	8	—	mA
		5.0 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	12	—	mA
		5.0 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		—	16	—	mA
V_{OL}	Low Level Output Voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.6	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.6	V
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.6	V
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.6	V
V_{OH}	High Level Output Voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.6	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.6	—	—	V
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA		V_{DD} - 0.6	—	—	V
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA		V_{DD} - 0.6	—	—	V
R_{PU}	Internal Pull-up Resistor	V_{DD} = 5.0 V		—	50	—	kΩ
R_{PD}	Internal Pull-down Resistor	V_{DD} = 5.0 V		—	50	—	kΩ

ADC Characteristics

Table 28. ADC Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.5	5.0	5.5	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Positive Reference Voltage	—	—	—	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 5.0 V, 500 ksps	—	1.4	1.5	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 5.0 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	8	MHz
f_S	Sampling Rate	—	50	—	500	ksps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	Bits
INL	Integral Non-linearity Error	f_S = 500 ksps, V_{DDA} = 5.0 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 500 ksps, V_{DDA} = 5.0 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

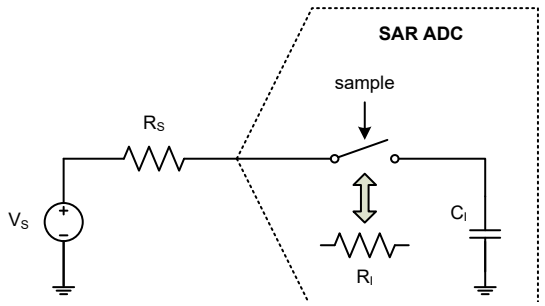


Figure 32. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF+}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Internal Reference Voltage Characteristics

Table 29. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		2.8	—	5.5	V
V_{REF}	Internal Reference Voltage after Factory Trimming, @ T_A = 25 °C	V_{DDA} ≥ 2.8 V	VREFSEL[1:0] = 00	2.44	2.50	2.56	V
		V_{DDA} ≥ 3.3 V	VREFSEL[1:0] = 01	2.92	3.00	3.08	
		V_{DDA} ≥ 4.3 V	VREFSEL[1:0] = 10	3.90	4.00	4.10	
		V_{DDA} ≥ 4.8 V	VREFSEL[1:0] = 11	4.39	4.50	4.61	
ACC_{VREF}	Reference Voltage Accuracy after Trimming	V_{DDA} = 2.8 V ~ 5.5 V, V_{REF} = 2.5 V, T_A = -40 °C ~ 85 °C		-2	—	+2	%
t_{STABLE}	Reference Voltage Stable Time	—		—	—	100	ms
t_{SREFV}	ADC Sampling Time when Reading Reference Voltage	—		10	—	—	μs
I_{DD}	Operating Current	—		—	50	70	μA
I_{DDPWD}	Power Down Current	—		—	—	0.01	μA

Note: 1. Data based on characterization results only, not tested in production.
2. The trimming bits of the internal reference voltage are 7-bit resolution.

SCTM Characteristics

Table 30. SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	Bits

Individual Cell Voltage Monitor Electrical Characteristics

Table 31. Individual Cell Voltage Monitor Electrical Characteristics

V_{IN} = 36 V, C_{REG} = 4.7 μF, T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply and Input						
V_{IN}	Supply Voltage	—	7.5	—	36	V
$I_{IN(STB)}$	Supply Current (Standby)	EN_S = EN_VREF = IMCE = ISCE = '0', EN_OTD = '0', DN0 = DN1 = DCN = '0'	—	3.5	6	μA
$I_{IN(STB\_DSG)}$	VIN Supply Current with DGN0 and Short Current Detection is Activated	EN_S = EN_VREF = IMCE = EN_OTD = '0', ISCE = '1', DN0 = '1', DN1 = DCN = '0'	—	18	20	μA
I_{OPR_DGNx}	VIN Operating Current when DGN0 and DGN1 Outputs are On	DN0 = DN1 = '1', DCN = '0'	—	15	—	μA
I_{SLP}	Standby Current in SLEEP Mode	SLP1 = '0', SLP0 = '1', V_{HVWK} = 0 V	—	0.1	0.2	μA
Voltage Regulator						
V_{REFO}	Regulator Output Voltage	I_{LOAD} = 10 mA	4.95	5	5.05	V
I_{REG}	Regulator Maximum Output Current	V_{IN} = 7.5 V, T_A = - 40 ~ 85 °C	50	—	—	mA
ΔV_{REG}	Load Regulation	I_{LOAD} = 0 ~ 50 mA	—	—	50	mV
$\frac{\Delta V_{REG}}{(V_{REG} \times \Delta V_{IN})}$	Line Regulation	V_{IN} = 7.5 ~ 36 V, I_{LOAD} = 10 mA	—	0.02	—	%/V
$\frac{\Delta V_{REG}}{(V_{REG} \times \Delta T_A)}$	V_{REG} Temperature Coefficient	I_{LOAD} = 1 mA, T_A = -40 ~ 85°C	—	±100	—	ppm/°C
R_{DIS}	V_{REG} Discharge Resistance	SLP1 = '0', SLP0 = '1', V_{REG} = 1 V, I_{REG1} denotes VREG input current at V_{REG} = 1 V, R_{DIS} = V_{REG} / I_{REG1}	—	330	—	Ω
Cell Balancer						
R_{CB}	Cell Balance Resistance	V_{Bi} = 4.5 V (i = 1 ~ 8), VBATi series resistors = 0 Ω	80	110	140	Ω
		V_{Bi} = 2.5 V (i = 1 ~ 8), VBATi series resistors = 0 Ω	120	160	200	Ω
Reference Voltage						
V_{REFO}	Reference Voltage	EN_VREF = '1'	2.492	2.5	2.508	V
$\frac{\Delta V_{REFO}}{(V_{REFO} \times \Delta T_A)}$ (Note)	VREFO Temperature Coefficient	I_{LOAD} = 1 μA, T_A = -40 ~ 85 °C	—	—	±15	mV
I_{VREFO_SOUR}	VREFO Pin Output Source Current	C_{VREFO} = 0.1 μF. Peak current at EN_VREF '0' → '1' rising edge	—	2	—	mA
I_{VREFO_SINK}	VREFO Pin Output Sink Current	C_{VREFO} = 0.1 μF. Peak current at EN_VREF '1' → '0' falling edge	—	1	—	mA
t_{S_VREFO}	VREFO Pin Settling Time	Settling time from V_{REFO} = 0 V to 2.475 V. C_{VREFO} = 30 pF	—	20	30	μs
Input/Output Logic						
R_{PD}	DN0, DN1, DCN Pull Down Resistance	—	—	370	—	kΩ
$V_{L(INTB)}$	INTB 'Low' Output Voltage	Load current = 500 μA, V_{REG} = 5V	—	—	0.1	V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{PU_INTB}	INTB Pulled High to VREG Resistance	—	—	50	—	kΩ
High Voltage Wake-Up						
V_{WKTH}	HVWK1 and HVWK2 Threshold Voltage	—	—	5.5	—	V
T_{WKDB}	HVWK1 and HVWK2 Debounce Time	—	1	—	—	ms
I_{WK}	HVWK1 and HVWK2 Input Current	V_{HVWK} = 36 V	—	50	—	μA
Cell Voltage Monitor						
V_{Bi}	Cell Voltage	i = 1 ~ 8	1.5	—	4.5	V
$V_{B(MIN)}$	Input Voltage between VBATi and VBATi-1 for Cell Voltage Monitoring	—	—	1.5	—	V
$I_{Bi(PWR)}$	Cell Input Leakage Current when VIN Powered	V_{Bi} = 5 V (i = 1 ~ 8). EN_S = '0'. V_{IN} = V_{BAT8}	-0.1	—	0.1	μA
$I_{Bi(ACT)}$	Cell Input Current when Voltage Monitoring	V_{Bi} = 4.2 V × i. EN_S bit = '1'. V_{IN} = 36 V. i = 1 ~ 8	—	15	—	μA
V_{OUT_VM}	Cell Voltage Monitor Output Accuracy	V_{Bi} - V_{Bi-1} = 4.2 V. i = 1 ~ 8, T_A = 25°C	2.094	2.100	2.106	V
		V_{Bi} - V_{Bi-1} = 4.2 V. i = 1 ~ 8. T_A = -40 ~ 85°C	2.092	2.100	2.108	V
I_{VOUT_SOUR}	Cell Voltage Monitor Output Source Current	V_{Bi} - V_{Bi-1} = 4.2 V. i = 1 ~ 8. C_{VOUT} = 0.1 μF, Peak current at EN_S '0' → '1' rising edge	—	2	—	mA
I_{VOUT_SINK}	Cell Voltage Monitor Output Sink Current	V_{Bi} - V_{Bi-1} = 4.2 V. i = 1 ~ 8. C_{VOUT} = 0.1 μF. Peak current at EN_S '1' → '0' falling edge	—	1	—	mA
HS Gate Charge Pump						
V_{CP_UVLO+}	V(VCP, BAT) Turn On Level	V(VCP,BAT) rises	—	3	—	V
V_{CP_UVLO-}	V(VCP, BAT) Turn Off Level	V(VCP,BAT) falls	—	2.5	—	V
V_{CP}	VCP Output Voltage	EN_CP = '1', BAT = V_{IN} > 13 V	V_{IN} + 10	V_{IN} + 12	V_{IN} + 16	V
t_{CP_ON}	Rising Time of the Voltage Difference between VCP and VBAT	External capacitor 22 nF between VCP and BAT. V_{IN} = 36 V, V(VCP, BAT) rises from 10 % to 90 % (V_{CP} - V_{BAT}) (Note)	—	25	—	ms
f_{CP}	Charge Pump Switching Frequency	EN_CP = '1'	—	600	—	kHz
Gate Drivers						
V_Z	DGNx Clamp Voltage	DNx = '1', V_{IN} > 13 V	10	12	16	V
		DNx = '1', V_{IN} ≤ 13 V	—	V_{IN} - 0.7	—	V
t_r	DGNx Rising Time	C_{DGNx} = 15 nF (Note)	—	0.5	1.0	μs
t_f	DGNx Falling Time	C_{DGNx} = 15 nF (Note)	—	0.5	1.0	μs
t_{PD_HL}	DGNx Falling Propagation Delay Time	C_{DGNx} = 15 nF (Note)	—	0.5	1.0	μs
t_{PD_LH}	DGNx Rising Propagation Delay Time	C_{DGNx} = 15 nF (Note)	—	0.5	1.0	μs
t_{MM}	DGNx Delay Time Mismatch	C_{DGNx} = 15 nF, t_{MM} = $\lvert t_{PD\_LHx} - t_{PD\_HLx} \rvert$	—	0.5	1.0	μs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{SOURCE}	DGNx Source Current	C_{DGNx} = 1 μF, peak current at DNx '0' → '1' rising edge	—	850	—	mA
I_{SINK}	DGNx Sink Current	C_{DGNx} = 1 μF, peak current at DNx '1' → '0' falling edge	—	850	—	mA
R_{PL_S}	DGNx Pull Low Resistance at Sleep and Standby Mode	DNx = '0', SLP1 = '0' & SLP0 = '1' & HVWKx = '0' or HVWKx = '1', resistance between DGNx and GND	—	10	—	Ω
V_{DGCN_ON}	DGCN Gate Drive Turn-on Voltage	EN_CP = '1', DCN = '1'	—	V_{CP}	—	V
V_{DGCN_OFF}	DGCN Gate Drive Turn-off Voltage	EN_CP = '1', DCN = '0'	—	V_{IN}	—	V
R_{DGCN_ON}	DGCN Gate Drive Turn-on Resistance	EN_CP = '1', DCN = '1'	—	2	—	kΩ
R_{DGCN_OFF}	DGCN Gate Drive Turn-off Resistance	EN_CP = '1', DCN = '0'	—	150	—	Ω
t_{rC}	Rising Time of the Voltage Difference between DGCN and BAT	EN_CP = '1', $C_{DGCN-BAT}$ = 15 nF, V_{IN} = 36 V, V(DGCN, BAT) rises from 10 % to 90 % (V_{DGCN} - V_{BAT}) (Note)	—	220	—	μs
t_{fC}	Falling Time of the Voltage Difference between DGCN and BAT	EN_CP = '1', $C_{DGCN-BAT}$ = 15 nF, V_{IN} = 36 V, V(DGCN, BAT) falls from 90 % to 10 % (V_{DGCN} - V_{BAT}) (Note)	—	5	—	μs

Note: These parameters are periodically sampled but not 100% tested.

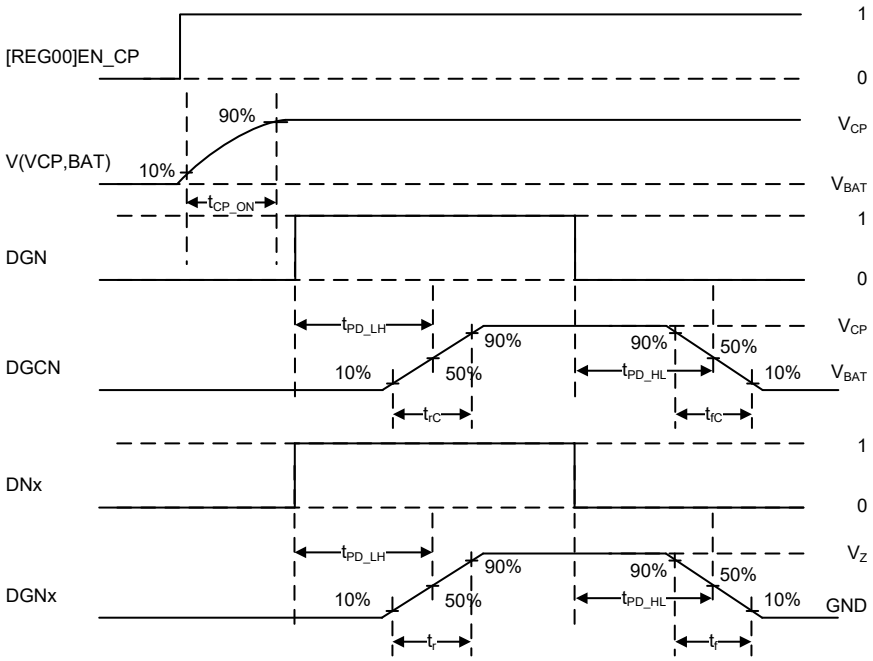


Figure 33. Individual Cell Voltage Monitor Characteristics

Table 32. Individual Cell Voltage Monitor Electrical Characteristics (ISP-ISN Shunt Resistor = 5 mΩ)

V_{IN} = 36 V, C_{REG} = 4.7 μF, T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Current Monitor						
$G_{IM(R10)}$	IMON Output Voltage Amplify Rate	IMCE = '1', IAR = '0', T_A = 25 °C	9.7	10	10.3	V/V
		IMCE = '1', IAR = '0', T_A = -40 ~ 85 °C	9.5	10	10.5	V/V
$G_{IM(R50)}$		IMCE = '1', IAR = '1', T_A = 25 °C	48.5	50	51.5	V/V
		IMCE = '1', IAR = '1', T_A = -40 ~ 85 °C	47.5	50	52.5	V/V
$I_{MR(R10)}$	Current Monitor Range	IMCE = '1', IAR = '0', V_{REG} = 5 V, V_{REFO} = 2.5 V, shunt resistor = 5 mΩ	-6	—	36	A
		IMCE = '1', IAR = '0', V_{REG} = 5 V, V_{REFO} = 2.5 V, shunt resistor = 2 mΩ	-15	—	90	A
$I_{MR(R50)}$		IMCE = '1', IAR = '1', V_{REG} = 5 V, V_{REFO} = 2.5 V, shunt resistor = 5 mΩ	-1.2	—	6.6	A
		IMCE = '1', IAR = '1', V_{REG} = 5 V, V_{REFO} = 2.5 V, shunt resistor = 2 mΩ	-3.0	—	16.5	A
$V_{IMO(R10)}$	IMON Output Voltage at No Sensing Current	V_{ISP} - V_{ISN} = 0 V, IMCE = '1', ZERO = '0', IAR = '0'	0.3	0.5	0.7	V
$V_{IMO(R50)}$		V_{ISP} - V_{ISN} = 0 V, IMCE = '1', ZERO = '0', IAR = '1'	0.3	0.5	0.85	V
$V_{IMZ(R10)}$	IMON Output Voltage at ZERO State	IMCE = '1', ZERO = '1', IAR = '0'	0.3	0.5	0.7	V
$V_{IMZ(R50)}$		IMCE = '1', ZERO = '1', IAR = '1'	0.3	0.5	0.85	V
$I_{IMO(SOURCE)}$	IMON Output Source Current	—	100	—	—	μA
$I_{IMO(SINK)}$	IMON Output Sink Current	—	100	—	—	μA
$t_{IMZS(R10)}$	IMON Settling Time at ZERO State	IAR = '0', ZERO = '1', timing from IMCE = '1' to V_{IMON} settled at V_{IMZ}	—	—	100	μs
$t_{IMZS(R50)}$		IAR = '1', ZERO = '1', timing from IMCE = '1' to V_{IMON} settled at V_{IMZ}	—	—	500	μs
I_{IS}	ISP, ISN Input Current	V_{ISP} = V_{ISN} = 0 V, IAR = '0', ZERO = '0'	—	-0.46	—	μA
$t_{IMR\_P(R10)}$	IMON Output Rising Time (V_{ISP}>V_{ISN})	IAR = '0', ZERO = '0', IMCE = '1', V_{ISN} = 0 V, V_{ISP} rises from 0 V to 0.1 V in 10 μs	—	60	—	μs
$t_{IMR\_P(R50)}$		IAR = '1', ZERO = '0', IMCE = '1', V_{ISN} = 0 V, V_{ISP} rises from 0V to 0.1 V in 10 μs	—	300	—	μs
$t_{IMF\_P(R10)}$	IMON Output Falling Time (V_{ISP}>V_{ISN})	IAR = '0', ZERO = '0', IMCE = '1', V_{ISN} = 0 V, V_{ISP} falls from 0.1 V to 0 V in 10 μs	—	60	—	μs
$t_{IMF\_P(R50)}$		IAR = '1', ZERO = '0', IMCE = '1', V_{ISN} = 0 V, V_{ISP} falls from 0.1 V to 0 V in 10 μs	—	300	—	μs
$t_{IMR\_N(R10)}$	IMON Output Rising Time (V_{ISP}<V_{ISN})	IAR = '0', ZERO = '0', IMCE = '1', V_{ISP} = 0 V, V_{ISN} rises from 0 V to 0.1 V in 10 μs	—	60	—	μs
$t_{IMR\_N(R50)}$		IAR = '1', ZERO = '0', IMCE = '1', V_{ISP} = 0 V, V_{ISN} rises from 0 V to 0.1 V in 10 μs	—	300	—	μs
$t_{IMF\_N(R10)}$	IMON Output Falling Time (V_{ISP} < V_{ISN})	IAR = '0', ZERO = '0', IMCE = '1', V_{ISP} = 0 V, V_{ISN} falls from 0.1 V to 0 V in 10 μs	—	30	—	μs
$t_{IMF\_N(R50)}$		IAR = '1', ZERO = '0', IMCE = '1', V_{ISP} = 0 V, V_{ISN} falls from 0.1 V to 0 V in 10 μs	—	30	—	μs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Short-Current Detection						
V_{SCTH}	Short Circuit Detection Threshold voltage	ISCE = '1', SC_[2:0] = 0b001	—	105	—	mV
t_{SCDB}	Short Circuit Detection Debounce Time	ISCE = '1', TD_[4:0] = 0b00001 (default value)	—	6.32	—	μs
t_{SCPD}	Short Circuit Detection Propagation Delay Time	ISCE = '1', TD_[4:0] = 0b00000, INTB sink current = 50 μA. Propagation delay time from V_{ISP} > V_{SCTH} to INTB pulled 'Low'	—	1	—	μs
Over-Temperature Detection						
T_{OTD}	Over-temperature Detection Threshold	EN_OTD = '1', OTDTH[1:0] = 0b00	—	85	—	°C
		EN_OTD = '1', OTDTH[1:0] = 0b01	—	100	—	°C
		EN_OTD = '1', OTDTH[1:0] = 0b10	—	125	—	°C
		EN_OTD = '1', OTDTH[1:0] = 0b11 (default value)	—	150	—	°C
T_{HYS}	Over-temperature Detection Hysteresis	EN_OTD = '1'	—	20	—	°C

Individual Cell Voltage Monitor I²C Interface Characteristic

Table 33. Individual Cell Voltage Monitor I²C Interface Characteristic

V_{IN} = 36 V and T_A = 25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Clock Frequency	—	—	—	400	kHz
t_{BUF}	Bus Free Time	Bus free time between STOP and START	1.3	—	—	μs
$t_{HD:STA}$	START Hold Time	After this period, the first clock pulse is generated	0.6	—	—	μs
t_{LOW}	SCL Low Time	—	1.3	—	—	μs
t_{HIGH}	SCL High Time	—	0.6	—	—	μs
$t_{SU:STA}$	START Setup Time	Only relevant for REPEATED START	0.6	—	—	μs
$t_{HD:DAT}$	Data Hold Time	—	0	—	—	ns
$t_{SU:DAT}$	Data Setup Time	—	100	—	—	ns
t_R	Rising Time	SDA and SCL	—	—	0.3	μs
t_F	Falling Time	SDA and SCL	—	—	0.3	μs
$t_{SU:STO}$	STOP Setup Time	—	0.6	—	—	μs
t_{AA}	Output Valid from Clock	—	—	—	0.9	μs
t_{SP}	Input Filter Time Constant	SDA and SCL noise suppression time	—	—	20	ns
t_{OUT}	I²C Time-out	—	—	32	—	ms

Note: These parameters are periodically sampled but not 100% tested.

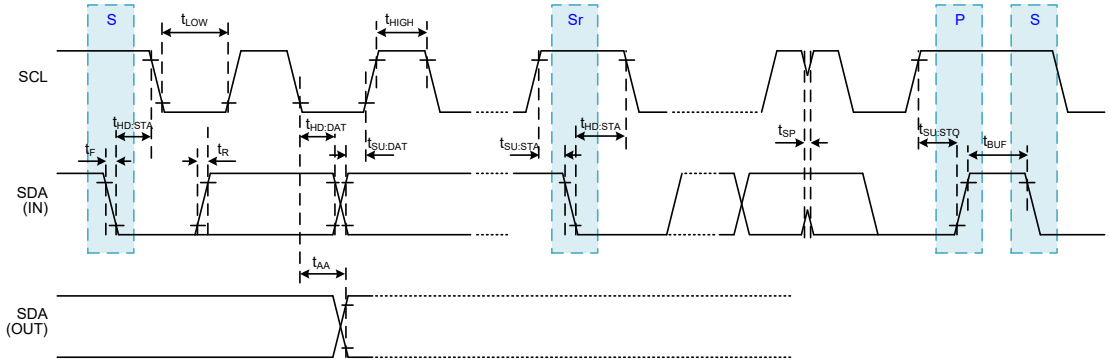


Figure 34. Individual Cell Voltage Monitor I²C Timing Diagram

I²C Characteristics

Table 34. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	—	1.6	—	0.475	—	0.25	μs
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.

2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 16 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

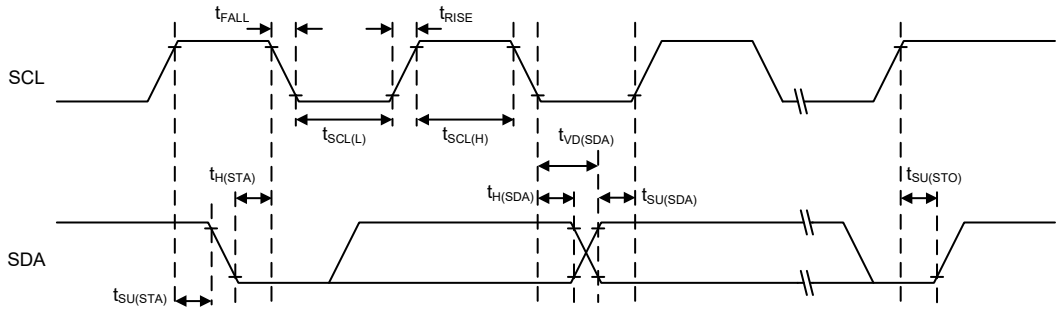


Figure 35. I²C Timing Diagram

SPI Characteristics

Table 35. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

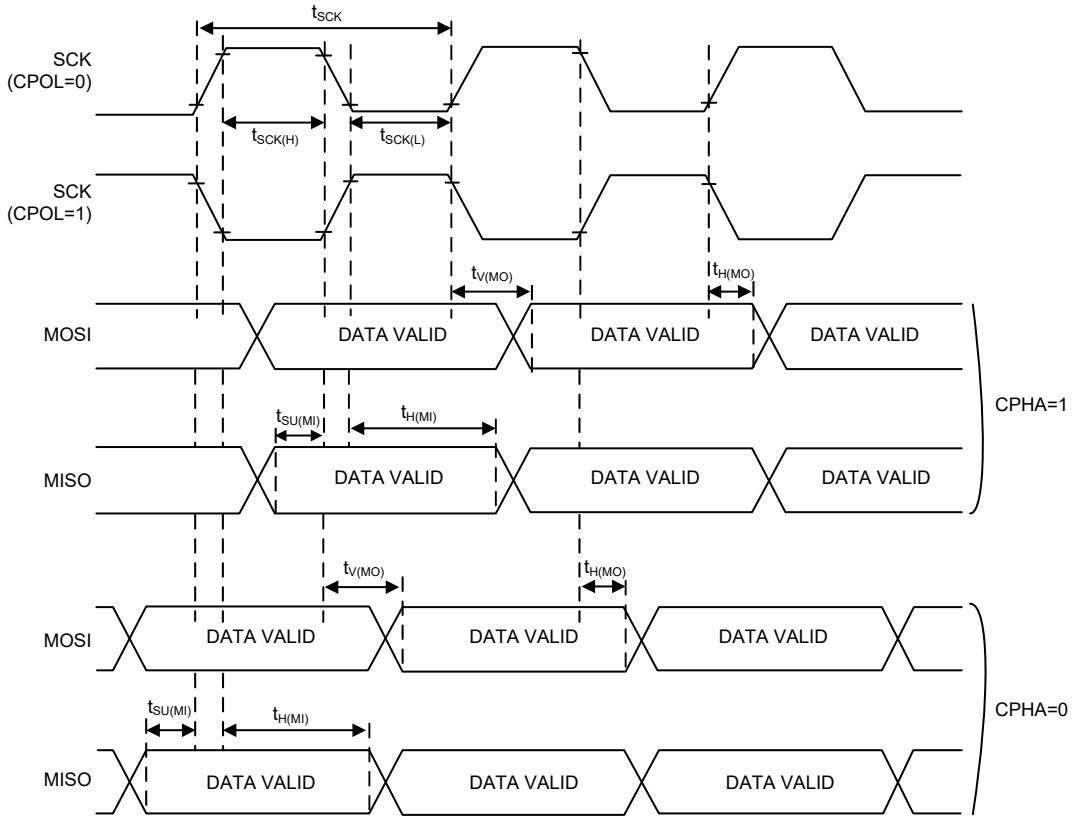


Figure 36. SPI Timing Diagram – SPI Master Mode

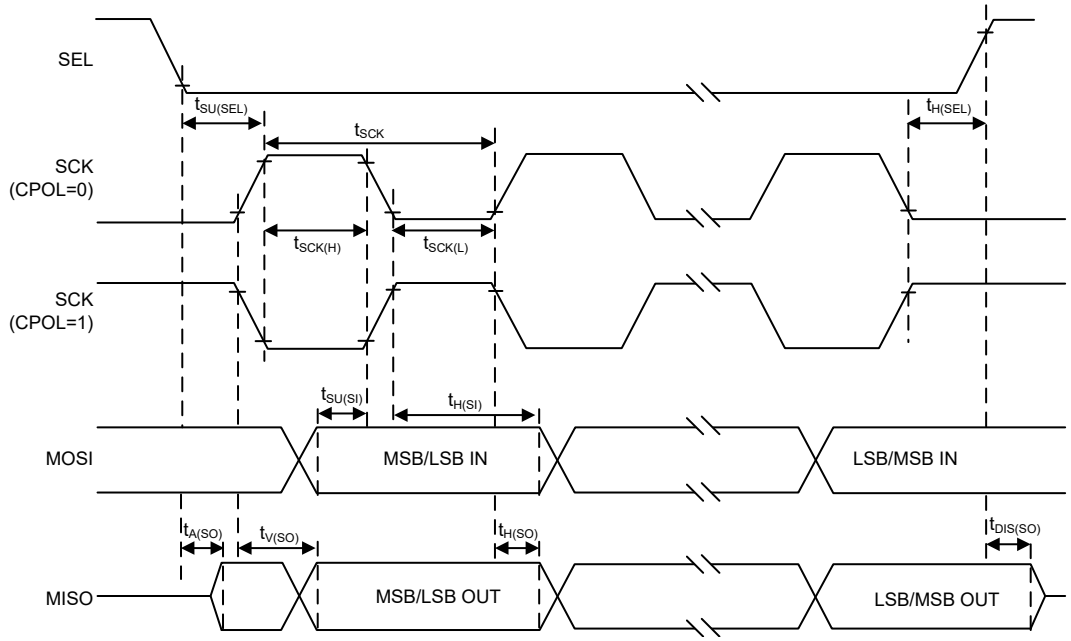


Figure 37. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

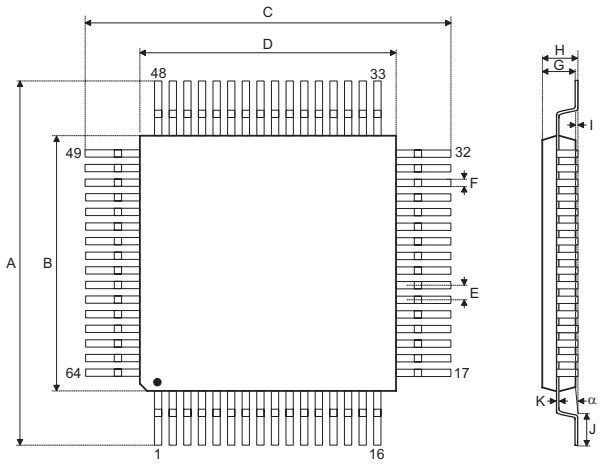
7 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

64-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.016 BSC	
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.40 BSC	
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°