HOLTEK

HT32F65433A Datasheet

32-Bit Arm® Cortex®-M0+ BLDC Motor Microcontroller with 36 V Half-bridge P/N Gate-Driver, 32 KB Flash and 8 KB SRAM with 2 Msps ADC, CMP, OPA, PGA, PDMA, DIV, UART, SPI, I²C, MCTM, GPTM, SCTM, BFTM, CRC, UID, LSTM and WDT

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1 General Description

The Holtek HT32F65433A device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. The device provides 32 KB of embedded Flash memory for code/data storage and 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, PDMA, ADC, OPA, PGA, CMP, I^2C, UART, SPI, MCTM, GPTM, SCTM, BFTM, CRC-16/32, 96-bit Unique ID, LSTM, WDT, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The device also includes a gate-driver for 3-phase motor driving applications. The gate-driver has several internal protection functions and provides an integrated 5 V low quiescent current LDO which can provide power supply for internal and external circuits.

The above features ensure that the device is suitable for use in floor fans, air purifiers, water pumps, fans and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- 32 KB on-chip Flash memory for instruction/data and option byte storage
- 8 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions, pre-fetch buffer and branch cache for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power On Reset / Power Down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 5.0 V operating voltage and 25 ºC operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a Low Speed Internal RC oscillator (LSI), a Phase Lock Loop (PLL), clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from HSI, LSI or system PLL. The Watchdog Timer (WDT) and Low Speed Timer (LSTM) use the LSI as their clock source.

Power Management – PWRCU

- V_{DD} power supply: 2.5 V to 5.5 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} and V_{CORE} power domains
- Two power saving modes: Sleep and Deep-Sleep modes

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides two types of power saving modes such as Sleep and Deep-Sleep modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

Gate-Driver

- 3-Channel Half-Bridge Driver: Driver 3 High-Side P-type MOSFETs and 3 Low-Side N-type MOSFETs
- Motor Power Supply Range V_{CC}: 6.0 V to 32 V
- Maximum Motor Sustainable Voltage up to 36 V
- Integrated 50 mA LDO with 5.0 V ±2.0 % Accuracy
- Low Sleep Current $\leq 2\ \mu A$ ($V_{REG} = 0\ V$)

- Support clamping voltage of |12VGS| when High-Side P-type MOSFETs and Low-Side N-type MOSFETs are conducted
- Integrated Dead time with 120 ns
- Support external signal wake-up, implementing ultra-low power consumption when the device in the SLEEP mode
- FG High-Voltage Open-Drain Output, providing Motor Speed Information
- Gate Driving Current Capability
    - 0.35 A Peak Source Current
    - 0.5 A Peak Sink Current
- Supports both CMOS/TTL Logic
- Protection Features
    - V_{CC} Power Supply Input Under Voltage Lock-Out (VCC_UVLO)
    - 5 V LDO Output Under Voltage Lock-Out (VREG_UVLO)

External Interrupt/Event Controller – EXTI

- Up to 8 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 8 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR A/D engines
- Up to 2 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are multiplexed channels, which include 12 external channels on which the external analog signal can be supplied and 1 internal channels. If the input voltage is required to remain within a specific threshold window, the Analog Watchdog function will monitor and detect the signals. An interrupt will then be generated to inform the device that the input voltage is higher or lower than the preset thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D conversion can be operated in one shot, continuous and discontinuous conversion mode.

Programmable Gain Amplifier – PGA

- Each programmable gain amplifier has fixed dedicated I/O pins
- Internal output path to A/D converter or comparator
- 5-bit scaler can be configurable for input offset calibration

The PGA has dedicated input/output pins, which are the input pair of PGAnN and PGAnP, and an analog output pin of PGAnO. The analog output signals can also be connected internally to the ADC analog channels or the Comparator positive input.

Operational Amplifier – OPA

- Fixed dedicated I/O pins
- Internal output paths to the A/D converter or comparator
- Input offset calibration

An operational amplifier is integrated in the device.

Comparator – CMP

- Two Rail-to-rail comparators
- Each comparator has configurable negative or positive inputs used for flexible voltage selection
  - Dedicated I/O pins
  - Internal voltage reference provided by 8-bit scaler – For CMP0 only
  - Internal operational amplifier output
- Programmable hysteresis
- Programmable respond speed and power consumption
- Comparator output can be routed to I/O pin, to multiple timer or ADC trigger input
- 8-bit scaler can be configured to dedicated I/O for voltage reference
- Configurable inverting input from CMP0N, CMP1N or CVREF
- Interrupt generation capability with wakeup from Sleep or Deep-Sleep mode through the EXTI controller

Two general purpose comparators, CMP, are implemented within the device. They can be configured either as standalone comparators or combined with the different kinds of peripheral IP. Each comparator is capable of asserting interrupts to the NVIC or waking up the CPU from the Sleep or Deep-Sleep mode through the EXTI wakeup event management unit.

I/O Ports – GPIO

- Up to 24 GPIOs
- Port A, B, C are mapped to 8-line EXTI interrupts
- Almost I/O pins are configurable output driving current

There are up to 24 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Compare Match Output
- PWM waveform generation with edge-aligned and center-aligned counting modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Break input to force the timer's output signals into a reset state or in a known state

The Motor Control Timer Module, MCTM, consists of a single 16-bit up/down counter, four 16-bit Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR), one 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes which include output waveform generation for signals such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and break input.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with edge-aligned and center-aligned counting modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder and Pulse/Direction Mode
- Master/Slave mode controller

The General-Purpose Timer, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM outputs. The GPTM also supports an encoder interface using a quadrature decoder with two inputs.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with edge-aligned counting mode

The Single Channel Timer, SCTM, consists of one 16-bit up-counter, one 16-bit Channel 0 Capture / Compare Register (CH0CCR), one 16-bit Counter-Reload Register (CRR), one 16-bit Channel 1 Capture Register (CH1CCR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM outputs.

Basic Function Timer – BFTM

- 16-bit compare match up-counter – no I/O control
- One shot mode – stops counting when compare match occurs
- Repetitive mode – restarts counter when compare match occurs

The Basic Function Timer, BFTM, is a simple 16-bit up-counting counter designed to measure time intervals, generate one shot pulses or generate repetitive interrupts. The BFTM can operate in two modes which are repetitive and one shot modes. In the repetitive mode, the counter is restarted at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with a 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Registers write protection function

The Watchdog Timer is a hardware timing circuitry that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Low Speed Timer – LSTM

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Low Speed Timer, LSTM, circuitry includes the APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. The LSTM circuits are located in the V_{CORE} power domain. When the device enters the power-saving mode, the LSTM counter is used as a wakeup timer to let the system resume from the power saving mode.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Supports 7-bit addressing mode and general call addressing
- Supports two 7-bit slave addresses

The I²C module is an internal circuit allowing communication with an external I²C interface which is an industry standard two-wire serial interface used for connection to external hardware. These two serial lines are known as a serial data line SDA, and a serial clock line SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode; 400 kHz in the Fast mode; 1 MHz in the Fast plus mode. The SCL period generation registers are used to set different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for master mode and (f_{PCLK}/3) MHz for slave mode
- FIFO Depth: 4 levels

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamlined data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication capability
- Supports LIN (Local Interconnect Network) mode
- Supports single-wire mode
- Fully programmable serial communication characteristics including:
    - Word length: 7, 8 or 9-bit character
    - Parity: Even, odd or no-parity bit generation and detection
    - Stop bit: 1 or 2 stop bits generation
    - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,

  $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,

  $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,

  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger sources:

  ADC, UART, GPTM, SCTM and software request

The Peripheral Direct Memory Access circuitry, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error flag

The divider is the truncated division and requires a software triggered start signal by controlling the “START” bit in the control register. The divider calculation complete flag will be set to 1 after 8 clock cycles, however, if the divisor register data is zero during the calculation, the division by zero error flag will be set to 1.

Unique Identifier – UID

- Total 96-bit UID is unique and not duplicate with other HT32 MCU devices
- It is unchangeable and determined by MCU manufacturer

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 28-pin SSOP, 32-pin QFN and 48-pin LQFP-EP packages
- Operation temperature: -40 °C to 105 °C

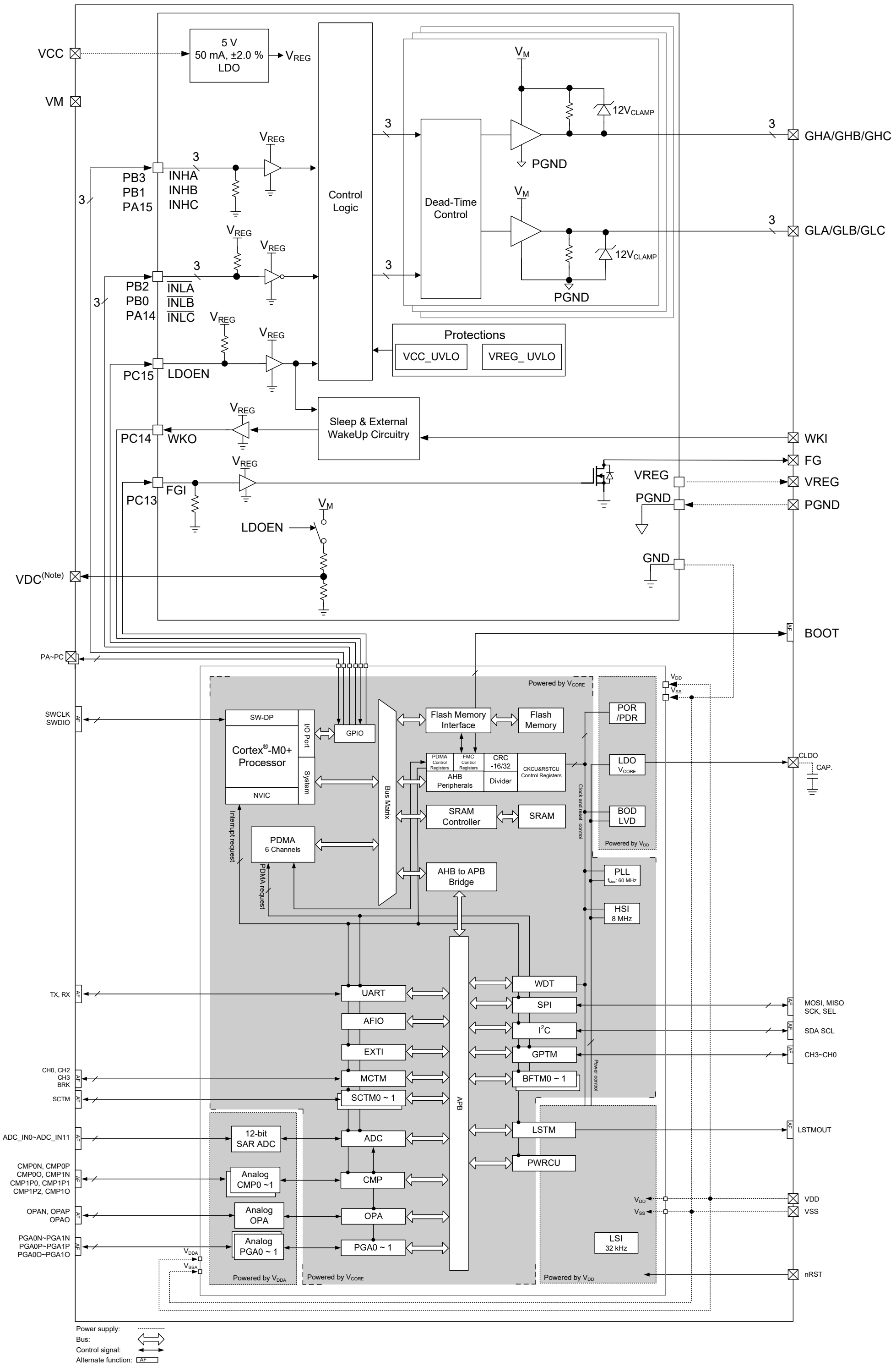
3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F65433A
Main Flash (KB)		31
Option Bytes Flash (KB)		1
SRAM (KB)		8
Timers	MCTM	1
	GPTM	1
	SCTM	2
	BFTM	2
	LSTM	1
	WDT	1
Communication	UART	1
	SPI	1
	I²C	1
PDMA		6 channels
Hardware Divider		1
CRC-16/32		1
EXTI		8
12-bit 2 Msps ADC		1
Number of channels		12 external channels
CMP		2
Programmable Gain Amplifer		2
Operational Amplifier		1
Gate-Driver		1
GPIO		24 (Max.)
CPU frequency		Up to 60 MHz
Supply voltage (V_{CC})		6 V ~ 32 V
Operating voltage (V_{DD})		2.5 V ~ 5.5 V
5 V LDO output drive current		50 mA
Operating temperature		-40 C ~ 105 °C
Package		28-pin SSOP, 32-pin QFN and 48-pin LQFP-EP

Block Diagram



Note: For the 28-pin SSOP and 32-pin QFN packages, the VDC and PA0/ADC_IN7 lines are connected internally.

Figure 1. Block Diagram

Memory Map

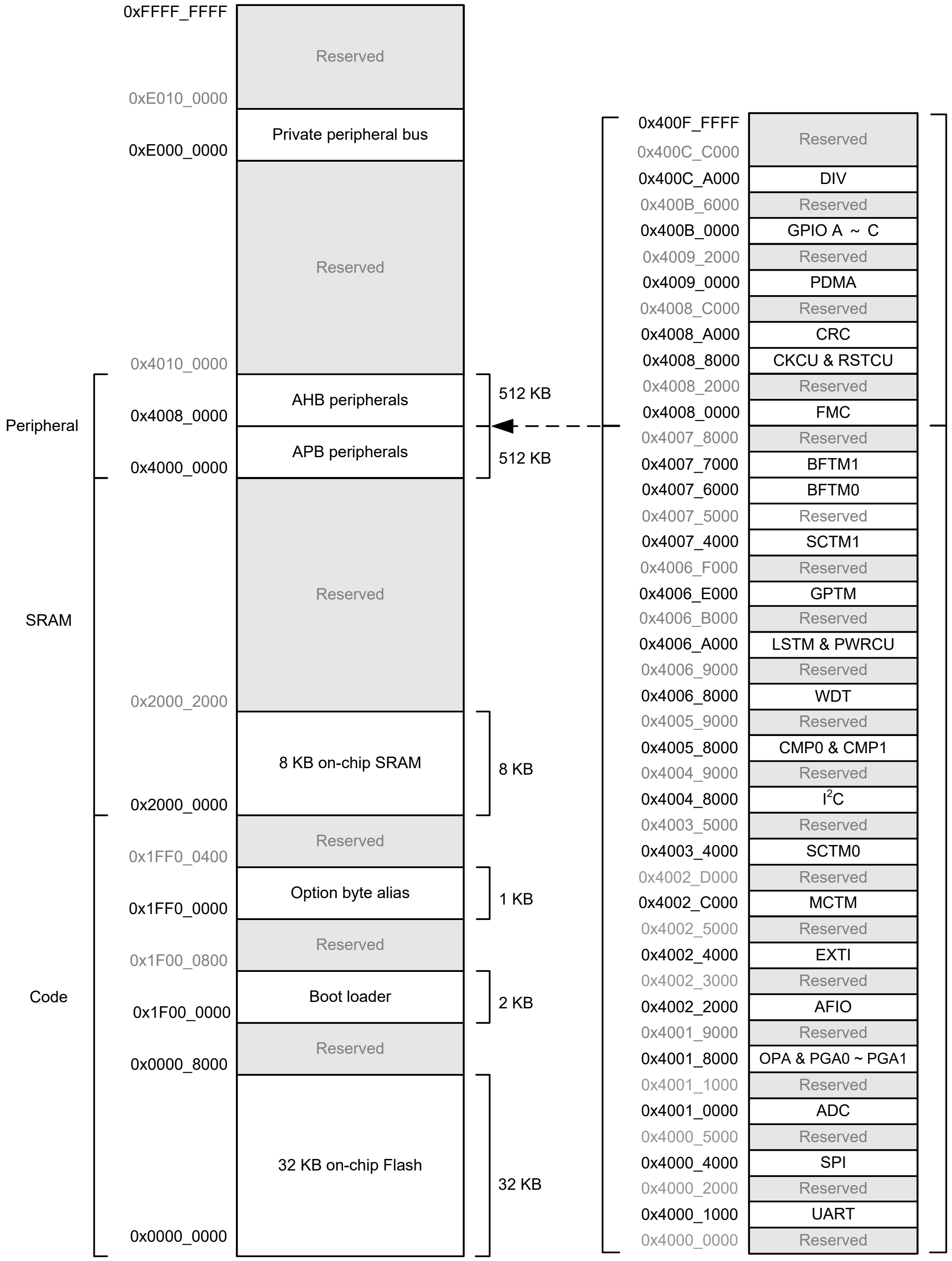


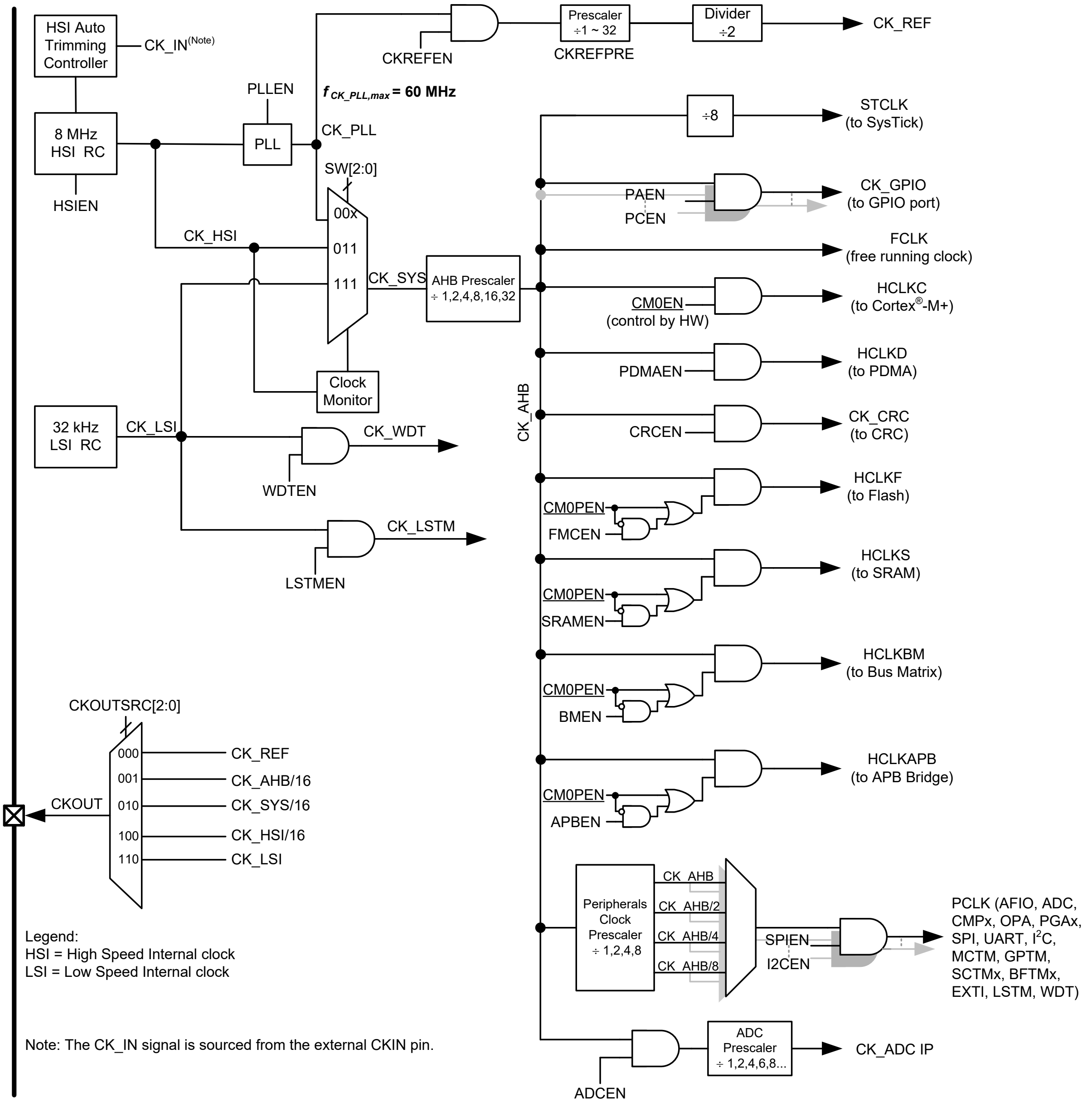
Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	Reserved	APB
0x4000_1000	0x4000_1FFF	UART	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4001_7FFF	Reserved	
0x4001_8000	0x4001_8FFF	OPA & PGA0 ~ PGA1	
0x4001_9000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^{2}C	
0x4004_9000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	CMP0 & CMP1	
0x4005_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	LSTM & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure



Legend:
HSI = High Speed Internal clock
LSI = Low Speed Internal clock

Note: The CK_IN signal is sourced from the external CKIN pin.

Figure 3. Clock Structure

4 Gate-Driver

The device includes a 3-channelgate-drivers, which can be used for high-side P-type MOSFETs and low-side N-type MOSFETs driving. It includes a 5 V LDO, 3-channel high-side and low-side gate-driver circuits. The device also has two protection functions, which are V_{CC} Power Supply Input Under Voltage Lock-Out and 5 V LDO Output Under Voltage Lock-Out, to avoid abnormal output situations.

The input signals of INHx, $\overline{\text{INLx}}$ and LDOEN are input to the control logic which will determine the high-side and low-side gate-driver outputs. The INHx has an internal pull-down resistor and the $\overline{\text{INLx}}$ has an internal pull-up resistor. Additionally, there is a fixed dead time insertion when switching between the high-side and low-side gate driving to avoid short-circuit between V_M and ground.

The gate-driver output voltage will vary with the power supply. The gate-driver provides 0.35 A peak source current and 0.5 A peak sink current when V_{CC} is 24 V. Either high-side and low-side gate has an internal hold-off resistor in order to avoid error conduction of external power MOSFET due to interference when the power is off.

The gate-driver also provide a high voltage open-drain output FG signal, providing information about rotation speed of the motor.

In addition, if the gate-driver enters the SLEEP mode, all functions will be turned off to greatly reduce the sleep current. It is important not to confuse this SLEEP mode with the Sleep mode which is described in the "Power Management Control Unit" section of this datasheet.

Voltage Regulator

The integrated 5 V LDO can supply power for both internal and external circuits, with a output current over 50 mA. The LDO will act as a fully turned on switch when the power supply V_{CC} is less than 5 V, in which condition its output voltage is almost equal to the power supply if there is no load.

Gate-Driver Control Logic

As a gate-driver for driving high-side P-type MOSFETs and low-side N-type MOSFETs, the control signals are input from LDOEN, INHx, $\overline{\text{INLx}}$. Usually a 6-wire input control method is used, where the dead time width is determined by the control signals but has a minimum value equal to the fixed dead time designed in the gate-driver.

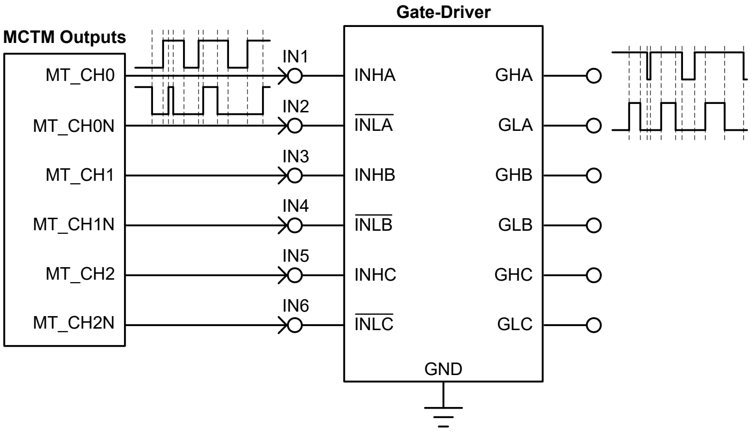


Figure 4. 6-Wire Control

Both high-side and low-side gate-driver outputs are controlled by the LDOEN, INHx and $\overline{\text{INLx}}$ input signals. For example, the on/off true table of the external power MOSFETs is shown as follows.

Table 3. Gate-Driver Operation Truth Table

LDOEN	INHx	$\overline{\text{INLx}}$	GHx-to-PGND	GLx-to-PGND	V_{REG}	External High-Side Power MOSFET	External Low-Side Power MOSFET
0	X	X	H	L	0V	OFF	OFF
1	0	0	H	H	V_{REG}	OFF	ON
1	0	1	H	L	V_{REG}	OFF	OFF
1	1	0	H	L	V_{REG}	OFF	OFF
1	1	1	L	L	V_{REG}	ON	OFF

X: No care; L: Low; H: High

Protection Function Operation

When the device operates in an abnormal situation, such as a V_{CC} Power Supply Input Under Voltage Lock-Out or 5 V LDO Output Under Voltage Lock-Out condition has occurred, it will activate the corresponding protection mechanism to turn off the affected power MOSFET. The protection mechanisms are summarized below.

Table 4. Protection Function Conditions

Protection	Protection Entry Condition	Protection Reaction			Release Condition
		V_{REG}	GHx-to-PGND	GLx-to-PGND	
VCC_UVLO	$V_{CC} < V_{CC\_UVLO-}$	0V	H	L	$V_{CC} \geq V_{CC\_UVLO+}$
VREG_UVLO	$V_{REG} < V_{REG\_UVLO-}$	—	H	L	$V_{REG} \geq V_{REG\_UVLO+}$

L: Low; H: High

Note: The LDO will not be turned off after the protection is triggered.

V_{CC} Power Supply Input Under Voltage Lock-Out – VCC_UVLO

This integrated protection function is to avoid unstable gate-driver output when the power supply voltage falls to a certain low level. During V_{CC} power-on period, both high-side and low-side power MOSFETs are turned off and the LDO is in the sleep state and the LDO output is 0 V before the power supply voltage reaching the threshold V_{CC_UVLO+}. When the power supply voltage is greater than V_{CC_UVLO+}, the gate-driver outputs are determined by the input signals, the LDO is woken-up and the LDO output is determined by the input signals. If the power supply voltage falls below the under voltage lock-out threshold V_{CC_UVLO-}, both high-side andlow-side power MOSFETs will remain off and the LDO will enter sleep state and output 0V.

5 V LDO Output Under Voltage Lock-Out – VREG_UVLO

When the internal 5 V LDO output voltage, V_{REG}, is too low, the integrated 5 V LDO output under voltage lock-out function will be activated to avoid unstable signals input to the gate-driver. After V_{REG} exceeds the threshold V_{REG_UVLO+}, the gate-driver output is determined by the input signals. If V_{REG} is less than the under voltage lock-out threshold V_{REG_UVLO-}, both high-side and low-side power MOSFETs will remain off.

Ultra-low Power Consumption

When the control signal LDOEN is cleared to zero, the LDO will be turned off, that is, the system power in the V_{REG} domain will be turned off. In the SLEEP mode, the current consumption is less than 2 µA, the gate-driver will wait for an external wake-up signal by monitoring the WKI pin. Once a valid wake-up signal on the WKI pin is triggered, if the voltage level is boosted by more than 4 V within 1 ms, the LDO output will be restored and the system will return to normal operation.

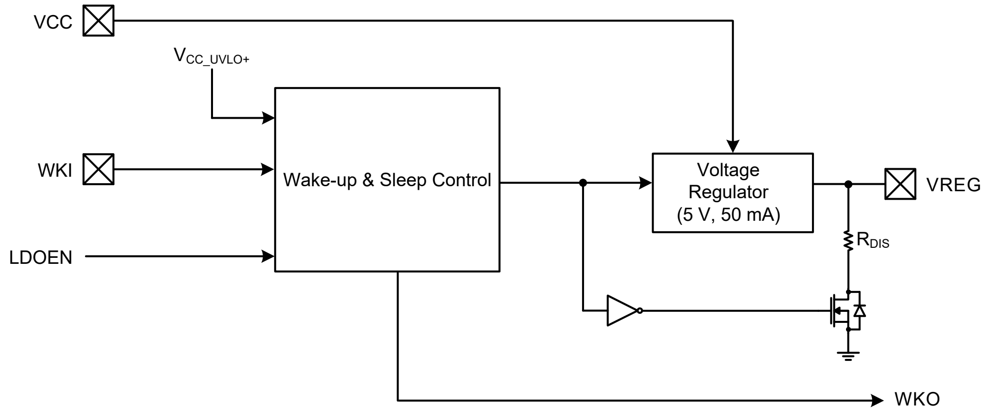


Figure 5. Enter the SLEEP Mode and Wake-up Function Block Diagram

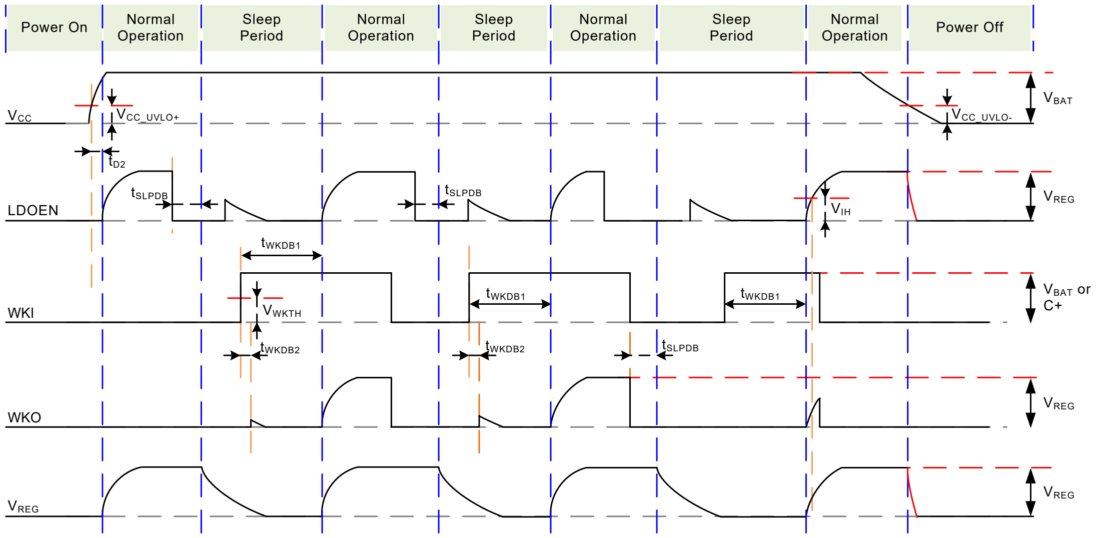


Figure 6. Enter the SLEEP Mode and Wake-up Function Timing

After V_{CC} power on, the gate-driver waits for VREG to rise up. The control signal LDOEN reset to ‘0’, VREG turns off. Whether VREG is turned on or not, WKI can control WKO signal.

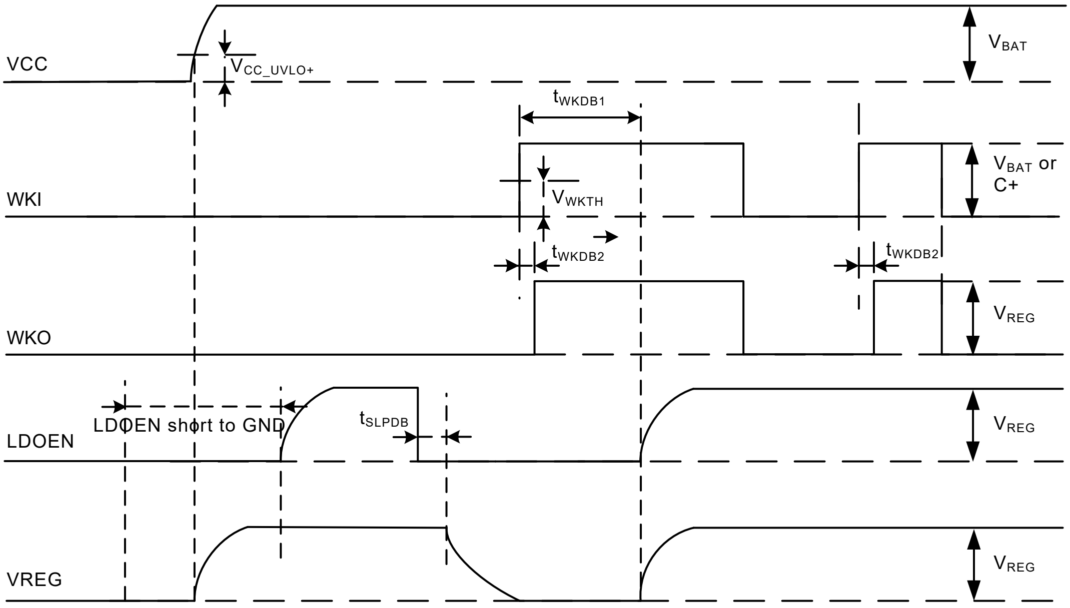


Figure 7. After Power on Enter SLEEP Mode and WKI Control WKO Timing

FG High Voltage Motor Speed Signal

The gate-driver provides a high-voltage open-drain mechanism, which can convert the low-voltage signal input from the FGI to a high-voltage signal and output it to the FG pin. This mechanism provides an external interface to monitor the motor speed signal. When FGI input is high level, the FG output will be 0 V, and when FGI input is low, the FG output is in high impedance state.

Table 5. FG Output Truth Table

LDOEN	FGI	FG
LDOEN = ‘0’	X	Z
LDOEN = ‘1’	‘1’	L
LDOEN = ‘1’	‘0’	Z

X: No care; L: Low; Z: High impedance

Component Selections

Gate Resistor Circuit

The main function of the gate resistors, R_{G1}, R_{G2}, R_{G3} and R_{G4}, is to reduce the vibration of U, V, W output voltages and reduce the EMI noise generation. Adjusting R_{G1} and R_{G3} controls the on time of the high-side and low-side switches, adjusting R_{G2} and R_{G4} controls the off time of the high-side and low-side switches. The gate resistors are optional and can be used according to the requirements.

It is recommended to select the gate resistance value according to the desired gate voltage rising time (t_r) or falling time (t_f), which are shown in the figure below. R_{G1}, R_{G2}, R_{G3} and R_{G4}, if used, are recommended to have a typical value of 10 Ω ~ 200 Ω. It is recommended to use a 1N4148 switch diode for both D_{G1} and D_{G2}.

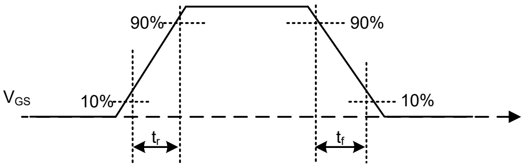


Figure 8. Gate Voltage (V_{GS}) Rising Time (t_r) and Falling Time (t_f)

Current Sensing Resistors

The current sensing resistors, R_S, turns the current flowing through it into a voltage for the controller to detect. The current sensing resistors are optional and can be used according to the requirements. It is recommended that the current sensing resistors be used when the cross voltage is less than 0.5 V.

Pay attention to the power that the current sensing resistors can withstand, P_{RS}, which is calculated by $P_{RS} = R_S \times I_{RMS}^2$, where R_S is the resistance value, I_{RMS} is the effective value of the current flowing through the resistor. The package of the current sensing resistor should be selected based on the power calculated above.

FG Pull-Up Resistors

The suggested value for the pull-up resistor, R1, connected between the FG pin and the V_M is 10 kΩ.

Gate-Driver Supply Capacitor

The power supply regulator capacitors, C1 and C5 can reduce input voltage fluctuation. C1 is recommended to use at least a 4.7 µF capacitor and C5 is recommended to use at least a 10 µF capacitor.

Power Supply Bypass Capacitor

When the board power supply is mains, the power supply bypass capacitor, C4, can filter out the high-frequency noise input from the power supply. It is recommended to use a 0.1 µF capacitor. This capacitor is optional and can be used according to the requirements.

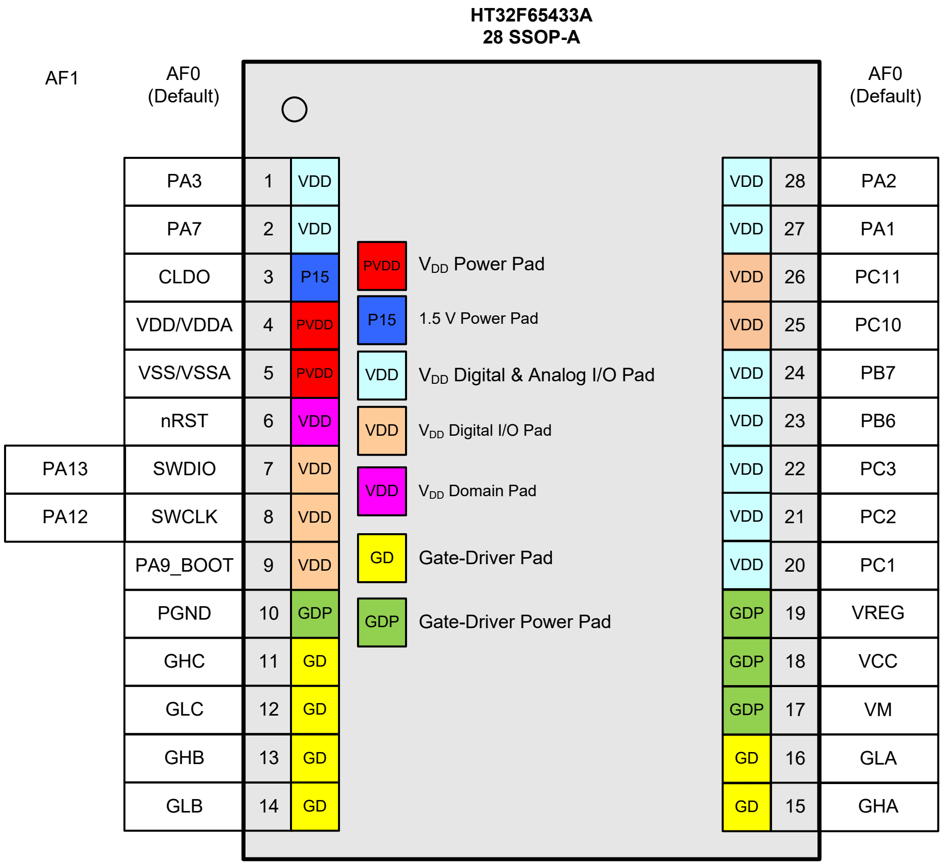
Motor Supply Capacitor

The motor power supply capacitor, C3, can absorb the current that is fed back to the V_M power supply when the motor is running, and can also provide a transient power for motor to compensate for the power response speed or the influence of external wire length.

LDO Output Capacitor

The LDO output regulator capacitor, C2, can reduce the voltage ripple of the LDO output. It is recommended to use at least a 2.2 µF capacitor.

5 Pin Assignment



HT32F65433A
28 SSOP-A

AF1	AF0 (Default)	Pin	Pad	Pad	Pin	AF0 (Default)
	PA3	1	VDD	VDD	28	PA2
	PA7	2	VDD	VDD	27	PA1
	CLDO	3	P15	VDD	26	PC11
	VDD/VDDA	4	PVDD	VDD	25	PC10
	VSS/VSSA	5	PVDD	VDD	24	PB7
	nRST	6	VDD	VDD	23	PB6
PA13	SWDIO	7	VDD	VDD	22	PC3
PA12	SWCLK	8	VDD	VDD	21	PC2
	PA9_BOOT	9	VDD	VDD	20	PC1
	PGND	10	GDP	GDP	19	VREG
	GHC	11	GD	GDP	18	VCC
	GLC	12	GD	GDP	17	VM
	GHB	13	GD	GD	16	GLA
	GLB	14	GD	GD	15	GHA

Pad	Description
PVDD	V_{DD} Power Pad
P15	1.5 V Power Pad
VDD	V_{DD} Digital & Analog I/O Pad
VDD	V_{DD} Digital I/O Pad
VDD	V_{DD} Domain Pad
GD	Gate-Driver Pad
GDP	Gate-Driver Power Pad

Figure 9. 28-pin SSOP Pin Assignment

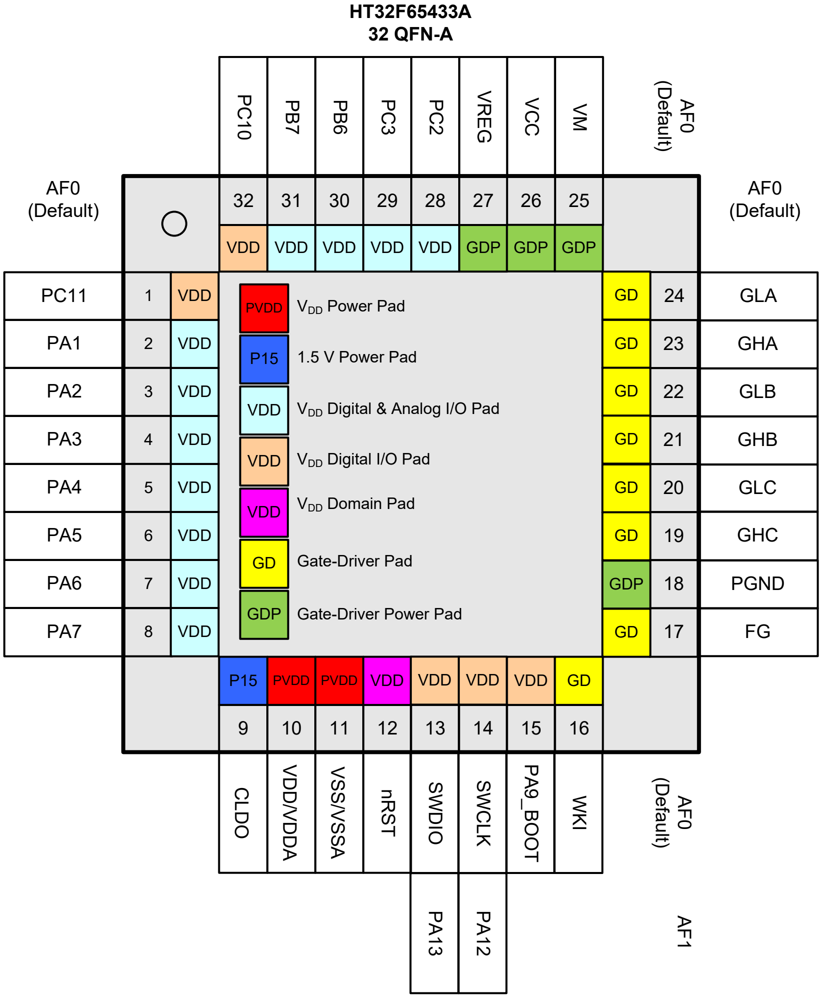


Figure 10. 32-pin QFN Pin Assignment

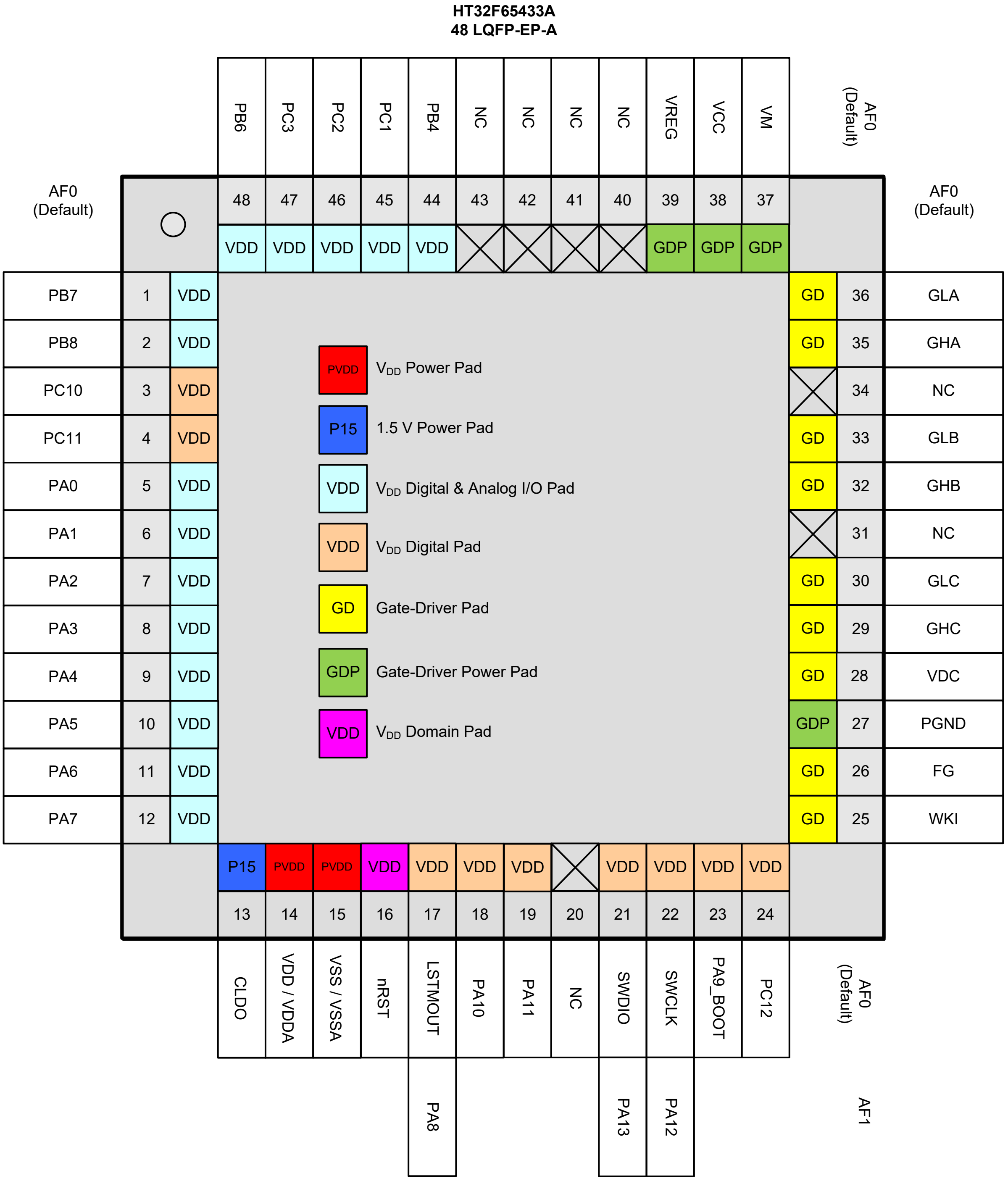


Figure 11. 48-pin LQFP-EP Pin Assignment

Table 6. Pin Assignment

Packages			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LOFP_EP	**32 QFN**	**28 SSOP**	**System Default**	**GPIO**	**ADC**	**CMP**	**GPTM /MCTM**	**SPI**	**UART**	**I^{2}C**	**PGA /OPA**	**SCTM**	**N/A**	**N/A**	**N/A**	**MCTM**	**MCTM**	**System Other**
5			PA0		ADC_IN7		GT_CH2	SPI_MISO		I2C_SDA	PGA0O	SCTM1						
6	2	27	PA1		ADC_IN6		GT_CH0	SPI_MOSI		I2C_SCL	PGA0N							
7	3	28	PA2		ADC_IN5		GT_CH1	SPI_SCK	UR_RX	I2C_SDA	PGA0P	SCTM0						
8	4	1	PA3		ADC_IN4	CMP1P0	GT_CH0	SPI_SEL	UR_TX	I2C_SCL		SCTM1						
9	5		PA4		ADC_IN3	CMP1P1	GT_CH1	SPI_MISO	UR_RX	I2C_SCL		SCTM0						
10	6		PA5		ADC_IN2	CMP1P2	GT_CH2	SPI_MOSI	UR_TX	I2C_SDA		SCTM1						
11	7		PA6		ADC_IN1	CMP1N	GT_CH3	SPI_SCK				SCTM1						
12	8	2	PA7		ADC_IN0	CMP1O	MT_BRK	SPI_SEL				SCTM0						VBG
13	9	3	CLDO															
14	10	4	VDD/ VDDA															
15	11	5	VSS/VSSA															
16	12	6	nRST															
17			LSTMOUT	PA8			GT_CH2	SPI_SEL	UR_TX			SCTM0						WAKEUP
18			PA10				GT_CH3	SPI_MOSI	UR_RX			SCTM1						
19			PA11				GT_CH0	SPI_MISO	UR_TX									
21	13	7	SWDIO	PA13			MT_CH3	SPI_MOSI	UR_RX	I2C_SDA		SCTM0						
22	14	8	SWCLK	PA12			MT_BRK	SPI_MISO	UR_TX	I2C_SCL		SCTM1						
23	15	9	PA9_BOOT				MT_BRK	SPI_SCK	UR_RX							MT_CH2	MT_CH0	CKOUT
24			PC12						UR_RX	I2C_SCL		SCTM0						
25	16		WKI															
26	17		FG															
27	18	10	PGND															
28			VDC															
29	19	11	GHC															
30	20	12	GLC															
32	21	13	GHB															
33	22	14	GLB															
35	23	15	GHA															
36	24	16	GLA															
37	25	17	VM															
38	26	18	VCC															
39	27	19	VREG															
44			PB4			CMP1O	MT_BRK					SCTM1						
45		20	PC1		ADC_IN11	CMP0N	MT_BRK	SPI_SCK	UR_RX	I2C_SDA								
46	28	21	PC2		ADC_IN10	CMP0P	MT_CH3	SPI_SEL										
47	29	22	PC3		ADC_IN9	CMP0O	GT_CH0	SPI_MOSI	UR_TX	I2C_SCL	OPAO							
48	30	23	PB6				GT_CH1	SPI_MISO	UR_RX	I2C_SDA	OPAN	SCTM1						
1	31	24	PB7				GT_CH2	SPI_MOSI	UR_TX	I2C_SCL	OPAP	SCTM1						
2			PB8		ADC_IN8	CMP0O	MT_CH3		UR_TX	I2C_SDA	PGA1O	SCTM0						

Packages			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LOFP_EP	32 QFN	28 SSOP	System Default	GPIO	ADC	CMP	GPTM /MCTM	SPI	UART	I^2C	PGA /OPA	SCTM	N/A	N/A	N/A	MCTM	MCTM	System Other
3	32	25	PC10				GT_CH0		UR_RX		PGA1N							
4	1	26	PC11				GT_CH1	SPI_MISO		I2C_SCL	PGA1P	SCTM0						CKIN
20, 31, 34, 40~43			NC															

Table 7. Pin Description

Pin Number			Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP-EP	32 QFN	28 SSOP					Default Function (AF0)
5			PA0	AI/O	5V	4/8/12/16 mA	PA0
6	2	27	PA1	AI/O	5V	4/8/12/16 mA	PA1
7	3	28	PA2	AI/O	5V	4/8/12/16 mA	PA2
8	4	1	PA3	AI/O	5V	4/8/12/16 mA	PA3
9	5		PA4	AI/O	5V	4/8/12/16 mA	PA4, this pin provides a UART_RX function in the Boot loader mode.
10	6		PA5	AI/O	5V	4/8/12/16 mA	PA5, this pin provides a UART_TX function in the Boot loader more.
11	7		PA6	AI/O	5V	4/8/12/16 mA	PA6
12	8	2	PA7	AI/O	5V	4/8/12/16 mA	PA7
13	9	3	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connected a 2.2 μF capacitor as close As possible between this pin and VSS.
14	10	4	VDD/VDDA	P	—	—	Digital and analog voltage input
15	11	5	VSS/VSSA(5)	P	—	—	Ground reference
16	12	6	nRST	I	5V_PU	—	External reset pin
17			PA8	I/O	5V	4/8/12/16 mA	LSTMOUT
18			PA10	I/O	5V	4/8/12/16 mA	PA10
19			PA11	I/O	5V	4/8/12/16 mA	PA11
21	13	7	SWDIO	I/O	5V_PU	4/8/12/16 mA	PA13
22	14	8	SWCLK	I/O	5V_PU	4/8/12/16 mA	PA12
23	15	9	PA9_BOOT	I/O	5V_PU	4/8/12/16 mA	PA9_BOOT
24			PC12	I/O	5V	4/8/12/16 mA	PC12
25	16		WKI	I	—	—	External wake-up input. Keep floating when no use
26	17		FG	O	—	—	High voltage level shifter open-drain output
27	18	10	PGND	P	—	—	Gate-driver ground terminal
28			VDC	O	—	—	Motor power supply voltage divider output
29	19	11	GHC	O	—	—	High-side P-type MOSFET gate drive phase C
30	20	12	GLC	O	—	—	Low-side N-type MOSFET gate drive phase C
32	21	13	GHB	O	—	—	High-side P-type MOSFET gate drive phase B
33	22	14	GLB	O	—	—	Low-side N-type MOSFET gate drive phase B
35	23	15	GHA	O	—	—	High-side P-type MOSFET gate drive phase A
36	24	16	GLA	O	—	—	Low-side N-type MOSFET gate drive phase A
37	25	17	VM	P	—	—	Motor supply and gate-driver supply input
38	26	18	VCC	P	—	—	VCC Power supply input
39	27	19	VREG	O	—	—	Supplied from V_{CC}. Regulated 5 V output
44			PB4	AI/O	5V	4/8/12/16 mA	PB4
45		20	PC1	AI/O	5V	4/8/12/16 mA	PC1
46	28	21	PC2	AI/O	5V	4/8/12/16 mA	PC2
47	29	22	PC3	AI/O	5V	4/8/12/16 mA	PC3

Pin Number			Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP-EP	32 QFN	28 SSOP					Default Function (AF0)
48	30	23	PB6	AI/O	5V	4/8/12/16 mA	PB6
1	31	24	PB7	AI/O	5V	4/8/12/16 mA	PB7
2			PB8	AI/O	5V	4/8/12/16 mA	PB8
3	32	25	PC10	I/O	5V	4/8/12/16 mA	PC10
4	1	26	PC11	I/O	5V	4/8/12/16 mA	PC11
20, 31, 34, 40~43			NC	—	—	—	Not connected

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, the UART interface can be used for communication.
5. The VSS/VSSA is internally connected to the gate-drive GND line.

Internal Connection Signals

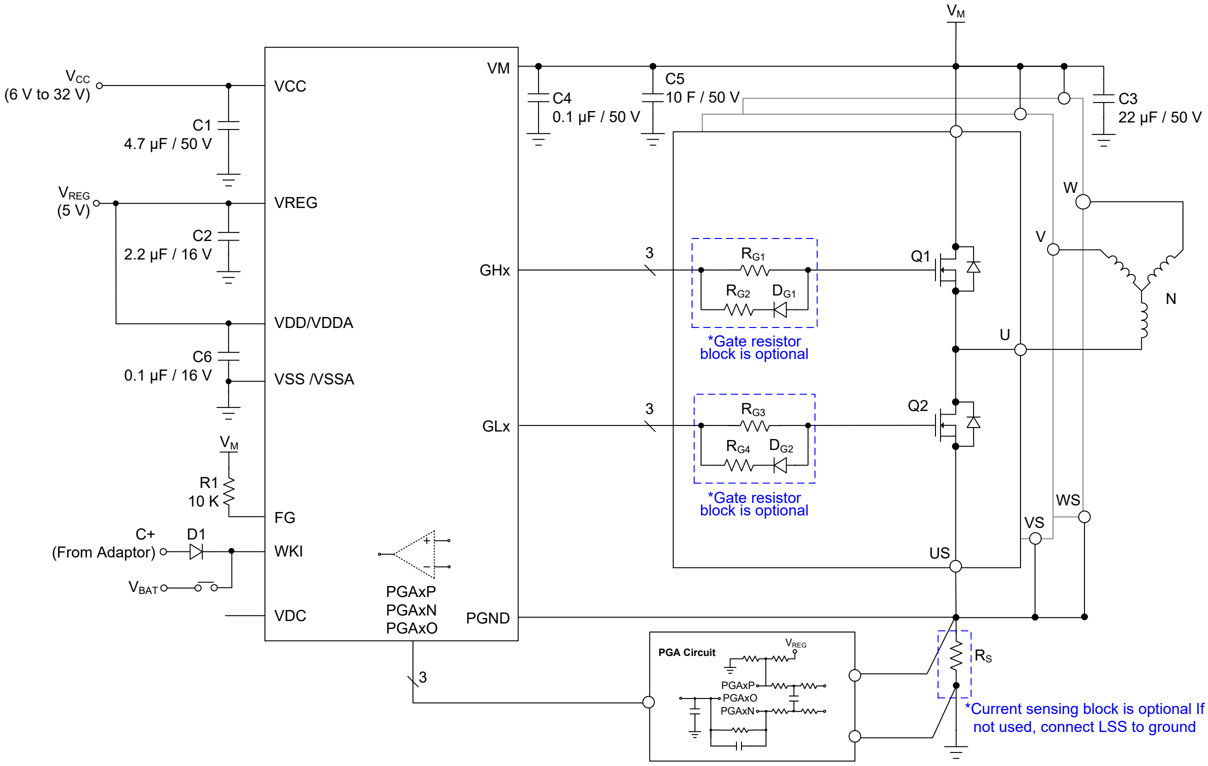
The MCU generated signals such as the MCTM channel outputs have been internally connected to the gate-driver inputs for control purpose. The connections are listed in the following table and the related control registers should be configured correctly using application program.

Table 8. Internal Connection Signal Lines

Packages			MCU Signal Name	Connection Gate-driver Signal Name	Description
48 LQFP-EP	32 QFN	28 SSOP			
●	●	●	PB3/MT_CH0 (MCTM)	INHA	Control input for high-side gate drive phase A. High active The MCU AFIO setting should be AF4 to select the MCTM pin function.
●	●	●	PB2/MT_CH0N (MCTM)	$\overline{\text{INLA}}$	Control input for low-side gate drive phase A. Low active The MCU AFIO setting should be AF4 to select the MCTM pin function.
●	●	●	PB1/MT_CH1 (MCTM)	INHB	Control input for high-side gate drive phase B. High active The MCU AFIO setting should be AF4 to select the MCTM pin function.
●	●	●	PB0/MT_CH1N (MCTM)	$\overline{\text{INLB}}$	Control input for low-side gate drive phase B. Low active The MCU AFIO setting should be AF4 to select the MCTM pin function.
●	●	●	PA15/MT_CH2 (MCTM)	INHC	Control input for high-side gate drive phase C. High active The MCU AFIO setting should be AF4 to select the MCTM pin function.
●	●	●	PA14/MT_CH2N (MCTM)	$\overline{\text{INLC}}$	Control input for low-side gate drive phase C. Low active The MCU AFIO setting should be AF4 to select the MCTM pin function.
●	●	●	PC15	LDOEN	LDO enable pin. It is pulled-up and connected to VREG internally. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
●	●		PC14	WKO	External wake-up output. An external high voltage wake-up sighnal input on the WKI pin will be converted into a low voltage, V_{REG},which is output by the WKO pin and can be used as an interrupt signal for the MCU. Keep floating when no use. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
●	●		PC13	FGI	Control input of high voltage level shifter to FG. The MCU AFIO setting should be AF0 to select the General Purpose Input/Output pin function.
	●	●	PA0/ADC_IN7 (ADC)	VDC	Motor power supply voltage divider output The MCU AFIO setting should be AF2 to select the ADC pin function.

Note: For the 28-pin SSOP package, the WKO and FGI lines are not availabled; for the 48-pin LQFP-EP package, the VDC line is routed to the external package.

6 Application Circuit



Note: For the 28-pin SSOP and 32-pin QFN packages, the VDC and PA0/ADC_IN7 lines are connected internally.

Figure 12. Application Circuit

7 Electrical Characteristics

Power Supply Scheme

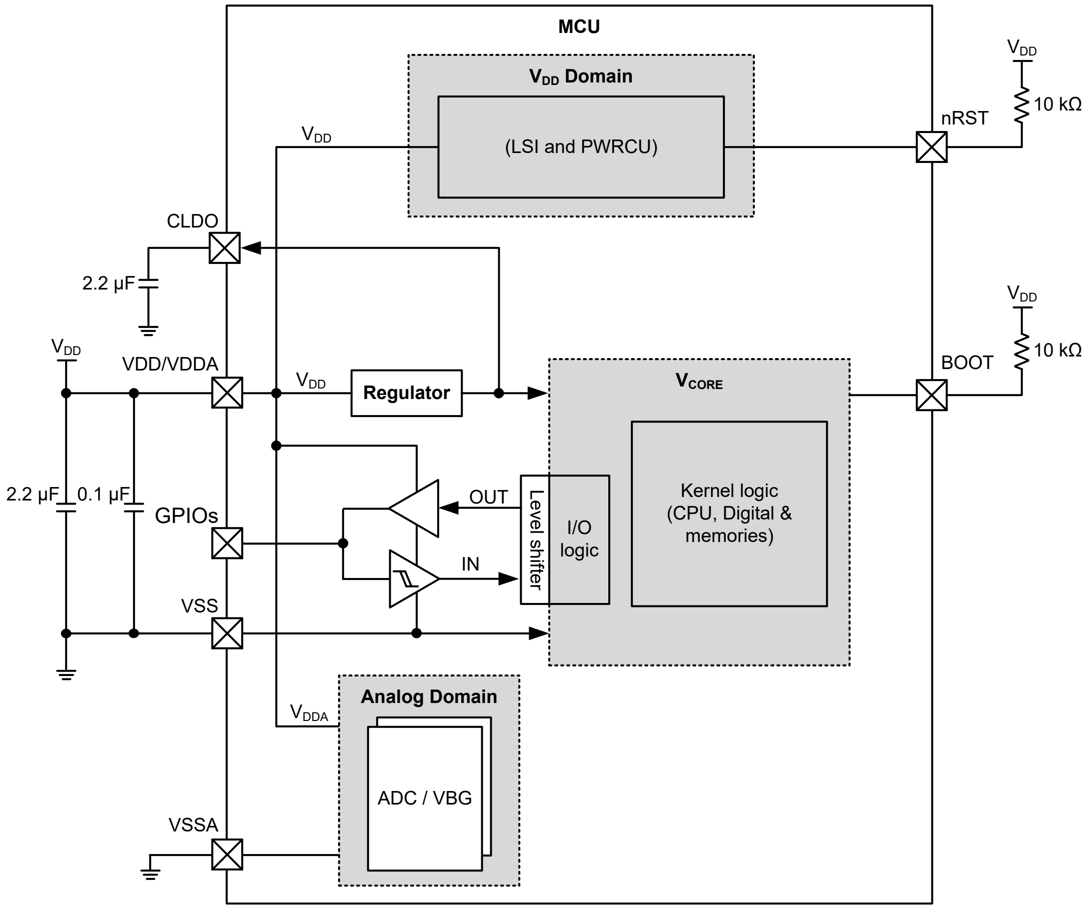


Figure 13. Power Supply Scheme

Note: 1. All regulator capacitors must be placed as close to the MCU as possible.
2. It is recommended that the pull-up resistor of the BOOT pin is 10 kΩ.
3. It is recommended that the pull-up resistor of the nRST pin is 10 kΩ.

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute Maximum Ratings

Parameter		Value	Unit
VCC, VM, WKI, FG		-0.3 to 36	V
VM-to-GHx		-0.3 to 36	V
GLx-to-PGND		-0.3 to 36	V
VREG		-0.3 to 7.0	V
PGND		-0.7 to 0.7	V
Operating Ambient Temperature Range		-40 to 105	°C
Maximum Junction Temperature		150	°C
Storage Temperature Range		-60 to 150	°C
Lead Temperature (Soldering 10s)		260	°C
Electrostatic Discharge Voltage	Human Body Model	±2000	V
Junction-to-Ambient Thermal Resistance, θ_{JA}	48LQFP-EP	50	°C/W
	32QFN	47	°C/W
	28SSOP	80	°C/W

Recommended DC Operating Conditions

Table 10. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	—	6	—	32	V
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
V_{DDA}	Analog Operating Voltage	—	2.5	5.0	5.5	V

On-Chip LDO Voltage Regulator Characteristics

Table 11. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{LDO} = 20 mA and voltage variation = ±5 %, After trimming	1.38	1.5	1.62	V
I_{LDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

The current consumption is influenced by several parameters and factors, including the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is configured under the following conditions for current consumption measured:

- All I/O pins are set to a high-impedance (floating) state.
- All peripherals are disabled unless specifically stated otherwise.
- The Flash memory access time is optimized using the minimum wait states number, depending on the f_{HCLK} frequency.
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$.

Table 12. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Run Mode)	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, all peripherals enabled	—	10.9	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, all peripherals disabled	—	6.7	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, all peripherals enabled	—	9.6	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, all peripherals disabled	—	9.6	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, all peripherals enabled	—	6.7	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, all peripherals disabled	—	3.1	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, all peripherals enabled	—	1.9	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, all peripherals disabled	—	1.3	—	mA
		V_{DD} = 5.0 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, all peripherals enabled	—	34	—	μA
		V_{DD} = 5.0 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, all peripherals disabled	—	31.6	—	μA
	Supply Current (Sleep Mode)	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, all peripherals enabled	—	6	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, all peripherals disabled	—	1	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, all peripherals enabled	—	4.1	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, all peripherals disabled	—	0.8	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, all peripherals enabled	—	2.4	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, all peripherals disabled	—	0.6	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, all peripherals enabled	—	1	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, all peripherals disabled	—	0.26	—	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Deep-Sleep Mode)	V_{DD} = 5.0 V, all clock off (HSI), LDO in low power mode, LSI on, LSTM on	—	27.3	—	µA

Note: 1. HSI means 8 MHz high speed internal oscillator.
2. LSI means 32 kHz low speed internal oscillator.
3. Code = while (1) {208 NOP} executed in Flash.

Reset and Supply Monitor Characteristics

Table 13. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 105 °C	2.22	2.35	2.48	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})		2.12	2.20	2.33	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 14. LVD / BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown-Out Detection	T_A = -40 °C ~ 105 °C, After factory-trimmed V_{DD} Falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3.53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 5.0 V	—	—	—	5	µs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 5.0 V	—	—	200	—	µs
I_{DDLVD}	Operation Current (2)	V_{DD} = 5.0 V	—	—	10	20	µA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

Internal Clock Characteristics

Table 15. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 105 °C	2.5	—	5.5	V
f_{HSI}	HSI Frequency	V_{DD} = 5.0 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 5.0 V, T_A = 25 °C	-2	—	+2	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = -20 °C ~ 105 °C	-3	—	+3	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = -40 °C ~ -20 °C or T_A = 85 °C ~ 105 °C	-3.5	—	+3.5	%
Duty	HSI Oscillator Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	HSI Oscillator Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	µA
	HSI Oscillator Power Down Current		—	—	0.05	µA
t_{SUHSI}	HSI Oscillator Startup Time	f_{HSI} = 8 MHz	—	—	10	µs

Table 16. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	2.5	—	5.5	V
f_{LSI}	LSI Frequency	V_{DD} = 5.0 V, T_A = -40 °C ~ 105 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 5.0 V	-10	—	10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 5.0 V	—	0.4	0.8	µA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 5.0 V	—	—	100	µs

System PLL Characteristics

Table 17. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	60	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	µs

Memory Characteristics

Table 18. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program/Erase Cycles before failure (Endurance)	T_A = -40 °C ~ 105 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 105 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 105 °C	20	—	—	µs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 105 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 105 °C	10	—	—	ms

I/O Port Characteristics

Table 19. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	5.0 V I/O	$V_I = V_{SS}$, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin		—	—	3	
I_{IH}	High Level Input Current	5.0 V I/O	$V_I = V_{DD}$, On-chip pull-down resister disabled	—	—	3	μA
		Reset pin		—	—	3	
V_{IL}	Low Level Input Voltage	5.0 V I/O		- 0.5	—	V_{DD} × 0.35	V
		Reset pin		0.5	—	V_{DD} × 0.35	
V_{IH}	High Level Input Voltage	5.0 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	
I_{OL}	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V_{OL} = 0.6 V		4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.6 V		8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OL} = 0.6 V		12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OL} = 0.6 V		16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		4	—	—	mA
		5.0 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		8	—	—	mA
		5.0 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		12	—	—	mA
		5.0 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.6 V		16	—	—	mA
V_{OL}	Low Level Output Voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.6	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.6	
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.6	
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.6	
V_{OH}	High Level Output Voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.6	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.6	—	—	
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA		V_{DD} - 0.6	—	—	
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA		V_{DD} - 0.6	—	—	
R_{PU}	Internal Pull-up Resistor	5.0 V I/O, V_{DD} = 5.0 V		—	60	—	kΩ
R_{PD}	Internal Pull-down Resistor	5.0 V I/O, V_{DD} = 5.0 V		—	60	—	kΩ

Bandgap Voltage Characteristics

Table 20. Bandgap Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.2	5.0	5.5	V
V_{BG}	Bandgap Reference Voltage	V_{DDA} = 2.2 V ~ 5.5 V @T_A = -40 °C ~ 105 °C	1.208	1.22	1.232	V
t_{SBG}	ADC Sampling Time when Reading Bandgap Voltage	—	5	—	—	µs

ADC Characteristics

Table 21. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	A/D Converter Operating Voltage	—	2.5	5.0	5.5	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	A/D Converter Operating Current	V_{DDA} = 5.0 V	—	0.85	1	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 5.0 V	—	—	0.1	µA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	32	MHz
f_S	Sampling Rate	—	0.05	—	2	Msps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0]=2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup Time	—	—	—	1	µs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 ksps, V_{DDA} = 5.0 V	—	—	±2	LSB
DNL	Differential Non-linearity Error	f_S = 750 ksps, V_{DDA} = 5.0 V	—	—	±1	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

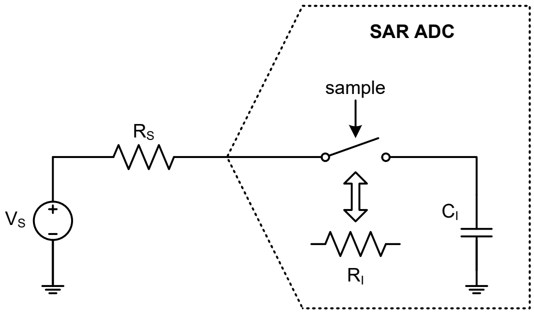


Figure 14. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below 1/4 LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC}C_I\ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Comparator Characteristics

Table 22. Comparator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	Comparator mode		2.5	5.0	5.5	V
V_{IN}	Input Common Mode Voltage Range	CP or CN		V_{SSA}	—	V_{DDA}	V
V_{IOS}	Input Offset Voltage(Note)	—		-15	—	15	mV
V_{HYS}	Input Hysteresis V_{DDA} = 5.0 V	No hysteresis, CMPHM [1:0] = 00		—	0	—	mV
		Low hysteresis, CMPHM [1:0] = 01		—	30	—	mV
		Middle hysteresis, CMPHM [1:0] = 10		—	60	—	mV
		High hysteresis, CMPHM [1:0] = 11		—	100	—	mV
t_{RT}	Response Time Input Overdrive = ±100 mV	High Speed Mode	V_{DDA} ≥ 2.7 V	—	50	100	ns
			V_{DDA} < 2.7 V	—	100	250	
		Low Speed Mode		—	2	5	µs
I_{CMP}	Current Consumption V_{DDA} = 5.0 V	High Speed Mode		—	180	—	µA
		Low Speed Mode		—	30	—	µA
t_{CMPST}	Comparator Startup Time	Comparator enabled to output valid		—	—	50	µs
I_{CMP_DN}	Power Down Supply Current	CMPEN = 0, CVREN = 0, CVROE = 0		—	—	0.1	µA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Comparator Voltage Reference (CVR)						
V_{CVR}	Output Range	—	V_{SSA}	—	V_{DDA}	V
N_{Bits}	CVR Scaler Resolution	—	—	8	—	bits
t_{CVRST}	Settling Time	CVR Scaler Settling Time from CVRVAL = “00000000” to “11111111”	—	—	100	μs
I_{CVR}	Current Consumption V_{DDA} = 5.0 V	CVREN=1, CVROE=0	—	65	—	μA
		CVREN=1, CVROE=1	—	80	110	μA

Note: Data based on characterization results only, not tested in production.

Programmable Gain Amplifier

Table 23. Programmable Gain Amplifier Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	3.0	5.0	5.5	V
I_{OPA_DN}	Power Down Current	—	—	—	0.1	μA
I_{OPA}	Operating Current	V_{DD} = 3.3 V	—	800	—	μA
V_{OS}	Input Offset Voltage	Without calibration (PGAOnOF[4:0] = 10000B), V_{IN} = 0 ~ V_{CM_max}/2	-15	—	+15	mV
		With calibration, V_{IN} = 0 ~ V_{CM_max}/2	-2	—	+2	
G_E	DC Gain Error	Gain = 6/8/12/16/24/32 (PGAnPGA = 1, PGAnHVDDAEN[1:0] = 0b0X, PGAnNUG = 0 and PGAnREF[1:0] = b00), V_{OUT} = 0.2 ~ (V_{DD} - 0.2 V)	—	—	2	%
		Gain = 5/7/11/15/23/31 (PGAnPGA = 1, PGAnHVDDAEN[1:0] = 0b10, PGAnNUG = 0 and PGAnREF[1:0] = b00) V_{OUT} = 0.2 ~ (V_{DD} - 0.2 V)				
V_{OR}	Maximum Output Voltage Range	—	V_{SS} + 0.2	—	V_{DD} - 0.2	V
I_{OS}	Input Offset Current	V_{IN} = 1/2 V_{CM}	—	1	10	nA
PSRR	Power Supply Rejection Ratio	—	—	60	—	dB
CMRR	Common Mode Rejection Ratio	V_{CM} = 0 ~ (V_{DD} - 1.4)	—	60	—	dB
SR	Slew Rate+, Slew Rate-	R_L = 100 kΩ, C_L = 50 pF	—	6	—	V/μs
GBW	Gain Band Width	R_L = 100 kΩ, C_L = 50 pF	—	6	—	MHz
A_{OL}	Open Loop Gain	R_L = 100 kΩ, C_L = 50 pF	60	80	—	dB
PM	Phase Margin	RL = 100 kΩ, C_L = 50 pF	50	60	—	Deg
V_{CM}	Common Mode Voltage Range	—	V_{SS}	—	V_{DD} - 1.4	V

Operational Amplifier

Table 24. Operational Amplifier Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	OPA mode	3.0	5.0	5.5	V
I_{OPA_DN}	Power Down Current	—	—	—	0.1	μA
I_{OPA}	Operating Current	V_{DD} = 5V	—	800	—	μA
V_{OS}	Input Offset Voltage	Without calibration (OPAOOF[4:0] = 10000B) $V_{IN} = 0 \sim V_{CM\_max}/2$	-15	—	+15	mV
		With calibration, $V_{IN} = 0 \sim V_{CM\_max}/2$	-2	—	+2	
V_{OR}	Maximum Output Voltage Range	—	V_{SS} + 0.2	—	V_{DD} - 0.2	V
I_{OS}	Input Offset Current	V_{IN} = 1/2 V_{CM}	—	1	10	nA
PSRR	Power Supply Rejection Ratio	—	—	60	—	dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0 \sim (V_{DD} - 1.4)$	—	60	—	dB
SR	Slew Rate+, Slew Rate-	R_L = 100 kΩ, C_L = 50 pF	—	6	—	V/μs
GBW	Gain Band Width	R_L = 100 kΩ, C_L = 50 pF	—	6	—	MHz
A_{OL}	Open Loop Gain	R_L = 100 kΩ, C_L = 50 pF	60	80	—	dB
PM	Phase Margin	R_L = 100 kΩ, C_L = 50 pF	50	60	—	Deg
V_{CM}	Common Mode Voltage Range	—	V_{SS}	—	V_{DD} - 1.4	V

GPTM / MCTM / SCTM Characteristics

Table 25. GPTM/ MCTM / SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM, MCTM, SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

Gate-Driver Characteristics

$V_{CC} = V_M$ = 24 V, C1 = 4.7 μF, C2 = 2.2 μF and T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply/Regulators						
V_{CC}	Supply Voltage	—	6.0	—	32.0	V
I_{CC}	Supply Standby Current	LDOEN = ‘1’, V_{REG} with no load	—	5	10	μA
$I_{CC(SLP)}$	Supply Sleep Current	LDOEN = ‘0’	—	—	2	μA
V_{REG}	VREG Output Voltage	I_{LOAD} = 1 mA	4.9	5.0	5.1	V
Gate-Driver (GHx, GLx)						
I_{DRVP}	High-Side and Low-Side Gate Peak Source Current	C_{LOAD} = 200 nF	—	350	—	mA
I_{DRVN}	High-Side and Low-Side Gate Peak Sink Current	C_{LOAD} = 200 nF	—	500	—	mA
t_{DEAD}	Dead Time	—	—	120	200	ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{DEAD_MIS}	Dead Time Mismatch	Dead time difference between rising and falling edges	—	50	—	ns
t_{PD}	Propagation Delay	INHx to GHx and $\overline{\text{INLx}}$ to GLx transition (No connected capacitor with GHx/GLx)	—	160	250	ns
t_{PD_MIS}	High-Side/Low-Side Propagation delay mismatch	Propagation delay difference between different phase or different side.	—	100	—	ns
R_{OFF1}	Low-Side Gate Hold-off Resistor	GLx to PGND	—	150	—	kΩ
R_{OFF2}	High-Side Gate Hold-off Resistor	VM to GHx	—	150	—	kΩ
Protections						
V_{CC_UVLO+}	V_{CC} Turn On Level	V_{CC} rises	—	—	5.5	V
V_{CC_UVLO-}	V_{CC} Turn Off Level	V_{CC} falls	3	—	—	V
V_{REG_UVLO+}	V_{REG} Turn On Level	V_{REG} rises	—	—	4.5	V
V_{REG_UVLO-}	V_{REG} Turn Off Level	V_{REG} falls	3.0	—	—	V
External Wake-up						
t_{WKDB1}	Debounce Time between WKI Input being Triggered to LDO Wake-up	—	—	1.2	—	ms
t_{WKDB2}	Debounce Time between WKI Input being Triggered and WKO output	—	—	10	—	µs
Voltage Divider						
V_{DIV}	Power Supply Voltage Divider VDC Output Voltage	LDOEN = '1'	2.85	3.00	3.15	V
R_{DIV}	Power Supply Voltage Divider Resistor	LDOEN = '0' disable voltage divider	—	8	—	kΩ

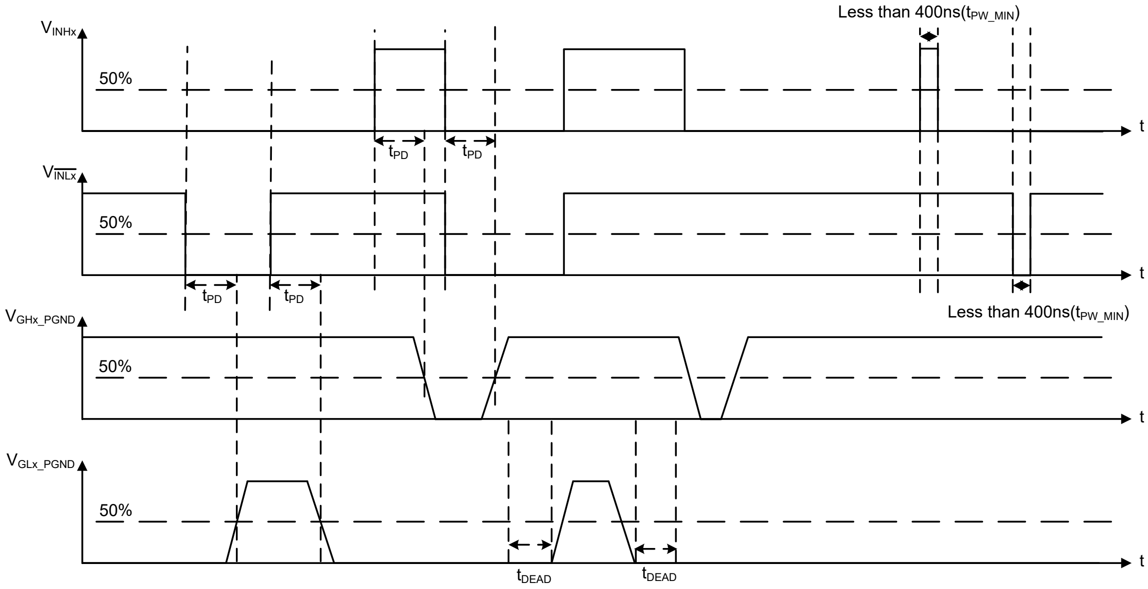


Figure 15. Gate-Driver Timing Diagram

I²C Characteristics

Table 26. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time [5]	0	—	0	—	0	—	ns
	SDA Data Hold Time [6]	—	1.6	—	0.475	—	0.25	μs
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.

2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

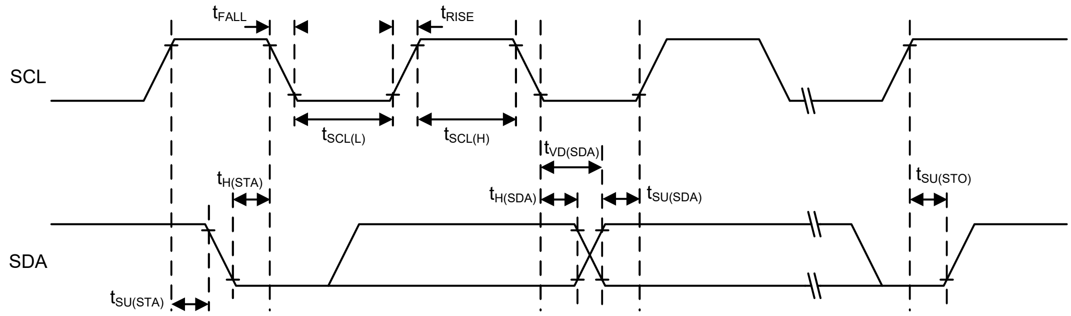


Figure 16. I²C Timing Diagram

SPI Characteristics

Table 27. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

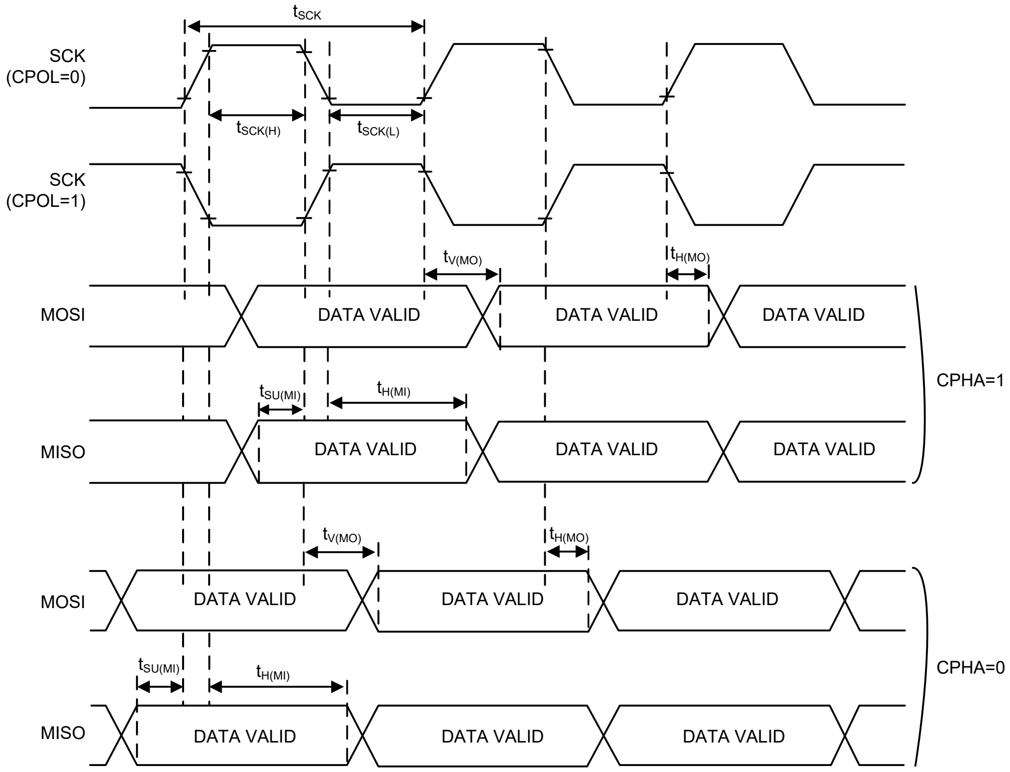


Figure 17. SPI Timing Diagram – SPI Master Mode

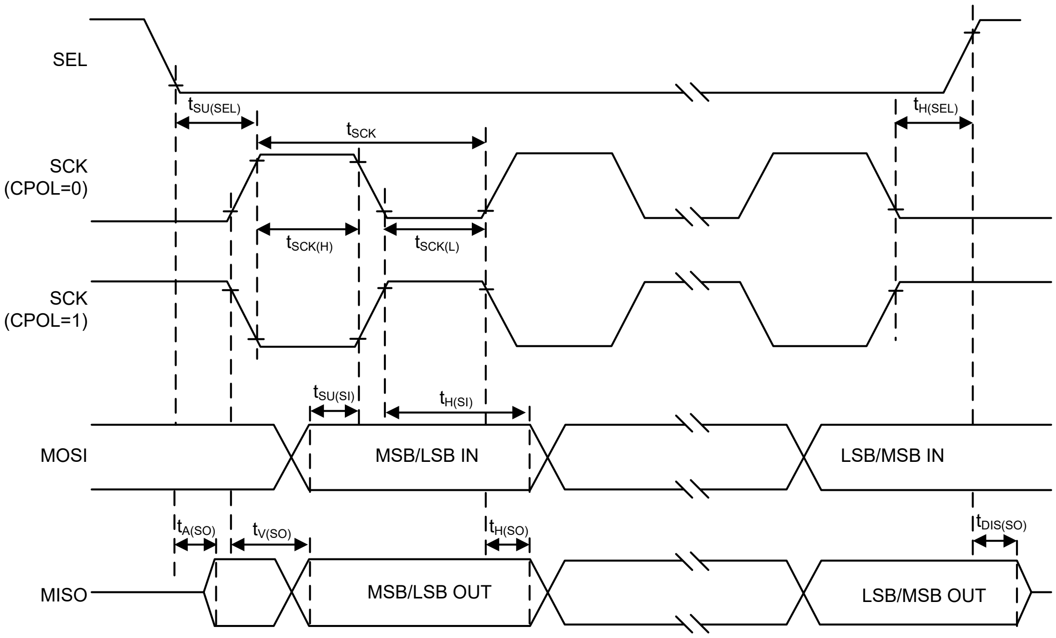


Figure 18. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

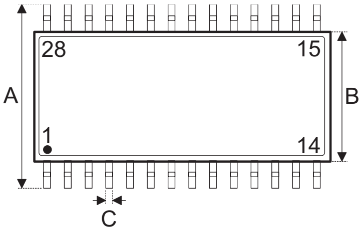
8 Package Information

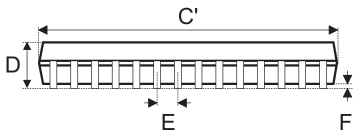
Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

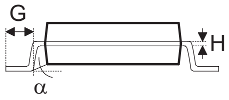
Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

28-pin SSOP (150mil) Outline Dimensions



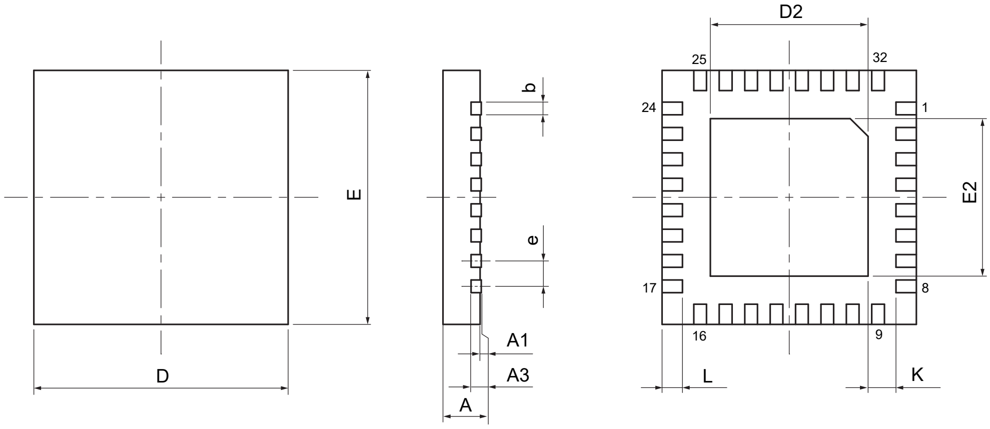




Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.236 BSC		
B	0.154 BSC		
C	0.008	—	0.012
C’	0.390 BSC		
D	—	—	0.069
E	0.025 BSC		
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	6.00 BSC		
B	3.90 BSC		
C	0.20	—	0.30
C’	9.90 BSC		
D	—	—	1.75
E	0.635 BSC		
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°

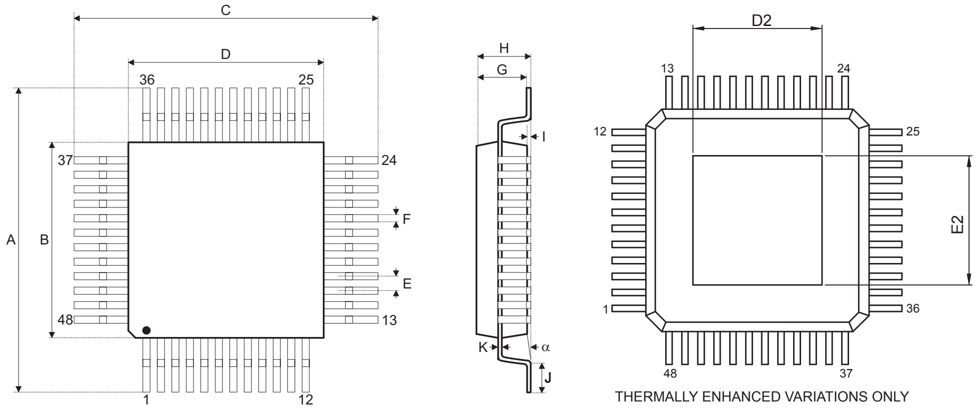
SAW Type 32-pin QFN (4mm × 4mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.006	0.008	0.010
D		0.157 BSC	
E		0.157 BSC	
e		0.016 BSC	
D2	0.100	—	0.108
E2	0.100	—	0.108
L	0.010	—	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.55	—	2.75
E2	2.55	—	2.75
L	0.25	—	0.45
K	0.20	—	—

48-pin LQFP-EP (7 mm × 7 mm) Outline Dimensions



THERMALLY ENHANCED VARIATIONS ONLY

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.020 BSC	
D2	0.170	—	0.211
E2	0.170	—	0.211
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.50 BSC	
D2	4.31	—	5.36
E2	4.31	—	5.36
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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