



HT32F67741 Datasheet

**32-Bit Arm® Cortex®-M0+ BT5.2 BLE Microcontroller,
up to 64 KB Flash and 8 KB SRAM with 1 Msps ADC, USART,
UART, SPI, I²C, MCTM, GPTM, SCTM, BFTM, CRC, RTC, WDT**

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1 General Description

The Holtek HT32F67741 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 40 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 64 KB of embedded Flash memory for code/data storage and up to 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Bluetooth Low Energy 5.2 controller, SPI, USART, UART, I²C, MCTM, GPTM, SCTM, BFTM, ADC, CRC-16/32, RTC, WDT and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wake-up latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of BLE products such as health care products, home appliances, smart device information beacons, data loggers, human interface device service, etc.

arm CORTEX

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 40 MHz operating frequency
- 0.93 DMIPS/MHz – Dhrystone v2.1
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- Up to 64 KB on-chip Flash memory for instruction/data and option byte storage
- Up to 8 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M0+ processor accesses and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

Bluetooth Low Energy Controller – BLEC

- 2.4 GHz RF transceiver compatible with Bluetooth Low Energy (BLE) 5.2 specification
- 16 MHz external crystal reference clock
- GFSK modulation, Frequency-Hopping Spread Spectrum (FHSS)
- Support LE 1 Mbps, 2 Mbps
- Receiver supports programmable gain control of over 70 dB
- Excellent receiver sensitivity of -94 dBm @ 1 Mbps
- Programmable transmitter output power up to +3.5 dBm
- Software-based True Random Number Generator (TRNG)
- Three operating modes: Normal, Deep-Sleep and Power-Down

The Bluetooth Low Energy Controller, BLEC, is an ultra-low power 2.4 GHz RF transceiver compatible with the BLE 5.2 specification. With excellent receiver sensitivity and very low active RF current consumption, the device provides an excellent battery lifetime. The BLEC includes the RF transceiver, modem, protocol processing logic, link layer controller and link layer firmware library which support for Bluetooth 5.2 LE 1 Mbps and LE 2 Mbps connections. For power saving, the BLEC supports Deep-Sleep and Power-Down modes, which can be combined with the PWRCU (Power Management Control Unit) Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down operating modes to reduce power consumption for BLE applications.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
 - Power On Reset / Power Down Reset – POR/PDR
 - Brown Out Detector – BOD
 - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to $\pm 2\%$ accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillators and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M0+ are derived from the system clock (CK_SYS) which can source from the HSI, HSE, LSI, LSE or system PLL. The Watchdog Timer and RealTime Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- Single V_{DD} power supply: 2.0 V to 3.6 V
- Integrated 1.5 V regulator for CPU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- Two power domains: V_{DD} , V_{CORE}
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes.

These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger sources and types
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wake-up enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 6 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are multiplexed channels, which include up to 6 external analog signal channels and 2 internal channels. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The A/D Conversion can be operated in one shot, continuous and discontinuous conversion modes.

I/O Ports – GPIO

- Up to 25 GPIOs
- Port A, B, C are mapped to 16-line EXTI interrupts
- Almost all I/O pins have a configurable output driving current

There are up to 25 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function

- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Supports 3-phase motor control and hall sensor interface
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of one 16-bit up/down counter; four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR), one 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single-Channel Timers – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single Channel Timer Module, SCTM, consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM output.

Basic Function Timers – BFTM

- 32-bit compare match count-up counter – no I/O control features
- One shot mode – stops counting when compare match occurs
- Repetitive mode – restarts counting when compare match occurs

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit count-down counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, a WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. The register write protect function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real-Time Clock – RTC

- 24-bit count-up counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} power domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wake-up timer to generate a system resume signal from the Power-Down mode.

Inter-Integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two-line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: (1) 100 kHz in the Standard mode, (2) 400 kHz in the Fast mode and (3) 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an

arbitration detection and clock synchronization function to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to ($f_{PCLK}/2$) MHz for the master mode and ($f_{PCLK}/3$) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to ($f_{PCLK}/16$) MHz for asynchronous mode and ($f_{PCLK}/8$) MHz for synchronous mode
- Full duplex communication
- Fully programmable serial communication characteristics including:
 - Word length: 7, 8 or 9-bit character
 - Parity: Even, odd, or no-parity bit generation and detection
 - Stop bit: 1 or 2 stop bit generation
 - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes an 8-level transmitter FIFO, TX FIFO, and an 8-level receiver FIFO, RX FIFO. The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to $f_{\text{PCLK}}/16$ MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
 - Word length: 7, 8 or 9-bit character
 - Parity: Even, odd or no-parity bit generation and detection
 - Stop bit: 1 or 2 stop bit generation
 - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
 $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
 $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
 $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoints or code / literal patches
- 2 comparators for hardware watch points

Package and Operation Temperature

- 46-pin QFN package
- Operation temperature range: -40 °C to +85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F67741
Main Flash (KB)		63
Option Bytes Flash (KB)		1
SRAM (KB)		8
Timers	MCTM	1
	GPTM	1
	SCTM	4
	BFTM	2
	WDT	1
	RTC	1
Communication	SPI	2
	USART	1
	UART	2
	I ² C	2
BLE		1
CRC-16/32		1
EXTI		16
12-bit ADC		1
Number of channels		6 Channels
GPIO		25
CPU frequency		Up to 40 MHz
Operating voltage		2.0 V ~ 3.6 V
Operating temperature		-40 °C ~ +85 °C
Package		46-pin QFN

Block Diagram

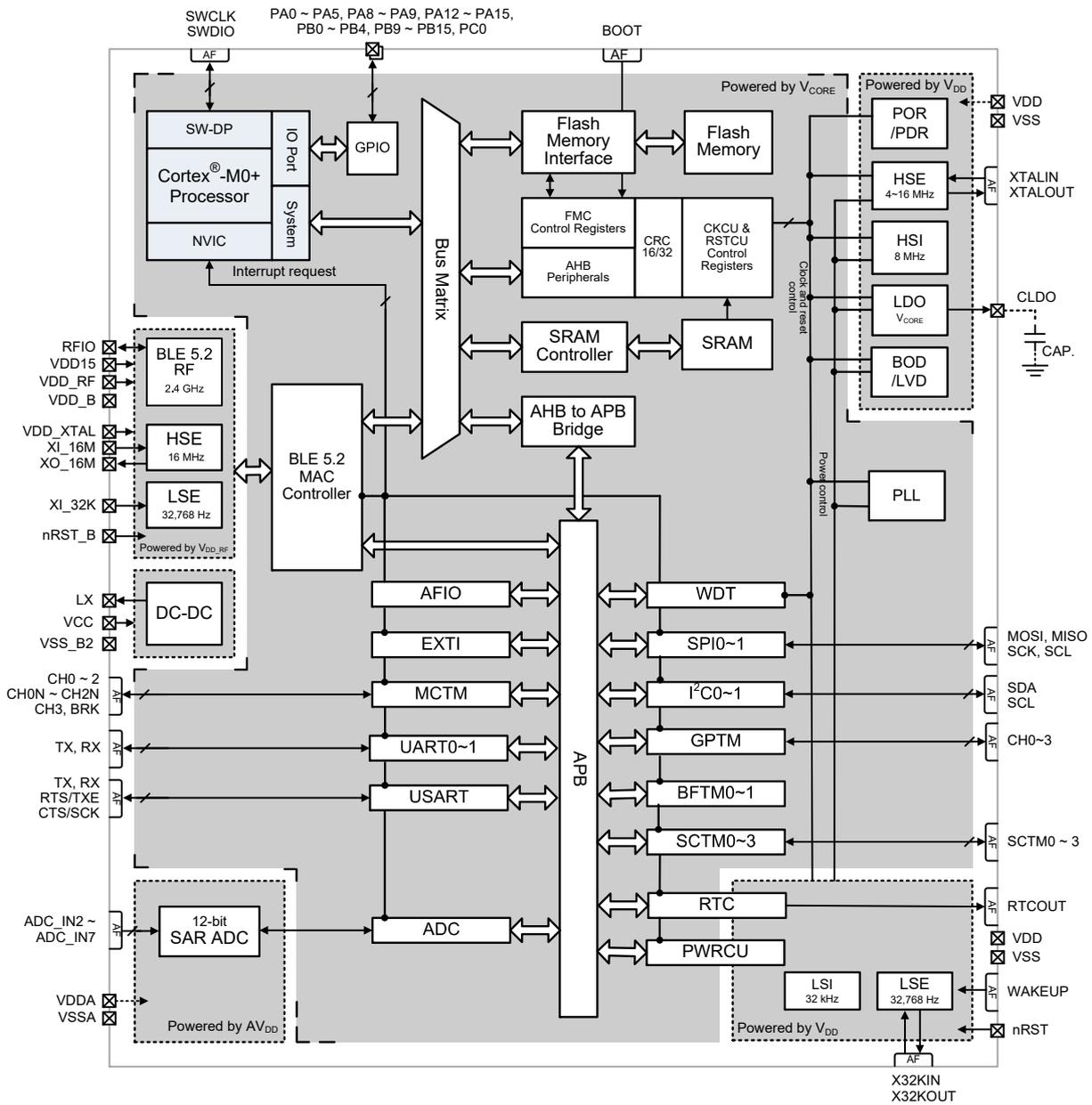


Figure 1. Block Diagram

Memory Map

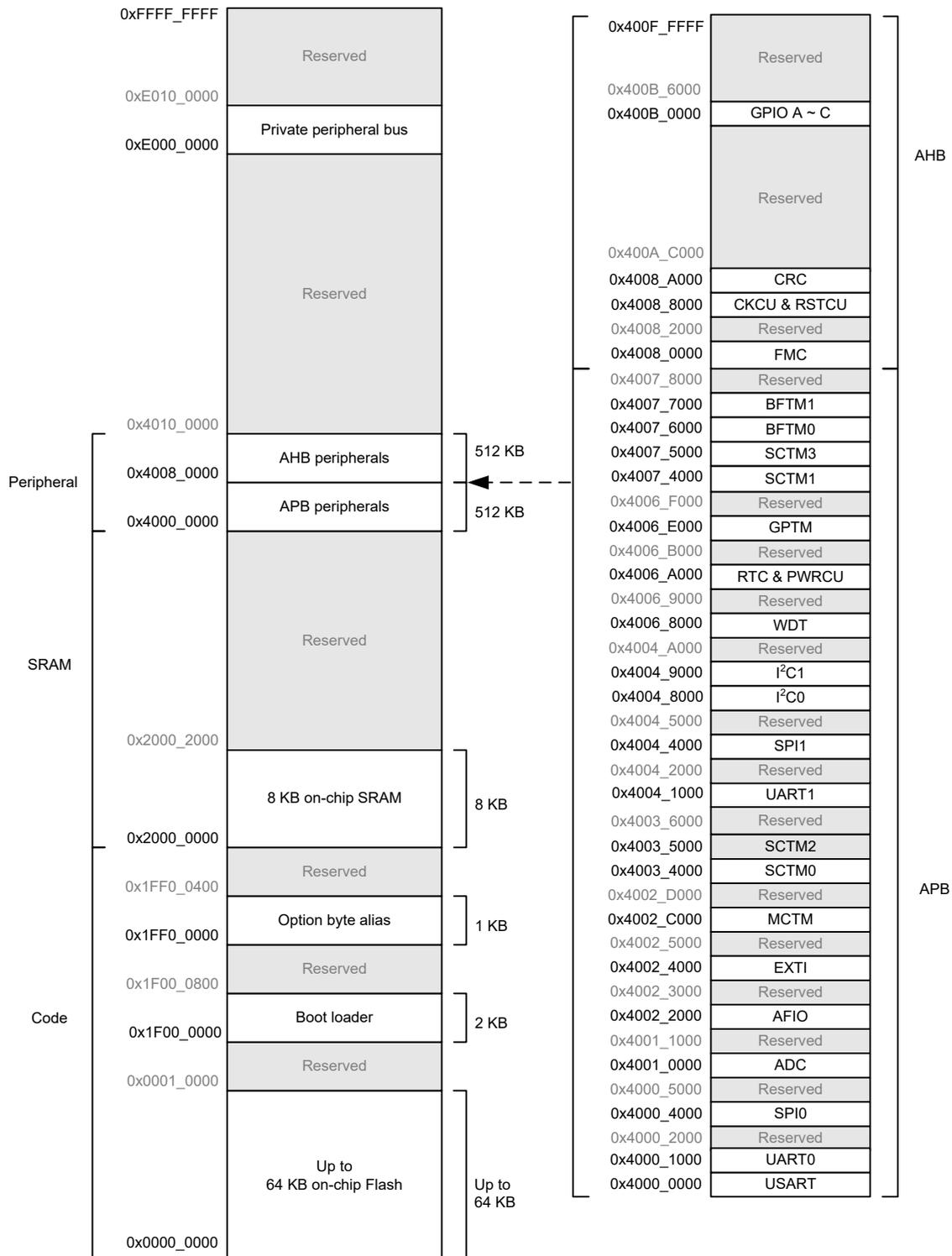


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I ² C0	
0x4004_9000	0x4004_9FFF	I ² C1	
0x4004_A000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	SCTM3	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400F_FFFF	Reserved	

Clock Structure

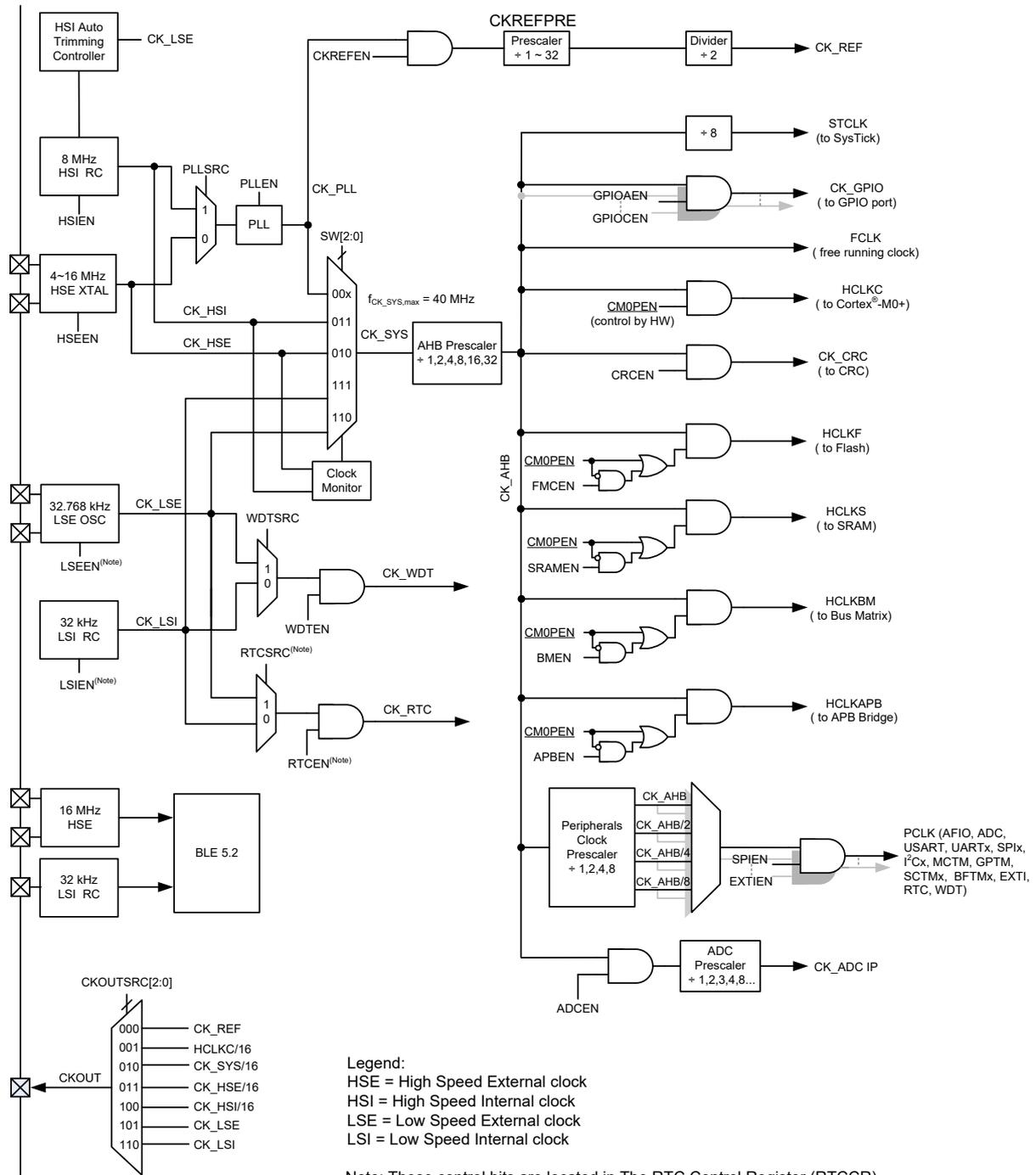


Figure 3. Clock Structure

4 Pin Assignment

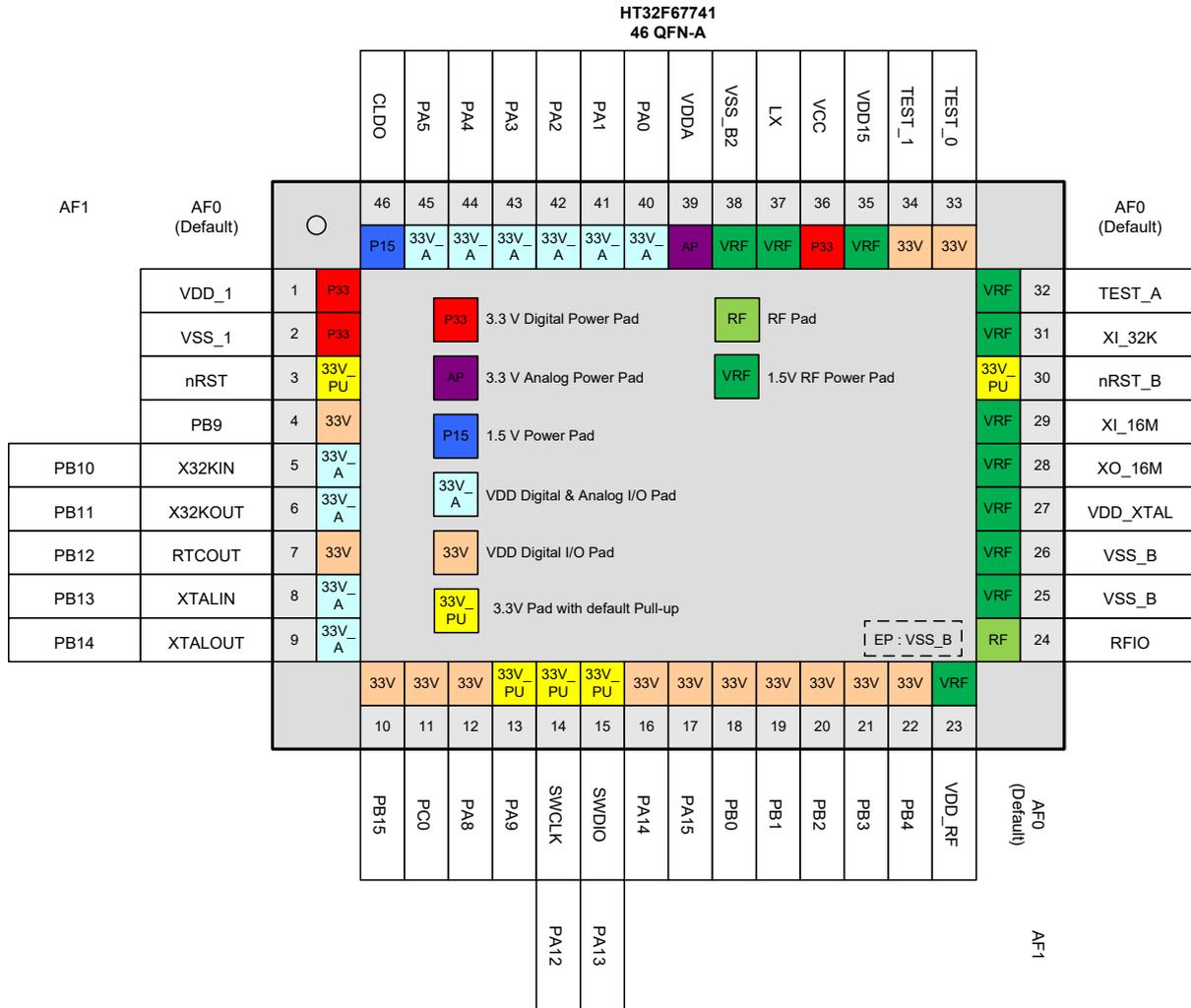


Figure 4. 46-pin QFN Pin Assignment

Table 3. Pin Assignment

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
46QFN	System Default	GPIO	ADC	N/A	GPTM/MCTM	SPI	USART/UART	I ² C	N/A	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
40	PA0		ADC_IN2		GT_CH0	SPI1_SCK	USR_RTS	I2C1_SCL								
41	PA1		ADC_IN3		GT_CH1	SPI1_MOSI	USR_CTS	I2C1_SDA								
42	PA2		ADC_IN4		GT_CH2	SPI1_MISO	USR_TX									
43	PA3		ADC_IN5		GT_CH3	SPI1_SEL	USR_RX									
44	PA4		ADC_IN6		GT_CH0	SPI0_SCK	UR1_TX	I2C0_SCL								
45	PA5		ADC_IN7		GT_CH1	SPI0_MOSI	UR1_RX	I2C0_SDA								
46	CLDO															
1	VDD_1															
2	VSS_1															
3	nRST															
4	PB9				MT_CH3											
5	X32KIN	PB10			GT_CH0	SPI1_SEL	USR_TX							SCTM2		
6	X32KOUT	PB11			GT_CH1	SPI1_SCK	USR_RX							SCTM3		
7	RTCOUT	PB12				SPI0_MISO	UR0_RX							SCTM0		WAKEUP
8	XTALIN	PB13					UR0_TX	I2C0_SCL								
9	XTALOUT	PB14					UR0_RX	I2C0_SDA								
10	PB15				MT_CH0	SPI0_SEL		I2C1_SCL								
11	PC0				MT_CH0N	SPI0_SCK		I2C1_SDA						SCTM3		
12	PA8						USR_TX							SCTM2		
13	PA9					SPI0_MOSI								SCTM3		CKOUT
14	SWCLK	PA12														
15	SWDIO	PA13														
16	PA14				MT_CH0	SPI1_SEL	USR_RTS	I2C1_SCL								
17	PA15				MT_CH0N	SPI1_SCK	USR_CTS	I2C1_SDA						SCTM1		
18	PB0				MT_CH1	SPI1_MOSI	USR_TX	I2C0_SCL								
19	PB1				MT_CH1N	SPI1_MISO	USR_RX	I2C0_SDA						SCTM2		
20	PB2				MT_CH2	SPI0_SEL	UR1_TX									
21	PB3				MT_CH2N	SPI0_SCK	UR1_RX							SCTM1		
22	PB4				MT_BRK	SPI0_MOSI	UR1_TX									
23	VDD_RF															

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
46QFN	System Default	GPIO	ADC	N/A	GPTM /MCTM	SPI	USART /UART	I ² C	N/A	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
24	RFIO															
25	VSS_B															
26	VSS_B															
27	VDD_XTAL															
28	XO_16M															
29	XI_16M															
30	nRST_B															
31	XI_32K															
32	TEST_A															
33	TEST_0															
34	TEST_1															
35	VDD15															
36	VCC															
37	LX															
38	VSS_B2															
39	VDDA															

Table 4. Pin Description

Pin Number	Pin Name	Type ⁽¹⁾	I/O Structure ⁽²⁾	Output Driving	Description
					Default Function (AF0)
40	PA0	AI/O	33V	4/8/12/16 mA	PA0
41	PA1	AI/O	33V	4/8/12/16 mA	PA1
42	PA2	AI/O	33V	4/8/12/16 mA	PA2
43	PA3	AI/O	33V	4/8/12/16 mA	PA3
44	PA4	AI/O	33V	4/8/12/16 mA	PA4, this pin provides a UART_TX function in the Boot loader mode.
45	PA5	AI/O	33V	4/8/12/16 mA	PA5, this pin provides a UART_RX function in the Boot loader mode.
46	CLDO	I/O	33V	4/8/12/16 mA	Core power LDO V _{CORE} output. It is recommended to connect a 1 μF capacitor as close as possible between this pin and VSS.
1	VDD_1	P	—	—	Voltage for digital I/O
2	VSS_1	P	—	—	Ground reference for digital I/O
3	nRST	I	33V_PU	—	External reset pin and external wake-up pin in the Power-Down mode
4	PB9	I/O	33V	4/8/12/16 mA	PB9
5	PB10	AI/O	33V	4/8/12/16 mA	X32KIN
6	PB11	AI/O	33V	4/8/12/16 mA	X32KOUT
7	PB12	I/O	33V	4/8/12/16 mA	RTCOUT
8	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
9	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
10	PB15	I/O	33V	4/8/12/16 mA	PB15
11	PC0	I/O	33V	4/8/12/16 mA	PC0
12	PA8	I/O	33V	4/8/12/16 mA	PA8
13	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
14	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
15	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
16	PA14	I/O	33V	4/8/12/16 mA	PA14
17	PA15	I/O	33V	4/8/12/16 mA	PA15
18	PB0	I/O	33V	4/8/12/16 mA	PB0
19	PB1	I/O	33V	4/8/12/16 mA	PB1
20	PB2	I/O	33V	4/8/12/16 mA	PB2
21	PB3	I/O	33V	4/8/12/16 mA	PB3
22	PB4	I/O	33V	4/8/12/16 mA	PB4
23	VDD_RF	P	15V	—	RF power
24	RFIO	AI/O	15V	—	RF I/O
25	VSS_B	P	—	—	RF power ground
26	VSS_B	P	—	—	RF power ground
27	VDD_XTAL	P	15V	—	BLE 16 MHz Crystal oscillator power
28	XO_16M	AO	15V	—	BLE 16 MHz Crystal oscillator output
29	XI_16M	AI	15V	—	BLE 16 MHz Crystal oscillator input
30	nRST_B	I	33V_PU	—	BLE hardware reset

Pin Number	Pin Name	Type ⁽¹⁾	I/O Structure ⁽²⁾	Output Driving	Description
					Default Function (AF0)
31	XI_32K	AI	—	—	BLE 32.768 kHz Crystal oscillator
32	TEST_A	AO	15V	—	Test pin
33	TEST_0	I/O	33V	—	Test pin
34	TEST_1	I/O	33V	—	Test pin
35	VDD15	P	—	—	BLE internal power
36	VCC	P	—	—	BLE digital power
37	LX	AO	15V	—	RF DC-DC switching output
38	VSS_B2	P	—	—	BLE ground reference for digital I/O
39	VDDA	P	—	—	Analog voltage for ADC and Comparator

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply

2. 33V = 3.3 V tolerant, PU = Pull-up, 15V = 1.5 V

3. The EP means the exposed pad on the packages. It must be connected to ground.

4. In the Boot loader mode, the UART interface is available for communication.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	External Main Supply Voltage	V _{SS} - 0.3	V _{SS} + 3.6	V
V _{CC}	External RF Supply Voltage	V _{SS} - 0.3	V _{SS} + 3.6	V
V _{DDA}	External Analog Supply Voltage	V _{SS_B} - 0.3	V _{SS_B} + 3.6	V
V _{IN}	Input Voltage on I/O	V _{SS} - 0.3	V _{DD} + 0.3	V
T _A	Ambient Operating Temperature Range	-40	+85	°C
T _{STG}	Storage Temperature Range	-60	+150	°C
T _J	Maximum Junction Temperature	—	+125	°C
P _D	Total Power Dissipation	—	500	mW
V _{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	I/O Operating Voltage	—	2	3.0	3.6	V
V _{CC}	RF Operating Voltage	—	2	3.0	3.6	V
LX	RF DC-DC Output Voltage	—	—	1.5	—	V
V _{DDA}	Analog Operating Voltage	—	2.5	3.0	3.6	V

BLE Characteristics

Table 7. BLE Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Crystal Oscillator 16 MHz					
	Frequency	—	16	—	MHz
	Frequency Accuracy Requirement	-30	—	30	ppm
ESR	Equivalent Series Resistance	—	—	80	Ω
C ₀	Crystal Shunt Capacitance	—	—	3	pF
CL	Crystal Load Capacitance	—	7	—	pF

Symbol	Parameter	Min.	Typ.	Max.	Unit	
Crystal Oscillator 32.768 kHz						
	Frequency	—	32.768	—	kHz	
	Frequency Accuracy Requirement	-20	—	20	ppm	
ESR	Equivalent Series Resistance	—	—	70	kΩ	
C0	Crystal Shunt Capacitance	—	—	2	pF	
CL	Crystal Load Capacitance	—	12.5	—	pF	
RX Characteristics						
PSENS	Sensitivity @ 1 Mbps	—	-94	—	dBm	
	Sensitivity @ 2 Mbps	—	-91	—	dBm	
CI0	In-band Blocking	Co-channel Interference		—	7	dB
CI1		Interference at $f_{\text{OFFS}} = \pm 1$ MHz	-9	—	-6	dB
CI2		Interference at $f_{\text{OFFS}} = \pm 2$ MHz	—	-44	—	dB
CI3		Interference at $f_{\text{OFFS}} = \pm 3$ MHz	—	-50	—	dB
CI4		Interference at f_{IMAGE}	—	-25	—	dB
CI5		Interference at $f_{\text{IMAGE}} \pm 1$ MHz	—	-35	—	dB
Intermodulation	$P_{\text{in}} = -64$ dBm; $P_{\text{unwant}} = -50$ dBm; $f_0 = 2 \times f_1 - f_2$, $f_2 - f_1 = 3$ MHz or 4 MHz or 5 MHz	-25	—	-22	dBm	
TX Characteristics						
P_{TX}	Output Power	—	3.5	—	dBm	
P_{BW}	Modulation 20 dB Bandwidth	—	—	1	MHz	
P_{RF1}	Out of Band Emission 2 MHz	—	-20	—	dB	
P_{RF2}	Out of Band Emission 3 MHz	—	-58	—	dB	
Dev	Transmit FM Deviation	115	250	300	kHz	
Drift	Transmit Drift in Any Position	—	—	400	Hz / μ s	

On-Chip LDO Voltage Regulator Characteristics

Table 8. LDO Characteristics

$T_A = 25$ °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	$V_{\text{DD}} \geq 2.0$ V regulator input @ $I_{\text{LDO}} = 35$ mA and voltage variant = ± 5 %, after trimming.	1.425	1.5	1.57	V
I_{LDO}	Output Current	$V_{\text{DD}} = 2.0$ V regulator input @ $V_{\text{LDO}} = 1.5$ V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	—	1	—	μ F

Power Consumption

Table 9. BLE Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{RX}	Supply Current (RX Mode)	V _{CC} = 3 V	—	8	—	mA
I _{TX}	Supply Current (TX Mode with 0 dBm Output Power)	V _{CC} = 3 V	—	5.83	—	mA
I _{SLEEP}	Supply Current (BLE Deep-Sleep Mode)	V _{CC} = 3 V	—	1.6	—	μA
I _{ACT}	Supply Current (BLE Normal Mode where BLE is Active)	V _{CC} = 3 V	—	1.38	—	mA
I _{PDN}	Supply Current (BLE Power-Down Mode)	V _{CC} = 3 V	—	1	—	μA

Table 10. Microcontroller Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Typ	Max @ T _A		Unit
				25 °C	85 °C	
I _{DD}	Supply Current (Run Mode)	V _{DD} = 3.0 V, HSI = 8 MHz, PLL = 40 MHz, f _{CPU} = 40 MHz, f _{BUS} = 40 MHz, all peripherals enabled	10.8	12.4	—	mA
		V _{DD} = 3.0 V, HSI = 8 MHz, PLL = 40 MHz, f _{CPU} = 40 MHz, f _{BUS} = 40 MHz, all peripherals disabled	6.0	6.9	—	
		V _{DD} = 3.0 V, HSI = 8 MHz, PLL = 40 MHz, f _{CPU} = 32 kHz, f _{BUS} = 32 kHz, all peripherals enabled	45	60	—	μA
		V _{DD} = 3.0 V, HSI = 8 MHz, PLL = 40 MHz, f _{CPU} = 32 kHz, f _{BUS} = 32 kHz, all peripherals disabled	40	53	—	
	Supply Current (Sleep Mode)	V _{DD} = 3.0 V, HSI = 8 MHz, PLL = 40 MHz, f _{CPU} = 0 MHz, f _{BUS} = 40 MHz, all peripherals enabled	6.5	7.5	—	mA
		V _{DD} = 3.0 V, HSI = 8 MHz, PLL = 40 MHz, f _{CPU} = 0 MHz, f _{BUS} = 40 MHz, all peripherals disabled	1.5	1.7	—	
	Supply Current (Deep-Sleep1 Mode)	V _{DD} = 3.0 V, HSE/HSI/PLL/LSE clocks off, LDO in low power mode, LSI on, RTC on	32.4	49.6	—	μA
	Supply Current (Deep-Sleep2 Mode)	V _{DD} = 3.0 V, HSE/HSI/PLL/LSE clocks off, LDO off, LSI on, RTC on	3.2	4.9	—	
Supply Current (Power-Down Mode)	V _{DD} = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC on	1.40	2.2	—		
	V _{DD} = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC off	1.35	2.1	—		

- Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
 2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
 3. RTC means real-time clock.
 4. Code = while (1) {208 NOP} executed in Flash.
 5. f_{BUS} means f_{HCLK} and f_{PCLK}.

Reset and Supply Monitor Characteristics

Table 11. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{POR}	Power On Reset Threshold (Rising Voltage on V _{DD})	T _A = -40 °C ~ +85 °C	1.66	1.79	1.90	V
V _{PDR}	Power Down Reset Threshold (Falling Voltage on V _{DD})	T _A = -40 °C ~ +85 °C	1.49	1.64	1.78	V
V _{PORHYST}	POR Hysteresis	—	—	150	—	mV
t _{POR}	Reset Delay Time	V _{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.

2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 12. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
V _{BOD}	Voltage of Brown Out Detection	T _A = -40 °C ~ +85 °C After factory-trimmed (V _{DD} Falling edge)	2.02	2.1	2.18	V	
V _{LVD}	Voltage of Low Voltage Detection	T _A = -40°C ~ +85°C (V _{DD} Falling edge)	LVDS = 000	2.17	2.25	2.33	V
			LVDS = 001	2.32	2.4	2.48	V
			LVDS = 010	2.47	2.55	2.63	V
			LVDS = 011	2.62	2.7	2.78	V
			LVDS = 100	2.77	2.85	2.93	V
			LVDS = 101	2.92	3.0	3.08	V
			LVDS = 110	3.07	3.15	3.23	V
LVDS = 111	3.22	3.3	3.38	V			
V _{LVDHYST}	LVD Hysteresis	V _{DD} = 3.3 V	—	—	100	mV	
t _{suLVD}	LVD Setup Time	V _{DD} = 3.3 V	—	—	5	μs	
t _{aiLVD}	LVD Active Delay Time	V _{DD} = 3.3 V	—	—	—	ms	
I _{DDLVD}	Operation Current ⁽³⁾	V _{DD} = 3.3 V	—	—	5	μA	

Note: 1. Data based on characterization results only, not tested in production.

2. Bandgap current is not included.

3. The LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 13. High Speed External Clock (HSE) Characteristics

$T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	2.0	—	3.6	V
f_{CK_HSE}	HSE Oscillator Frequency	—	4	—	16	MHz
C_L	Load Capacitance	$V_{DD} = 3.3\text{ V}$, $R_{ESR} = 100\ \Omega$ @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT Pins	—	—	1	—	M Ω
R_{ESR}	Equivalent Series Resistance	$V_{DD} = 3.3\text{ V}$, $C_L = 12\text{ pF}$ @ 16 MHz, HSEGAIN = 0 $V_{DD} = 2.4\text{ V}$, $C_L = 12\text{ pF}$ @ 16 MHz, HSEGAIN = 1	—	—	160	Ω
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	$V_{DD} = 3.3\text{ V}$ @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	$V_{DD} = 3.3\text{ V}$	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	$V_{DD} = 3.3\text{ V}$	—	—	4	ms

Table 14. Low Speed External Clock (LSE) Characteristics

$T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	2.0	—	3.6	V
f_{CK_LSE}	LSE Oscillator Frequency	$V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}$	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	M Ω
R_{ESR}	Equivalent Series Resistance	$V_{DD} = 3.3\text{ V}$	30	—	TBD	k Ω
C_L	Recommended Load Capacitance	$V_{DD} = 3.3\text{ V}$	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	$f_{CK_LSE} = 32.768\text{ kHz}$, $R_{ESR} = 50\text{ k}\Omega$, $C_L \geq 7\text{ pF}$, $V_{DD} = 2.0\text{ V} \sim 2.7\text{ V}$, $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	$f_{CK_LSE} = 32.768\text{ kHz}$, $R_{ESR} = 50\text{ k}\Omega$, $C_L < 7\text{ pF}$, $V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}$, $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	—	1.8	3.3	μA
	Oscillator Power Down Current	—	—	—	0.01	μA
t_{SULSE}	Startup Time (Low Current Mode)	$f_{CK_LSE} = 32.768\text{ kHz}$, $V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}$	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 15. High Speed Internal Clock (HSI) Characteristics

$T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	2.0	—	3.6	V
f_{CK_HSI}	HSI Oscillator Frequency	$V_{DD} = 3.3\text{ V @ } 25\text{ }^\circ\text{C}$	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	$V_{DD} = 3.3\text{ V}, T_A = 25\text{ }^\circ\text{C}$	-2	—	2	%
		$V_{DD} = 2.5\text{ V} \sim 3.6\text{ V}, T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	-3	—	3	%
		$V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}, T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	-4	—	4	%
Duty	Duty Cycle	$f_{CK_HSI} = 8\text{ MHz}$	35	—	65	%
I_{DDHSI}	HSI Oscillator Supply Current	$f_{CK_HSI} = 8\text{ MHz}$	—	300	500	μA
	HSI Oscillator Power Down Current		—	—	0.05	μA
t_{SUHSI}	HSI Oscillator Startup Time	$f_{CK_HSI} = 8\text{ MHz}$	—	—	10	μs

Table 16. Low Speed Internal Clock (LSI) Characteristics

$T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{CK_LSI}	LSI Oscillator Frequency	$V_{DD} = 3.3\text{ V}, T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	21	32	43	kHz
ACC_{LSI}	LSI Oscillator Frequency Accuracy	After factory-trimmed, $V_{DD} = 3.3\text{ V}, T_A = 25\text{ }^\circ\text{C}$	-10	—	+10	%
$I_{DDL SI}$	LSI Oscillator Operating Current	$V_{DD} = 3.3\text{ V}, T_A = 25\text{ }^\circ\text{C}$	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	$V_{DD} = 3.3\text{ V}, T_A = 25\text{ }^\circ\text{C}$	—	—	100	μs

System PLL Characteristics

Table 17. System PLL Characteristics

$T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	40	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 18. Flash Memory Characteristics

$T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before Failure (Endurance)	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	20	—	—	K Cycles
t_{RET}	Data Retention Time	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	10	—	—	Years
t_{PROG}	Word Programming Time	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	20	—	—	μs
t_{ERASE}	Page Erase Time	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	2	—	—	ms
t_{MERASE}	Mass Erase Time	$T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$	10	—	—	ms

I/O Port Characteristics

Table 19. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
I _{IL}	Low Level Input Current	3.3 V I/O	V _I = V _{SS} , On-chip pull-up resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
I _{IH}	High Level Input Current	3.3 V I/O	V _I = V _{DD} , On-chip pull-down resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
V _{IL}	Low Level Input Voltage	3.3 V I/O	-0.4	—	V _{DD} × 0.35	V	
		Reset pin	-0.4	—	V _{DD} × 0.35		
V _{IH}	High Level Input Voltage	3.3 V I/O	V _{DD} × 0.65	—	V _{DD} + 0.5	V	
		Reset pin	V _{DD} × 0.65	—	V _{DD} + 0.5		
V _{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O	—	0.12 × V _{DD}	—	mV	
		Reset pin	—	0.12 × V _{DD}	—		
I _{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V _{OL} = 0.4 V	4	—	—	mA	
		3.3 V I/O 8 mA drive, V _{OL} = 0.4 V	8	—	—		
		3.3 V I/O 12 mA drive, V _{OL} = 0.4 V	12	—	—		
		3.3 V I/O 16 mA drive, V _{OL} = 0.4 V	16	—	—		
I _{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, V _{OH} = V _{DD} - 0.4 V	4	—	—	mA	
		3.3 V I/O 8 mA drive, V _{OH} = V _{DD} - 0.4 V	8	—	—		
		3.3 V I/O 12 mA drive, V _{OH} = V _{DD} - 0.4 V	12	—	—		
		3.3 V I/O 16 mA drive, V _{OH} = V _{DD} - 0.4 V	16	—	—		
V _{OL}	Low Level Output Voltage	3.3 V 4 mA drive I/O, I _{OL} = 4 mA	—	—	0.4	V	
		3.3 V 8 mA drive I/O, I _{OL} = 8 mA	—	—	0.4		
		3.3 V 12 mA drive I/O, I _{OL} = 12 mA	—	—	0.4		
		3.3 V 16 mA drive I/O, I _{OL} = 16 mA	—	—	0.4		
V _{OH}	High Level Output Voltage	3.3 V 4 mA drive I/O, I _{OH} = 4 mA	V _{DD} - 0.4	—	—	V	
		3.3 V 8 mA drive I/O, I _{OH} = 8 mA	V _{DD} - 0.4	—	—		
		3.3 V 12 mA drive I/O, I _{OH} = 12 mA	V _{DD} - 0.4	—	—		
		3.3 V 16 mA drive I/O, I _{OH} = 16 mA	V _{DD} - 0.4	—	—		
R _{PU}	Internal Pull-up Resistor	3.3 V I/O	—	46	—	kΩ	
R _{PD}	Internal Pull-down Resistor	3.3 V I/O	—	46	—	kΩ	

ADC Characteristics

Table 20. ADC Characteristics

$T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.5	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	A/D Converter Current Consumption	$V_{DDA} = 3.3\text{ V}$	—	1	—	mA
I_{ADC_DN}	A/D Converter Power Down Current Consumption	$V_{DDA} = 3.3\text{ V}$	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	Mbps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0]=2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	k Ω
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	$f_S = 750\text{ kbps}$, $V_{DDA} = 3.3\text{ V}$	—	± 2	± 5	LSB
DNL	Differential Non-linearity Error	$f_S = 750\text{ kbps}$, $V_{DDA} = 3.3\text{ V}$	—	± 1	—	LSB
E_O	Offset Error	—	—	—	± 10	LSB
E_G	Gain Error	—	—	—	± 10	LSB

Note: 1. Data based on characterization results only, not tested in production.

- Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.
- The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S . Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I , must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

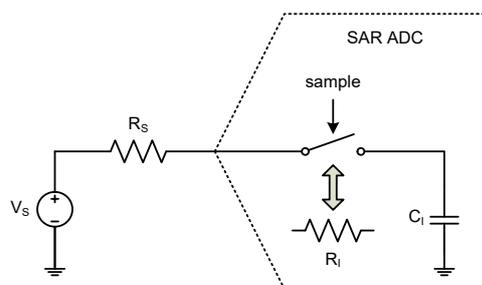


Figure 5. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below 1/4 LSB is ensured by using the following equation:

$$R_s < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_t$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_s may be larger than the value indicated by the equation above.

SCTM/GPTM//MCTM Characteristics

Table 21. SCTM/GPTM/MCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM and MCTM	—	—	—	40	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 22. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time ⁽⁵⁾	0	—	0	—	0	—	ns
	SDA Data Hold Time ⁽⁶⁾	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.

2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.

3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.

4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 20 MHz.

5. This characteristic parameter of the I²C bus timing is based on: COMB_FILTER_En = 0 and SEQ_FILTER = 00.

6. This characteristic parameter of the I²C bus timing is based on: COMB_FILTER_En = 1 and SEQ_FILTER = 00.

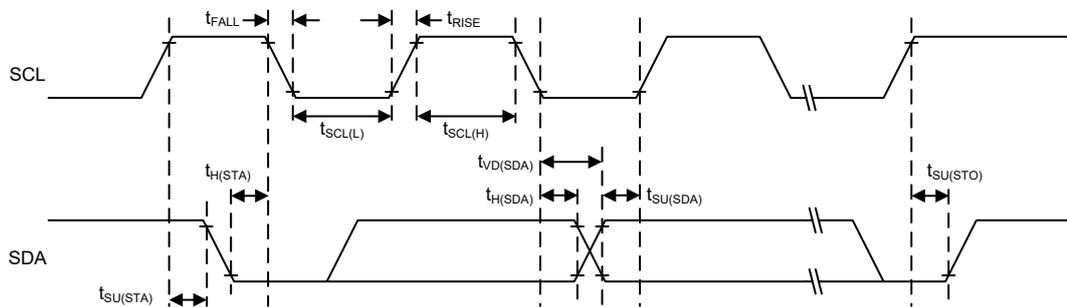


Figure 6. I²C Timing Diagram

SPI Characteristics

Table 23. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK} ($1/t_{SCK}$)	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High / Low Time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK} ($1/t_{SCK}$)	SPI slave output SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3 \times t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2 \times t_{PCLK}$	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3 \times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

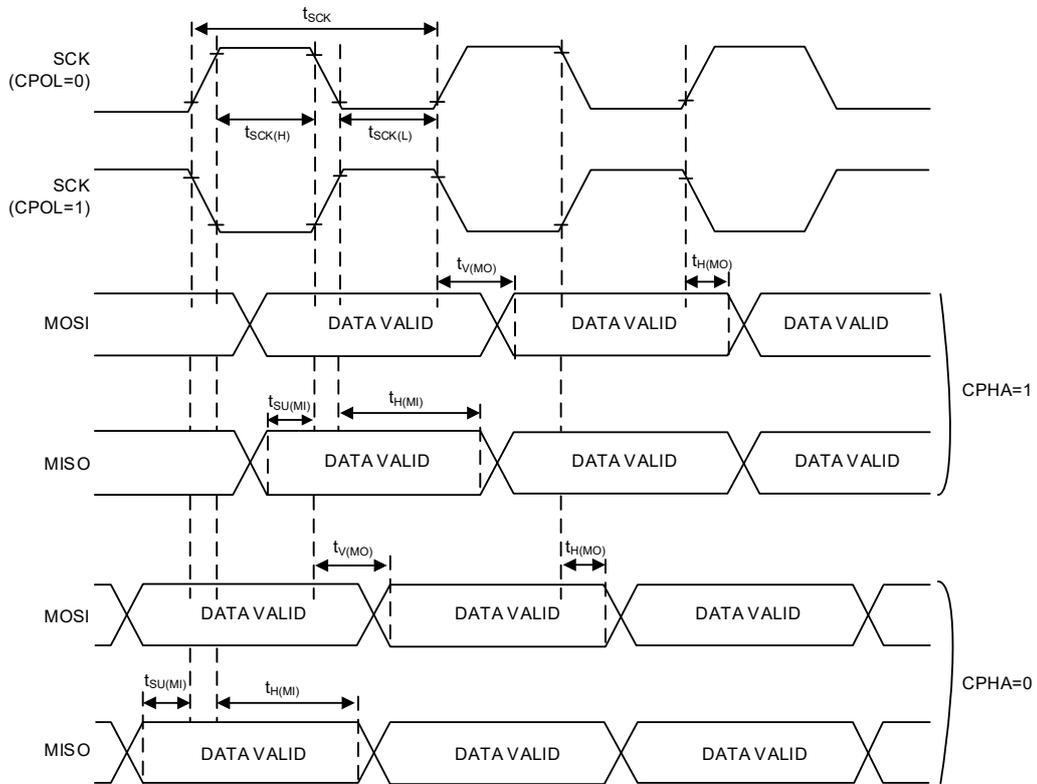


Figure 7. SPI Timing Diagrams – SPI Master Mode

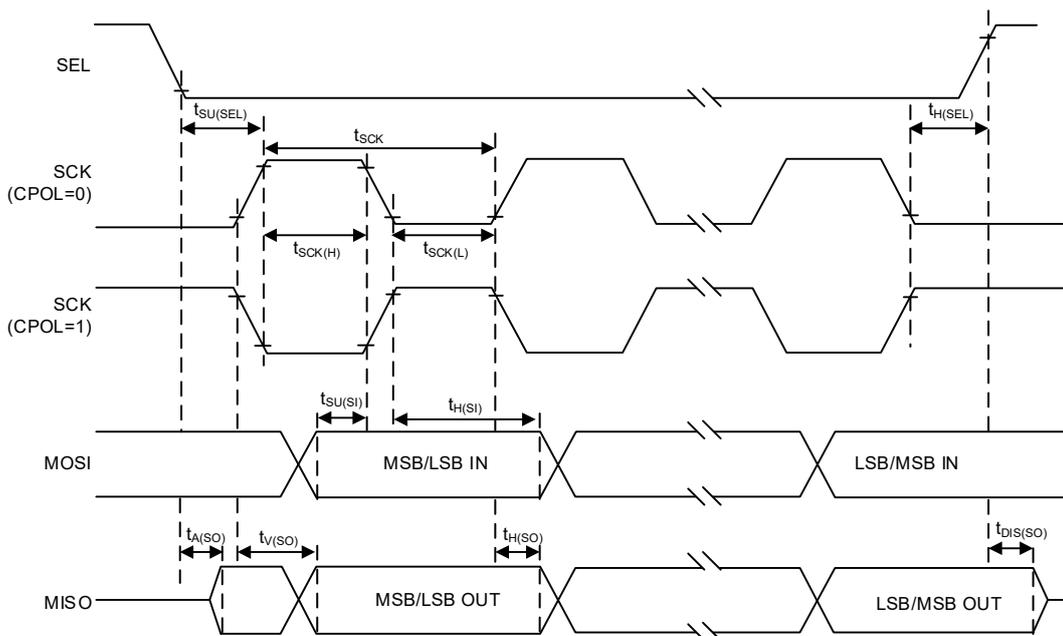


Figure 8. SPI Timing Diagrams – SPI Slave Mode with CPHA = 1

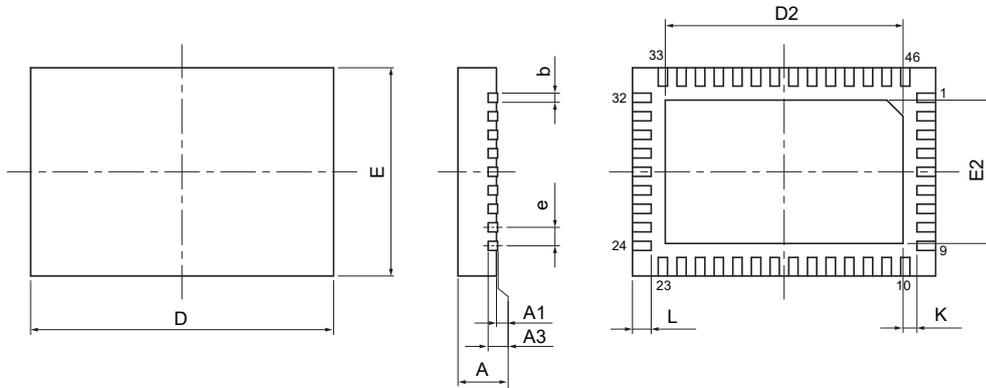
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package Information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

SAW Type 46-pin (6.5mm×4.5mm×0.75mm) QFN Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 REF	—
b	0.006	0.008	0.010
D	—	0.256 BSC	—
E	—	0.177 BSC	—
e	—	0.016 BSC	—
D2	0.197	—	0.205
E2	0.118	—	0.126
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 REF	—
b	0.15	0.20	0.25
D	—	6.50 BSC	—
E	—	4.50 BSC	—
e	—	0.40 BSC	—
D2	5.00	—	5.20
E2	3.00	—	3.20
L	0.35	0.40	0.45
K	0.20	—	—

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