HOLTEK

HT32L52231/HT32L52241 Datasheet

32-Bit Arm® Cortex®-M0+ Microcontroller, up to 64 KB Flash and 8 KB SRAM with 1 Msps ADC, PDMA, DIV, USART, UART, SPI, I²C, MCTM, GPTM, SCTM, BFTM, CRC, UID, RTC and WDT

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1 General Description

The Holtek HT32L52231/52241 devices are high performance, ultra-low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The devices operate at a frequency of up to 48 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 64 KB of embedded Flash memory for code / data storage and up to 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as PDMA, Hardware Divider DIV, ADC, I^{2}C, USART, UART, SPI, MCTM, GPTM, SCTM, BFTM, CRC-16/32, 96-bit Unique ID, RTC, WDT and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in ultra-low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as handheld devices, personal medical devices, home automation, industrial sensors and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 48 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- Up to 64 KB on-chip Flash memory for instruction/data and option byte storage
- Up to 8 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the HT32L52231/52241 series devices, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and a cache buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a cache buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
    - Power On Reset / Power Down Reset – POR / PDR
    - Brown-out Detector – BOD
    - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ± 1 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock pre-scaler, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M0+ are derived from the system clock (CK_SYS) which can source from the HSI, HSE, LSI, LSE or system PLL. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management – PWRCU

- Single V_{DD} power supply: 1.65 V to 3.6 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- V_{DD} and V_{CORE} power domains
- Six power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Deep-Sleep3, Power-Down, Deep Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2, Deep-Sleep3, Power-Down and Deep Power-Down modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger sources and types
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels
- Build-in bandgap voltage (V_{BG}) for internal analog input channel
- External reference voltage input possibility
- Conversion range: $V_{REF+} \sim V_{SSA}$

A 12-bit multi-channel Analog to Digital Converter is integrated in the devices. There are multiplexed channels, which include up to 12 external analog signal channels and 4 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

The internal voltage reference generator (VREF) which can provide a stable bandgap voltage (V_{BG}) for the A/D Converter is internally connected to the ADC input channel. The precise voltage of the V_{BG} is individually measured for each part by Holtek during production test.

The internal temperature sensor (TS) can be used to measure the junction temperature (T_j) of the devices. The temperature sensor is internally connected to the ADC input channels which are used to convert the sensor output voltage to a digital value. The temperature sensor output voltage changes linearly with temperature.

I/O Ports – GPIO

- Up to 40 GPIOs
- Port A, B, C are mapped to 16-Line EXTI interrupts
- Almost all I/O pins have configurable output driving current
- Almost all I/O pins are 5 V-tolerant except for pins shared with analog inputs

There are up to 40 General Purpose I/O pins, GPIO, for the implementation of logic input / output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion

- Supports 3-phase motor control and hall sensor interface
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer Module, MCTM, consists of a single 16-bit up/down counter, four 16-bit Capture / Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR), 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer Module, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture / Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a quadrature decoder with two inputs.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single Channel Timer Module, SCTM, consists of one 16-bit up-counter, one 16-bit Capture / Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control / status registers. They can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM output.

Basic Function Timer – BFTM

- 32-bit compare match count-up counter - no I/O control
- One shot mode - counter stops counting when compare match occurs
- Repetitive mode - counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals, generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes which are repetitive and one shot modes. In the repetitive mode, the counter will be restarted at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuitry that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real-Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} power domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detection and clock synchronization to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line SCK, and the slave select line SEL. One SPI device acts as a master who controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive the data bits, the streamlined data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to (f_{PCLK}/16) MHz for asynchronous mode and (f_{PCLK}/8) MHz for synchronous mode
- Full duplex communication
- Supports LIN (Local Interconnect Network) mode
- Supports single-wire mode
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes an 8-level transmitter FIFO, (TX_FIFO) and an 8-level receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of the transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to $f_{PCLK}/16$ MHz
- Full duplex communication
- Supports LIN (Local Interconnect Network) mode
- Supports single-wire mode
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16}+X^{15}+X^{2}+1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16}+X^{12}+X^{5}+1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16- or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports Address increment, decrement and fixed modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger sources:
  ADC, SPI, USART, UART, I^2C, MCTM, GPTM and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed / unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and requires a software triggered start signal by controlling register the "START" bit in the control register. The divider calculation complete flag will be set to 1 after 8 clock cycles, however, if the divisor register data is zero during the calculation, the division by zero error flag will be set to 1.

Unique Identifier – UID

- Total 96-bit UID is unique and not duplicate with other HT32 MCU devices
- It is unchangeable and determined by MCU manufacturer

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 32-pin QFN and 48-pin LQFP packages
- Operation temperature range: -40 °C to 105 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32L52231	HT32L52241
Main Flash (KB)		32	63
Option Byte Flash (KB)		1	1
SRAM (KB)		4	8
Timers	MCTM	1	
	GPTM	1	
	SCTM	2	
	BFTM	2	
	RTC	1	
	WDT	1	
Communication	SPI	2	
	USART	1	
	UART	2	
	I²C	2	
Hardware Divider		1	
PDMA		6 Channels	
CRC-16/32		1	
EXTI		16	
12-bit ADC		1	
Number of channels		12 External Channels	
GPIO		Up to 40	
CPU frequency		Up to 48 MHz	
Operating voltage		1.65 V ~ 3.6 V	
Operating temperature		-40 °C ~ 105 °C	
Package		32-pin QFN, 48-pin LQFP	

Block Diagram

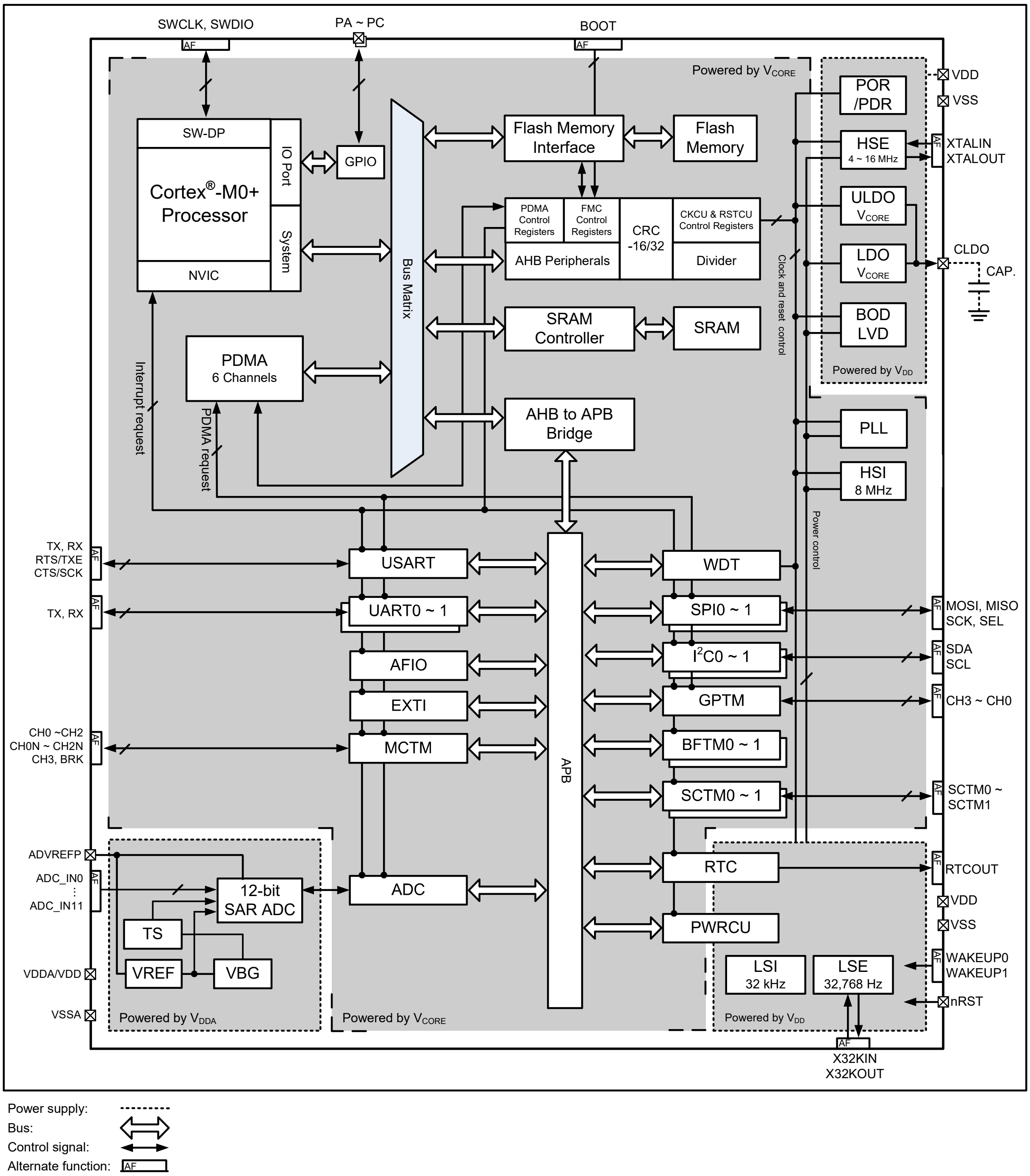


Figure 1. Block Diagram

Memory Map

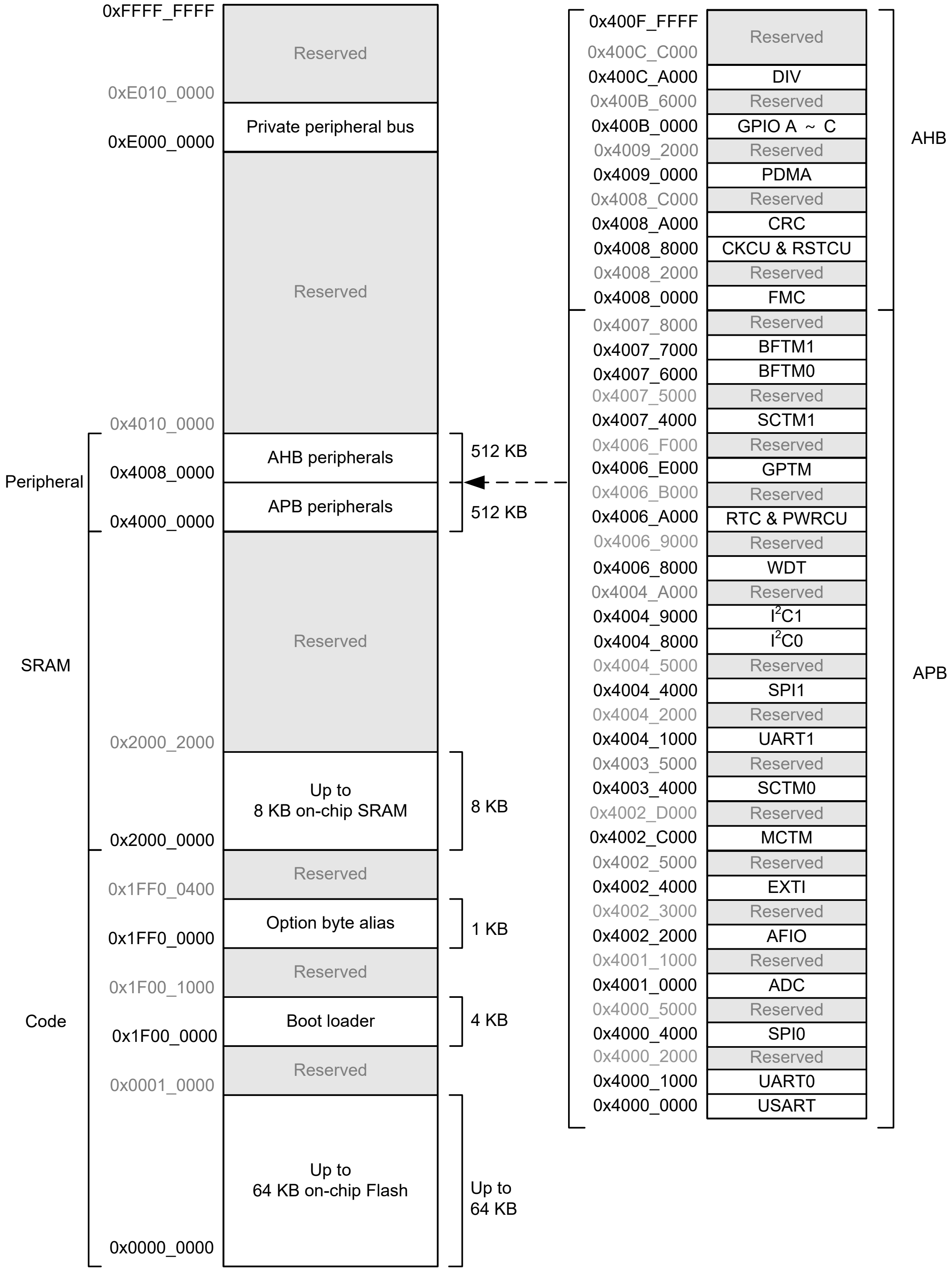


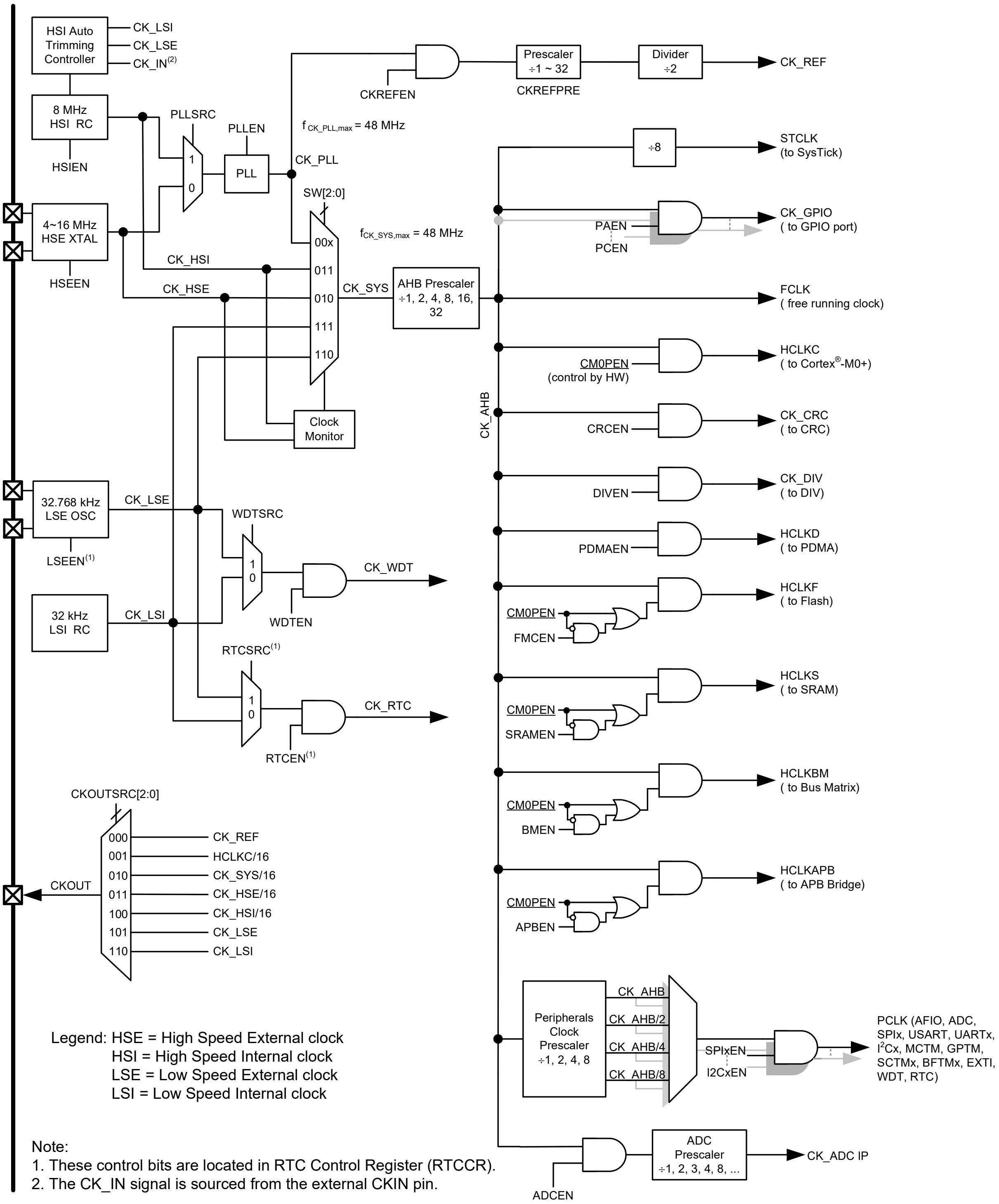
Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C0	
0x4004_9000	0x4004_9FFF	I^2C1	
0x4004_A000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure



Legend: HSE = High Speed External clock
HSI = High Speed Internal clock
LSE = Low Speed External clock
LSI = Low Speed Internal clock

Note:
1. These control bits are located in RTC Control Register (RTCCR).
2. The CK_IN signal is sourced from the external CKIN pin.

Figure 3. Clock Structure

4 Pin Assignment

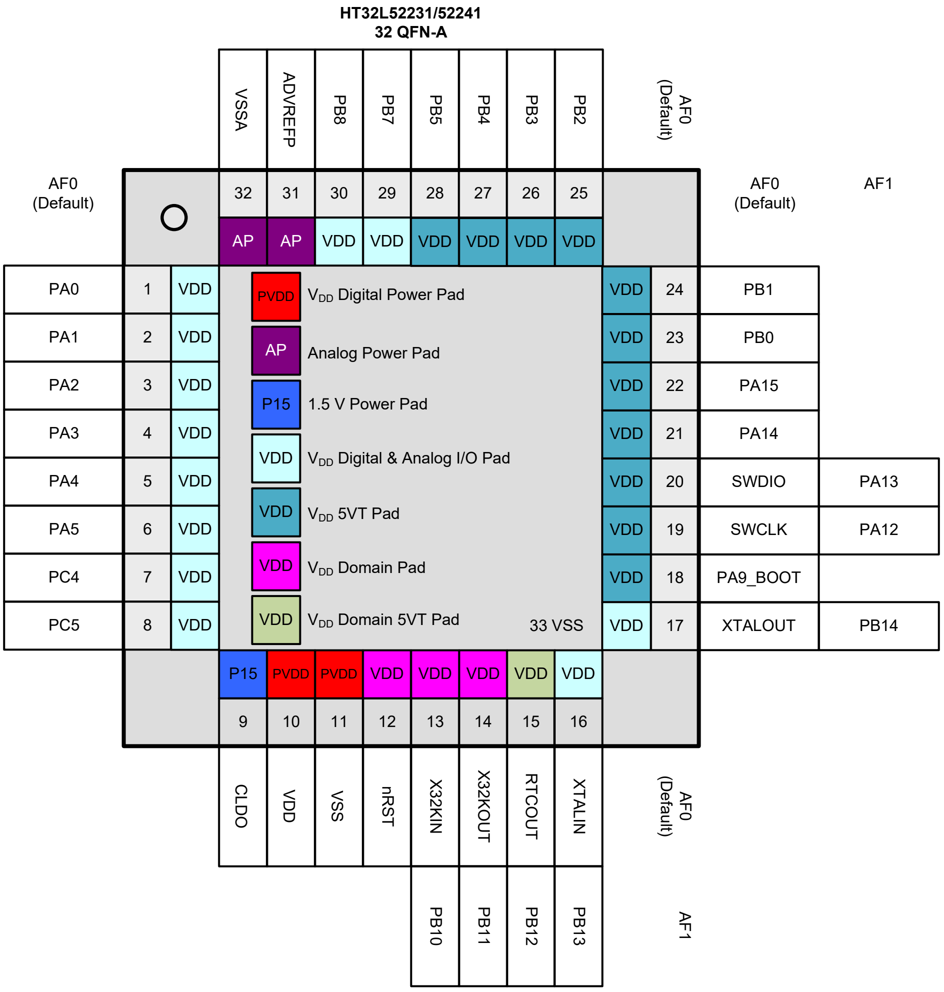


Figure 4. 32-pin QFN Pin Assignment

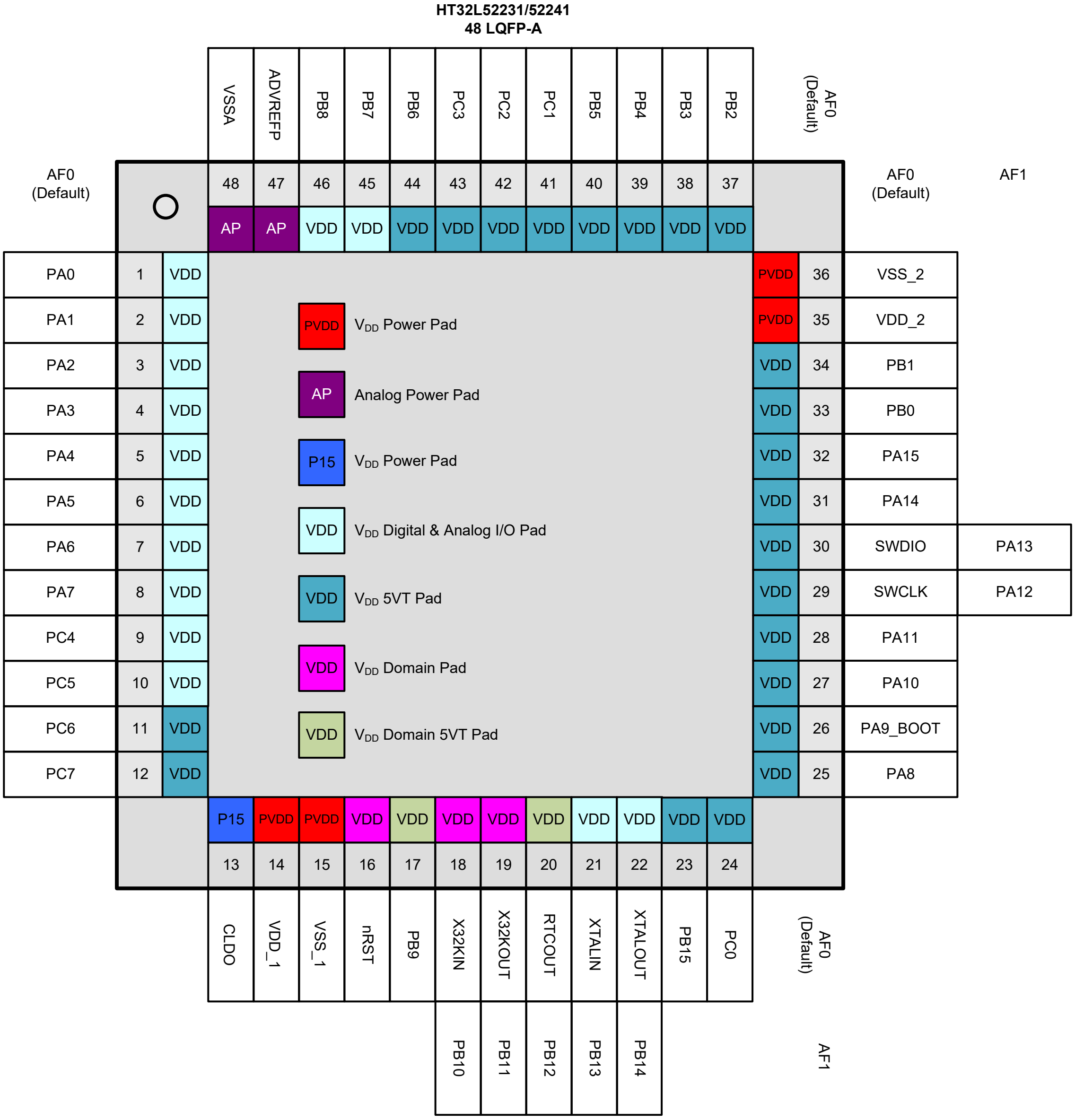


Figure 5. 48-pin LQFP Pin Assignment

Table 3. Pin Assignment

Package		Alternate Function Mapping															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	32 QFN	System Default	GPIO	ADC	N/A	MCTM /GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
1	1	PA0		ADC_IN2		GT_CH0	SPI1_SCK	USR_RTS	I2C1_SCL								VBG
2	2	PA1		ADC_IN3		GT_CH1	SPI1_MOSI	USR_CTS	I2C1_SDA								
3	3	PA2		ADC_IN4		GT_CH2	SPI1_MISO	USR_TX									
4	4	PA3		ADC_IN5		GT_CH3	SPI1_SEL	USR_RX									
5	5	PA4		ADC_IN6		GT_CH0	SPI0_SCK	UR1_TX	I2C0_SCL								
6	6	PA5		ADC_IN7		GT_CH1	SPI0_MOSI	UR1_RX	I2C0_SDA								
7		PA6		ADC_IN8		GT_CH2	SPI0_MISO										
8		PA7		ADC_IN9		GT_CH3	SPI0_SEL										
9	7	PC4		ADC_IN10		GT_CH0	SPI1_SEL	USR_TX	I2C1_SCL						SCTM0		
10	8	PC5		ADC_IN11		GT_CH1	SPI1_SCK	USR_RX	I2C1_SDA						SCTM1		
11		PC6				MT_CH2		UR0_TX	I2C0_SCL								
12		PC7				MT_CH2N		UR0_RX	I2C0_SDA								
13	9	CLDO															
14	10	VDD_1															
15	11	VSS_1															
16	12	nRST															
17		PB9				MT_CH3											WAKEUP1
18	13	X32KIN	PB10			GT_CH0	SPI1_SEL	USR_TX							SCTM0		
19	14	X32KOUT	PB11			GT_CH1	SPI1_SCK	USR_RX							SCTM1		
20	15	RTCOUT	PB12				SPI0_MISO	UR0_RX							SCTM0		WAKEUP0
21	16	XTALIN	PB13			MT_CH1		UR0_TX	I2C0_SCL								
22	17	XTALOUT	PB14			MT_CH1N		UR0_RX	I2C0_SDA								
23		PB15				MT_CH0	SPI0_SEL		I2C1_SCL								
24		PC0				MT_CH0N	SPI0_SCK		I2C1_SDA						SCTM1		
25		PA8						USR_TX							SCTM0		
26	18	PA9_BOOT					SPI0_MOSI								SCTM1		CKOUT
27		PA10				MT_CH1	SPI0_MOSI	USR_RX									
28		PA11				MT_CH1N	SPI0_MISO								SCTM0		
29	19	SWCLK	PA12														

Package		Alternate Function Mapping															
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	32 QFN	System Default	GPIO	ADC	N/A	MCTM /GPTM	SPI	USART /UART	I^{2}C	N/A	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
30	20	SWDIO	PA13														
31	21	PA14				MT_CH0	SPI1_SEL	USR_RTS	I2C1_SCL								
32	22	PA15				MT_CH0N	SPI1_SCK	USR_CTS	I2C1_SDA						SCTM1		
33	23	PB0				MT_CH1	SPI1_MOSI	USR_TX	I2C0_SCL								
34	24	PB1				MT_CH1N	SPI1_MISO	USR_RX	I2C0_SDA						SCTM0		
35		VDD_2															
36	EP	VSS_2															
37	25	PB2				MT_CH2	SPI0_SEL	UR1_TX									CKIN
38	26	PB3				MT_CH2N	SPI0_SCK	UR1_RX							SCTM1		
39	27	PB4				MT_BRK	SPI0_MOSI	UR1_TX							SCTM0		
40	28	PB5				GT_CH2	SPI0_MISO	UR1_RX									
41		PC1				MT_CH0	SPI1_SEL	UR1_TX									
42		PC2				MT_CH0N	SPI1_SCK										
43		PC3				MT_BRK	SPI1_MOSI	UR1_RX									
44		PB6				GT_CH3	SPI1_MISO	UR0_TX									
45	29	PB7		ADC_IN0		MT_CH1	SPI0_MISO	UR0_TX	I2C1_SCL								
46	30	PB8		ADC_IN1		MT_CH1N	SPI0_SEL	UR0_RX	I2C1_SDA								
47	31	ADVREFP															
48	32	VSSA															

Note: The EP is meant the exposed pad of the QFN package.

Table 4. Pin Description

Pin Number		Pin Name	Type [(1)]	I/O Structure [(2)]	Output Driving	Description
48LQFP	32QFN					Default Function (AF0)
1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2
4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3
5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4, this pin provides a UART_TX function in the Boot loader mode.
6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5, this pin provides a UART_RX function in the Boot loader mode.
7		PA6	AI/O	33V	4/8/12/16 mA	PA6
8		PA7	AI/O	33V	4/8/12/16 mA	PA7
9	7	PC4	AI/O	33V	4/8/12/16 mA	PC4
10	8	PC5	AI/O	33V	4/8/12/16 mA	PC5
11		PC6	I/O	33V	4/8/12/16 mA	PC6
12		PC7	I/O	33V	4/8/12/16 mA	PC7
13	9	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connect a 2.2 μF capacitor as close as possible between this pin and VSS_1.
14	10	VDD_1	P	—	—	Voltage for digital I/O
15	11	VSS_1	P	—	—	Ground reference for digital I/O
16	12	nRST[(3)]	I	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
17		PB9[(3)]	I/O (V_{DD})	5VT	4/8/12/16 mA	PB9
18	13	PB10[(3)]	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KIN
19	14	PB11[(3)]	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KOUT
20	15	PB12[(3)]	I/O (V_{DD})	5VT	4/8/12/16 mA	RTCOUT
21	16	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
22	17	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
23		PB15	I/O	5VT	4/8/12/16 mA	PB15
24		PC0	I/O	5VT	4/8/12/16 mA	PC0
25		PA8	I/O	5VT	4/8/12/16 mA	PA8
26	18	PA9	I/O	5VT_PU	4/8/12/16 mA	PA9_BOOT
27		PA10	I/O	5VT	4/8/12/16 mA	PA10
28		PA11	I/O	5VT	4/8/12/16 mA	PA11
29	19	PA12	I/O	5VT_PU	4/8/12/16 mA	SWCLK
30	20	PA13	I/O	5VT_PU	4/8/12/16 mA	SWDIO
31	21	PA14	I/O	5VT	4/8/12/16 mA	PA14
32	22	PA15	I/O	5VT	4/8/12/16 mA	PA15
33	23	PB0	I/O	5VT	4/8/12/16 mA	PB0
34	24	PB1	I/O	5VT	4/8/12/16 mA	PB1
35		VDD_2	P	—	—	Voltage for digital I/O
36	EP	VSS_2	P	—	—	Ground reference for digital I/O
37	25	PB2	I/O	5VT	4/8/12/16 mA	PB2

Pin Number		Pin Name	Type (1)	I/O Structure (2)	Output Driving	Description
48LQFP	32QFN					Default Function (AF0)
38	26	PB3	I/O	5VT	4/8/12/16 mA	PB3
39	27	PB4	I/O	5VT	4/8/12/16 mA	PB4
40	28	PB5	I/O	5VT	4/8/12/16 mA	PB5
41		PC1	I/O	5VT	4/8/12/16 mA	PC1
42		PC2	I/O	5VT	4/8/12/16 mA	PC2
43		PC3	I/O	5VT	4/8/12/16 mA	PC3
44		PB6	I/O	5VT	4/8/12/16 mA	PB6
45	29	PB7	AI/O	33V	4/8/12/16 mA	PB7
46	30	PB8	AI/O	33V	4/8/12/16 mA	PB8
47	31	ADVREFP	P	—	—	Analog voltage for ADC
48	32	VSSA	P	—	—	Ground reference for the ADC

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, V_{DD} = V_{DD} Power, EP = Exposed Pad.
2. 33V = 3.3 V-tolerant, 5VT = 5 V-tolerant , PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, the UART interface is available for communication.

5 Electrical Characteristics

Power Supply Scheme

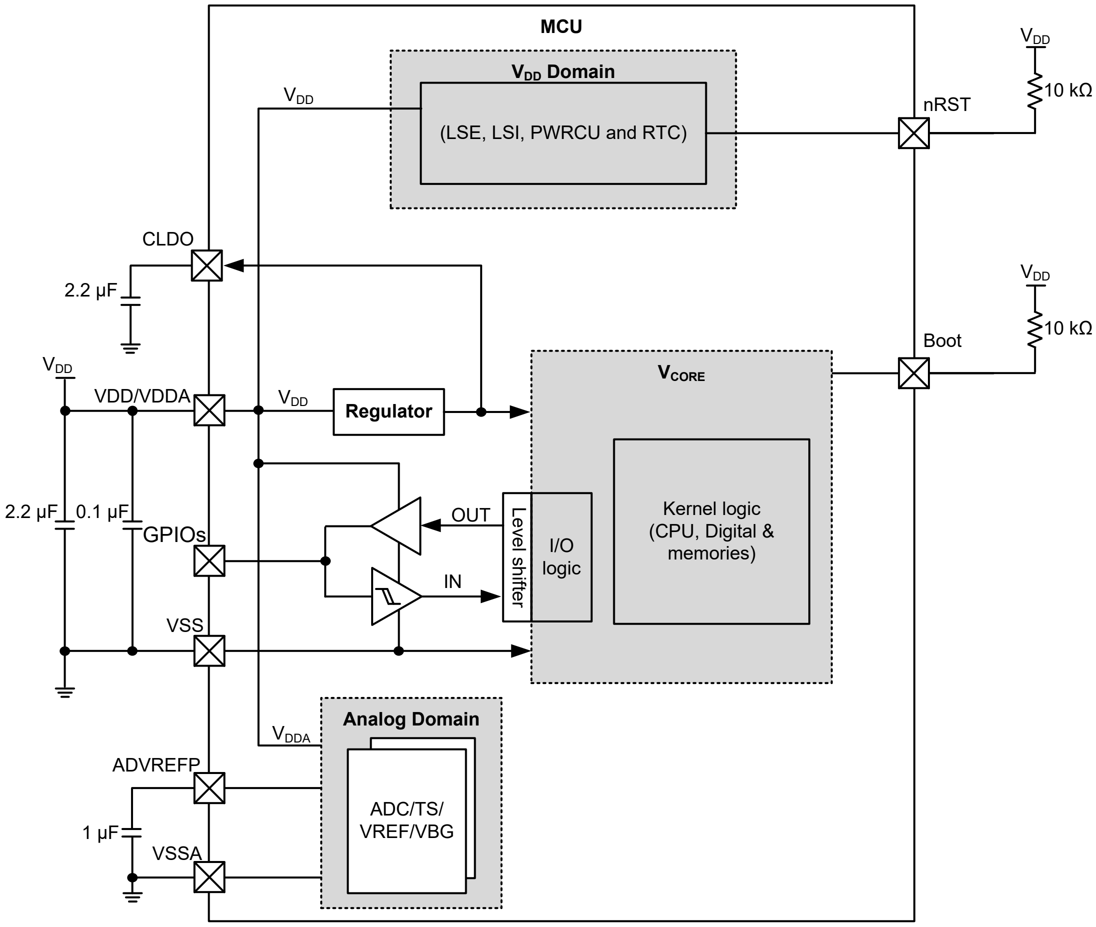


Figure 6. Power Supply Scheme

Note: 1. All regulator capacitors must be placed as close to the MCU as possible.
2. It is recommended that the pull-up resistor of the Boot pin is 10 kΩ.
3. It is recommended that the pull-up resistor of the nRST pin is 10 kΩ.

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{IN}	Input Voltage on 5 V-tolerant I/O	V_{SS} - 0.3	V_{SS} + 5.5	V
	Input Voltage on Other I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	105	°C
T_{STG}	Storage Temperature Range	-60	150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	1.65	3.3	3.6	V
V_{DDA}	Analog Operating Voltage	—	2.0	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.0 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, after trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0 V Regulator input	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

On-Chip Ultra-low Power LDO Voltage Regulator Characteristics

Table 8. ULDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ULDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{ULDO} = 2 mA and voltage variant = ±5 %, after trimming	1.425	1.5	1.57	V
I_{ULDO}	Output Current	V_{DD} = 1.65 V ~ 3.6 V Regulator input @ V_{ULDO} = 1.5 V	—	2	5	mA
C_{ULDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	µF

Power Consumption

The current consumption is influenced by several parameters and factors, including the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is configured under the following conditions for current consumption measured:

- All I/O pins are set to a high-impedance (floating) state.
- All peripherals are disabled unless specifically stated otherwise.
- The Flash memory access time is optimized using the minimum wait states number, depending on the f_{HCLK} frequency.
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$.

Table 9. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max. @ T_A		Unit
						25 °C	105 °C	
I_{DD}	Supply Current (Run Mode)	48 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz	All peripherals enabled	9.2	9.8	—	mA
				All peripherals disabled	3.9	4.2	—	
		32 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 32 MHz	All peripherals enabled	6.5	6.9	—	
				All peripherals disabled	3.0	3.2	—	
		16 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 16 MHz	All peripherals enabled	3.4	3.6	—	
				All peripherals disabled	1.60	1.73	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = off	All peripherals enabled	1.67	1.79	—	
				All peripherals disabled	0.82	0.89	—	
		32 kHz	V_{DD} = 3.3 V, LSI = 32 kHz, LDO off, ULDO on	All peripherals enabled	7.0	7.6	—	µA
				All peripherals disabled	3.5	3.9	—	

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max. @ T_A		Unit
						25 °C	105 °C	
I_{DD}	Supply Current (Sleep Mode)	48 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz	All peripherals enabled	6.8	7.3	—	mA
				All peripherals disabled	0.81	0.90	—	
		32 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 32 MHz	All peripherals enabled	4.8	5.1	—	
				All peripherals disabled	0.68	0.77	—	
		16 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 16 MHz	All peripherals enabled	2.5	2.7	—	
				All peripherals disabled	0.56	0.65	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = off	All peripherals enabled	1.24	1.34	—	
				All peripherals disabled	295.9	345.7	—	µA
		32 kHz	V_{DD} = 3.3 V, LSI = 32 kHz, LDO off, ULDO on	All peripherals enabled	5.3	7.0	—	
				All peripherals disabled	1.41	1.75	—	
	Supply Current (Deep-Sleep 1 Mode)	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on		1.15	1.48	—	µA
	Supply Current (Deep-Sleep 2 Mode)	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on		1.15	1.48	—	µA
	Supply Current (Deep-Sleep 3 Mode)	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI off, RTC off		0.54	0.86	—	µA
	Supply Current (Power-Down mode)	—	V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC on		0.86	0.93	—	
			V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC off		0.75	0.81	—	µA
	Supply Current (Deep Power-Down Mode)	—	V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI off		0.12	0.14	—	

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real-time clock.
4. Code = while (1) {208 NOP} executed in Flash.

Reset and Supply Monitor Characteristics

Table 10. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 105 °C	0.6	—	3.6	V
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 105 °C	1.40	1.55	1.65	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})	T_A = -40 °C ~ 105 °C	1.27	1.45	1.57	V
$V_{PORHYST}$	POR Hysteresis	—	—	100	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO and ULDO will be turned off.

Table 11. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed	V_{DD} Falling edge	1.62	1.68	1.74	V
			V_{DD} Rising edge	1.68	1.74	1.8	
$V_{BODHYST}$	BOD Hysteresis	V_{DD} = 2.0 V	—	—	60	—	mV
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	1.67	1.75	1.83	V
			LVDS = 001	1.87	1.95	2.03	V
			LVDS = 010	2.07	2.15	2.23	V
			LVDS = 011	2.27	2.35	2.43	V
			LVDS = 100	2.47	2.55	2.63	V
			LVDS = 101	2.67	2.75	2.83	V
			LVDS = 110	2.87	2.95	3.03	V
			LVDS = 111	3.07	3.15	3.23	V
$V_{LVDHYST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	200	—	μs
I_{DDLVD}	Operation Current (2)	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 12. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	—	1.65	—	3.6	V
f_{HSE}	HSE Frequency	—	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT Pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 00	—	—	160	Ω
		V_{DD} = 2.4 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 11				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3 V	—	—	4	ms

Table 13. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	—	1.65	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 1.65 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{DD} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L \geq$ 7 pF V_{DD} = 1.65 V ~ 2.7 V T_A = -40 °C ~ 105 °C	—	3.3	6.3	µA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L <$ 7 pF V_{DD} = 1.65 V ~ 3.6 V T_A = -40 °C ~ 105 °C	—	1.8	3.3	µA
	LSE Oscillator Power Down Current	—	—	—	0.01	µA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 1.65 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Table 14. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	—	1.65	—	3.6	V
f_{HSI}	HSI Frequency	V_{DD} = 3.3 V, T_A = 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-1	—	1	%
		V_{DD} = 1.65 V ~ 3.6 V, T_A = -20 °C ~ 60 °C	-1.5	—	2	%
		V_{DD} = 1.65 V ~ 3.6 V T_A = -40 °C ~ 105 °C	-2.5	—	2.5	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	HSI Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	µA
	HSI Oscillator Power Down Current	f_{HSI} = 8 MHz	—	—	0.05	µA
t_{SUHSI}	HSI Oscillator Startup Time	f_{HSI} = 8 MHz	—	—	10	µs

Table 15. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 105 °C	1.65	—	3.6	V
f_{LSI}	LSI Frequency	V_{DD} = 3.3 V, T_A = -40 °C ~ 105 °C	21	32	43	kHz
ACC_{LSI}	LSI Oscillator Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V	—	—	100	μs

System PLL Characteristics

Table 16. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	PLL Output Clock	—	16	—	48	MHz
t_{LOCK}	PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 17. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before Failure (Endurance)	T_A = -40 °C ~ 105 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 105 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 105 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 105 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 105 °C	10	—	—	ms

I/O Port Characteristics

Table 18. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V I/O	V_I = V_{SS}, On-chip pull-up resistor disabled	—	—	3	μA
		5 V-tolerant I/O					
		Reset pin					
I_{IH}	High Level Input Current	3.3 V I/O	V_I = V_{DD}, On-chip pull-down resistor disabled	—	—	3	μA
		5 V-tolerant I/O					
		Reset pin					
V_{IL}	Low Level Input Voltage	3.3 V I/O		- 0.3	—	V_{DD} × 0.35	V
		5 V-tolerant I/O					
		Reset pin					

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.3	V
		5 V-tolerant I/O				5.5	
		Reset pin				V_{DD} + 0.3	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O		—	0.12 × V_{DD}	—	mV
		5 V-tolerant I/O					
		Reset pin					
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O	4 mA drive, V_{OL} = 0.4 V	4	—	—	mA
		5 V-tolerant I/O					
		3.3 V I/O	8 mA drive, V_{OL} = 0.4 V	8	—	—	mA
		5 V-tolerant I/O					
		3.3 V I/O	12 mA drive, V_{OL} = 0.4 V	12	—	—	mA
		5 V-tolerant I/O					
		3.3 V I/O	16 mA drive, V_{OL} = 0.4 V	16	—	—	mA
		5 V-tolerant I/O					
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O	4 mA drive, V_{OH} = V_{DD} - 0.4 V	4	—	—	mA
		5 V-tolerant I/O					
		3.3 V I/O	8 mA drive, V_{OH} = V_{DD} - 0.4 V	8	—	—	mA
		5 V-tolerant I/O					
		3.3 V I/O	12 mA drive, V_{OH} = V_{DD} - 0.4 V	12	—	—	mA
		5 V-tolerant I/O					
		3.3 V I/O	16 mA drive, V_{OH} = V_{DD} - 0.4 V	16	—	—	mA
		5 V-tolerant I/O					
V_{OL}	Low Level Output Voltage	3.3 V I/O	4 mA drive, I_{OL} = 4 mA	—	—	0.4	V
		5 V-tolerant I/O					
		3.3 V I/O	8 mA drive, I_{OL} = 8 mA	—	—	0.4	V
		5 V-tolerant I/O					
		3.3 V I/O	12 mA drive, I_{OL} = 12 mA	—	—	0.4	V
		5 V-tolerant I/O					
		3.3 V I/O	16 mA drive, I_{OL} = 16 mA	—	—	0.4	V
		5 V-tolerant I/O					
V_{OH}	High Level Output Voltage	3.3 V I/O	4 mA drive, I_{OH} = 4 mA	V_{DD} - 0.4	—	—	V
		5 V-tolerant I/O					
		3.3 V I/O	8 mA drive, I_{OH} = 8 mA	V_{DD} - 0.4	—	—	V
		5 V-tolerant I/O					
		3.3 V I/O	12 mA drive, I_{OH} = 12 mA	V_{DD} - 0.4	—	—	V
		5 V-tolerant I/O					
		3.3 V I/O	16 mA drive, I_{OH} = 16 mA	V_{DD} - 0.4	—	—	V
		5 V-tolerant I/O					

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{PU}	Internal Pull-up Resistor	3.3 V I/O @ 3.3 V	—	60	—	kΩ
		5 V-tolerant I/O @ 3.3 V				
R_{PD}	Internal Pull-down Resistor	3.3 V I/O @ 3.3 V	—	60	—	kΩ
		5 V-tolerant I/O @ 3.3 V				

ADC Characteristics

Table 19. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.0	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V, 1 Msps	—	0.4	0.5	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.01	µA
f_{ADC}	A/D Converter Clock	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	Msps
t_{DL}	Data Latency	—	—	13	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin / pad capacitance included	—	4	—	pF
t_{SU}	Startup Time	—	—	—	1	µs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 ksps, V_{DDA} = 2.5 V ~ 3.6 V, ADCLVM = 0	—	±2	±5	LSB
		f_S = 750 ksps, V_{DDA} = 2.0 V ~ 3.5 V, ADCLVM = 1				
DNL	Differential Non-linearity Error	f_S = 750 ksps, V_{DDA} = 2.5 V ~ 3.6 V, ADCLVM = 0	—	±1	—	LSB
		f_S = 750 ksps, V_{DDA} = 2.0 V ~ 3.5 V, ADCLVM = 1				
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.

3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

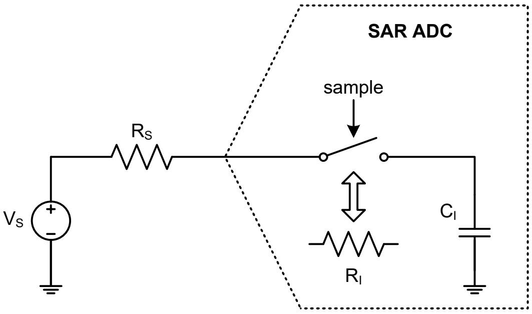


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

V_{DDA} Monitor Characteristics

Table 20. V_{DDA} Monitor Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R	V_{DDA} Resistor Bridge	—	—	50	—	kΩ
Q	V_{DDA} Measurement Ratio	—	—	2	—	—
E_R	Ratio Error	—	-1	—	+1	%
t_{SVDDA}	ADC Sampling Time when Reading the V_{DDA}	—	5	—	—	µs

Note: Data based on characterization results only, not tested in production.

Bandgap Voltage Characteristics

Table 21. Bandgap Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.0	3.3	3.6	V
V_{BG}	Bandgap Reference Voltage	V_{DDA} = 2.0 V ~ 3.6 V @ T_A = -40 °C ~ 105 °C	1.206	1.218	1.23	V
I_{BG}	Bandgap Voltage Current	V_{DDA} = 3 V @ T_A = -40 °C ~105 °C	—	57	90	µA
I_{BG_BUF}	Bandgap Buffer Current	V_{DDA} = 3 V @ T_A = -40 °C ~ 105 °C, VREFEN=1	—	75	120	µA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{BGST}	Bandgap Voltage Stable Time	V_{DDA} = 3.3 V @ T_A = -40 °C ~ 105 °C	—	5	20	μs
t_{SBG}	ADC Sampling Time when Reading Bandgap Voltage	—	5	—	—	μs
I_{BGPD}	Bandgap Voltage Power Down Current	—	—	—	0.01	μA

Note: Data based on characterization results only, not tested in production.

Internal Reference Voltage Characteristics

Table 22. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		2.3	—	3.6	V
V_{REF}	Internal Reference Voltage after Factory Trimming at 25 °C Temperature	V_{DDA} ≥ 2.3 V	VREFSEL[1:0] = 00	1.94	2.0	2.06	V
		V_{DDA} ≥ 2.8 V	VREFSEL[1:0] = 01	2.425	2.5	2.575	
		V_{DDA} ≥ 3.0 V	VREFSEL[1:0] = 10	2.619	2.7	2.781	
		V_{DDA} ≥ 3.3 V	VREFSEL[1:0] = 11	2.91	3.0	3.09	
C_L	Load Capacitor	—		0.1	2.2	4.7	μF
ACC_{VREF}	Reference Voltage Accuracy after Trimming	V_{DDA} = 2.3 V ~ 3.6 V, V_{REF} = 2.0 V, T_A = -40 °C ~ 105 °C		-1.5	—	1.5	%
t_{STABLE}	Reference Voltage Stable Time	V_{DDA} = 3.3 V, V_{BG} has been stabled, C_L = 2.2 μF, T_A = -40 °C ~ 105 °C, VREFOE = 1		—	—	350	μs
I_{DD}	Operating Current	V_{DDA} = 3.3 V, V_{REF} = 2.0 V, T_A = -40 °C ~ 105 °C, VREFOE = 1		—	20	30	μA
I_{DDPWD}	Reference Voltage Power Down Current	—		—	—	0.01	μA

Temperature Sensor Characteristics

Table 23. Temperature Sensor Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.0	3.3	3.6	V
T_L	Linearity with Temperature	T_A = -20 °C ~ 60 °C	—	—	±3	°C
		T_A = -40 °C ~ -20 °C & T_A = 60 °C ~ 105 °C	—	—	±5	
Avg_Slope	Temperature Sensitivity (Slope Voltage Versus Temperature)	—	—	-4.454	—	mV/°C
V_{25}(2)	Voltage at 25 °C	Voltage at 25 °C (±5 °C)	—	0.789	—	V
t_{STS}	ADC Sampling Time when Reading Temperature Sensor Voltage	—	10	—	—	μs
I_{TS}	Temperature Sensor Operating Current	V_{DDA} = 3.3 V @ T_A = -40 °C ~ 105 °C, TSEN=1	—	100	165	μA
I_{TSPD}	Temperature Sensor Power Down Current	—	—	—	0.01	μA

Note: 1. Data based on characterization results only, not tested in production.

2. Measure at V_{DDA} = 3.0 V and internal ADVREFP = 3.0 V. The V_{25} ADC conversion result is stored in the TSCAL.

SCTM / GPTM / MCTM Characteristics

Table 24. SCTM / GPTM / MCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for SCTM / GPTM / MCTM	—	—	—	48	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 25. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL And SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL And SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.

2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

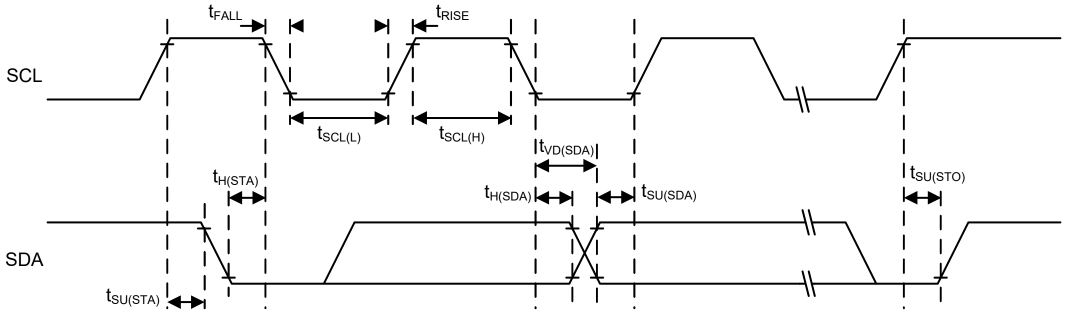


Figure 8. I²C Timing Diagrams

SPI Characteristics

Table 26. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High And Low Time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	-	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3 \times t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2 \times t_{PCLK}$	—	—	Ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3 \times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.

2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

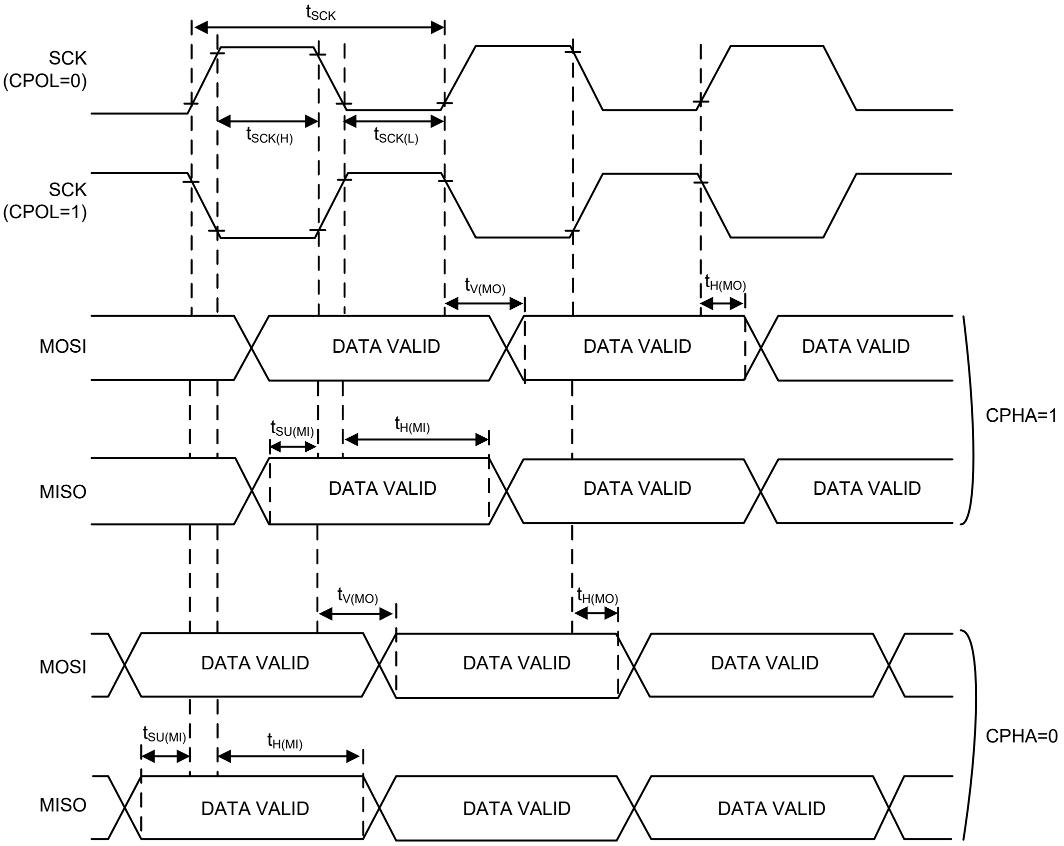


Figure 9. SPI Timing Diagrams – SPI Master Mode

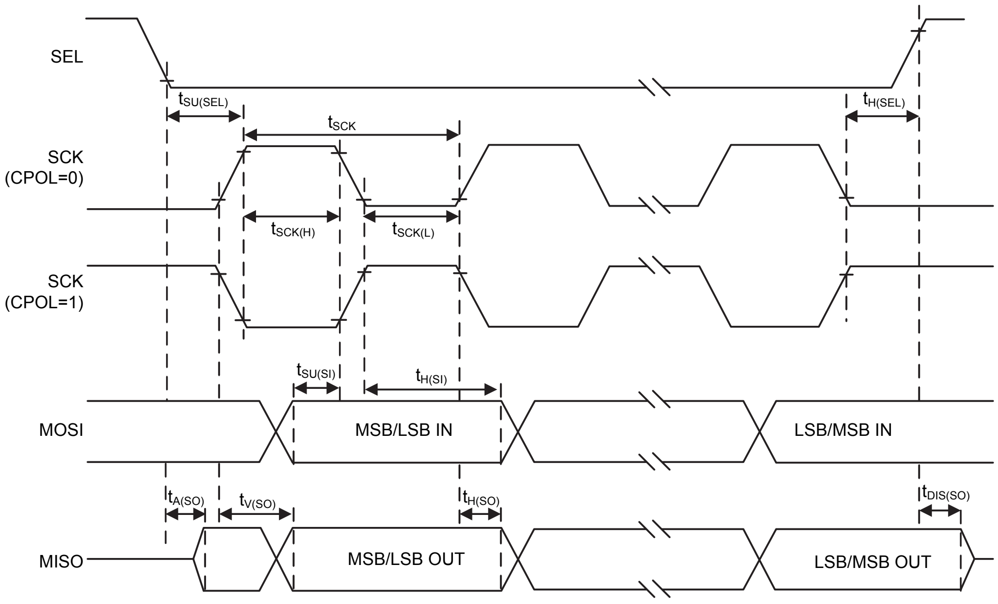


Figure 10. SPI Timing Diagrams – SPI Slave Mode with CPHA = 1

6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

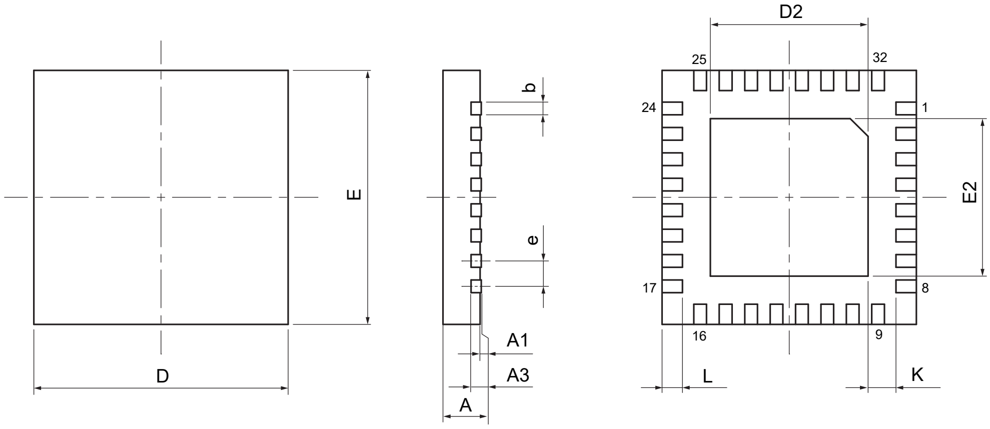
Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)

- The Operation Instruction of Packing Materials

- Carton information

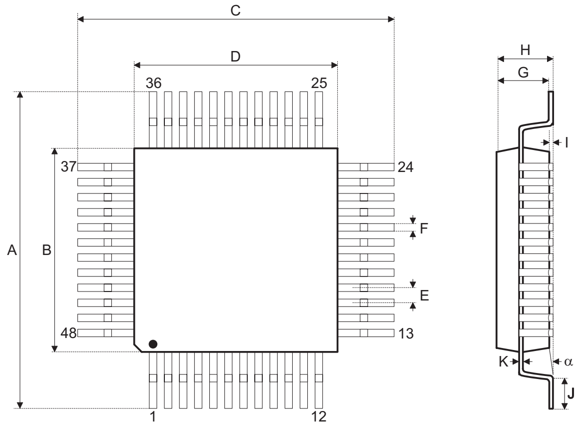
SAW Type 32-pin QFN (4mm×4mm×0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.006	0.008	0.010
D		0.157 BSC	
E		0.157 BSC	
e		0.016 BSC	
D2	0.100	—	0.108
E2	0.100	—	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.55	—	2.75
E2	2.55	—	2.75
L	0.35	0.40	0.45
K	0.20	—	—

48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.020 BSC	
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.50 BSC	
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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