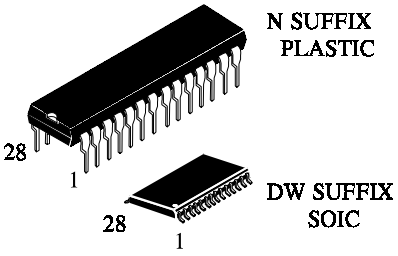
Voice Switched Speakerphone Circuit

The HT34118A Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high pass filter can be used to filter out 60 Hz noise in the reseive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The HT34118A may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The HT34118A can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and or other features of a featurephone.

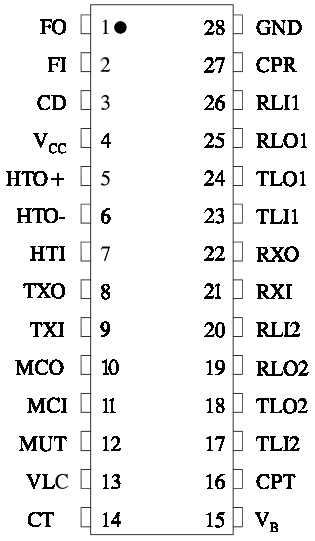
- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0-6.5 V)
- 4 Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors - Mute Function Included
- Chip Disable for Active Standby Operation
- On Board Filter Pinned-Out for User Deined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence



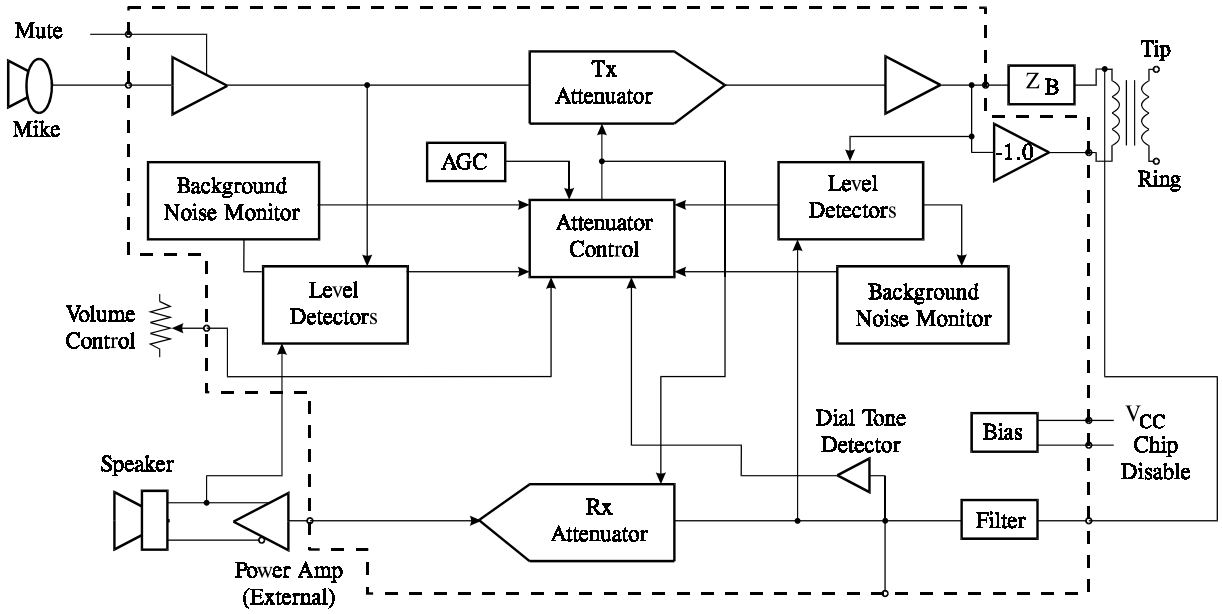
ORDERING INFORMATION

HT34118AN Plastic
HT34118ARW SOIC
T_A = -25° to 70° C for all packages

PIN ASSIGNMENT



SIMPLIFIED BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

INTRODUCTION

The fundamental difference between the operation of a speakerphone and a handset is that of half-duplex versus full-duplex. The handset is full duplex since conversation can occur in both directions (transmit and receive) simultaneousiy. A speakerphone has higher gain levels in both paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the system. The loop is formed by the receive and transmit paths, the hybrid, and the acoustic coupling (speaker to microphone). The only practical and economical solution used to data is to design the speakerphone to function in a half duplex mode - i.e., only one person speaks at a time, while the other listens. To achieve this requires a circuit which can detect who is talking, switch on the appropriate path (transmit or receive), and switch off (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately.By providing speech level detectors, the circuit operates in a “hand-free” mode, eliminating the need for a “push-to-talk” switch.

The handset, by the way, has the same loop as the speakerphone. But since the gains are considerably lower, and since the acoustic coupling from the earpiece to the mouthpiece is almost non-existent (the receiver is normally held against a person’s ear), oscillations don’t occur.

The HT34118A provides the necessary level detectors, attenuators, and switching control for a properly operating speakerphone. The detection sensitivity and timing are externally controllable. Additionally, the HT34118A provides background noise monitors which make the circuit insensitive to room and line noise, hybrid amplifiers for interfacing to Tip and Ring, the microphone amplifier, and other associated functions.

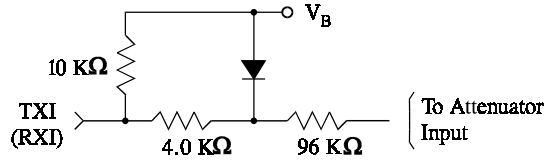
ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain (+6.0 dB), the other is at maximum attenuation (-46 dB), and vice versa. They are never both fully on or both fully off. The sum of their gains remains constant (within a nominal error band of ±0.1 dB) at a typical value of -40 dB. Their purpose is to control the transmit and receive paths to provide the half-duplex operation required in a speakerphone.

The attenuators are non-inverting, and have a -3.0 dB (from max gain) frequency of ≈100 KHz. The input impedance of each attenuator (TXI and RXI) is nominally 10 kΩ (see Figure 1), and the input signal should be limited to 350 mVrms (990 mVp-p) to prevent distortion. That maximum

recommended input signal is independent of the volume control setting. The diode clamp on the inputs limits the input swing, and therefore the maximum negative output swing. This is the reason for V_{RXOL} and V_{TXOL} specification being defined as they are in the Electrical Characteristics. The output impedance is $<10\ \Omega$ until the output current limit (typically 2.5 mA) is reached.

Figure 1. Attenuator Input Stage



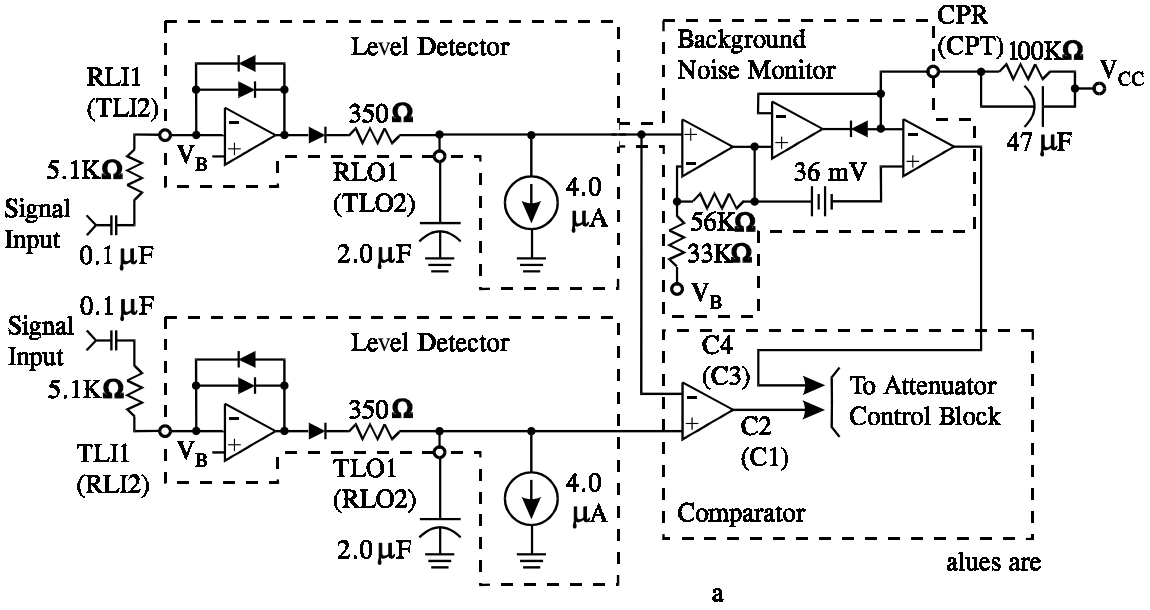
The attenuators are controlled by the single output of the Control Block, which is measurable at the C_T pin (Pin 14). When the C_T pin is at +240 millivolts with respect to V_B, the circuit is in the receive mode (receive attenuator is at +6.0 dB). When the C_T pin is at -240 millivolts with respect to V_B, the circuit is in the transmit mode (transmit attenuator is at +6.0 dB). The circuit is in an idle mode when the C_T voltage is equal to V_B, causing the attenuators' gains to be halfway between their fully on and fully off positions (-20 dB each). Monitoring the C_T voltage (with respect to V_B) is the most direct method of monitoring the circuit's mode.

The inputs to the Control Block are seven: 2 from the comparators operated by the level detectors, 2 from the background noise monitors, the volume control, the dial-tone detector, and the AGC circuit. These seven inputs are described below.

LEVEL DETECTORS

There are four level detectors - two on the receive side and two on the transmit side. Refer to Figure 2 - the terms in parentheses form one system, and the other terms form the second system

Figure 2. Level Detectors



Each level detector is a high gain amplifier with back-to-back diodes in the feedback path, resulting in non-linear gain, which permits operation over a wide dynamic range of speech levels. The sensitivity of each level detector is determined by the external resistor and capacitor at each input (TLI1, TLI2, RLI1, and RLI2). Each output charges an external capacitor through a diode and limiting resistor, thus providing a dc representation of the input ac signal level. The outputs have a guick rise time (determined by the capacitor and an internal 350 Ω resistor), and a slow decay time set by an internal current source and the capacitor. The capacitors on the four outputs should have the same value (±10%) to prevent timing problems.

Referring to Figure 8, on the receive side, one level detector (RLI1) is at the receive input receiving the same signal as at Tip and Ring, and

the other (RLI2) is at the output of the speaker amplifier. On the transmit side, one level detector (TLI2) is at the output of the microphone amplifier, while the other (TLI1) is at the hybrid output. Outputs RLO1 and TLO1 feed a comparator, the output of which goes to the Attenuator Control Block. Likewise, outputs RLO2 and TLO2 feed a second comparator which also goes to the Attenuator Control Block. The truth table for the effects of the level detectors on the Control Block is given in the section describing the Control Block.

BACKGROUND NOISE MONITORS

The purpose of the background noise monitors is to distinguish speech (which consists of bursts) from background noise (a relatively constant signal level). There are two background noise monitors - one for the receive path and one for the transmit path. Refering to Figure 2, the receive background noise monitor is operated on by the RLI1-RLO1 level detector, while the transmit background noise monitor is operated on by the TLI2-TLO2 level detector. They monitor the background noise by storing a dc voltage representative of the respective noise levels in capacitors at CPR and CPT. The voltages at these pins have slow rise times (determined by the external RC), but fast decay times. If the signal at RLI1 (or TLI2) changes slowly, the voltage at CPR (or CPT) will remain more positive than the voltage at the non-inverting input of the monitor's output comparator. When speech is present, the voltage on the noninverting input of the comparator will rise quicker than the voltage at the inverting input (due to the burst characteristic of speech), causing its output to change. This output is sensed by the Attenuator Control Block.

The 36 mV offset at the comparator's input keeps the comparator from changing state unless the speech level exceeds the background noise by ≈4.0 dB. The time constant of the external RC (≈4.7 seconds) determines the response time to background noise variations

VOLUME CONTROL

The volume control input at VLC (Pin 13) is sensed as a voltage with respect to V_B. The volume control affects the attenuators only in the receive mode. It has no effect in the idle or transmit modes.

When in the receive mode, the gain of the receive attenuator will be +6.0 dB, and the gain of the transmit attenuator will be -46 dB only when VLC is equal to V_B. As VLC is reduced below V_B, the gain of the receive attenuator is reduced, and the gain of the transmit attenuator is increased such that their sum remains constant. Changing the voltage at VLC changes the voltage at C_T (see the Attenuator Control Block section), which in turn controls the attenuators.

The volume control setting does not affect the maximum attenuator input signal at which notice able distortion occurs.

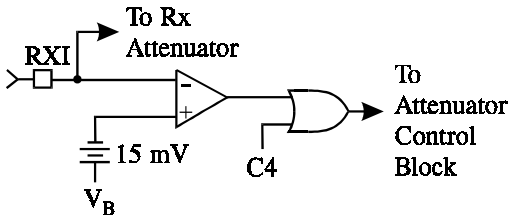
The bias current at VLC is typically 60 nA out of the pin, and does not vary significantly with the VLC voltage or with V_{CC}.

DIAL TONE DETECTOR

The dial tone detector is a comparator with one side connected to the receive input (RXI) and the other input connected to V_B with a 15 mV offset (see Figure 3). If the circuit is in the receive mode, and the incoming signal is greater than 15 mV (10 mVrms), the comparator's output will change, disabling the receive idle mode. Tthe receive attenuator will then be at a setting determined solely by the volume control.

The purpose of this circuit is to prevent the dial tone (which would be considered as continuous noise) from fading away as the circuit would have the tendency to swich to the idle mode. By disabling the receive idle mode, the dial tone remains at the normally expected full level.

Figure 3. Dial Tone Detector



AGS

The AGS circuit affects the circuit only in the receive mode, and only when the supply voltage (V_{CC}) is less than 3.5 volts. As V_{CC} falls below 3.5 volts, the gain of the receive attenuator is reduced. The transmit path attenuation changes such that the sum of the transmit and receive gains remains constant.

The purpose of this feature is to reduce the power (and current) used by the speaker when a line-powered speakerphone is connected to a long line, where the available power is limited. By reducing the speaker power, the voltage sag at V_{CC} is controlled, preventing possible erratic operation.

ATTENUATOR CONTROL BLOCK

The Attenuator Control Block has the seven inputs described above:

- Tthe output of the comparator operated by RLO2 and TLO2 (microphone/speaker side) - designated C1.
- The output of the comparator operated by RLO1 and TLO1 (Tip/Ring) side) - designated C2.
- The output of the transmit background noise monitor - designated C3.
- The output of the receive background noise monitor - designated C4.
- The volume control.
- The dial tone detector.
- The AGC circuit.

The single output of the Control Block controls the two attenuators. The effect of C1-C4 is as follows:

Inputs				Output
C1	C2	C3	C4	Mode
Tx	Tx	1	X	Transmit
Tx	Rx	Y	Y	Fast Idle
Rx	Tx	Y	Y	Fast Idle
Rx	Rx	X	1	Receive
Tx	Tx	0	X	Slow Idle
Tx	Rx	0	0	Slow Idle
Rx	Tx	0	0	Slow Idle
Rx	Rx	X	0	Slow Idle

X = Don't Care; Y = C3 and C4 are not both 0

A definition of the above terms:

1) "Transmit" means the transmit attenuator is fully on (+6.0 dB), and the receive attenuator is at max. attenuation (-46 dB).
2) "Receive" means both attenuators are controlled by the volume control. At max. volume, the receive attenuator is fully on (6.0 dB), and the transmit attenuator is at max. attenuation (-46 dB).
3) "Fast Idle" means both transmit and receive speech are present in approximately equal levels. The attenuators are quickly switched (30 ms) to idle until one speech level dominates the other.
4) "Slow Idle" means speech has ceassed in both transmit and receive path. The attenuators are then slowly switched (1 second) to the idle mode.
5) Switching to the full transmit or receive modes from any other mode is at the fast rate (30 ms).

A summary of the truth table is as follows:

1) The circuit will switch to transmit if: a) both transmit level detectors sense higher signal levels relative to the respective receive level detectors (TLI1 versus RLI1, TLI2 versus RLI2), and b) the transmit background noise monitor indicates the presence of speech.

2) The circuit will switch to receive if: a) both receive level detectors sense higher signal levels relative to the respective transmit level detectors, and b) the receive background noise monitor indicates the presence of speech.

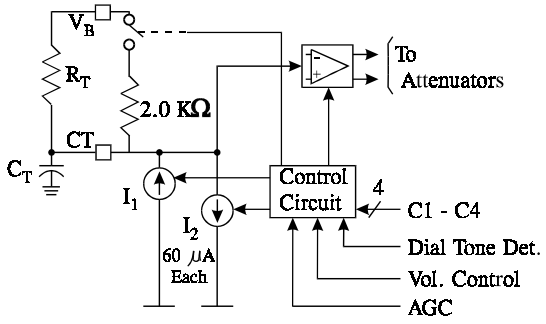
3) The circuit will switch to the fast idle mode if the level detectors disagree on the relative strengths of the signal levels, and at least one of the background noise monitors indicates speech. For example, refferring to the Expanded Logic Diagram (Figure 8), if there is sufficient signal at the microphone amp output (TLI2) to override the speaker signal (RLI2), and there is sufficient signal at the receive input (RLI1) to override the signal at the hybrid output (TLI1), and either or both background monitors indicate speech, then the circuit will be in the fast idle mode. Two conditions which can cause the fast idle mode to occur are a) when both talkers are attempting to gain control of the system by talking at the same time, and b) when one talker is in a very noisy environment, forcing the other talker to continually override that noise level. In general, the fast idle mode will occur infrequently.

4) The circuit will switch to the slow idle mode when a) both talkers are quiet (no speech present), or b) when one talker's speech level is continuously overriden by noise at the other speaker's location.

The time required to switch the circuit between transmit, receive, fast idle and slow idle is determined in part by the components at the C_T pin (Pin 14). A schematic of the C_T circuitry is shown in Figure 4 and operates as follows:

- R_T is typically 120 kΩ, and C_T typically 5.0 μF.
- To switch to the receive mode, I_1 is turned on (I_2 is off), charging the external capacitor to +240 mV above V_B. (An internal clamp prevents further charging of the capacitor.)
- To switch to the transmit mode, I_2 is turned on (I_1 is off) bringing down the voltage on the capacitor to -240 mV with respect to V_B.
- To switch to idle quickly (fast idle), the current sources are turned off, and the internal 2.0 kΩ resistor is switched in, discharging the capacitor to V_B with a time constant = 2.0 KΩ x C_T.
- To switch to idle slowly (slow idle), the current sources are turned off, the switch at the 2.0 kΩ resistor is open, and the capacitor discharges to V_B through the external resistor R_T with a time constant = R_T x C_T.

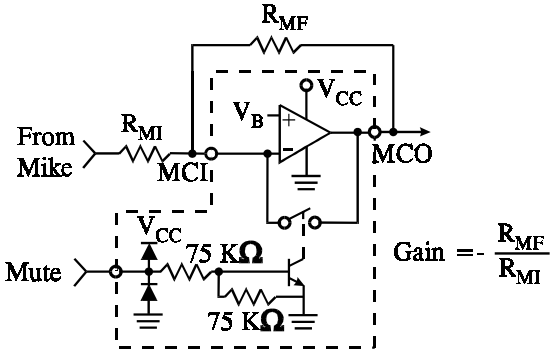
Figure 4. CT Attenuator Control Block Circuit



MICROPHONE AMPLIFIER

The microphone amplifier (Pin 10, 11) has the noninverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op-amps, the amplifier has an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 80 dB ($f < 100$ Hz), and the gain-bandwidth is typically 1.0 MHz. The maximum p-p output swing is typically 1.0 volt less than V_{CC} with an output impedance of $< 10\ \Omega$ until curent limiting is reached (typically 1.5 mA). Input bias current at MCI is typically 40 nA out of the pin.

Figure 5. Microphone Amplifier and MUTE



The muting function (Pin 12), when activated, will reduce the gain of the amplifier to = -39 dB (will RMI = 5.1 KΩ) by shorting the output to the inverting input (see Figure 5). The mute input has a threshold of 1.5 volt, and the voltage at this pin must be kept withing the range of ground and V_{CC}. If the mute function is not used, the pin should be grounded.

HYBRID AMPLIFIERS

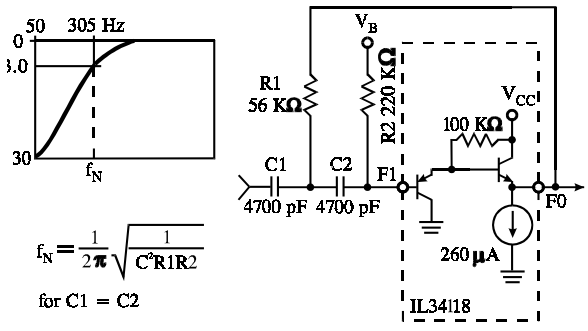
The two hybrid amplifiers (at HTO+, HTO-, and HTI), in conjunction with an external transformer, provide the two-to-four wire converter for interfacing to the telephone line. The gain of the first amplifier (HTI to HTO-) is set by external resistors (gain = $-R_{HF}/R_{HI}$ in Figure 8), and its output drives the second amplifier, the gain of which is internally set at -1.0. Unlike most op-amps, the amplifiers have an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain of the first amplifier is typically 80 dB, and the gain bandwidth of each amplifier is ≈1.0 MHz. The maximum p-p output swing of each amplifier is typically 1.2 volts less than V_{CC} with an output impedance of $< 10\ \Omega$ until current limiting is reached (typically 8.0 mA). The output current capability is guaranteed to be a minimum of 5.0 mA. The bias current at HTI is typically 30 nA out of the pin.

The connections to the coupling transformer are shown in the Expanded Logic Diagram (Figure 8). The block labeled Zbal is the balancing network necessary to match the line impedance.

FILTER

The operation of the filter circuit is determined by the external components. The circuit within the HT34118A, from pins FI to FO is a buffer with a high input impedance (> 1.0 MΩ), and a low output impedance ($< 50\ \Omega$). The configuration of the external components determines whether the circuit is a high-pass filter (as shown in Figure 8), a low-pass filter, or a band-pass filter.

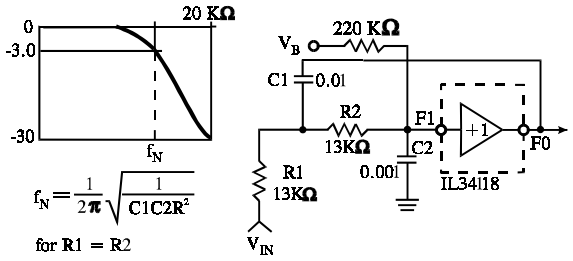
Figure 6. High Pass Filter



As a high pass filter, with the components shown in Figure 6 the filter will keep out 60 Hz (and 120 Hz) hum which can be picked up by the external telephone lines.

As a low pass filter (Figure 7), it can be used to roll off the high and frequencies in the receive circuit, which aids protecting against acoustic feedback problems. With an appropriate choice of an input coupling capacitor to the low pass filter, a band pass filter is formed.

Figure 7. Low Pass Filter



POWER SUPPLY, V_B, AND CHIP DISABLE

The power supply voltage at V_{CC} (Pin 4) is to be between 3.5 and 6.5 volts for normal operation, with reduced operation possible down to 2.8 volts.

The output voltage at V_B (Pin 15) is ≈(V_{CC} - 0.7)/2, and provides the ac ground for the system. The output impedance at V_B is ≈400 Ω, and in conjunction with the external capacitor at V_B, forms a low pass filter for power supply rejection.

Since V_B biases the microphone and hybrid amplifiers, the amount of supply rejection at their outputs is directly related to the rejection at V_B, as well as their respective gains.

The Chip Disable (Pin 3) permits powering down the IC to conserve power and/or for muting purposes. With CD≤0.8 volts, normal operation is in effect. With CD≥2.0 volts and ≤V_{CC}, the IC is powered down. In the powered down mode, the microphone and the hybrid amplifiers are disabled, and their outputs go to a high impedance state. Additionally, the bias is removed from the filter (Pins 1, 2), the attenuators (Pins 8, 9, 21, 22), or from Pins 13, 14, and 15 (the attenuators are disabled, however, and will not pass a signal). The input impedance at CD is typically 90 kΩ, has a threshold of ≈1.5 volts, and the voltage at this pin must be kept within the range of ground and V_{CC}. If CD is not used, the pin should be grounded.

PIN DESCRIPTION

Pin No	Designation	Description
1	FO	Filter output. Output impedance is less than 50Ω.
2	FI	Filter input. Input impedance is greater than 1.0 MΩ.
3	CD	Chip Disable. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) disables the IC to conserve power. Input impedance is nominally 90 KΩ.
4	V_{CC}	A supply voltage of +2.8 to +6.5 Volts is required, at ≈5.0 mA. As V_{CC} falls from 3.5 to 2.8 Volts, an AGC circuit reduces the receive attenuator gain by ≈25 dB (when in the receive mode).
5	HTO+	Output of the second hybrid amplifier. The gain is internally set at -1.0 to provide a differential output, in conjunction with HTO-, to the hybrid transformer.
6	HTO-	Output of the first hybrid amplifier. The gain of the amp is set by external resistors.
7	HTI	Input and summing node for the first hybrid amplifier. DC level is ≈V_B.
8	TXO	Output of the transmit attenuator. DC level is approximately V_B.
9	TXI	Input to the transmit attenuator. Max. signal level is 350 mVrms. Input impedance is ≈10 KΩ.
10	MCO	Output of the microphone amplifier. The gain of the amplifier is set by external resistors.
11	MCI	Input and summing node of the microphone amplifier. DC level is ≈V_B.

(continued)

PIN DESCRIPTION

Pin No	Designation	Description
12	MUT	Mute input. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) mutes the microphone amplifier without affecting the rest of the circuit. Input impedance is nominally 90Ω.
13	VLC	Volume control input. When VLC = V_B, the receive attenuator is at maximum gain when in the receive mode. When VLC = 0.3 V_B, the receive gain is down 35 dB. Does not affect the transmit mode.
14	C_T	An RC this pin sets the response time for the circuit to switch modes.
15	V_B	An output voltage ≈V_{CC}/2. This voltage is a system ac ground, and biases the volume control. A filter cap is required.
16	CPT	An RC at this pin sets the time constant for the transmit background monitor.
17	TLI2	Input to the transmit level detector on the mike speaker side.
18	TLO2	Output of the transmit level detector on the mike/speaker side, and input to the transmit background monitor.
19	RLO2	Output of the receive level detector on the mike/speaker side.
20	RLI2	Input to the receive level detector on the mike/speaker side.
21	RXI	Input to the receive attenuator and dial tone detector. Max input level is 350 mV RMS. Input impedance is ≈10 KΩ.
22	RXO	Output of the receive attenuator. DC level is approximately V_B.
23	TLI1	Input to the transmit level detector on the line side.
24	TLO1	Output of the transmit level detector on the line side.
25	RLO1	Output of the receive level detector on the line side, and input to the receive background monitor.
26	RLI1	Input the receive level detector on the line side.
27	CPR	An RC at this pin sets the time constant for the receive background monitor.
28	GND	Ground pin for the entire IC.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 14)	-1.0 to +7.0	V
V_{IN}	Input Voltage at CD(Pin 3), MUT (Pin 12)	-1.0 toV_{CC} +1.0 V	V
V_{IN}	Input Voltage at VLC (Pin 13)	-1.0 toV_{CC} +0.5 V	V
V_{IN}	Input Voltage at TXI(Pin 9), RXI (Pin 21), FI (Pin 2)	-0.5 toV_{CC} +0.5 V	V
Tstg	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage (Pin 4)	3.5	6.5	V
V_{IN}	Input Voltage at CD (Pin 3), MUT (Pin12)	0	V_{CC}	V
I_{VB}	V_B Current (Pin 15)		500	μA
V_{IN}	Input Voltage at VLC (Pin 13)	0.3 x V_B	V_B	V
V_{IN}	Attenuator Input Signal Voltage (Pins 9, 21)	0	350	mVrms
G	Microphone Amplifier, Hybrid Amplifier Gain	0	40	dB
I_L	Load Current RXO, TXO Pins 8,22) MCO (Pin 10) HTO-, HTO+ (Pins 6,5)	0 0 0	2.0 1.0 5.0	mA
T_A	Operating Temperature	-25	+70	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS(T_A = -25 to +70°C, V_{CC} = 5.0 V , CD = 0.8 V, unless noted)

Symbol	Parameter	Test Conditions	Guaranteed Limits		Unit
			Min	Max	
POWER SUPPLY					
I_{CC}	V_{CC} Sypply Current	V_{CC} =6.5 V, CD =0.8 V V_{CC} =6.5 V, CD =2.0 V	- -	10 1.0	mA
R_{CD}	CD Input Resistance	V_{CC} = V_{CD} = 6.5 V	37.5	-	KkΩ
V_{CDH}	CD Input High Voltage	V_{CC} = V_{CD} = 6.5 V	2.0	V_{CC}	V
V_{CDL}	CD Input Low Voltage	V_{CC} = V_{CD} = 6.5 V	0	0.8	V
V_B	V_B Output Voltage		13.5	3.0	V
ATTENUATOR (VLC = V_B, unless noted)					
G_{RX}	Receive Attenuator Gain (f =1.0 KHz)	Rx Mode, RXI=150 mVrms, (V_{CC}=5.0 V)	1.5	10.0	dB
G_{RX}		Rx Mode, RXI=150 mVrms (V_{CC}=3.5 V)	1.5	10.0	
ΔG_{RX1}*		Gain Change -V_{CC}=3.5 V versus V_{CC} =5.0 V	-0.5	+0.5	
ΔG_{RX2}*		AGC Gain Change - V_{CC}=2.8 V versus V_{CC}=5.0 V	-	-15	
G_{RX1} ΔG_{RX3}*		Idle Mode, RXI=150mVrms Range (Rx to Tx Mode)	-25 49	-15 54	
V_{CR}*	Volume Control Range	Rx Mode, 0.3V_B<V_{LC}<V_B	27	-	dB

(continued)

ELECTRICAL CHARACTERISTICS(T_A = -25 to +70°C, V_{CC} = 5.0 V , CD = 0.8 V, unless noted)

Symbol	Parameter	Test Conditions	Guaranteed Limits		Unit
			Min	Max	
ΔV_{RXO}	ΔRXO DC Voltage	Rx to Tx Mode	-	±190	mV
V_{RXOH}	RXO High Voltage	I_{OUT}= -1.0 mA,RXI=V_B+1.5V, V_{CT}=2.6 V	2.8	-	V
V_{RXOL}	RXO Low Voltage	I_{OUT}= +1.0 mA,RXI=V_B-1.0V, V_{CT}=2.6 V Output measured with respect to V_B	-	V_B-0.75	V
R_{RXI}	RXI Input Resistance	RXI=350 mVrms, f = 1.0 KHz	5.25	17.5	kΩ
G_{TX} G_{TXI} ΔG_{TXI}*	Trasmit Attenuator Gain (f =1.0 KHz)	Tx Mode, TXI=150 mVrms Idle Mode, RXI=-150 mVrms Range (Tx to Rx Mode)	1.5 -25 49	10.0 -15 54	dB
ΔV_{TXO}	ΔTXO DC Voltage	Tx to Rx Mode	-	±190	mV
V_{TXOH}	TXO High Voltage	I_{OUT}= -1.0 mA,TXI=V_B+1.5V, V_{CT}=1.6 V	2.8	-	V
V_{TXOL}	TXO Low Voltage	I_{OUT}= +1.0 mA,TXI=V_B-1.0V, V_{CT}=1.6 V Output measured with respect to V_B	-	V_B-0.75	V
R_{TXI}	TXI Input Resistance	TXI=350 mVrms, f = 1.0 KHz	5.25	17.5	KΩ
ATTENUATOR CONTROL					
I_{CTR}	C_T Source Current (switching to Rx mode)	f = 1 KHz, V_{LC} = V_B =CT	-106	-30	μA
I_{CTT}	C_T Sink Current (switching to Tx mode)	f = 1 KHz, V_{LC} = V_B =CT	+30	+106	μA
R_{FI}*	C_T Fast Idle Internal Resistance		1.5	3.6	KΩ
V_{DT}*	Dial Tone Detector Threshold		10	20	mV
MICROPHONE AMLIFIER (V_{MUT} ≤ 0.8 V, A+ = 31 dB, unless otherwise noted)					
MCO_{VOS}	Output Offset	V_{MCO} - V_B, Freedback R= 180 KΩ	-62	+62	mV
A_{VOLM}	Open Loop Gain	f = 100 Hz	60	-	dB
V_{MCOH}	Output High Voltage	I_{OUT}=-1.0 mA,V_{MCI}=V_B+1.5 V	2.8	-	V
V_{MCOL}	Output LowVoltage	I_{OUT}=1.0 mA, V_{MCI}=V_B - 1.0 V	-	250	mV
GMT	Muting (ΔGain)	f = 1.0 Khz,V_{MCI} = 150 mV 0.8 V ≤ V_{MUT} ≤ 2.0 V	52	-	dB
R_{MUT}	MUT Input Resistance	V_{CC} = V_{MUT} = 6.5 V	37.5	-	KΩ
V_{MUTH}	MUT Input-High		2.0	V_{CC}	V
V_{MUTL}	MUT Input-Low		0	0.8	V

(continued)

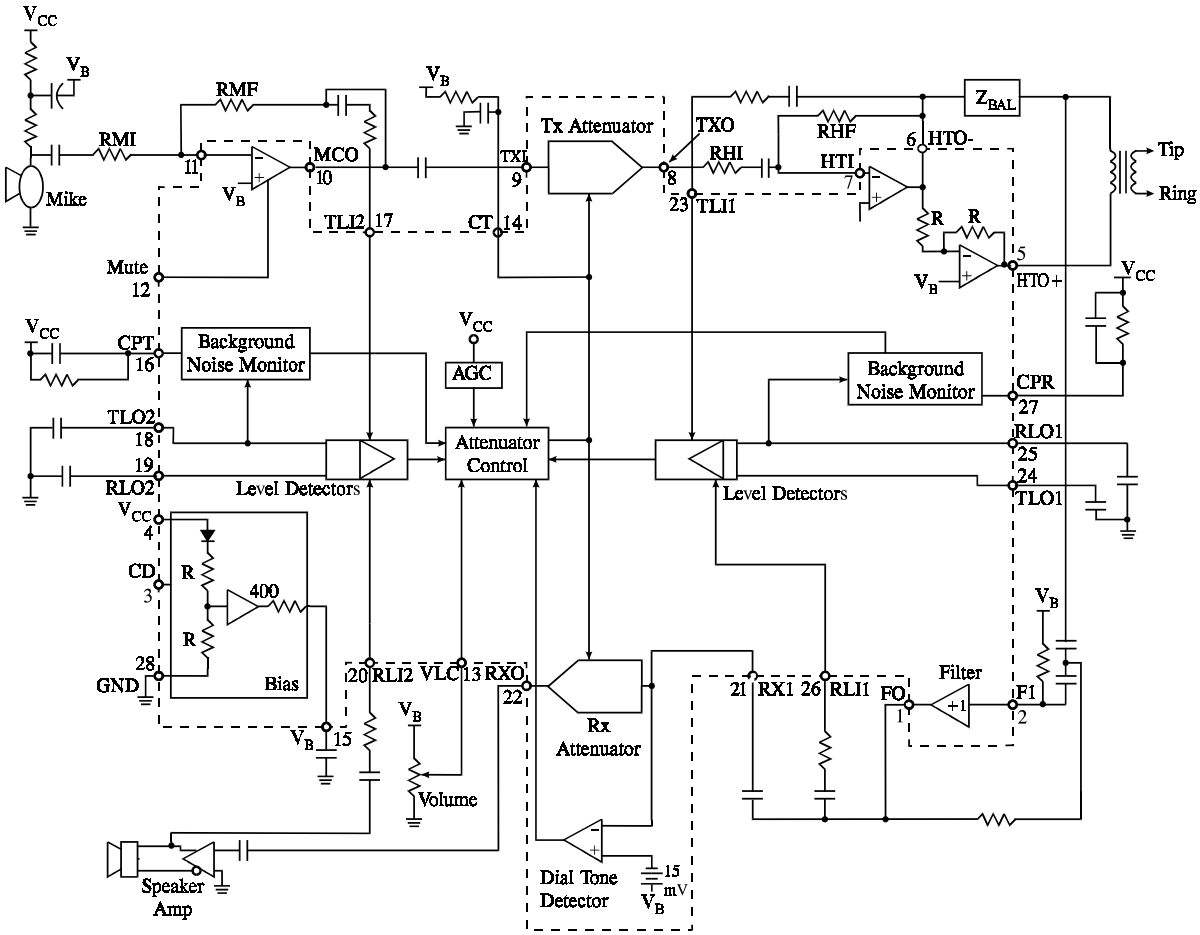
ELECTRICAL CHARACTERISTICS(T_A = -25 to +70°C, V_{CC} = 5.0 V , CD = 0.8 V, unless noted)

Symbol	Parameter	Test Conditions	Guaranteed Limits		Unit
			Min	Max	
HYBRID AMPLIFIERS					
H_{VOS}	HTO - Offset	V_{HTO-} - V_B, Freedback R= 51 KΩ	V_B - 25	V_B +25	mV
HB_{VOS}	HTO - to HTO+ Offset	Freedback R= 51 KΩ	V_B - 37	V_B +37	mV
A_{VOLH}	Open Loop Gain	HTI to HTO-, f = 100 Hz, V_{HTI} = 20 mV	57	-	dB
A_{VCLH}	Closed Loop Gain	HTO- to HTO+	-2.8	2.2	dB
V_{HT-H}	HTO- High Voltage	I_{OUT}=-5.0 mA, V_{HTI}=V_B -1.0 V	2.8	-	V
V_{HT-L}	HTO- Low Voltage	I_{OUT}=5.0 mA, V_{HTI}=V_B +1.5 V	-	375	mV
V_{HT+H}	HTO+ High Voltage	I_{OUT}=-5.0 mA,V_{HTI}=V_B +1.5 V	2.8	-	V
V_{HT+L}	HTO+ Low Voltage	I_{OUT}=5.0 mA, V_{HTI}=V_B -1.0 V	-	562	mV
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS					
I_{TH}*	Transmit-Recieve Switching Threshold	Ratio of Current at RLI1 + RLI2 to 20 μA at TLI1 + TLI2 to switch from Tx to Rx	0.8	1.2	
FILTER					
FO_{VOS}	Voltage Offset at FO	V_{FO} -V_B, 220 KΩ from V_B to FI	V_B-250	V_B +25	mV
I_{FO}	FO Sink Current	V_B = V_{FO}, V_{FI} = 0 V	112	500	μA

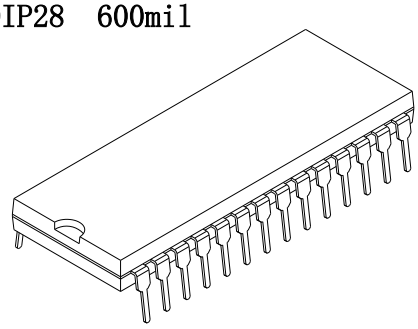
Note. 1. All currents into a device pin are positive, those out of a pin are negative. Algebraic convention rather than magnitude is used to define limits.

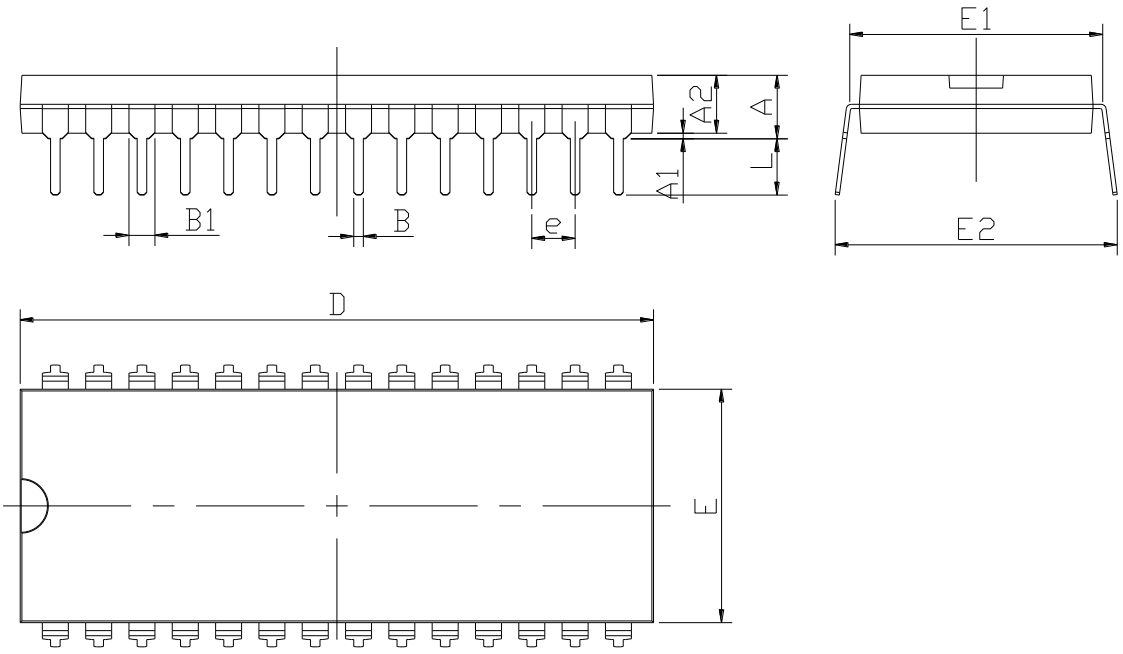
* @25°C

EXPANDED LOGIC DIAGRAM



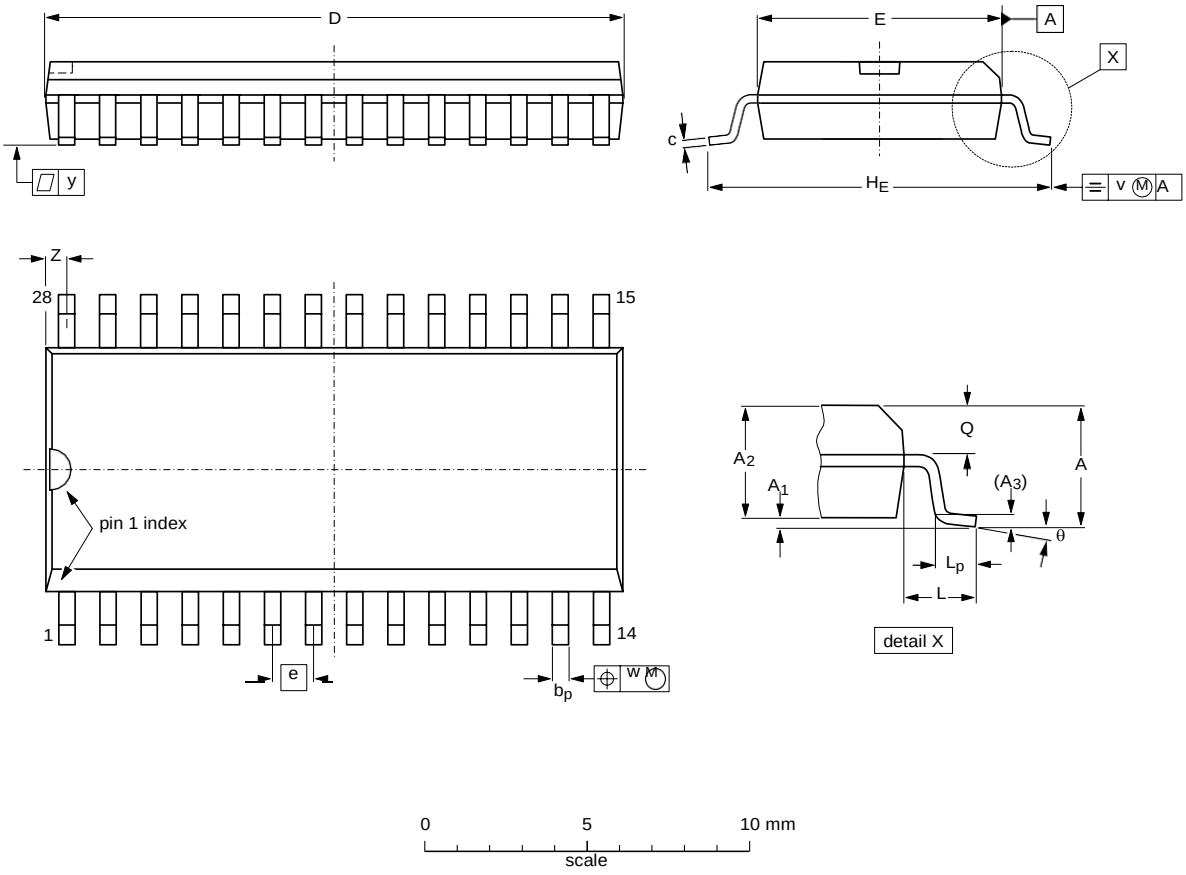
DIP28 600mil





Symbol	Dimensions in Milimeters		Demensions in Inches	
	Min	Max	Min	Max
A	4.160	4.760	0.164	0.187
A1	0.510		0.020	
A2	3.300	3.700	0.130	0.146
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	36.940	37.340	1.454	1.470
E	13.500	13.900	0.531	0.547
E1	14.990	15.490	0.590	0.610
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	16.200	16.800	0.638	0.661

SOP28 7.5 mm



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT136-1	075E06	MS-013				~~99-12-27~~ 03-02-19