# HT45B1S
# IGBT Driver with LDO and Voltage Detector

## Features

- Integrated Low Dropout Voltage Regulator – LDO
  - Output driving capability: 150mA (max)
  - Low quiescent current: 7μA (typ)
  - Low drop voltage
- Integrated Level Shifter
- Voltage detect protection for level shift output enable control
  - Detect $V_{DD}$
  - Detect $V_{CC2}$
- Package: 8-SOP

## Applications

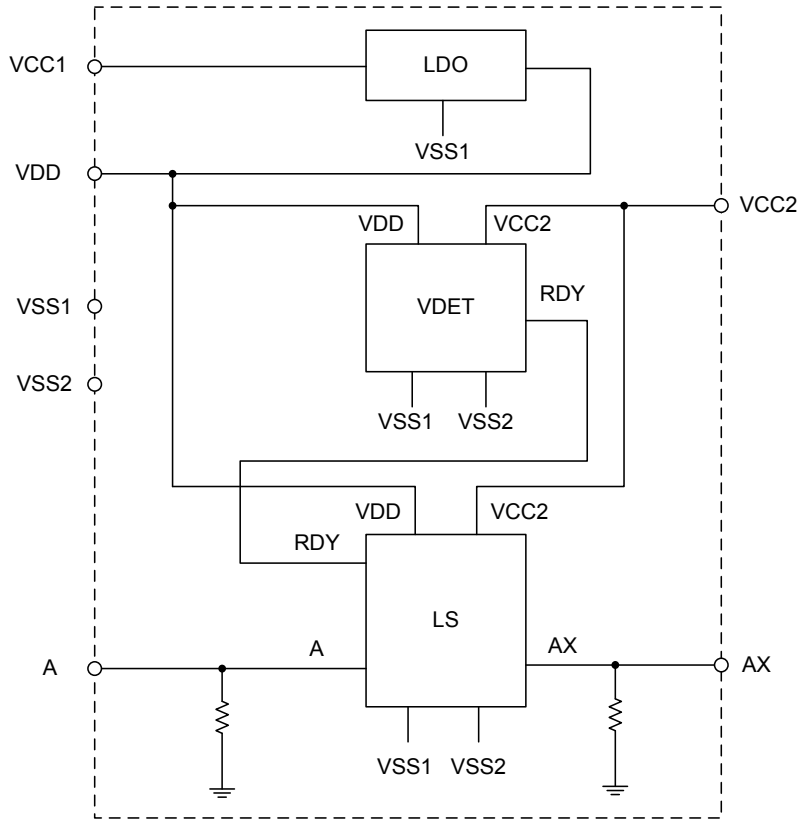
- Battery powered systems
- Communication equipments
- Audio/video equipment
- Home appliances

## General Description

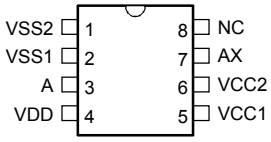
This IGBT driver device is specifically designed for applications which require low level logic levels such as those from microcontrollers to interface to power insulated gate bipolar transistors. As the device includes an internal LDO, a level shifter and voltage detector circuits, it integrates into a single package the external components usually required by these applications. This functional integration enables the device to offer the advantages of reduced circuitry and consequently reduced costs in these applications.

The device contains all the level shifting circuitry required match the high voltage and high current requirements of IGBT devices. To prevent malfunctions and possible system damage, an internal voltage detector monitors the system voltage level to determine if the level shifter can be enabled or not.

## Block Diagram



## Pin Assignment




**HT45B1S**
**8 SOP-A**

## Pin Description

| Pin Name | Type | Description |
|---|---|---|
| A | I | Level shift input<br>There is a 20kΩ pull-low resistor internally connected to this pin. |
| AX | O | Level shift output<br>There is a 22kΩ pull-low resistor internally connected to this pin. |
| VCC1 | PWR | LDO positive power supply pin |
| VCC2 | PWR | Level shifter positive power supply pin |
| VDD | PWR | LDO voltage output |
| VSS1 | PWR | LDO negative power supply pin, ground. |
| VSS2 | PWR | Level shift and voltage detector negative power supply pin – ground. |
| NC | — | Not connected, can not be used. |

## Absolute Maximum Ratings

Supply Voltage .....-0.3V to 30.0V

Storage Temperature .....-50°C to 125°C

Operating Temperature .....-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to these devices. Functional operation of these devices at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect devices reliability.

# Electrical Characteristics

## LDO Characteristics

Output Voltage V5=5V, -40°C≤Ta≤85°C, $V_{IN}$=$V_{OUT}$+1.0V, Ta=25°C, unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage (VCC1) | — | 6 | — | 24 | V |
| $V_{OUT}$ | Output Voltage | $I_O$ =1mA, Ta=25°C | -2% | 5 | 2% | V |
| | | $I_O$ =1mA, -40°C≤Ta<85°C | -5% | 5 | 5% | V |
| $\Delta V_{LOAD}$ | Load Regulation (Note1) | $V_{IN}$=7V, 1mA≤$I_O$≤150mA, Ta=25°C | — | 0.02 | 0.04 | %/mA |
| | | $V_{IN}$=6V, 1mA≤$I_O$≤70mA, Ta=25°C | — | 0.03 | 0.06 | %/mA |
| $V_{DROP}$ | Drop Out Voltage (Note2) | $I_O$ =1mA, $\Delta V_O$=2% | — | — | 100 | mV |
| $I_{QS}$ | Quiescent Current | $V_{IN}$=12V, $I_O$=0mA, no load | — | 7 | 14 | μA |
| $\Delta V_{LINE}$ | Line Regulation | 6V≤$V_{IN}$≤24V, $I_O$ =1mA | — | — | 0.2 | %/V |
| $\frac{\Delta V_{OUT}}{\Delta Ta}$ | Temperature Coefficient | $I_O$ =10mA<br>0°C<Ta<70°C | — | ±1.5 | ±2 | mV/°C |

Note: 1. Load regulation is measured at a constant junction temperature, using pulse testing with a low ON time and is guaranteed up to the maximum power dissipation. Power dissipation is determined by the input/output differential voltage and the output current. Guaranteed maximum power dissipation will not be available over the full input/output range. The maximum allowable power dissipation at any ambient temperature is $P_D=(T_{J(MAX)}-T_a)/\theta_{JA}$

2. Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at $V_{IN}$=$V_{OUT}$+1V.

## Level Shift/Voltage Detector Electrical Characteristics

$V_{DD}$=5V, $V_{CC2}$=12V, Ta=25°C, unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC2}$ | Level Shift Power Supply | — | 6 | — | 24 | V |
| $I_{OPR1}$ | VCC1 Operating Current (Note1) | $V_{DD}$=5V, $V_{CC2}$=12V, A=0, no load | — | 7 | 14 | μA |
| $I_{OPR2}$ | VCC2 Operating Current (Note1) | $V_{CC2}$=12V, A=0, no load | — | 10 | 20 | μA |
| **Level Shift** | | | | | | |
| $V_{IH}$ | Input High Voltage | — | 0.6$V_{DD}$ | — | $V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage | — | 0 | — | 0.3$V_{DD}$ | V |
| $I_{SOURCE}$ | Output Source Current for AX pin | $V_{OH}$=10.4V, Ta= -40°C~85°C | -105 | -150 | — | mA |
| $I_{SINK}$ | Output Sink Current for AX pin | $V_{OH}$=1.6V, Ta= -40°C~85°C | 105 | 150 | — | mA |
| $R_{PD1}$ | Level Shift Output pull-low resistor | — | -30% | 22 | +30% | kΩ |
| $R_{PD2}$ | Level Shift Input pull-low resistor | — | -30% | 20 | +30% | kΩ |
| **Voltage Detector** | | | | | | |
| $V_{DET1}$ | $V_{DD}$ Detect Level | Ta= -40°C~85°C | -10% | 3.0 | +10% | V |
| | Hysteresis | Ta= -40°C~85°C | — | 250 | — | mV |
| $V_{DET2}$ | $V_{CC2}$ Detect Level | Ta= -40°C~85°C | -10% | 9 | +10% | V |
| | Hysteresis | Ta= -40°C~85°C | — | 750 | — | mV |

Note: Operating or Standby current includes the power consumption of level shift circuitry and voltage detector.

## Functional Description

The device includes an LDO, a Level shifters and a voltage detection circuit. The following is a description of their operation.

### LDO

The system is supplied by a higher system voltage – approximately 6V to 24V – on input pin VCC1. An internal LDO reduces this higher voltage to a 5V level which is supplied on output pin VDD. This lower voltage level is used by the internal logic circuits but as it can supply up to 150mA it can also be used by external circuitry.

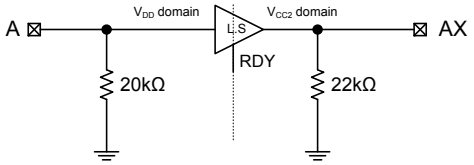
### Level Shifter

The internal level shifter input is pin A with input logic levels referenced by $V_{DD}$. The level shifter output is pin AX, whose levels are referenced by the higher voltage level $V_{CC2}$. Internal circuits ensure a reliable transfer of voltage levels from the $V_{DD}$ reference level to the $V_{CC2}$ reference level which can then be used for IGBT driving purposes. Both level shifter pins, A and AX, are connected via pull-low resistors to ground.

| VDET "RDY" Signal | AX Output |
|---|---|
| 0 | Floating |
| 1 | A |

For voltage detection VDET, RDY=0 means $V_{CC2}$ or $V_{DD}$ is below the normal operation level, and AX will be forced to a floating state.

Note that the system power $V_{CC1}$ must be powered on earlier that $V_{CC2}$, or $V_{CC1}$ and $V_{CC2}$ are powered on simultaneously, in order to avoid circuit malfunctions.

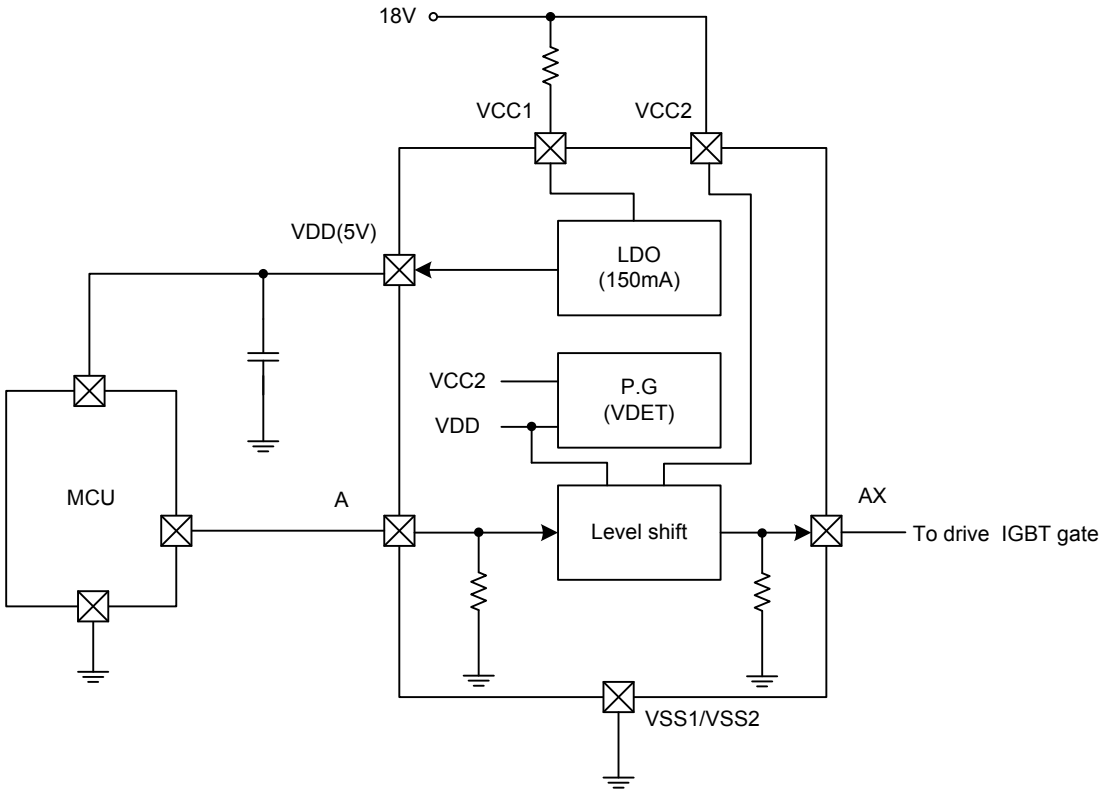



**Level Shifter Control Circuit**

### Voltage Detector

An internal voltage detector monitors the integrity of the $V_{DD}$ and $V_{CC2}$ voltage levels. If the voltage levels are normal, then the level shifter will be enabled to operate normally. Abnormal $V_{DD}$ or $V_{CC2}$ voltage levels will result in the level shifter being disabled to prevent system malfunctions and possible circuit damage.

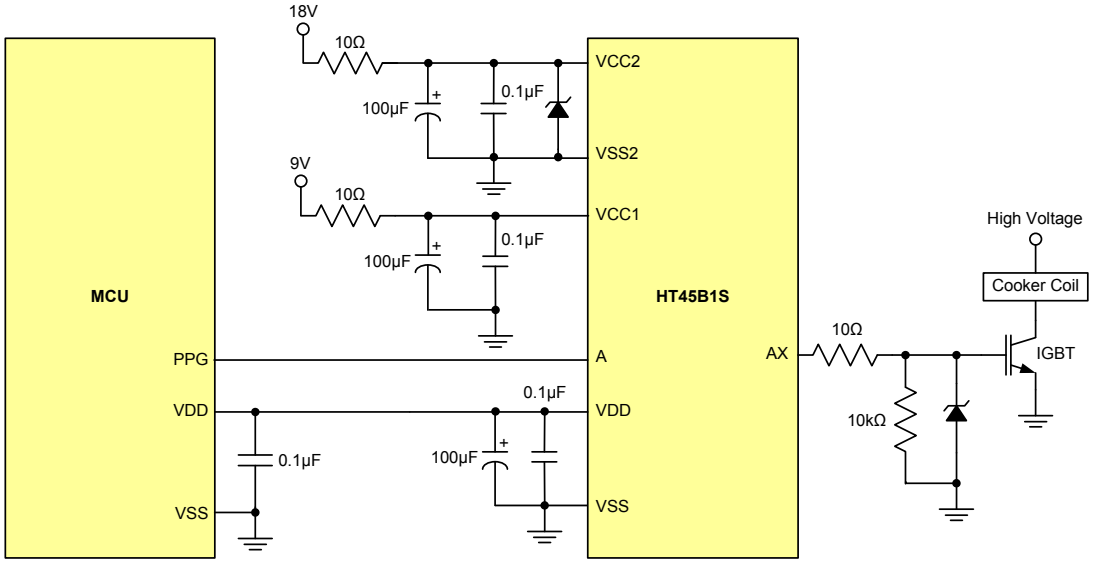
## Application Circuits




### Application Description

The system power $V_{CC1}$ (6V~24V) provides the device power. The LDO output voltage $V_{DD}$ (5V) is provided for the internal logic circuit and external low-voltage components, such as the MCU. The Level Shifters provide high output current for external components, such as IGBT. VDD is the voltage level for the input terminal of the Level shift, A. While $V_{CC2}$ is the voltage level for the output terminal of the Level shift, AX.

## Application Circuits Example




Notes: 1. The power supply decoupling capacitors and zener diode connected to VDD, VCC1 and VCC2 must all be located close to the ICs power supply pins.

2. The IGBT resistor and zener diode drive circuit must be located close to the IGBT transistor.

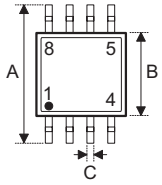
## Package Information

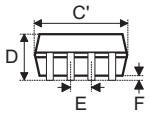
Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

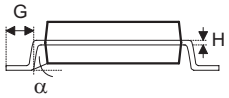
Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

## 8-pin SOP (150mil) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 0.236 BSC | — |
| B | — | 0.154 BSC | — |
| C | 0.012 | — | 0.020 |
| C’ | — | 0.193 BSC | — |
| D | — | — | 0.069 |
| E | — | 0.050 BSC | — |
| F | 0.004 | — | 0.010 |
| G | 0.016 | — | 0.050 |
| H | 0.004 | — | 0.010 |
| α | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 6 BSC | — |
| B | — | 3.9 BSC | — |
| C | 0.31 | — | 0.51 |
| C’ | — | 4.9 BSC | — |
| D | — | — | 1.75 |
| E | — | 1.27 BSC | — |
| F | 0.10 | — | 0.25 |
| G | 0.40 | — | 1.27 |
| H | 0.10 | — | 0.25 |
| α | 0° | — | 8° |