

2*30W I²S Input Stereo Class D Amplifier

■ FEATURES

- Power supply: 4.5V - 26V
- Audio Performance
 - Output Power (BTL)
 - 2×25W (PVDD=16V, R_L=4Ω, THD+N=1%)
 - 2×30W (PVDD=24V, R_L=8Ω, THD+N=1%)
 - Output Power (PBTL)
 - 60W (PVDD=24V, R_L=4Ω, THD+N=1%)
 - 21 W (PVDD=12V, R_L=3Ω, THD+N=1%)
 - THD+N
 - 0.05% (PVDD=12V, R_L=4Ω, P_o=1W)
 - 0.02% (PVDD=24V, R_L=8Ω, P_o=1W)
 - Noise
 - 75uV (Gain = 25.2dB, A weighted)
 - Efficiency
 - 91 % (PVDD=12V, R_L=4Ω, P_o=10W)
- Audio I/O Configuration
 - Single Stereo I²S Input
 - BTL or PBTL output
 - 32, 44.1, 48, 88.2, 96kHz Sample Rates
- General Operational Features
 - Selectable Hardware or I²C Control mode
 - Integrated Digital Output Clipper and AGC
 - Integrated Thermal Foldback Function
 - Programmable I²C Address (110110x^[R/W])
 - Adjustable Switching Frequency for Class D

- Robustness Features
 - Clock Error, DC, and Short-Circuit Protection
 - Overtemperature and Programmable Overcurrent Protection
- Packages
 - Pb-free Packages, QFN36-PP

■ APPLICATIONS

- Bluetooth/Wi-Fi Speakers
- Portable Speakers
- Smart speakers
- LCD TV/Monitor
- Sound Bars, Docking stations, PC Audio

■ DESCRIPTION

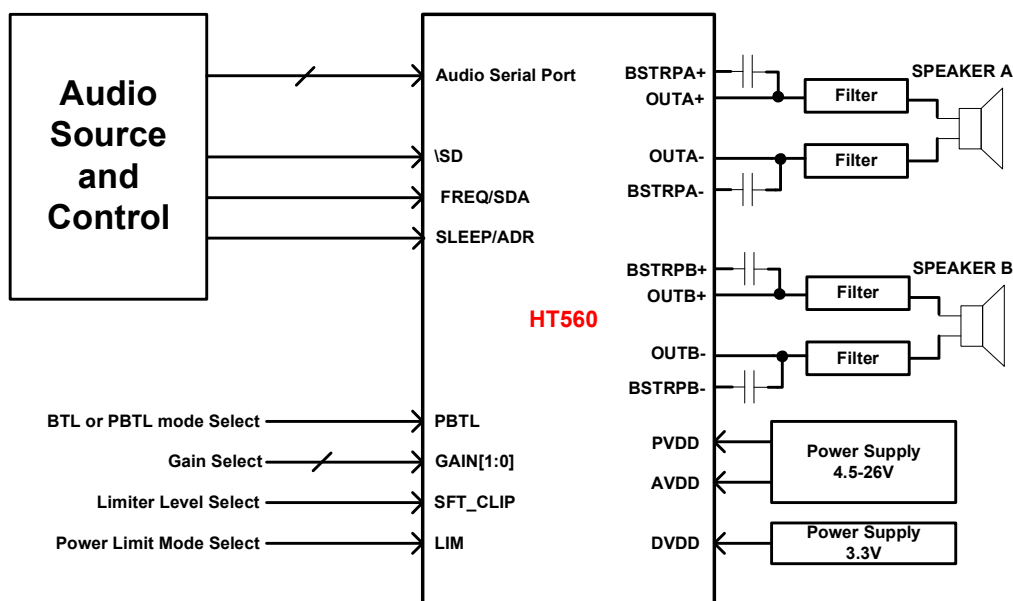
The HT560 is a stereo Class D audio amplifier with an I²S input serial port. It supports a variety of audio clock configurations via two speed modes.

The outputs of the HT560 can be configured to drive two speakers in stereo BTL mode or mono PBTL mode.

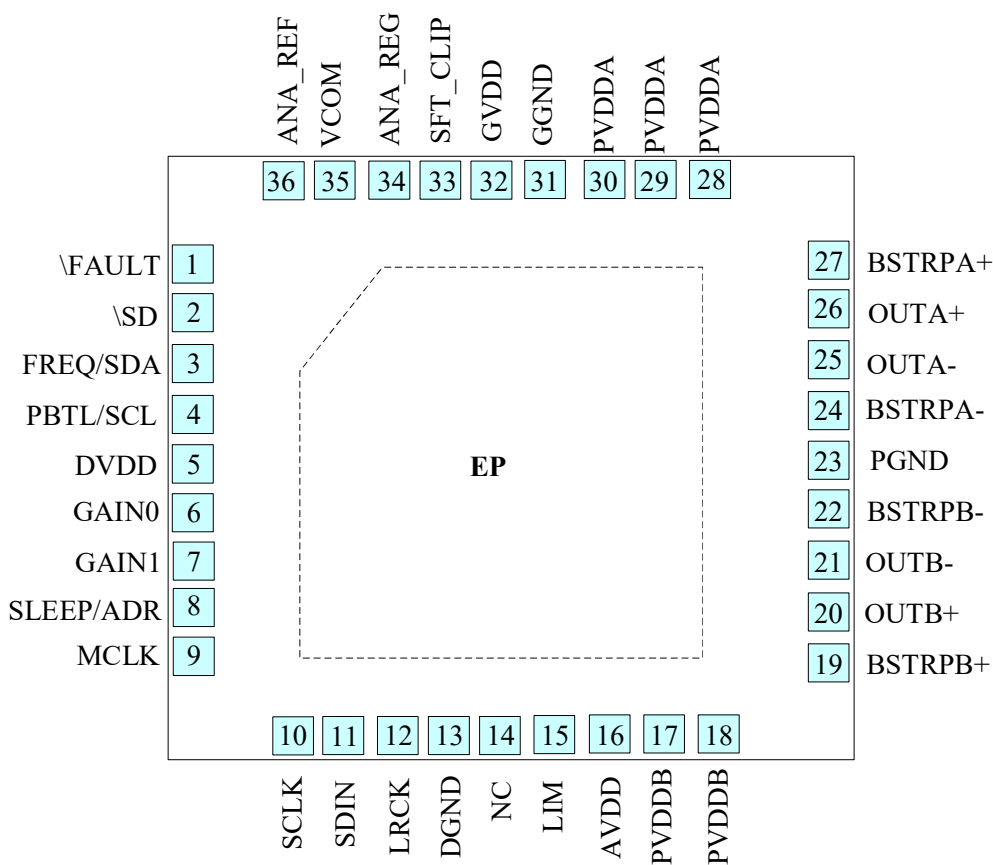
The HT560 also includes hardware and I²C control modes, integrated digital clipper, AGC, several gain options, and a wide power supply operating range to enable use in a multitude of applications.

An optimal mix of thermal performance and device cost is provided in the 110-mΩ R_{DS(ON)} of the output MOSFETs. Additionally, a thermally enhanced 36-Pin QFN provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

■ TYPICAL APPLICATION



■ TERMINAL CONFIGURATION



Top View

■ TERMINAL FUNCTION


| Terminal No. | Name | I/O*1 | Description |
|--------------|-----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | \FAULT | O | Speaker amplifier fault terminal, which is pulled LOW when an internal fault occurs |
| 2 | \SD | I | Places the speaker amplifier in shutdown mode while pulled down. |
| 3 | FREQ/SDA | I | Dual function pin that functions as an I ² C data input pin in I ² C Control Mode or as a Frequency Select terminal when in Hardware Control Mode. |
| 4 | PBTL/SCL | I | Dual function pin that functions as an I ² C clock input terminal in I ² C Control Mode or configures the device to operate in pre-filter Parallel Bridge Tied Load (PBTL) mode when in Hardware Control Mode. |
| 5 | DVDD | P | Power supply for the internal digital circuitry |
| 6 | GAIN0 | I | Adjusts the LSB of the multi-bit gain of the speaker amplifier |
| 7 | GAIN1 | I | Adjusts the MSB of the multi-bit gain of the speaker amplifier |
| 8 | SLLEP/ADR | I | In Hardware Control Mode, places the speaker amplifier in sleep mode. In I ² C Control Mode, is used to determine the I ² C Address of the device |
| 9 | MCLK | I | Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking |
| 10 | SCLK | I | Bit clock for the digital signal that is active on the serial data port's input data line |
| 11 | SDIN | I | Data line to the serial data port |

| | | | |
|----|-----------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12 | LRCK | I | Word select clock for the digital signal that is active on the serial port's input data line |
| 13 | DGND | G | Ground for digital circuitry (NOTE: This pin should be connected to the system ground) |
| 14 | NC | - | Not connected inside the device (all "no connect" pins should be connected to ground for best thermal performance, however they can be used as routing channels if required.) |
| 15 | LIM | I | Selects mode of Digital Output Clipper or AGC |
| 16 | AVDD | P | Power supply for internal analog circuitry |
| 17 | PVDDDB | P | Power Supply for internal power circuitry of Channel B |
| 18 | PVDDDB | P | |
| 19 | BSB+ | BST | Connection point for the OUTB+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTB+ |
| 20 | OUTB+ | O | Positive pin for differential speaker amplifier output B |
| 21 | OUTB- | O | Negative pin for differential speaker amplifier output B |
| 22 | BSB- | BST | Connection point for the OUTB- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTB- |
| 23 | PGND | G | Ground for power device circuitry (NOTE: This terminal should be connected to the system ground) |
| 24 | BSA- | BST | Connection point for the OUTA- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTA- |
| 25 | OUTA- | O | Negative pin for differential speaker amplifier output A |
| 26 | OUTA+ | O | Positive pin for differential speaker amplifier output A |
| 27 | BSA+ | BST | Connection point for the OUTA+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTA |
| 28 | PVDDA | P | Power Supply for internal power circuitry of Channel A |
| 29 | PVDDA | P | |
| 30 | PVDDA | P | |
| 31 | GGND | G | Ground for gate drive circuitry (this terminal should be connected to the system ground) |
| 32 | GVDD | O | Voltage regulator derived from PVDD supply (NOTE: This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry) |
| 33 | SFT_CLIP | I | Sets the maximum output voltage before clipping (Limiter Level) |
| 34 | ANA_REG | P | Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry) |
| 35 | VCOM | P | Bias voltage for internal PWM conversion block |
| 36 | ANA_REF | P | Connection point for internal reference used by ANA_REG and VCOM filter capacitors. And connect to system GND net. |
| / | EP | G | Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder. For proper electrical operation, this ground pad must be connected to the system ground. |

*1: I: Input; O: Output; G: Ground; P: Power; BST: BOOT Strap

ORDERING INFORMATION

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Package type

| Part Number | Package Type | Marking | Operating Temperature Range | MOQ/Shipping Package |
|-------------|--------------|----------------------|-----------------------------|--------------------------|
| HT560SQ | QFN36-PP | HT560sq UVWXYZ *1 | -25°C~85°C | Tape and Reel 3000PCS |

*1: WXYZ/UVWXYZ is production track code.

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嘉兴禾润电子科技有限公司**Jiaxing Heroic Electronic Technology Co., Ltd.**

地址：浙江省嘉兴市凌公塘路3339号JRC大厦A座三层

Add: A 3rd floor, JRC Building, No. 3339, LingGongTang Road, Jiaxing, Zhejiang Province

Sales: 0573-82585539, sales@heroic.com.cn

Support: 0573-82586151, support@heroic.com.cn

Fax: 0573-82585078

Website: www.heroic.com.cn; wap.heroic.com.cn

Wechat MP: HEROIC_JX

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