2*20W I²S Input, Inductor Free, Stereo Class D Amplifier

■ FEATURES

- Power supply:
  -PVDD: 4.5V – 16V; -DVDD/AVDD: 3.3V
- Audio Performance
  -BTL, 2×20W (PVDD=14.5V, R_L=4Ω, THD+N=1%)
  -PBTL, 24W (PVDD=15V, R_L=4Ω, THD+N=1%)
  -THD+N=0.04% (PVDD=12V, R_L=4Ω, Po=1W)
  -Noise: 85uV (Gain = 16dBV, A weighted)
- Low Quiescent Current in 1SPW mode
  -12mA at PVDD = 12V, no filter
- Inductor-free Operation (Ferrite Bead) and EMC compliant for most cases
- Flexible Audio I/O
  - I²S, LJ, RJ, TDM input
  - 8, 16, 32, 44.1, 48, 88.2, 96, 192kHz Sample Rates
- General Operational Features
  - Hardware or Software Control mode
  - 4 Programmable I²C Addresses
  - Spread Switching Frequency for Class D
- Robustness Features
  - Clock Error, DC, Over Current, Overvoltage, Undervoltage, and Overtemperature Protection
- Packages: Pb-free Packages, QFN28L-4*4

■ APPLICATIONS

- Bluetooth/Wi-Fi Speakers
- Portable Speakers
- Smart speakers
- LCD TV/Monitor
- Sound Bars, Docking stations, PC Audio

■ DESCRIPTION

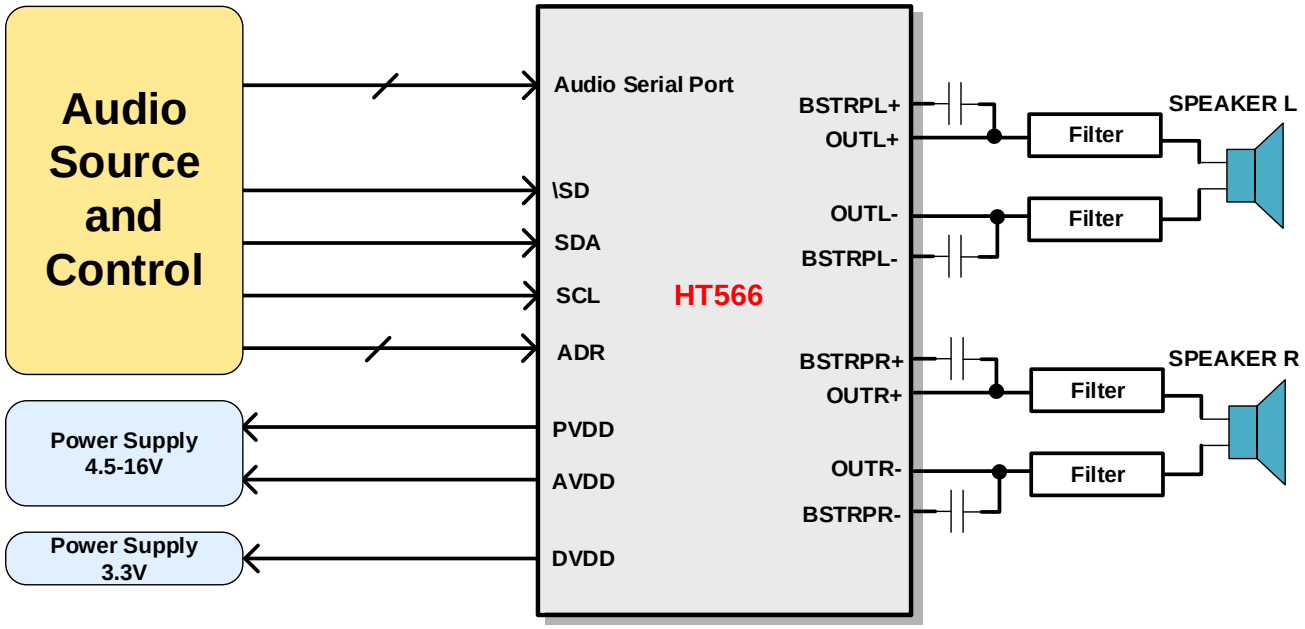
The HT566 is a stereo Class D audio amplifier with multiple audio format port (I²S, LJ, RJ, TDM). It supports a variety of audio clock configurations.

The outputs of the HT566 can be configured to drive two speakers in stereo BTL mode or mono PBTL mode.

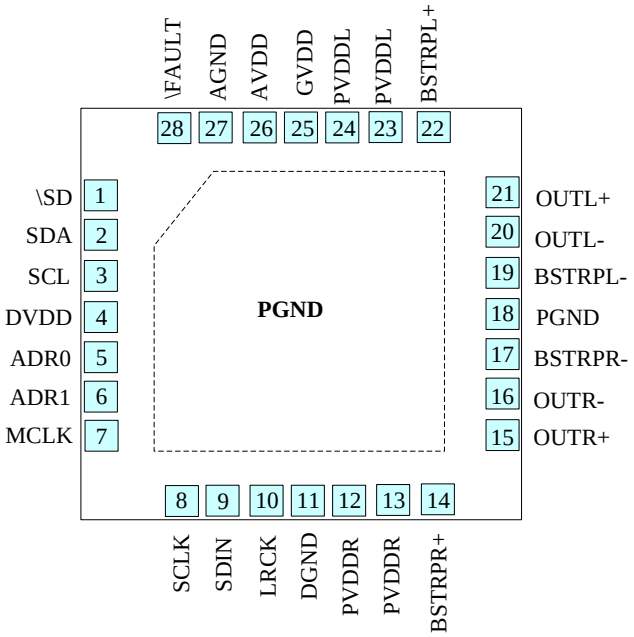
The HT566 also includes hardware and I²C control modes, integrated digital clipper, spread switching frequency for Class D, and a wide power supply operating range to enable use in a multitude of applications.

An optimal mix of thermal performance and device cost is provided in the 120-mΩ $R_{DS(ON)}$ of the output MOSFETs. Additionally, a thermally enhanced 36-Pin QFN provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

■ TYPICAL APPLICATION



■ TERMINAL CONFIGURATION



Top View

■ TERMINAL FUNCTION

Terminal No.	Name	I/O[1]	Description
1	\SD	I	Places the speaker amplifier in shutdown mode while pulled low level.
2	SDA	I	I²C data input pin.
3	SCL	I	I²C clock input terminal.
4	DVDD	P	Power supply for the internal digital circuitry
5	ADR0	I	Determine the I²C Address of the device
6	ADR1	I	Determine the I²C Address of the device
7	MCLK	I	Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking
8	SCLK	I	Bit clock for the digital signal that is active on the serial data port's input data line
9	SDIN	I	Data line to the serial data port
10	LRCK	I	Word select clock for the digital signal that is active on the serial port's input data line
11	DGND	G	Ground for digital circuitry (NOTE: This pin should be connected to the system ground)
12	PVDDR	P	Power Supply for internal power circuitry of Channel R
13	PVDDR	P	
14	BSBRPR+	BST	Connection point for the OUTR+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTR+
15	OUTR+	O	Positive pin for differential speaker amplifier output R
16	OUTR-	O	Negative pin for differential speaker amplifier output R
17	BSBRPR-	BST	Connection point for the OUTR- bootstrap capacitor, which is used to create

[1] : I: Input; O: Output; G: Ground; P: Power; BST: BOOT Strap; OD: Open drain

			a power supply for the high-side gate drive for OUTR-
18	PGND	G	Ground for power device circuitry (NOTE: This terminal should be connected to the system ground)
19	BSTRPL-	BST	Connection point for the OUTL- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTL-
20	OUTL-	O	Negative pin for differential speaker amplifier output L
21	OUTL+	O	Positive pin for differential speaker amplifier output L
22	BSBRPL+	BST	Connection point for the OUTL+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTL
23	PVDDL	P	Power Supply for internal power circuitry of Channel L
24	PVDDL	P	
25	GVDD	O	Voltage regulator derived from PVDD supply (NOTE: This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
26	AVDD	P	Power supply for internal analog circuitry
27	AGND	G	Ground for analog circuitry (NOTE: This pin should be connected to the system ground)
28	\FAULT	OD	Speaker amplifier fault terminal, which is pulled LOW when an internal fault occurs, open-drain output.
EP	PGND	G	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder. For proper electrical operation, this ground pad must be connected to the system ground.

■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	Shipping Package MOQ
HT566SQER	QFN28L	HT566SQ XXXXXXXX[1]	-25℃～85℃	Tape and Reel 2500PCS

[1] Production track code.

■ SPECIFICATIONS [1]

● Absolute Maximum Ratings [2]

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Power supply voltage for AVDD	AVDD	-0.3		4	V
Power supply voltage for PVDD	PVDD	-0.3		18	V
Power supply voltage for DVDD	DVDD	-0.3		4	V
DVDD Referenced Digital Input Voltages	V_I	-0.3		DVDD+0.3	V
Moisture Sensitivity Level (MSL)			MSL3		
Ambient Operating Temperature	T_A	-25		85	℃
Junction Temperature	T_J	-40		125	℃
Storage Temperature	T_{STG}	-40		125	℃

● Recommended Operating Conditions

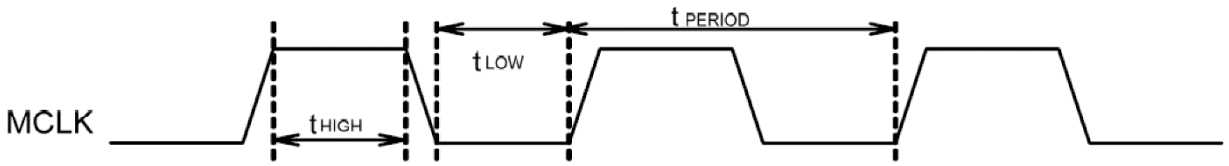
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage for AVDD	AVDD		3	3.3	3.6	V
Power supply voltage for PVDD	PVDD		4.5		16	V
Power supply voltage for DVDD	DVDD		3	3.3	3.6	V
Ambient Operating Temperature	T_a		-25	25	85	℃
DVDD Referenced Digital Input Voltages	V_I		0		DVDD	V
Minimum Speaker Load in BTL Mode	R_L		4			Ω
Minimum Speaker Load in PBTL Mode	R_L		2			Ω

● I/O pins

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Input Logic High threshold for DVDD referenced digital inputs	V_{IH1}	All Digital I/O pins including \FAULT, \SD, SDA, SCL, ADR0, ADR1, MCLK, SCLK, SDIN, LRCK	70			%DVDD
Input Logic LOW threshold for DVDD Referenced Digital Inputs	V_{IL1}				30	%DVDD
Input Logic HIGH Current Level	I_{IH1}				15	uA
Input Logic LOW Current Level	I_{IL1}				-15	uA
Output Logic LOW Voltage Level	V_{OH}		90			%DVDD
Output Logic LOW Voltage Level	V_{OL}				10	%DVDD

● Master Clock

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable MCLK Duty Cycle	D_{MCLK}		45	50	55	%
Supported MCLK Frequencies	f_{MCLK}	Values include: 128, 192, 256, 384, 512.	128		512	f_s
Pulse duration of MCLK high	t_{HIGH}		10.1			ns
Pulse duration of MCLK low	t_{LOW}		10.1			ns
Period of MCLK	t_{PERIOD}		20.2			ns

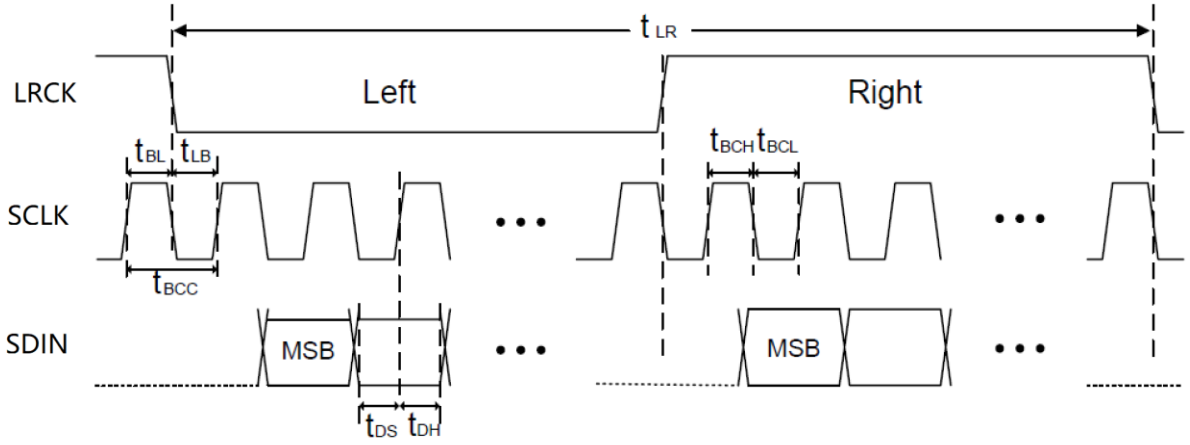


[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Serial Audio Port

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable SCLK Duty Cycle	D_{SCLK}		45	50	55	%
Supported Input Sample Rates ($1/t_{LR}$)	f_s		8		192	kHz
Required LRCK to SCLK Rising Edge	t_{LB}		15			ns
Required SCLK Rising Edge to LRCK edge	t_{BL}		15			ns
Supported SCLK Frequencies ($1/t_{BCC}$) for I2S	F_{SCLK}	Values include: 32, 48, 64	32		64	f_s
Supported SCLK Frequencies ($1/t_{BCC}$) for TDM	F_{SCLK}	Values include: 128, 256, 512	128		512	f_s
SCLK Pulse Width High	t_{BCL}			$t_{BCC}/2$		
SCLK Pulse Width Low	t_{BCH}			$t_{BCC}/2$		
Required SDIN Hold Time after SCLK, Rising Edge	t_{DH}		15			ns
Required SDIN Setup Time before SCLK Rising Edge	t_{DS}		15			ns



Protection Circuitry

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
PVDD Overvoltage Error Threshold	OVE_{RTH}	PVDD Rising		18		V
PVDD Overvoltage Error Threshold	OVE_{FTH}	PVDD Falling		17		V
PVDD Undervoltage Error Threshold	UVE_{RTH}	PVDD Falling		4.2		V
PVDD Undervoltage Error Threshold	UVE_{FTH}	PVDD Rising		4.4		V
Overtemperature Error Threshold	OTE_{TH}			150		℃
Overtemperature Error Hysteresis	OTE_{HYS}			15		℃
Overcurrent Error Threshold for each BTL Output	OCE_{TH}			7.5		A
DC Error Threshold	DCE_{TH}			2.6		V
Speaker Amplifier Fault Time Out period	T_{fault}	DCE		650		ms
		OTE or OCP		1.3		s

● Speaker Amplifier in All Modes

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Speaker Amplifier Gain	AV_{00}			22		dBV
Speaker Amplifier DC Offset	$\|V_{OS}\|$	BTL		1.5		mV
Speaker Amplifier Switching Frequency	$f_{SPK\_AMP(1)}$			360		kHz
On Resistance of Output MOSFET (both high-side and low-side)	$R_{DS(ON)}$			120		mΩ
–3-dB Corner Frequency of High-Pass Filter	f_C	f_S = 44.1 kHz		3.7		Hz
		f_S = 48 kHz		4		Hz
		f_S = 88.2 kHz		7.4		Hz
		f_S = 96 kHz		8		Hz

● Speaker Amplifier in Stereo Bridge Tied Load (BTL) Mode

TA = 25°, PVDD = 12V, DVDD= 3.3V, BTL mode, GAIN = 16dBV, 1SPW mode, fs = 48kHz, f_{SPK_AMP} = 360kHz (unless otherwise noted)

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V_N	PVDD = 12 V, GAIN =16dBV, R_{SPK} = 8 Ω or 4 Ω, 20-20kHz, A-Weighted		100		μV
Signal to Noise Ratio (Referenced to THD+N=1%)	SNR	PVDD = 12 V, R_{SPK} = 8 Ω or 4Ω, 20-20kHz, A-Weighted		97		dB
Maximum Instantaneous Output Power Per. Ch.	Po	PVDD = 12 V, R_{SPK} = 4 Ω, THD+N = 1%		14		W
		PVDD = 12 V, R_{SPK} = 8 Ω, THD+N = 1%		8		W
		PVDD = 14.5V, R_{SPK} = 4 Ω, THD+N = 1%		20		W
		PVDD = 15 V, R_{SPK} = 8 Ω, THD+N = 1%		12.5		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R_{SPK} = 4 Ω, Po = 1 W		0.05		%
		PVDD = 12 V, R_{SPK} =8 Ω, Po = 1 W		0.03		%
Cross-talk (worst case between L->R and R->L coupling)	X-Talk	PVDD = 12 V, GAIN = 16dBV, R_{SPK} = 4 Ω, Po = 1W		-82		dB

● Speaker Amplifier in Mono Parallel Bridge Tied Load (PBTL) Mode

TA = 25°, PVDD = 12V, DVDD= 3.3V, BTL mode, GAIN = 16dBV, 1SPW mode, fs = 48kHz, f_{SPK_AMP} = 360kHz (unless otherwise noted)

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V_N	PVDD = 12 V, GAIN = 16dBV, R_{SPK} = 8 Ω or 4 Ω, 20-20kHz, A-Weighted		85		μV
Signal to Noise Ratio (Referenced to THD+N =1%)	SNR	PVDD = 12 V, R_{SPK} = 8 Ω or 4Ω, 20-20kHz, A-Weighted		99		dB
Maximum Instantaneous Output Power.	Po	PVDD = 12 V, R_{SPK} = 4 Ω, THD+N = 1%		15.7		W
		PVDD = 12 V, R_{SPK} = 2 Ω, THD+N = 1%		26.3		W
		PVDD = 15 V, R_{SPK} = 4 Ω, THD+N = 1%		24		W
		PVDD = 15 V, R_{SPK} = 3 Ω, THD+N = 1%		30		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R_{SPK} = 4 Ω, Po = 1 W		0.08		%
		PVDD = 12 V, R_{SPK} = 2 Ω, Po = 1 W		0.1		%

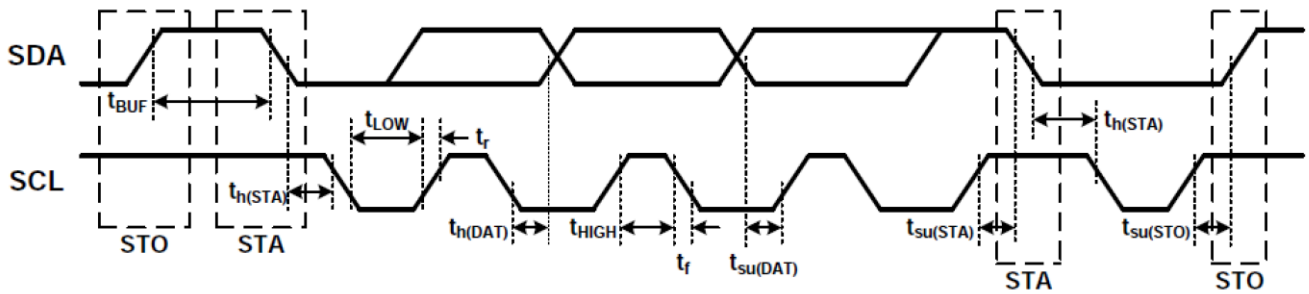
● Typical current consumption

TA = 25°, PVDD = 12V, DVDD= 3.3V, No Load, BTL mode, GAIN = 16dBV, 1SPW mode, fs = 48kHz, f_{SPK_AMP}=360kHz (unless otherwise noted)

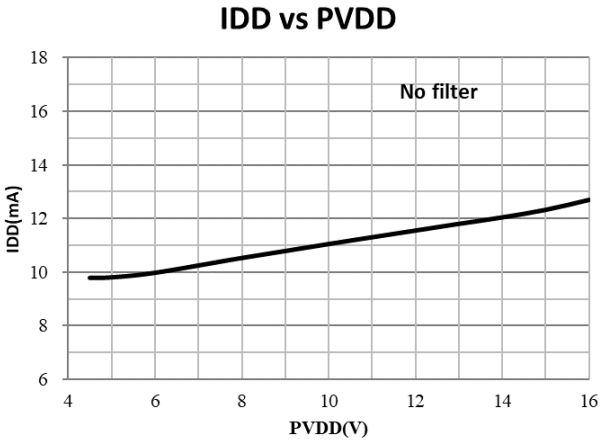
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
IDVDD						
Quiescent current in DVDD	I_{DVDD}	fs=48kHz MCLK=128*fs		2.91	3.3	mA
		fs=48kHz MCLK=256*fs		3.89	4.5	mA
		fs=48kHz MCLK=512*fs		4.67	5.0	mA
		fs=32kHz MCLK=128*fs		2.24	2.5	mA
		fs=32kHz MCLK=256*fs		2.89	3.1	mA
		fs=32kHz MCLK=512*fs		3.44	3.6	mA
DVDD current consumption in sleep mode	I_{DVDD_SLEEP}	SLEEP = H, fs=48kHz MCLK=256*fs		2.15	2.5	mA
		SLEEP = H, fs=32kHz MCLK=256*fs		1.97	2.2	mA
DVDD current consumption in SD mode	I_{DVDD_SD}	\SD = L, No clock		45	80	uA
IPVDD						
Quiescent current in PVDD	IPVDD	PVDD=12V		12		mA
PVDD current consumption in SD mode	I_{PVDD_SD}	PVDD=12V		12		uA

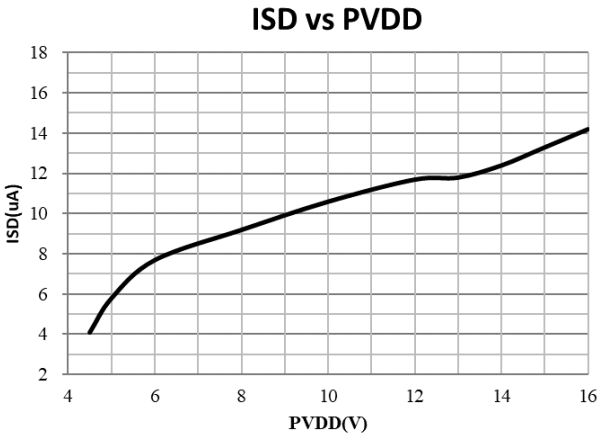
● I²C Control Port

PARAMETER	Symbol	Standard-Mode			Fast-Mode			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Allowable Load Capacitance for Each I²C Line	C_b			400			400	pF
Support SCL frequency	f_{SCL}			100			400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{h(STA)}$	4			0.6			us
Required Pulse Duration, SCL HIGH	t_{HIGH}	4			0.6			us
Required Pulse Duration, SCL LOW	t_{LOW}	4.7			1.3			us
Setup time for a repeated START condition	$t_{su(STA)}$	4.7			0.6			us
Data hold time	$t_{h(DAT)}$	0		3.45	0		0.9	us
Setup Time, SDA to SCL	$t_{su(DAT)}$	250			100			ns
Rise Time, SCL	T_{r_SCL}			1000			300	ns
Rise Time, SDA	T_{r_SDA}			$1/(4*f_{scl})$-0.25			$1/(4*f_{scl})$-0.25	us
Fall Time, SCL and SDA	T_f			300			300	ns
Setup Time, SCL to STOP condition	$t_{su(STO)}$	4			0.6			us
Bus Free time between STOP and START conditions	t_{BUF}	4.7			1.3			us

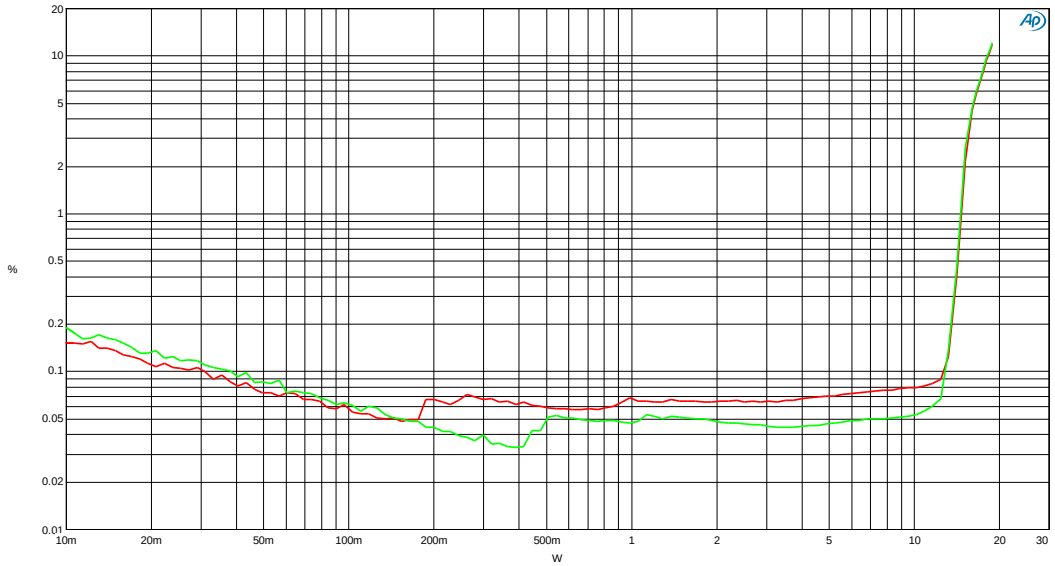


■ TYPICAL OPERATING CHARACTERISTICS

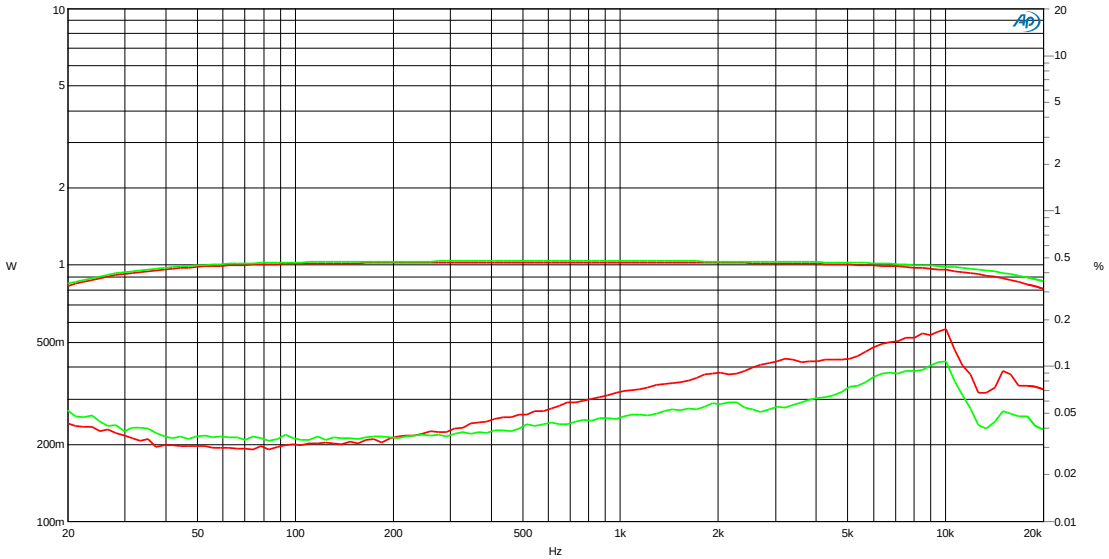




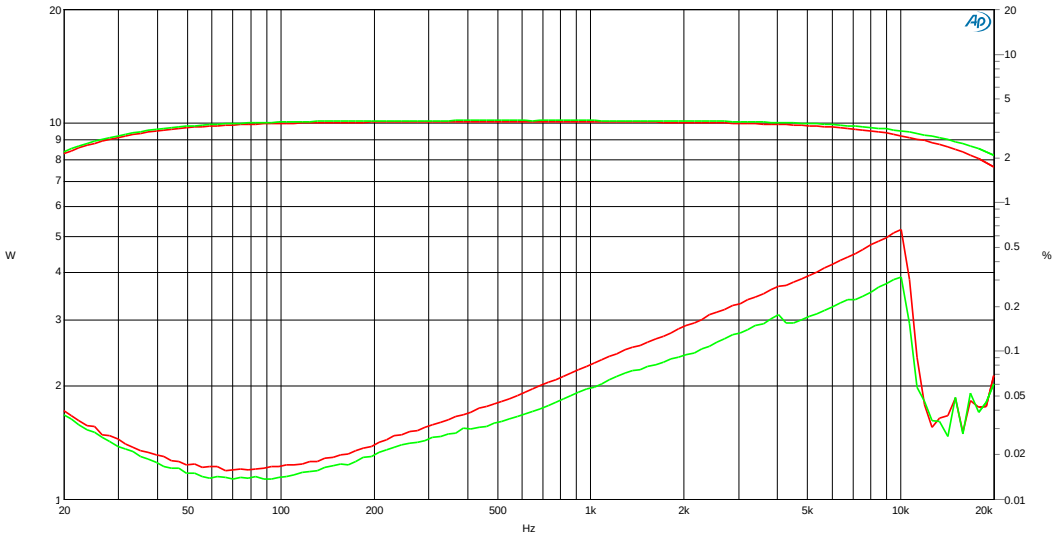
T_A = 25°C, PVDD =12V, **BTL mode**, f_{SPK_AMP} = 360 kHz, f_{IN} = 1 kHz, 1SPW mode, Load = 4ohm, Output filter is used as 300R ferrite bead and 1nF capacitor, unless otherwise noted.



Output Power vs THD+N

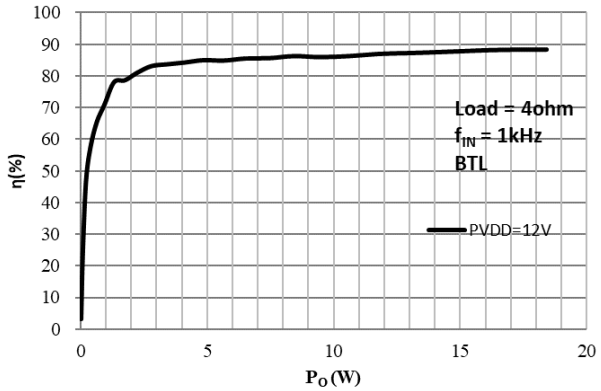


f_{IN} vs THD+N(Po=1W)

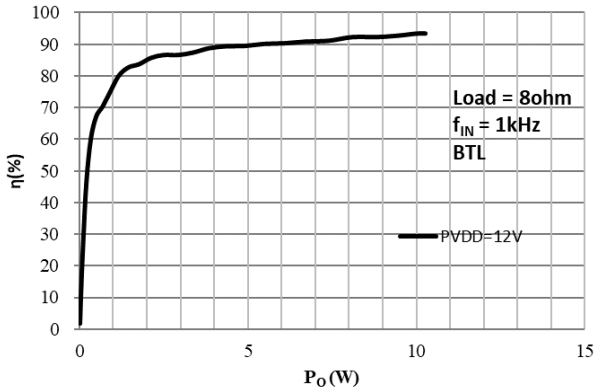


f_{IN} vs THD+N(Po=10W)

P_O vs η

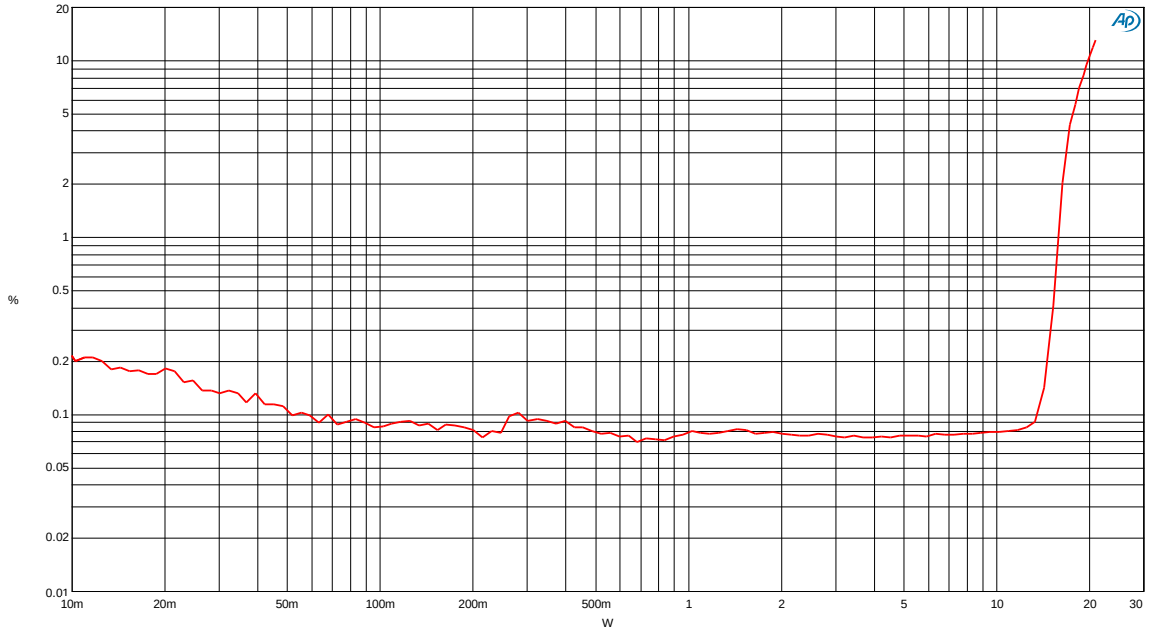


P_O vs η

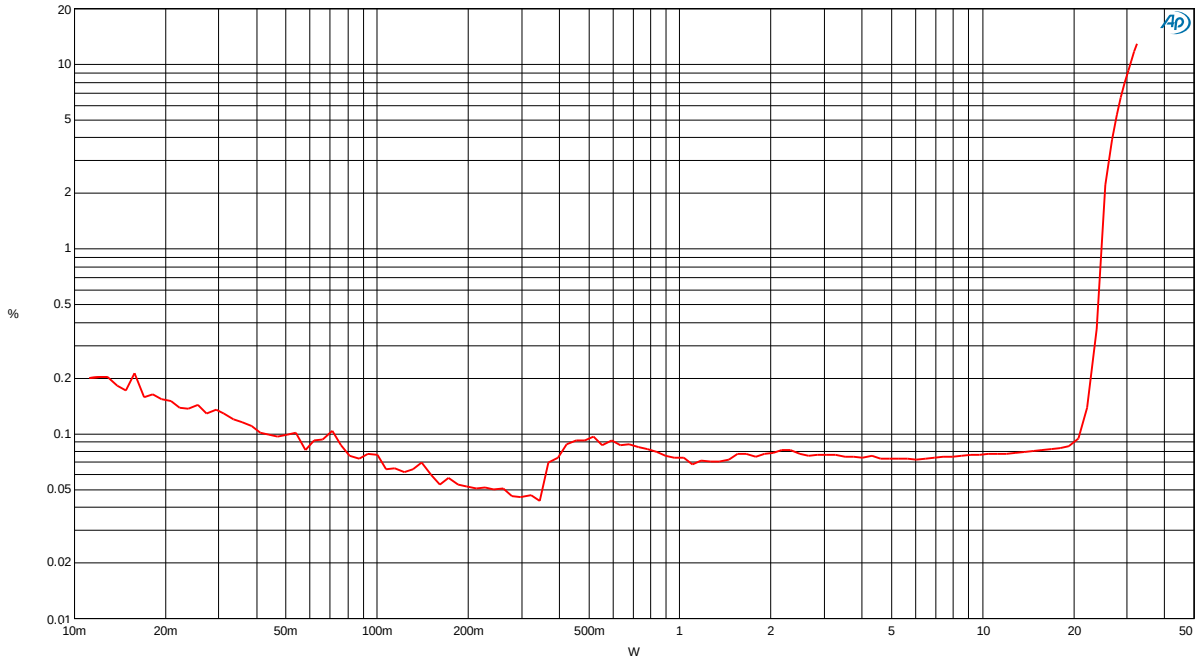


T_A = 25°C, PVDD =12V, **PBTL mode**, f_{SPK_AMP} = 360 kHz, f_{IN} = 1 kHz, 1SPW mode, Load = 4ohm, Output filter is used as 300R ferrite bead and 1nF capacitor, unless otherwise noted.

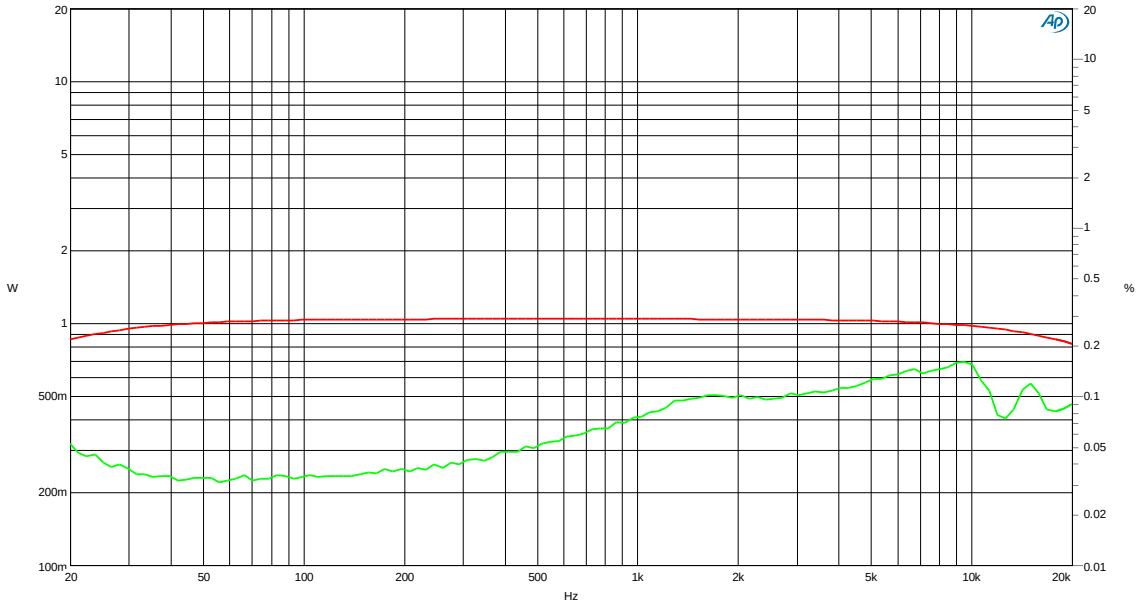
PBTL



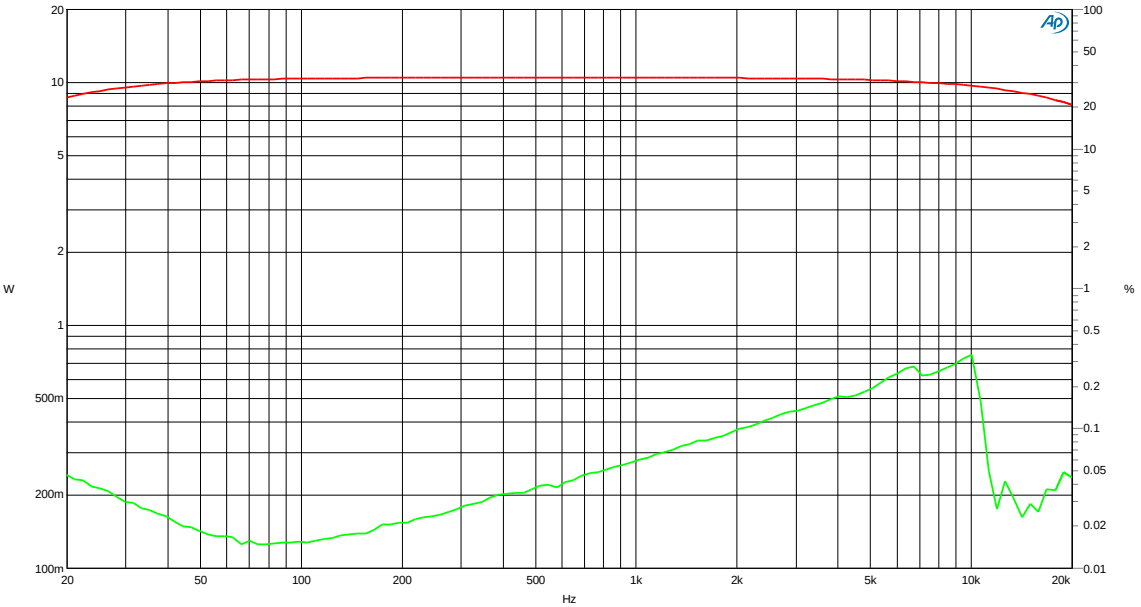
Output Power vs THD+N (PVDD=12V)



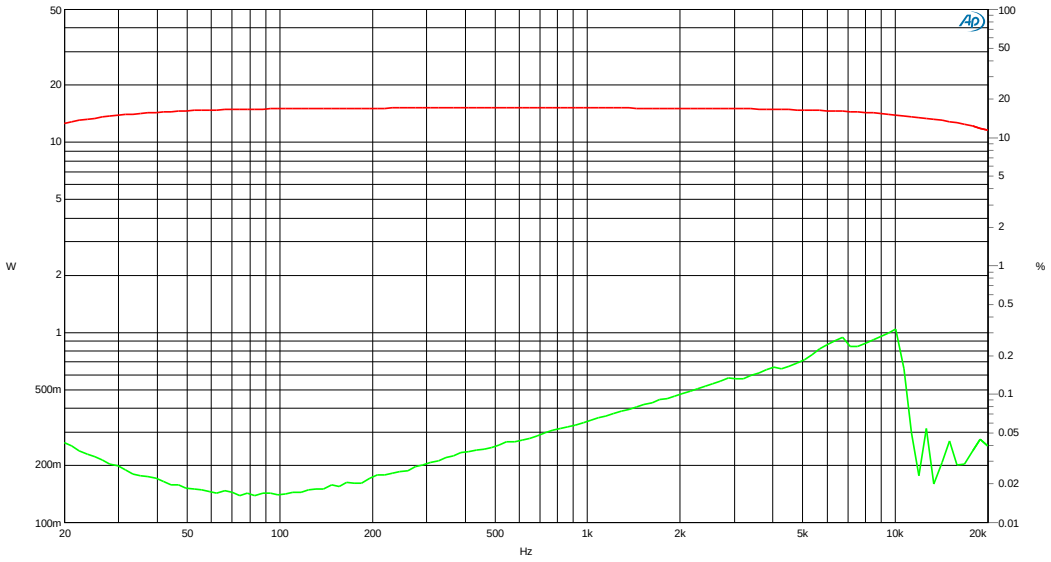
Output Power vs THD+N (PVDD=15V)



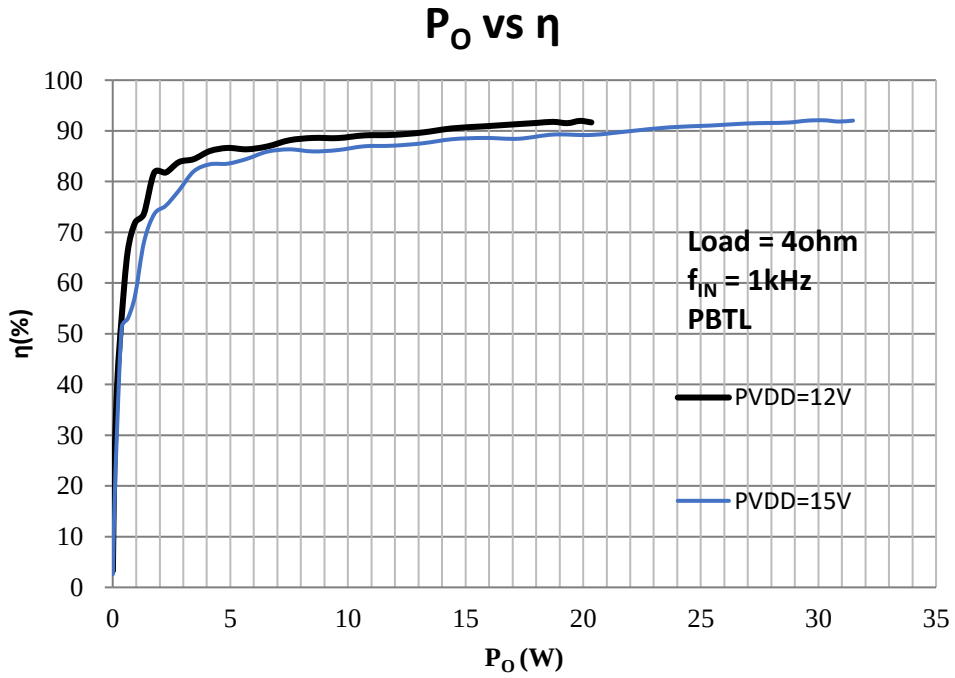
f_{IN} vs THD+N (Po=1W)



f_{IN} vs THD+N (Po=10W)



f_{IN} vs THD+N (PVDD=15V,Po=10W)



■ APPLICATION INFORMATION

The HT566 is a flexible and easy-to-use stereo class-D speaker amplifier with a digital input serial audio port. The HT566 supports a variety of audio clock configurations via two speed modes between 8kHz to 192kHz sample rate. The outputs of the HT566 can be configured to drive two speakers in stereo Bridge Tied Load (BTL) mode or a single speaker in Parallel Bridge Tied Load (PBTL) mode.

1 Power Supplies

Only two power supplies are required for the HT566. They are a 3.3-V power supply, called DVDD and AVDD for the small signal digital and analog and a higher voltage power supply, called PVDD for the output stage of the speaker. To enable use in a variety of applications, PVDD can be operated over a large range of voltages, which is 4.5V – 16V, and it is recommended to put paralleled capacitor of 100nF//1uF//220uF between each channel of PVDD and system ground.

2 Speaker Amplifier Audio Signal Path

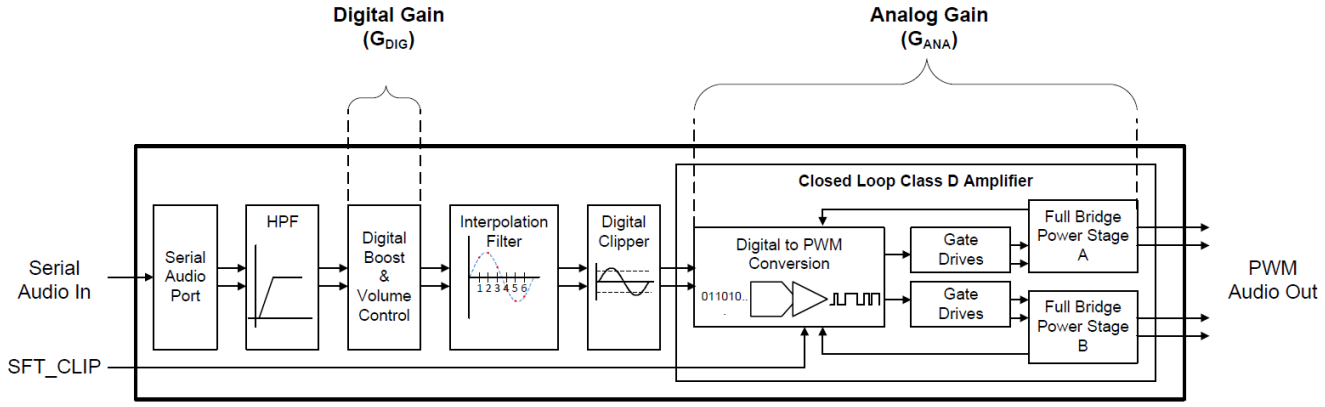


Figure 1 Speaker Amplifier Audio Signal Path

2.1 Serial Audio Port

The serial audio port receives audio in either I²S, Left Justified, Right Justified or TDM formats, up to 32-bit word length. Default setting is I²S and 24-bit word length. The supported clock rates and ratios are detailed below.

Table. 1 Supported SCLK rates for TDM

Maximum Sample Rate fs (kHz)	SCLK Rate (xfs)
8-48kHz	128, 256, 512
96kHz	128, 256
192kHz	128

Table. 2 Supported SCLK rates for IIS/LJ/RJ

Sample Rate fs (kHz)	MCLK rate (× fs)							
	128	192	256	384	512	768	1024	1152
	SCLK rate (× fs)							
8	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S
12	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S
16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
24	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
38	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
44.1	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S
88.2	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S
96	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S
128	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S
176.4	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S	N/S	N/S
192	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S	N/S	N/S

2.1.1 I²S

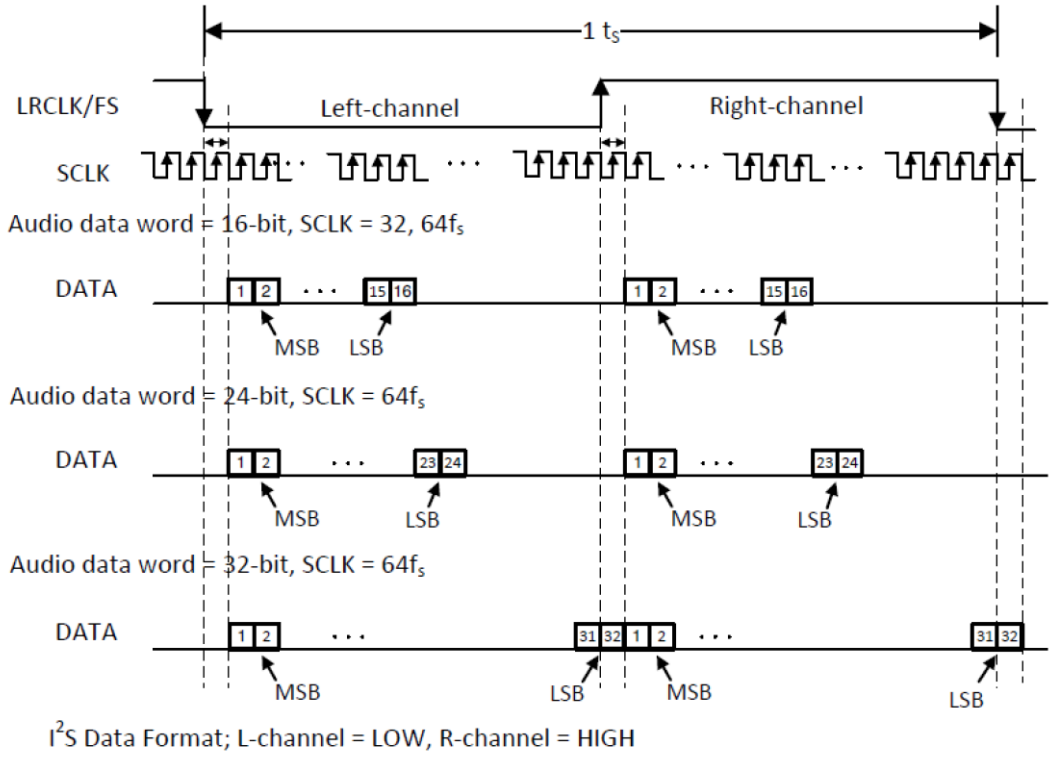


Figure 2 IIS Audio Data Format Timing

2.1.2 Left-Justified

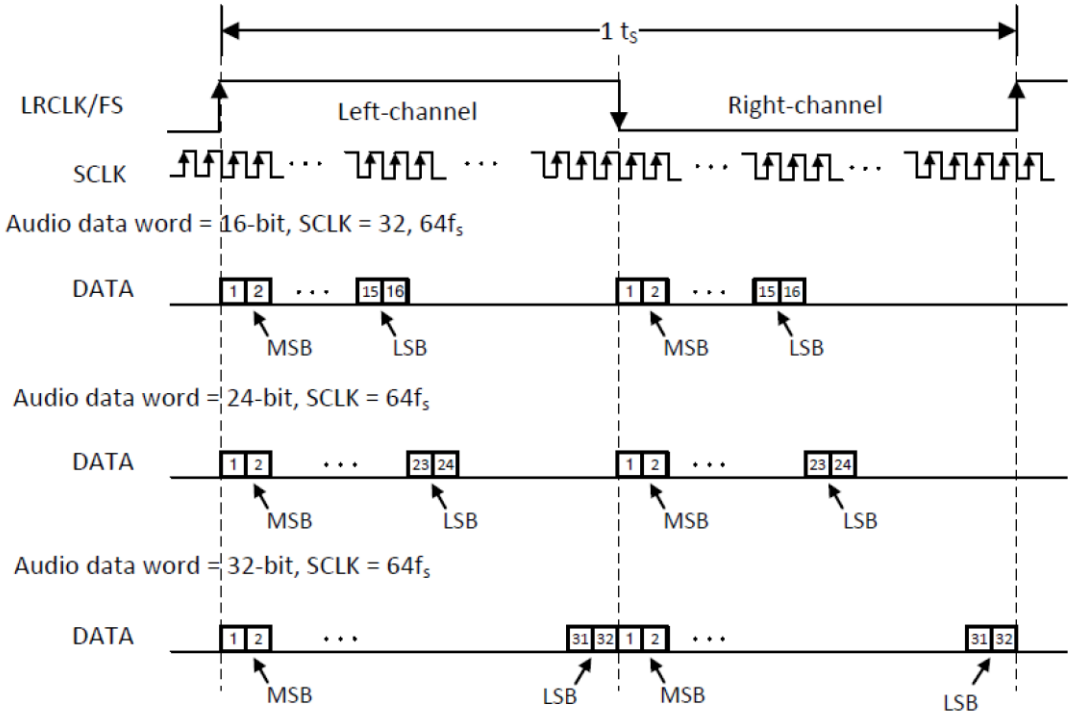


Figure 3 Left-Justified Audio Data Format Timing

2.1.3 Right-Justified

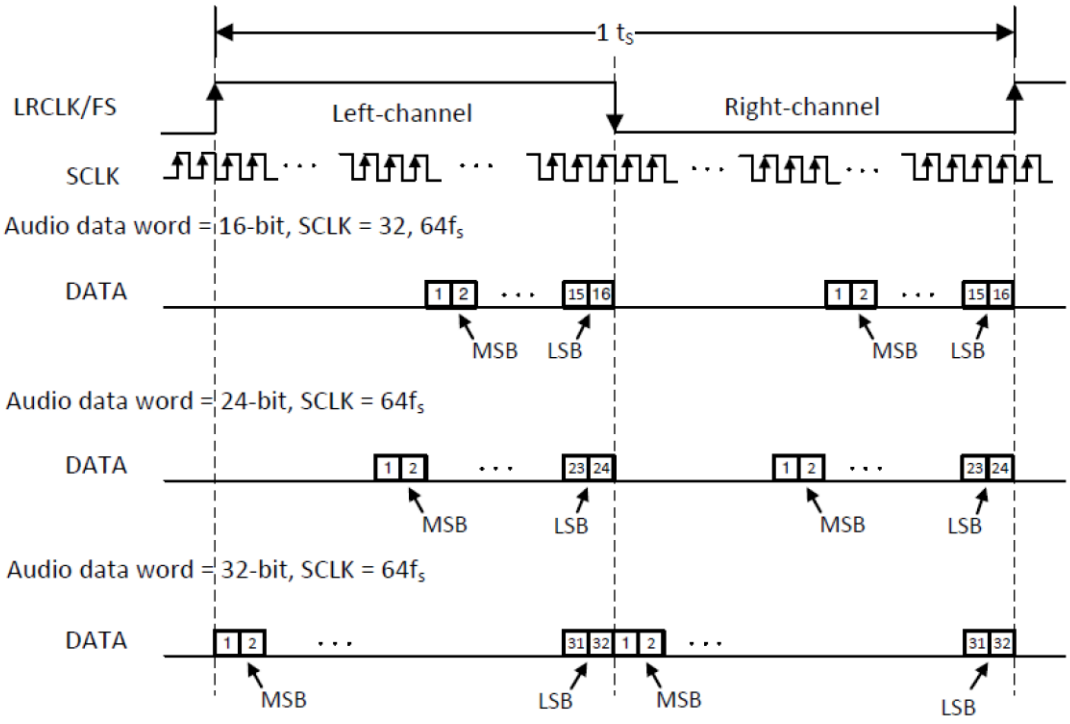


Figure 4 Right-Justified Audio Data Format Timing

2.1.4 TDM

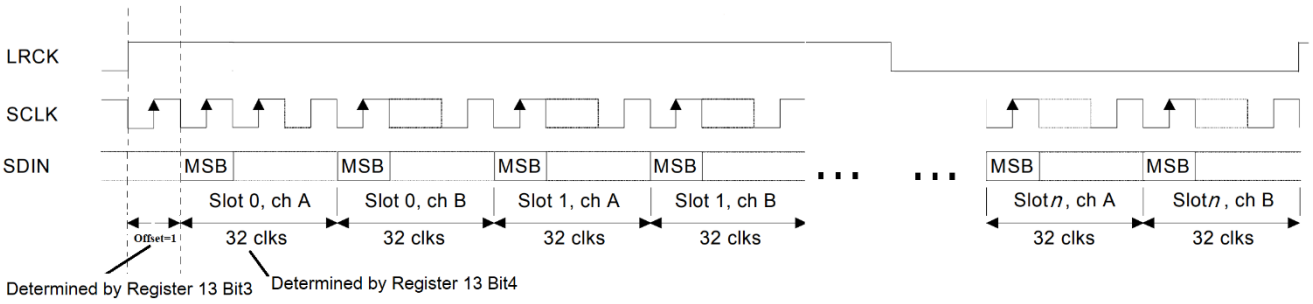


Figure 5 TDM Audio Data Format Timing

2.2 DC Blocking Filter

Excessive DC content in the audio signal can damage loudspeakers and even small amounts of DC offset in the signal path cause audible artifacts when muting and unmuting the speaker amplifier. For these reasons, the amplifier employs two separate DC blocking methods for the speaker amplifier. The first is a high-pass filter provided at the front of the data path to remove any DC from incoming audio data before it is presented to the audio path. The –3 dB corner frequencies for the filter are specified in the speaker amplifier electrical characteristics table. In Hardware Control mode, the DC blocking filter is active and cannot be disabled. In I²C Control mode, the filter can be bypassed by writing a 0 to bit 7 of register 0x14. The second method is a DC detection circuit that will shut down the power stage and issue a latching fault if DC is found to be present on the output due to some internal error of the device. This DC Error (DCE) protection is discussed in the Protection Circuitry section below.

2.3 Digital Boost and Volume Control

Following the high-pass filter, a digital boost block is included to provide additional digital gain if required for a given application as well as to set an appropriate clipping point for a given GAIN configuration. The digital boost block defaults to +0dB and is changeable through bit [1:0] of register 14. In most use cases, the digital boost block will remain unchanged, as the volume control offers sufficient digital gain for most applications. The HT566's digital volume control operates from Mute to 24 dB, in steps of 0.5 dB. The equation below illustrates how to set the 8-bit volume control register at address 0x15/0x16:

DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB])

Transitions between volume settings will occur at a rate of 0.5 dB every 8 LRCK cycles to ensure no audible artifacts occur during volume changes. This volume fade feature can be disabled via Bit 4 of Register 0x14.

2.4 Digital Clipper

A digital clipper is integrated in the oversampled domain to provide a component-free method to set the clip point of the speaker amplifier. Through the "Digital Clipper Level x" (at register address 0x10, 0x11, 0x12) controls in the I²C control port, the point at which the oversampled digital path clips can be set directly, which in turns sets the 10% THD+N operating point of the amplifier. This is useful for applications in which a single system is designed for use in several end applications that have different power rating specifications. Its place in the oversampled domain ensures that the digital clipper is acoustically appealing and reduces or eliminates tones which would otherwise foldback into the audio band during clipping events. Figure 6 shows a block diagram of the digital clipper.

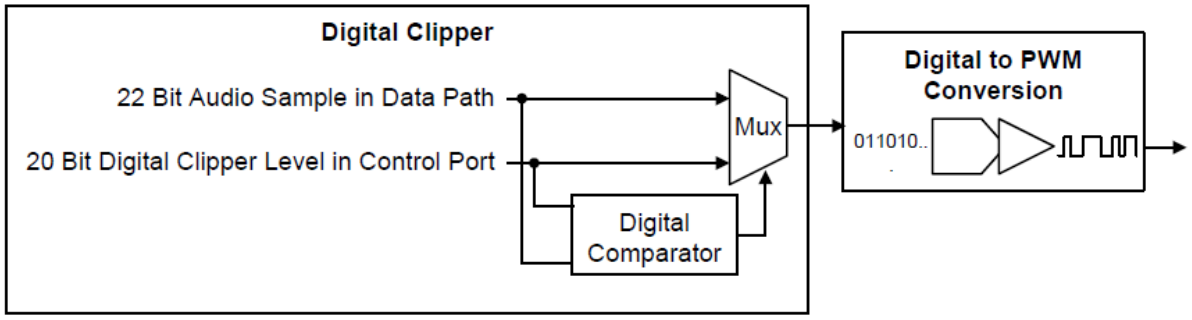


Figure 6 Digital Clipper Simplified Block Diagram

It is important to note that the actual signal developed across the speaker will be determined not only by the digital clipper, but also the analog gain of the amplifier. Depending on the analog gain settings and the PVDD level applied, clipping could occur as a result of the voltage swing that is determined by the gain being larger than the available PVDD supply rail.

2.5 Closed-Loop Class-D Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed-Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device.

The switching rate of the amplifier is internally fixed around 360 kHz.

3 Speaker Amplifier Protection Suite

The speaker amplifier in the HT566 includes a robust suite of error handling and protection features. It is protected against Over-Current, Under-Voltage, Over-Voltage, Over-Temperature, DC, and Clock Errors. The status of these errors is reported via the FAULT pin and the appropriate error status register in the I²C Control Port. The error or handling behavior of the device is characterized as being either "Latching" or "Non-Latching" depending on what is required to clear the fault and resume normal operation (that is playback of audio).

For latching errors, the \SD pin or the SD bit in the control port must be toggled in order to clear the error and resume normal operation. If the error is still present when the \SD pin or SD bit transitions from LOW back to HIGH, the device will again detect the error and enter into a fault state resulting in the error status bit being set in the control port and the \FAULT line being pulled LOW. If the error has been cleared (for example, the temperature of the device has decreased below the error threshold) the device will attempt to resume normal operation after the \SD pin or SD bit is toggled and the required fault time out period (T_{FAULT}) has passed. If the error is still present, the device will once again enter a fault state and must be placed into and brought back out of shutdown in order to attempt to clear the error.

Table. 3 Protection Suite Error Handling Summary

ERROR	CAUSE	FAULT TYPE	Error Is Cleared By
Overvoltage Error (OVE)	PVDD level rises above that specified by OVE_{RTH}	Non-latching	PVDD level returning below OVE_{FTH}
Undervoltage Error (UVE)	PVDD level drops below that specified by UVE_{RTH}	Non-latching	PVDD level returning above UVE_{RTH}
Clock Error (CLKE)	One or more of the following errors has occurred: 1. Non-supported MCLK to LRCK and/or SCLK to LRCK Ratio; 2. Non-supported MCLK or LRCK rate 3. MCLK, SCLK, or LRCK has stopped	Non-latching	Clocks returning to valid state
Overcurrent Error (OCE)	Speaker Amplifier output current has increased above the level specified by OCE_{TH}	Latching	\FAULT has passed AND \SD Pin or Bit Toggle
DC Detect Error (DCE)	DC offset voltage on the speaker amplifier output has increased above the level specified by the DCE_{TH}	Latching	\FAULT has passed AND \SD Pin or Bit Toggle
Overtemperature Error (OTE)	The temperature of the die has increased above the level specified by the OTE_{TH}	Latching	\FAULT has passed AND \SD Pin or Bit Toggle AND the temperature of the device has reached a level below that which is dictated by the OTE_{HYS} specification

For non-latching errors, the device will automatically resume normal operation (that is playback) once the error has

been cleared. The non-latching errors, with the exception of clock errors will not cause the \FAULT line to be pulled LOW. It is not necessary to toggle the \SD pin or SD bit in order to clear the error and resume normal operation for non-latching errors. Table. 3 details the types of errors protected by the HT566's Protection Suite and how each are handled.

3.1 \FAULT pin

In both hardware and I²C Control mode, the \FAULT pin of the HT566 serves as a fault indicator to notify the system that a fault has occurred with the speaker amplifier by being actively pulled LOW. This pin is an open-drain output pin and, unless one is provided internal to the receiver, requires an external pullup to set the net to a known value. The behavior of this pin varies based upon the type of error which has occurred.

In the case of a latching error, the fault line will remain LOW until such time that the HT566 has resumed normal operation (that is the \SD pin or bit has been toggled and T_{FAULT} has passed).

With the exception of clock errors, non-latching errors will not cause the \FAULT pin to be pulled LOW. Once a non-latching error has been cleared, normal operation will resume. For clocking errors, the \FAULT line will be pulled LOW, but upon clearing of the clock error normal operation will resume automatically, that is, with no T_{FAULT} delay.

One method which can be used to convert a latching error into an auto-recovered, non-latching error is to connect the \FAULT pin to the \SD pin. In this way, a fault condition will automatically toggle the \SD pin when the \FAULT pin goes LOW and returns HIGH after the \FAULT period has passed.

3.2 Over-current Protection

The HT566 features over-current conditions against the output stage short-circuit conditions. The short circuit protection fault is reported on the \FAULT pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is triggered.

3.3 Over-temperature Protection

Thermal protection on the HT566 device prevents damage to the device when the internal die temperature exceeds 150°C. This triggering point has a ±15°C tolerance from device to device. Once the die temperature exceeds the thermal triggering point, the device is switched to the shutdown state and the outputs are disabled. Thermal protection faults are reported on the \FAULT pin.

3.4 Over-voltage Protection

The HT566 device monitors the voltage on PVCC voltage threshold. When the voltage on PVCCL pin and PVCCR pin exceeds the over-voltage threshold (18 V typ), the OVP circuit puts the device into shutdown mode.

*3.5 Under-*voltage *Protection*

When the voltage on PVCCL pin and PVCCR pin falls below the under-voltage threshold (4.2 V typ), the UVP circuit puts the device into shutdown mode.

3.6 Clock error detection

When any clock of MCLK, SCLK, LRCK halt or shifted to a non-supported speed, the device reports Clock Error in bit [1:0] of Register 0x17.

3.7 DC Detect Protection

The HT566 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. A DC detect fault is reported on the \FAULT pin as a low state. The DC Detect fault also causes the amplifier to shutdown by changing the state of the outputs to Hi-Z.

A DC Detect Fault is issued when the output DC voltage sustain for more than 800 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 1 Hz. To avoid nuisance faults due to the DC detect circuit, hold the \SD pin low at power-up until the signals at the inputs are stable.

4 Device Functional Modes

4.1 Software Control

The HT566 device can be configured via an I²C communication port which is software control mode. Once all powers (PVDD, AVDD, DVDD) are brought up and stable, the device is ready for software control. Before the device is

configured into operation (that is bring \SD pin to high, or write Bit "SD" into 1), configure the device via I²C in the manner required by the use case, e.g., bit "PBTL" and "Format".

For systems which do not require the added flexibility of the I²C control port or do not have an I²C host controller, the HT566 can be used directly in Hardware Control Mode with default configurations. The only external I/O that can be controlled in Hardware Control Mode is the \SD pin.

4.2 Speaker Amplifier Shut Down (\SD pin)

The \SD pin is provided to place the speaker amplifier into shutdown. Driving this pin LOW will place the device into shutdown, while pulling it HIGH will bring the device into operation with two different modes, see as the following table. The shutdown mode is the lowest power consumption mode that the device can be placed in while the power supplies are up.

However, when \SD pin is pulled low, the software control mode is ready, the device is still capable of being configured through I²C port. If the \SD pin is pulled low, and bit SD is written into 1, the device is in operation mode with spread spectrum on.

Table. 4 \SD Pin Configuration

\SD Pin Voltage	Mode
<0.6V	Shutdown mode
1.5V - 2.2V	Operation mode with spread spectrum off
2.5V - DVDD	Operation mode with spread spectrum on

4.2.1 Spread Spectrum

The HT566 device has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM output to improve EMI performance. The spread spectrum scheme is internally fixed and is always turned on.

De-phase inverts the phase of the output PWM such that the idle output PWM waveforms of the two audio channels are inverted. De-phase does not affect the audio signal, or its polarity. De-phase only works with BD mode; it is auto-disabled in 1SPW mode.

4.3 Speaker Amplifier Operating Modes

The HT566 device can be used with two different amplifier configurations, can be configured by Bit 3 of Register 18: BTL Mode and PBTL Mode

4.3.1 BTL Mode

In BTL mode, the HT566 amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUTL+ and OUTL-, the amplified right signal is presented on differential output pair shown as OUTR+ and OUTR-.

4.3.2 PBTL Mode

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device.

On the input side of the HT566 device, the input signal to the PBTL amplifier is left frame of I2S or TDM data.

4.4 Class D Amplifier Modulation

The HT566 device can be used with two different Class D amplifier modulations, can be configured by Bit 7 of Register 19.

4.4.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTx+ and OUTx- are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle

of OUTx+ is greater than 50% and OUTx- is less than 50% for positive output voltages. The duty cycle of OUTx+ is less than 50% and OUTx- is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I2R losses in the load.

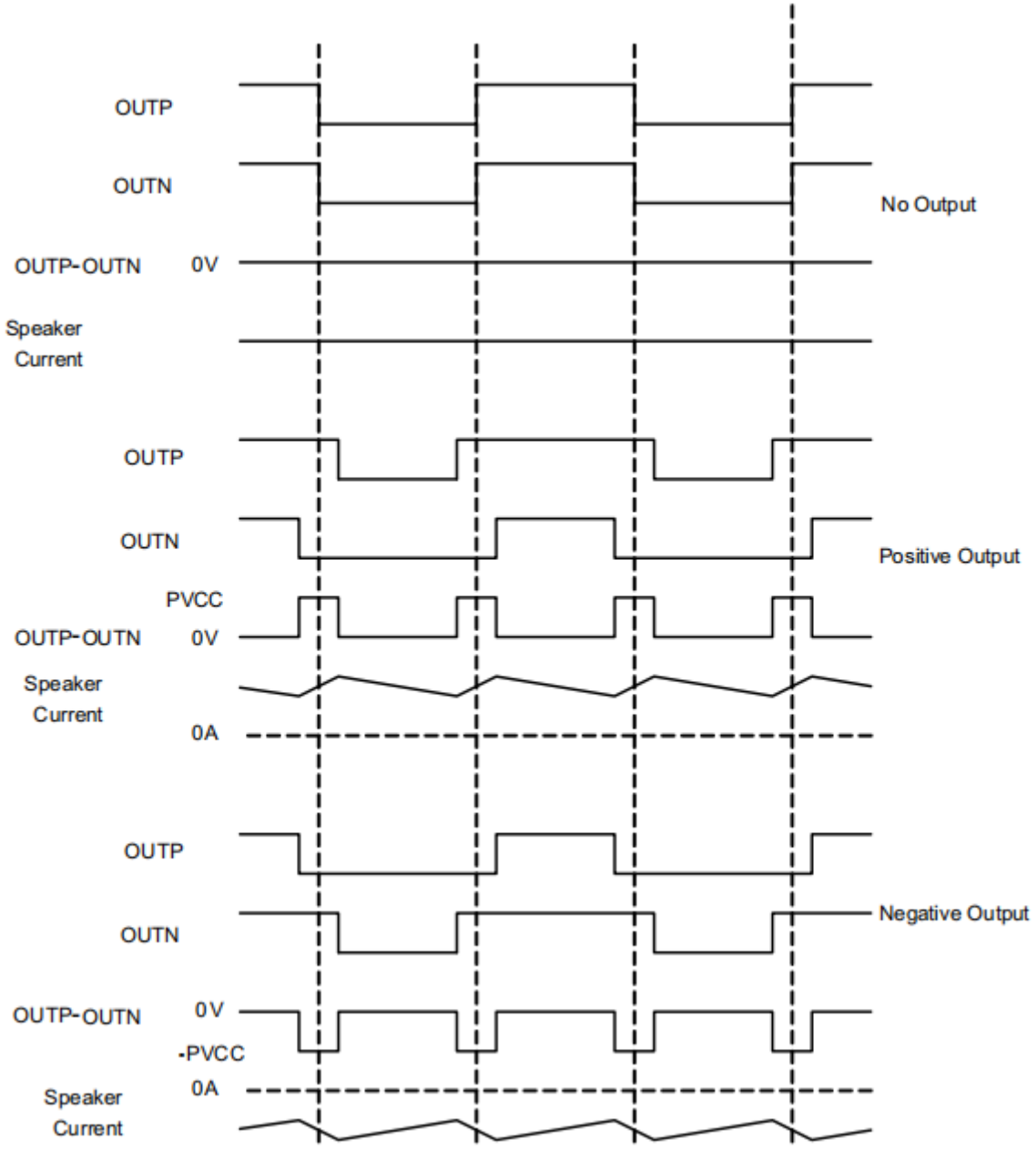


Figure 7 BD Modulation

4.4.2 Low-Idle-Current 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an audio signal is applied one output decreases and the other output increases. The decreasing output signal rails to GND. At which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

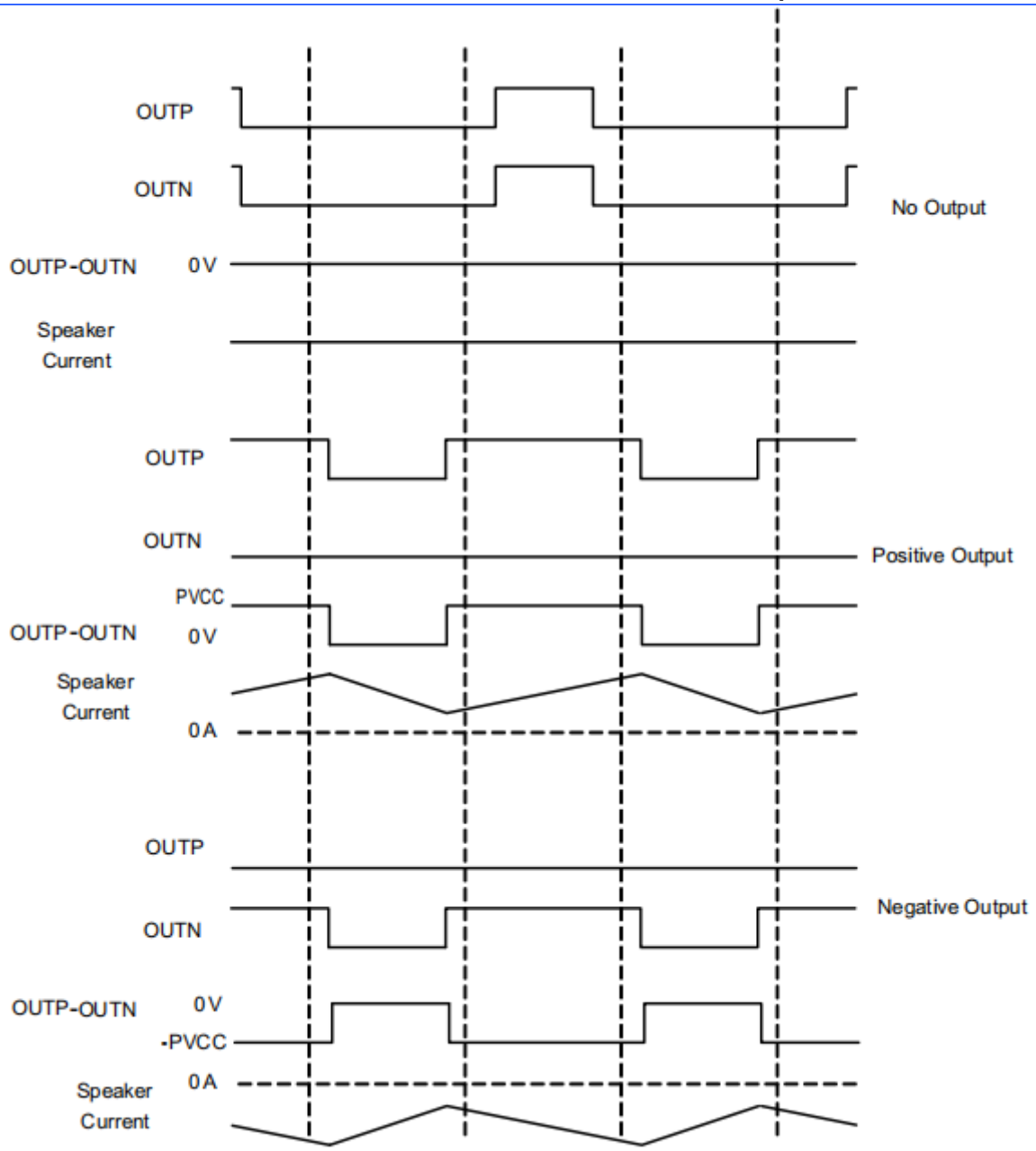


Figure 8 1SPW Modulation

4.5 I²C Control Port

4.5.1 I²C Device Address

Each device on the I²C bus has a unique address that allows it to appropriately transmit and receive data to and from the I²C master controller. As part of the I²C protocol, the I²C master broadcast an 8-bit word on the bus that contains a 7-bit device address in the upper 7 bits and a read or write bit for the LSB. The HT566 has a configurable I²C address. The ADR[1:0] can be used to set the device address of the HT566. The seven bit I²C device address is configured as "11011xx [R/W]", where "xx" corresponds to the state of the ADR[1:0] pin at first power up sequence of the device. [R/W] represents 1 when writing, [R/W] represents 0 when reading.

4.5.2 General Operation of the I²C Control Port

The HT566 device has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multi-master bus environment or wait-state insertion.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each

transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus.

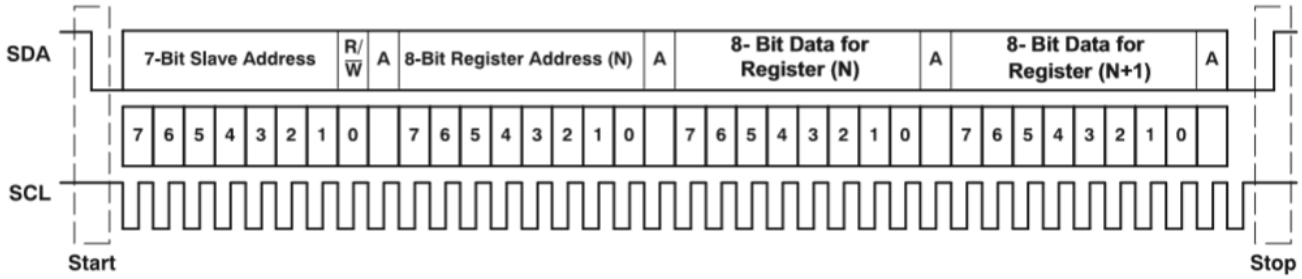


Figure 9 Typical I²C Sequence

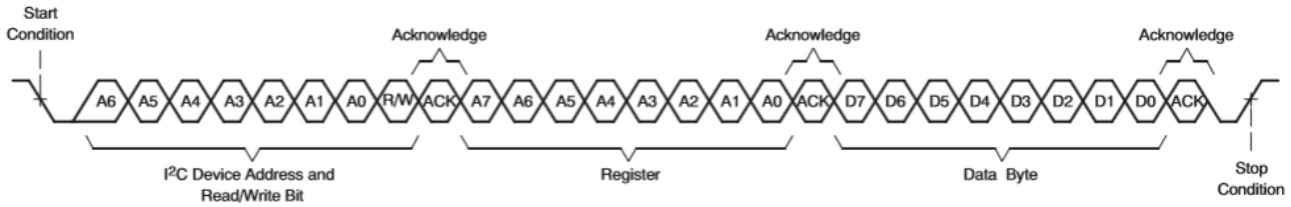


Figure 10 Single-Byte Write Transfer

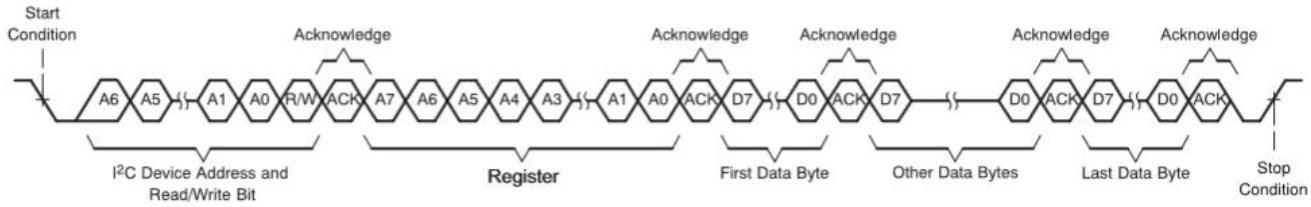


Figure 11 Multiple-Byte Write Transfer

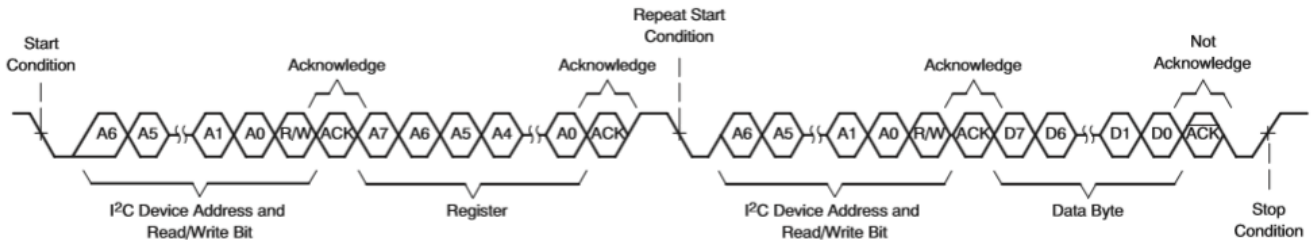


Figure 12 Single-Byte Read Transfer

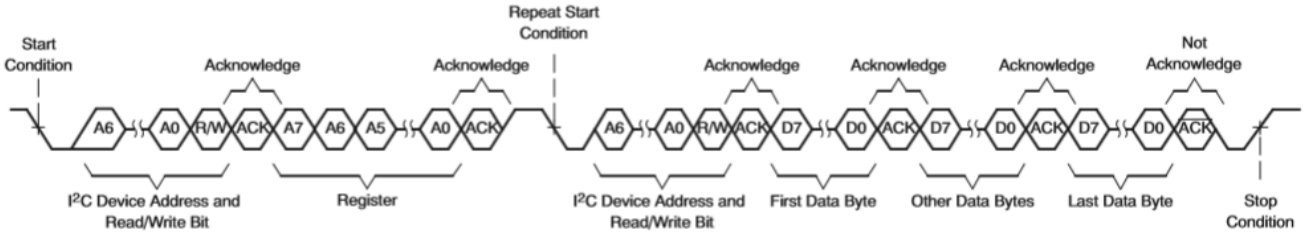


Figure 13 Multiple-Byte Read Transfer

5 *Register Map*

Table. 5 Register Map

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
0x10	Digital Clipper Level DigClip[19:12]								FFh
0x11	Digital Clipper Level DigClip[11:4]								FFh
0x12	Digital Clipper Level DigClip[3:0]				SLEEP	SD	MUTE_A	SPEED	F0h
0x13	Data Format		Word_Length		TDM_Offset	TDM_Slot			00h
0x14	HPF Byps	Left_Mix	Right_Mix	Fade	MUTE_L	MUTE_R	Digital Boost		90h
0x15	Left channel volume control								CFh
0x16	Right channel volume control								CFh
0x17	ch_Shift	Fade_Mode	SCLK_DET_EN	CLK_DET_EN	Reserved		CLK_Error	SCLK_Error	30h
0x18	Reserved	Analog Gain			PBTL	Reserved			02h
0x19	Modulation	Reserved						Gain_Group	70h

The register details are as follows. The blue fonts are the default settings when powering on.

Register Address: 0x10 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[19:12]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

Register Address: 0x11 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[11:4]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

The digital clipper level determined by DigClip[19:0] is the maximum output threshold level from DAC transferring to the analog Amplifier. The default value of the digital clipper level is the full scale of DAC output, and decreasing the value of DigClip[19:0] will decrease the digital clipper level as well.

Register Address: 0x12 (default F0h)

Bit	R/W	Label	Default	Description
7:4	R/W	DigClip[3:0]	1111	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.
3	R/W	SLEEP	0	0: the device is not in the SLEEP mode; 1: the device is in the SLEEP mode.
2	R/W	SD	0	0: the device is shut down; 1: the device is not shut down;
1	R/W	MUTE_A	0	0: The Amp output is not muted 1: The Amp output is muted
0	R/W	SPEED	0	0: Serial Audio Port will accept sample rates between 8k – 96kHz 1: Serial Audio Port will accept sample rates between 96kHz-192kHz

Register Address: 0x13 (default 00h)

Bit	R/W	Label	Default	Description
7:6	R/W	Format	00	Control the Serial Audio Port data format 00: I²S 01 : Left justified 10: Rright justified 11: TDM
5:4	R/W	Word_Length	00	Control the Serial Audio Port sample word length 00: 32bits

				01: 24 bits 10: 20bits 11: 16bits
3	R/W	TDM_Offset	0	Control the offset of TDM data in the audio frame. The offset is defined as the number of SCLK from starting (MSB) of audio frame to the starting of the desired audio sample, see Figure 5 TDM Audio Data Format. 0: offset = 0 SCLK 1: offset = 1 SCLK
2:0	R/W	TDM_Slot	000	Control the slot number of TDM data in the audio frame. The slot number is defined as Figure 5 TDM Audio Data Format. 000: Slot0_A + Slot0_B; 001: Slot1_A + Slot1_B; … 111: Slot7_A + Slot7_B;

Register Address: 0x14 (default 90h)

Bit	R/W	Label	Default	Description
7	R/W	HPF Byps	1	0: The internal high-pass filter in the digital path is bypassed 1: The internal high-pass filter in the digital path is not bypassed
6	R/W	Left_Mix	0	0: Left channel mixer is disabled 1: Left channel mixer is enabled, so that left = 1 / 2(left+right)
5	R/W	Right_Mix	0	0: Right channel mixer is disabled 1: Right channel mixer is enabled, so that right = 1 / 2(left+right)
4	R/W	Fade	1	0: Volume fading is disabled; 1: Volume fading is enabled
3	R/W	MUTE_L	0	MUTE the L channel digital output: 0: the left channel is not muted 1: the left channel is muted
2	R/W	MUTE_R	0	MUTE the R channel digital output: 0: the right channel is not muted 1: the right channel is muted
1:0	R/W	Dig Bst	00	Digital Boost setting 00: +0dB is added to the signal in the digital path 01: +6dB is added to the signal in the digital path 10: +12dB is added to the signal in the digital path 11: +18dB is added to the signal in the digital path

Register Address: 0x15 (Default CFh)

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_L	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB ……Gain decreased by 0.5dB every step 1100,1111: 0dB ……Gain decreased by 0.5dB every step 0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

Register Address: 0x16 (Default CFh)

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_R	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB ……Gain decreased by 0.5dB every step 1100,1111: 0dB ……Gain decreased by 0.5dB every step

				0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

Register Address: 0x17 (default 30h)

Bit	R/W	Label	Default	Description
7	R/W	ch_Shift	0	0: The left and right channels are shifted 1: The left and right channels are not shifted
6	R/W	Fade_Mode	0	0: The volume is fading by 0.5dB/8T_{LRCK} 1: The volume is fading by 0.5dB/T_{LRCK}
5	R/W	SCLK_DET_EN	1	SCLK error detection, such as SCLK missing detection, SCLK range detection, SCLK/LRCK detection. If error detection is enabled, once any such error is detected, the relevant error flag will change to 1. 0: SCLK error detection is disabled; 1: SCLK error detection is enabled.
4	R/W	CLK_DET_EN	1	Audio serial port clock error detection, including SCLK, MCLK, LRCK. Once any error such as missing or wrong range of these clocks is detected, the relevant error flag will change to 1. 0: CLOCK error detection is disabled; 1: CLOCK error detection is enabled.
3:2	R	Reserved	00	Unused, make it always 00
1	R	CLK_Error	0	Changes to 1 when Clock Error is detected; back to 0 when Clock Error evacuated;
0	R	SCLK_Error	0	Changes to 1 when SCLK Error is detected; back to 0 when SCLK Error evacuated;

Register Address: 0x18 (Default 02h)

Bit	R/W	Label	Default	Description	
7	R	Reserved	0	Unused, make it always 0	
6:4	R/W	A_GAIN	000	Set analog gain:	
				000: Gain0 = 20.6dB; Gain1 = 30.6dB	001: Gain0 = 19.6dB; Gan1 = 27.8dB
				010: Gain0 = 14.8dB; Gan1 = 25.8dB	011: Gain0 = 18.0dB; Gan1 = 24.1dB
				100: Gain0 = 17.3dB; Gan1 = 22.7dB	101: Gain0 = 16.6dB; Gan1 = 21.5dB
				110: Gain0 = 16.0dB; Gan1 = 20.4dB	111: Gain0 = 15.4dB; Gan1 = 19.5dB
3	R/W	PBTL	0	0: BTL mode; 1: PBTL mode.	
2:0	R	Reserved	010	Unused, make it always 010	

Register Address: 0x19 (default 70h)

Bit	R/W	Label	Default	Description
7	R/W	Modulation	0	0: BD mode; 1: 1SPW mode
6:1	R	Reserved	111000	Unused, make it always 111000
0	R/W	GAIN_Group	0	Select gain group for A_GAIN (register 0x18, bit [6:4]. 0: Gain0; 1: Gain1

6 Typical Applications

6.1 Startup Procedures

1. Configure I/O pins (ADR[1:0]);
2. \SD pin = Low;
3. Bring up power supplies (it does not matter if PVDD, AVDD or DVDD comes up first, provided the device is held in shutdown);
4. Once power supplies are stable, start MCLK, SCLK, LRCK;
5. Configure the device via the control port in the manner required by the use case; especially bit “PBTL”, “Format”.
6. Once power supplies and clocks are stable and the control port has been programmed, bring \SD pin High (if in Hardware Control Mode), or write bit “SD” (Bit 2 of Register 0x12) as 1;
7. The device is now in normal operation.

The sequence diagram is shown in Figure 14 and Table 9.

6.2 Power down Procedures

1. The device is in normal operation;
2. Fade out SDIN;
3. Pull \SD pin Low (if in Hardware Control Mode), or write bit “SD” (Bit 2 of Register 0x12) as 0;
4. The clocks can be stopped, and power supplies brought down;
5. The device is now fully shutdown and powered off.

The sequence diagram is shown in Figure 15 and Table 10.

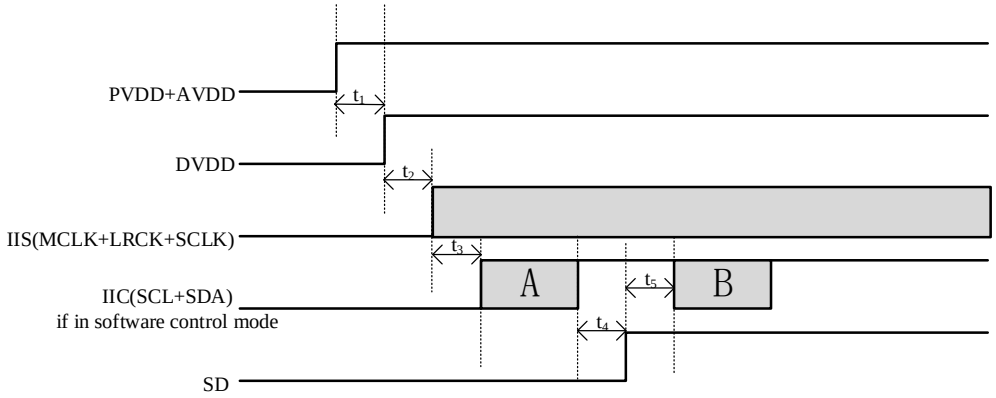


Figure 14 Power-on Sequence

Table. 6 Recommendations for Power-on Timing

Symbol	CONDITION	MIN	TYP	MAX	UNIT
t1		0			ms
t2		0			ms
t3		1			ms
t4		1			ms
t5		30			ms

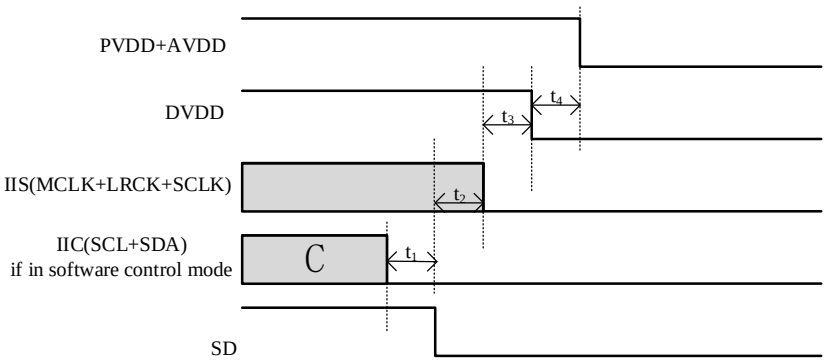
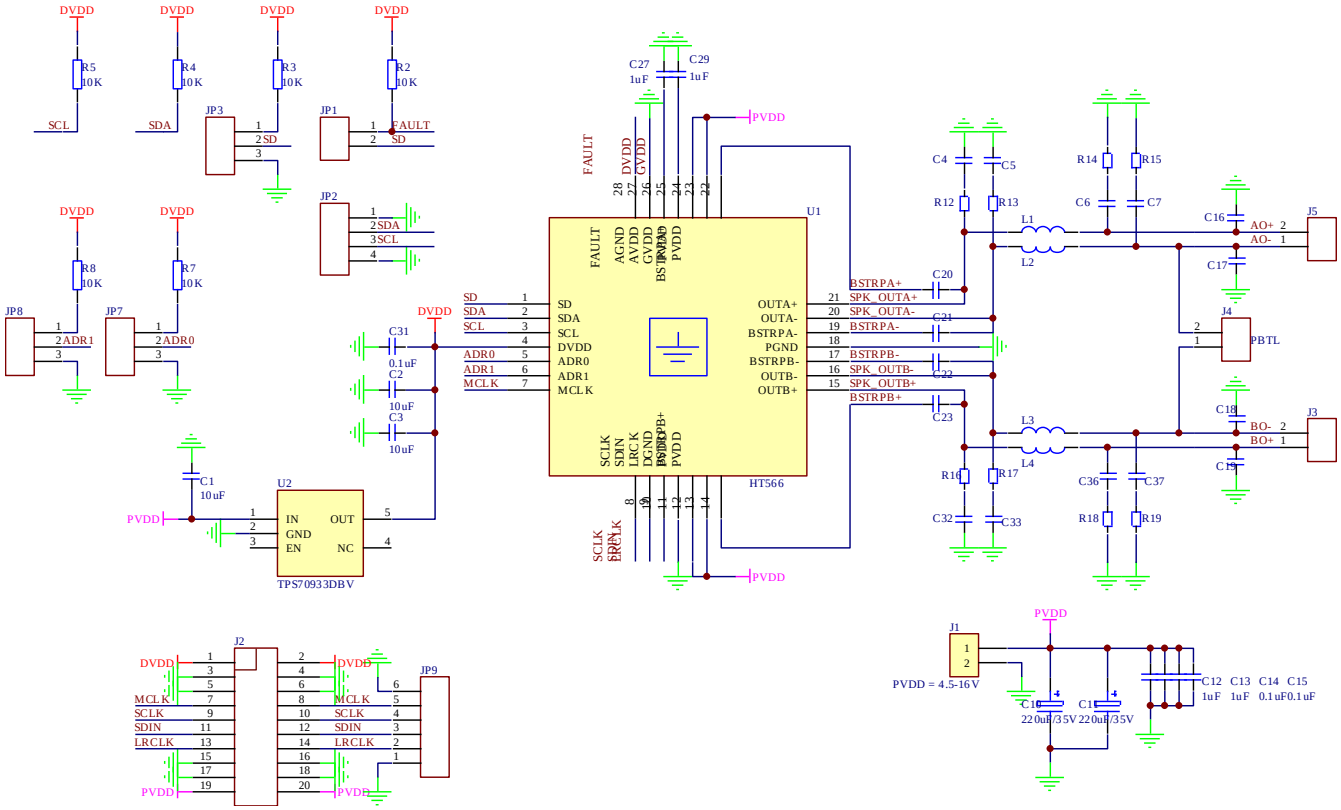


Figure 15 Power-off Sequence

Table. 7 Recommendations for Power-off Timing

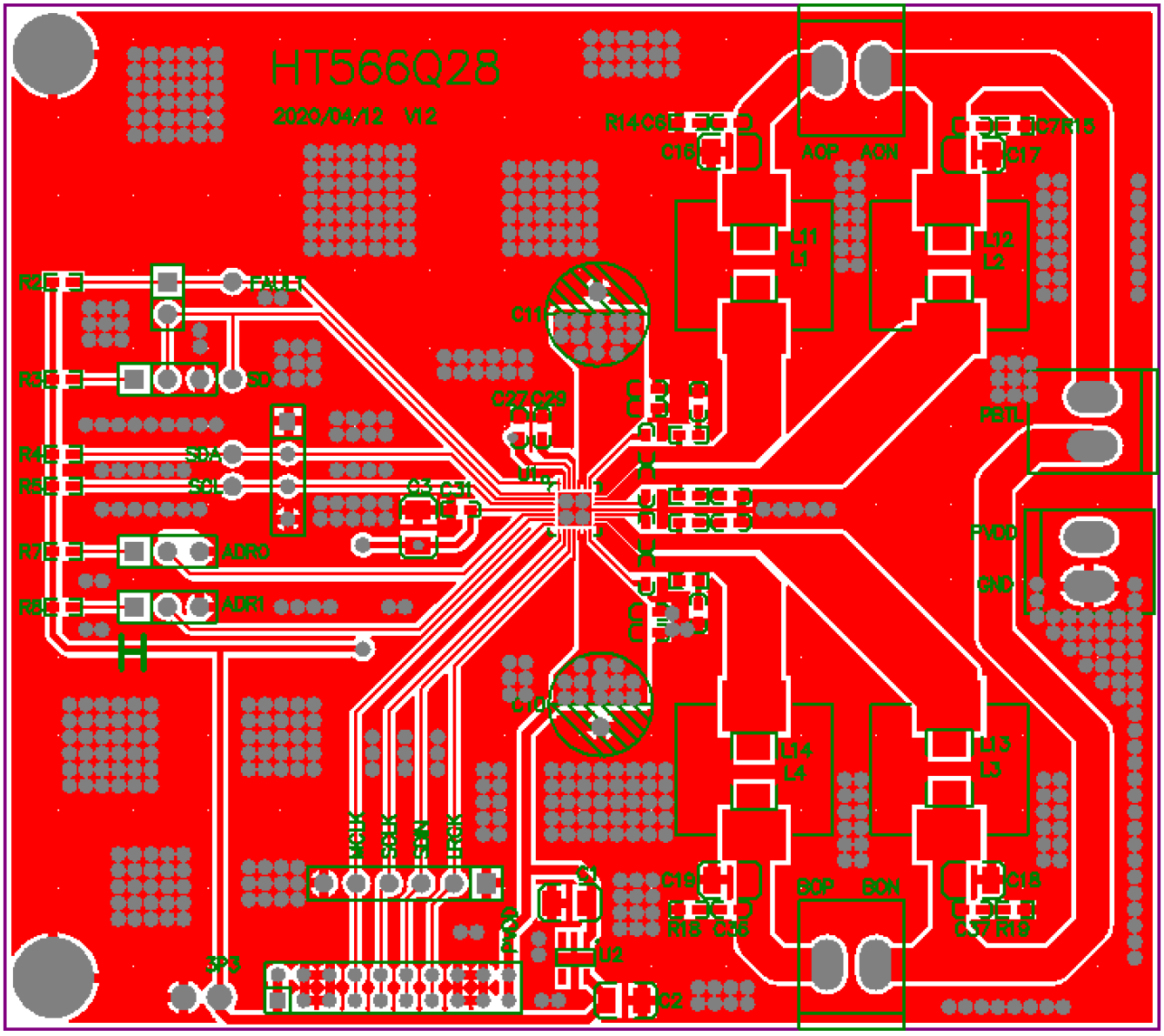
Symbol	CONDITION	MIN	TYP	MAX	UNIT
t_1		1			ms
t_2	Fade-out disabled	1			ms
	Fade-out enable	45			ms
t_3		1			ms
t_4		0			ms

6.3 Circuit Diagrams

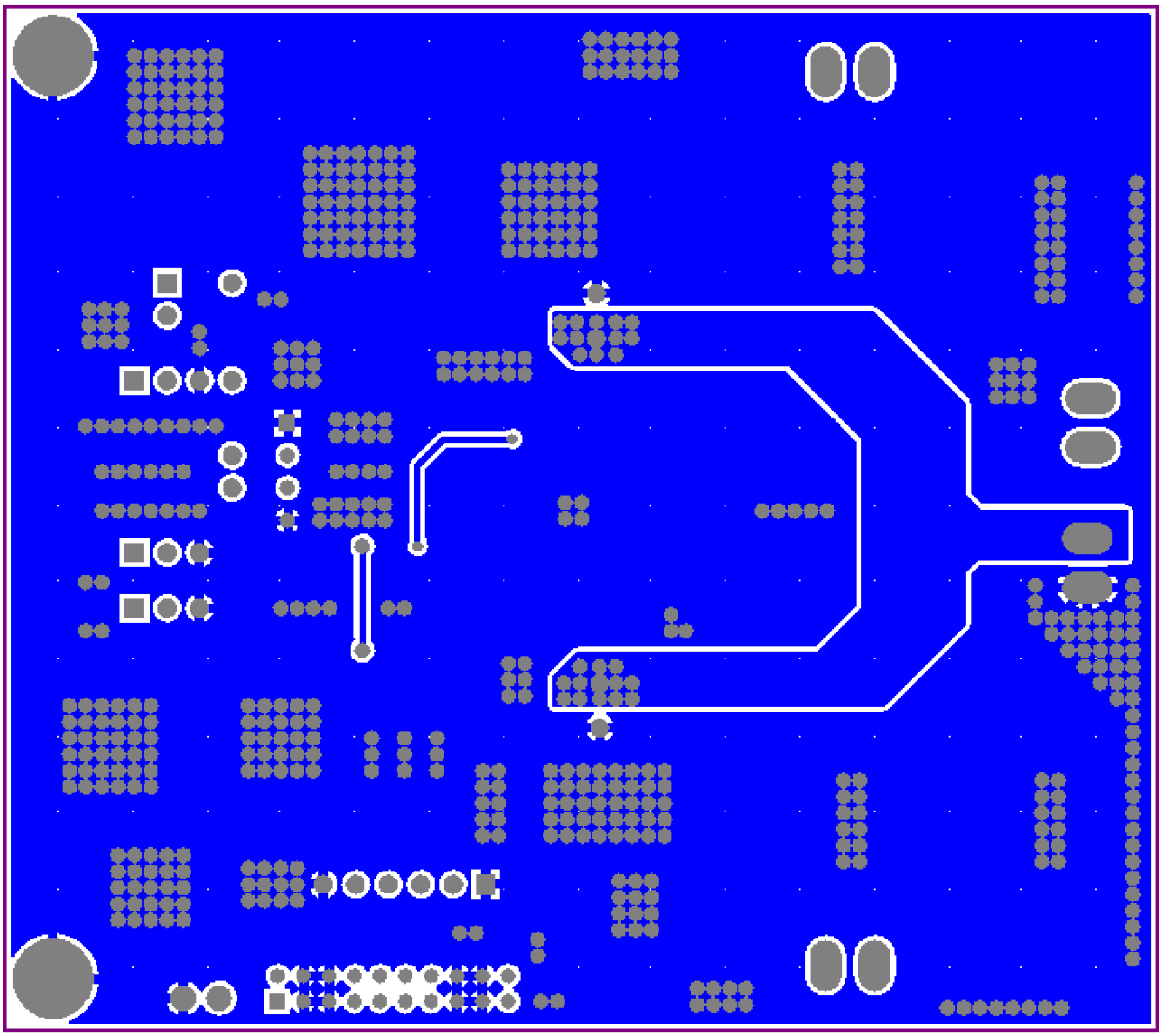


7 PCB Layout

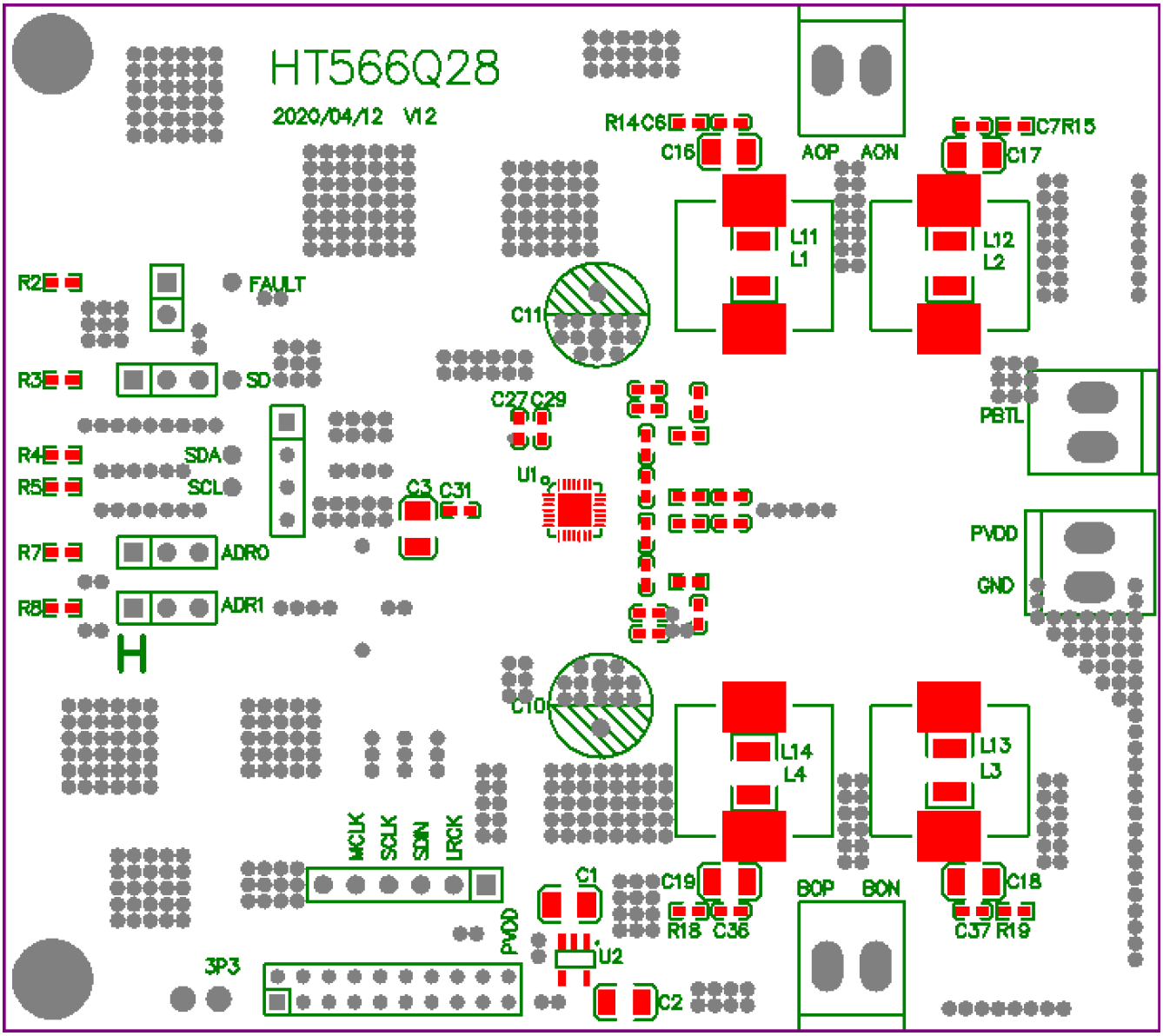
7.1 Top Layout



7.2 Bottom Layout

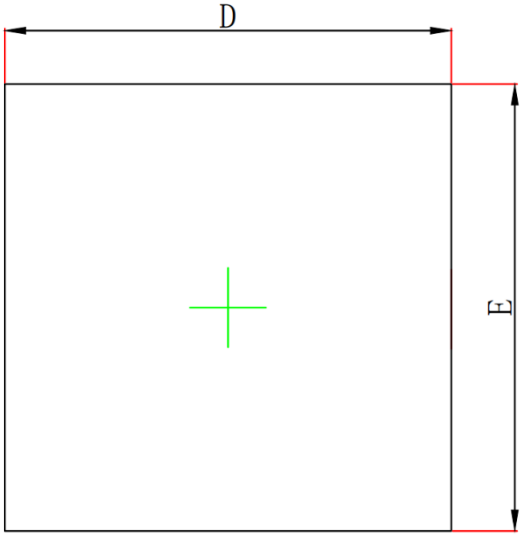


7.3 TopOverlayer

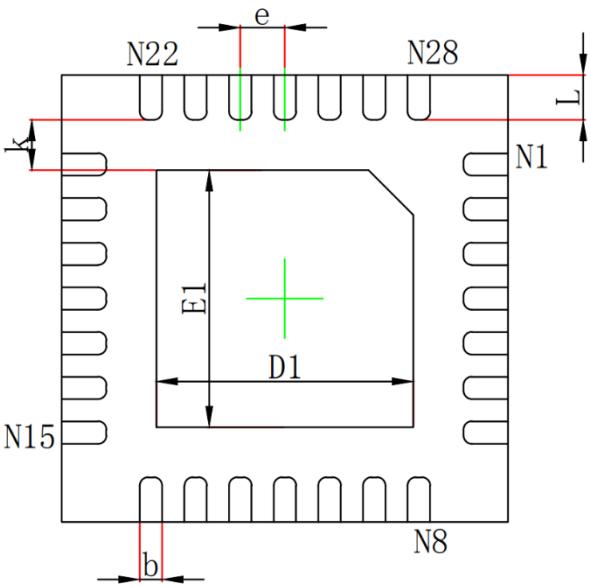


■ PACKAGE OUTLINE

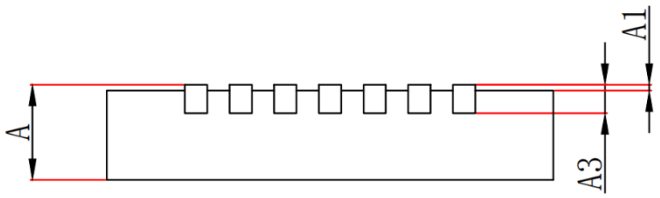
QFN28L 4*4 with exposed thermal pad



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.200	2.400	0.087	0.094
E1	2.200	2.400	0.087	0.094
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.400TYP.		0.016TYP.	
L	0.324	0.476	0.013	0.019

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