Analog-Input 24Bit, 48kHz Stereo ADC

FEATURES

- 24Bit Delta-Sigma Stereo ADC
- Differential Voltage Input: ±VDDA/3.3Vrms
- Audio Performance
  - THD+N: -88dB (Typical)
  - SNR: 89dB (PGA=30dB);
    106dB (PGA=0dB)
- Flexible PCM Audio Interface
  - Master- or Slave-Mode
  - Data Formats: 24Bit, 8-48kHz fs
  - TDM up to 16 channels
- Automatic Level Control (ALC) and noise gate
- Digital mic (PDM) available
- QFN3×3-20LPackage

APPLICATIONS

- Mic Array
- Digital TV
- Audio Speaker
- Audio Interface
- CD Recorder
- Multitrack Receiver
- Electric Musical Instrument

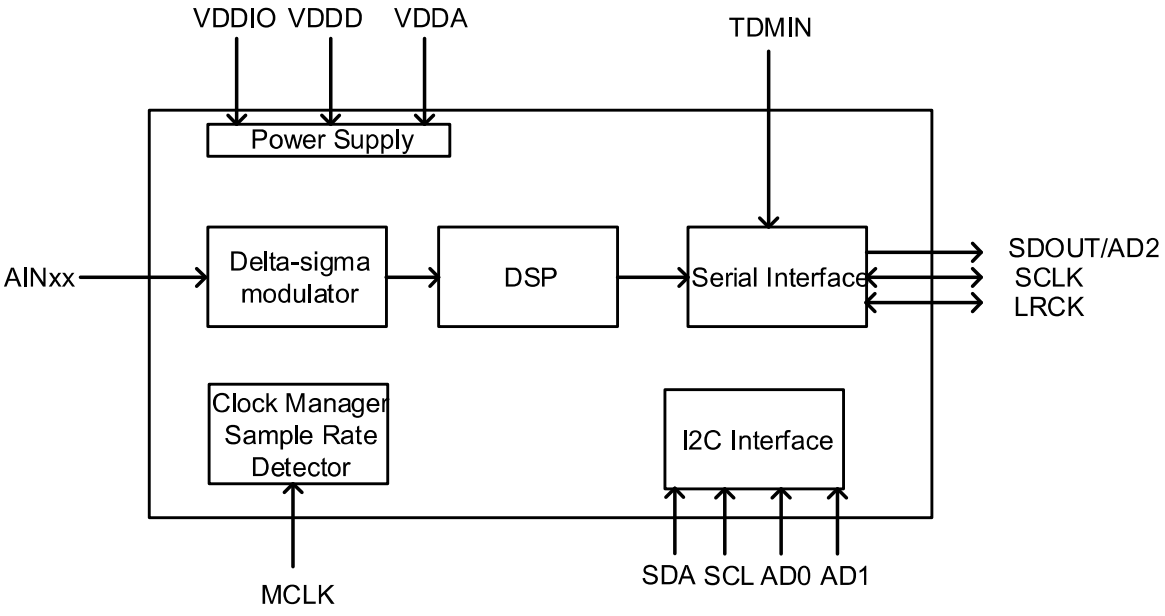
DESCRIPTION

The HT5943 device is a high-performance, low-cost, single-chip, stereo analog-to-digital converter with differential analog voltage input. Single end-ed analog input and PDM input is also supported.

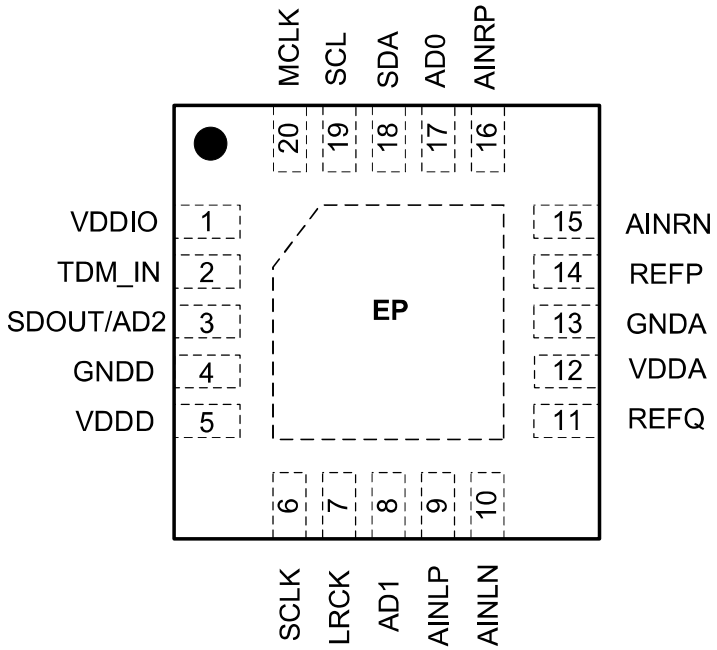
For various applications, the HT5943 device supports master and slave mode, and a variety of formats in serial audio interface, such as I^2S, left justified, DSP/PCM and TDM.

The device is available in QFN3×3-20Lpackage.

BLOCK DIAGRAM



TERMINAL CONFIGURATION



Top View

TERMINAL FUNCTION

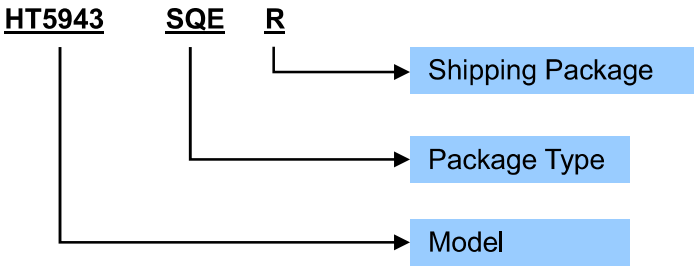
Terminal No.	NAME	I/O[1]	Description
1	VDDIO	P-	Power supply for digital input and output
2	TDM_IN	I	TDM data in
3	SDOUT/AD2	O/I	Serial data output/ device address selection AD2
4	GNDD	G	Digital GND
5	VDDD	P	Digital power supply
6	SCLK	I/O	Serial data bit-clock input or output
7	LRCK	I/O	Serial data left/right channel frame clock input or output
8	AD1	I	Device address selection AD1
9	AINLP	I	Analog positive polarity input for left channel
10	AINLN	I	Analog negative polarity input for left channel
11	REFQ	O	Reference-voltage decoupling
12	VDDA	P	Analog power supply
13	GNDA	G	Analog GND
14	REFP	O	Reference-voltage decoupling
15	AINRN	I	Analog negative polarity input for right channel
16	AINRP	I	Analog positive polarity input for right channel
17	AD0	I	Device address selection AD0
18	SDA	I/O	I^2C data
19	SCL	I	I^2Cclock
20	MCLK	I	Master clock

[1] I: input O: output G: GND P: Power

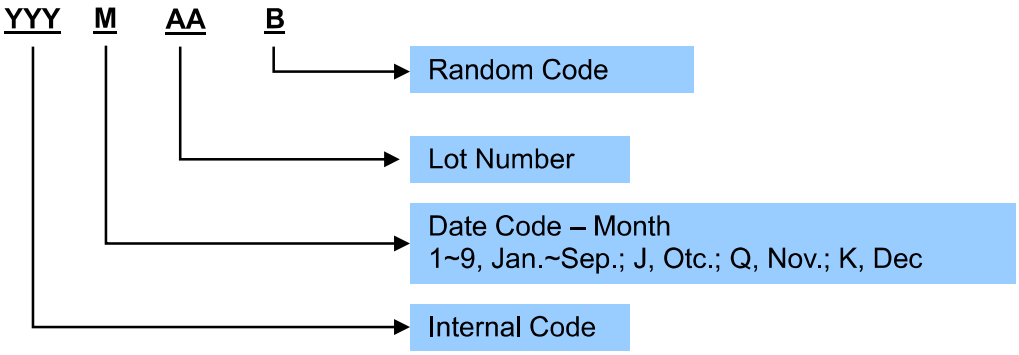
■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	Shipping Package / MOQ
HT5943SQER	QFN3×3-20L (SQE)	HT5943 YYYMAAB[1]	-40℃～85℃	Tape and Reel (R) / 5000pcs

Part Number



Production Tracking Code



[1]YYYMAAB is production tracking code

■ ELECTRICAL CHARACTERISTICS[1]

● Absolute Maximum Ratings[2]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Analog supply voltage range	VDDA	-0.3	3.6	V
Digital supply voltage range	VDDD/ VDDIO	-0.3	3.6	V
Digital input voltage	Vin	-0.3	(VDDIO+0.3)<3.6	V
Analog input voltage	Vin	-0.3	(VDDA+0.3)<3.6	V
Junction temperature range	T_J		150	℃
Storage temperature range	T_{STG}	-50	150	℃

● Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog supply voltage	VDDA	1.7	3.3	3.6	V
Digital supply voltage	VDDD/ VDDIO	1.7	3.3	3.6	V
Analog input voltage, full scale (-0dB)	Vin		±VDDA/3.3		V_{RMS}
High input logic level	V_{IH}	0.7			VDDIO
Low input logic level	V_{IL}			0.5	VDC
Digital input clock frequency, system clock		2.048		49.152	MHz
Digital input clock frequency, sampling clock		8		48	kHz
Output High-level Voltage	V_{OH}		VDDIO		
Output Low-level Voltage	V_{OL}		0		
Digital output load capacitance				20	pF
Operating ambient temperature range	T_A	-40		85	℃
Junction temperature	T_J			150	℃

● Dynamic Performance

T_A = 25°C, VDDA=VDDD=VDDIO = 3.3V, fs = 48kHz, MCLK/LRCK = 256, unlessotherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Total Harmonic Distortion + Noise	THD+N	VIN = -0.5dB, fs = 48kHz		-88		dB
Signal-to-noise ratio	SNR	fs = 48kHz, A-weighted, 30dB PGA		89		dB
		fs = 48kHz, A-weighted, 0dB PGA		106		dB
Channel separation	CS	fs = 48kHz		92		dB
Gain error				±1		%
Inter-channel Gain Mismatch				0.1		dB

[1] Depending on parts and PCB layout, characteristics may be changed.
[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability

● Analog Input

T_A = 25°C, VDDA=VDDD=VDDIO = 3.3V, fs = 48kHz, MCLK/LRCK = 256, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
REFP voltage				1.65		V
Input impedance		PGA = 0dB		20		kΩ

● Digital Filter Performance

T_A = 25°C, VDDA=VDDD=VDDIO = 3.3V, fs = 48kHz, MCLK/LRCK = 256, unlessotherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Pass band					0.454 f_S	Hz
Stop band			0.547f_S			Hz
Pass-band ripple					±0.05	dB
Stop-band attenuation			− 70			dB

● PowerCharacteristics

T_A = 25°C, VDDA=VDDD=VDDIO = 3.3V, fs = 48kHz, MCLK/LRCK = 256, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Analog supply current	I_{CC} (VDDA)	f_S = 48 kHz		6.5		mA
		Powered down		0		uA
Digital supply current	I_{DD} (VDDD+VDDIO)	f_S = 48 kHz		7.5		mA
		Powered down		0		uA

● Timing Requirements

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Serial-Clock frequency	f_{SCL}			100/400	kHz
Bus free time between a STOP and a START condition	t_{BUF}	4.7/1.3			us
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{h(STA)}$	4.0/0.6			us
Setup time for a repeated START condition	$t_{su(STA)}$	4.7/0.6			us
Setup Time for SCL to STOP condition	$t_{su(STO)}$	4.0/0.6			us
Data hold time	$t_{h(DAT)}$	0		3.45/0.9	us
Setup Time, SDA to SCL	$t_{su(DAT)}$	250/100			ns
Required Pulse Duration, SCL HIGH	t_{HIGH}	4.0/0.6			us
Required Pulse Duration, SCL LOW	t_{LOW}	4.7/1.3			us
Rise Time, SCL and SDA	t_r			1000/300	ns
Fall Time, SCL and SDA	t_f			1000/300	ns

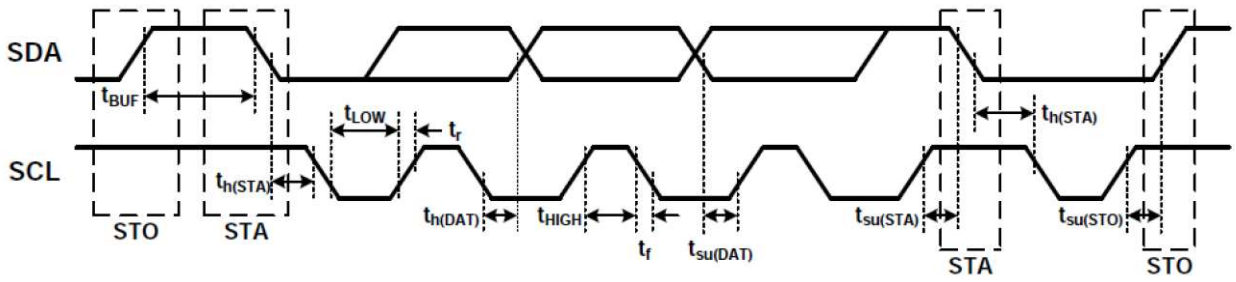


Figure 1 I²C Interface Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
MCLK frequency	f_{MCLK}			49.2	MHz
MCLK duty cycle	D_{MCLK}	40		60	%
LRCK frequency[1]	t_{LRCK}			50	kHz
LRCK duty cycle[2]	D_{LRCK}	40		60	%
SCLK frequency	f_{SCLK}			26	MHz
SCLK pulse width low	t_{SCLKL}	16			ns
SCLK Pulse width high	t_{SCLKH}	16			ns
SCLK falling to LRCK edge (master mode only)	t_{SLR}			10	ns
LRCK edge to SCLK rising	T_{LSR}	10			
SCLK falling to SDOUT valid, VDDD=3.3V	t_{SDO}		16		ns
SCLK falling to SDOUT valid, VDDD=1.8V			39		ns
LRCK edge to SDOUT valid[3], VDDD=3.3V	t_{LDO}			11	ns
LRCK edge to SDOUT valid[4], VDDD=1.8V				25	ns
TDMIN valid to SCLK rising setup time	t_{SDIS}	10			ns
SCLK rising to TDMIN hold time	T_{SDIH}	10			ns

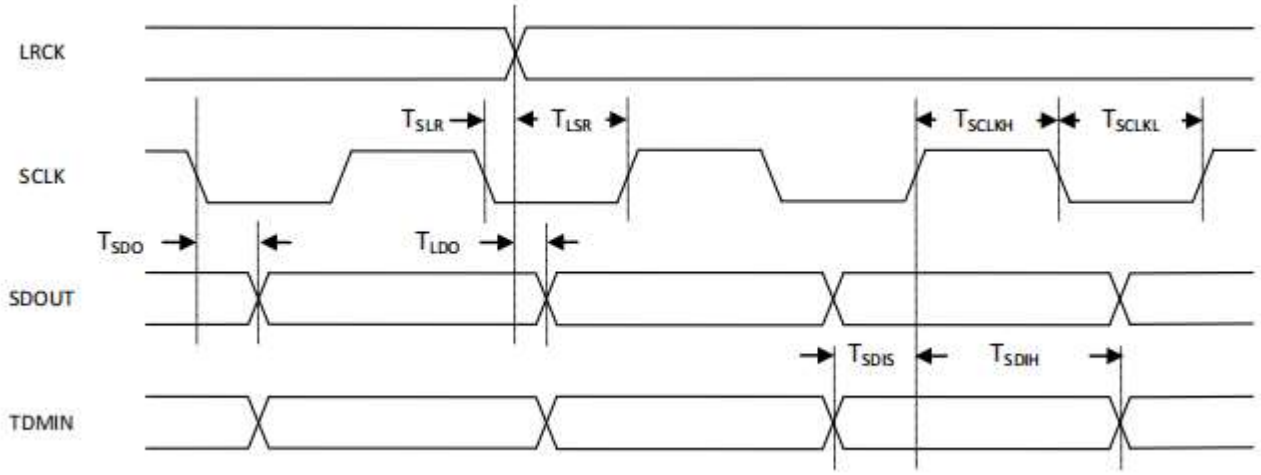


Figure 2Audio Data Interface Timing

[1]up to N*50 KHz when cascaded up to 8-ch through single I²S or TDM

[2] one SCLK period of high time in DSP/PCM modes

[3]only apply to MSB of Left Justified or DSP/PCM mode B

[4]only apply to MSB of Left Justified or DSP/PCM mode B

APPLICATION INFORMATION

The HT5943 device is a high-performance, low-cost, single-chip, stereo analog-to-digital converter with differential analog voltage input. Single end-ed analog input and PDM input is also supported.

For various applications, the HT5943 device supports master and slave mode, and a variety of formats in serial audio interface, such as I²S, left justified, DSP/PCM and TDM. In slave mode, LRCK and SCLK are provided externally and must be synchronized with the system clock in specific rates. In master mode, LRCK and SCLK are derived internally from master clock of HT5943.

The device is available in QFN3×3-20Lpackage.

1. I²C Communication

The HT5943 device has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multi-master bus environment or wait-state insertion.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus.

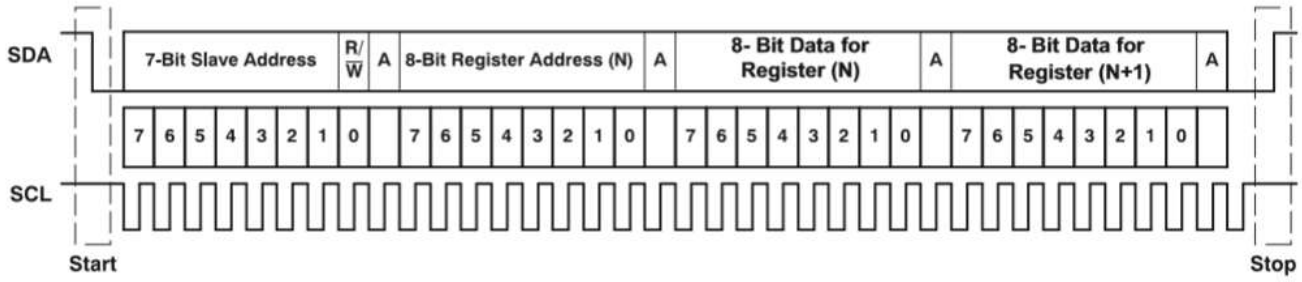


Figure 3 Typical I²C Sequence

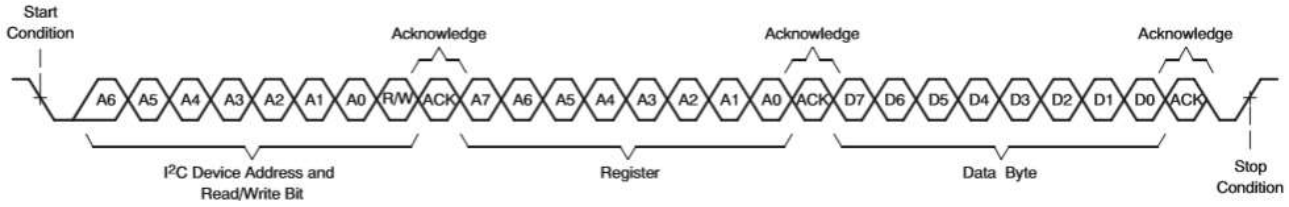


Figure 4 I²C Writing

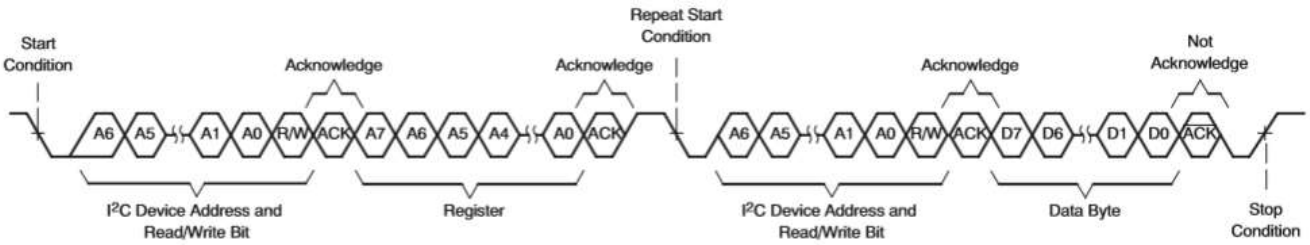


Figure 5 I²C Reading

2. *Device Address*

The device address of HT5943 can be set by AD2, AD1 and AD0 terminals, see as below.

Table1 Device Address

0	0	1	0	AD2	AD1	AD0	R/W

3. *Serial Audio Data Interface*

The serial audio data interface supports I²S, Left Justified, DSP/PCM or TDM formats.

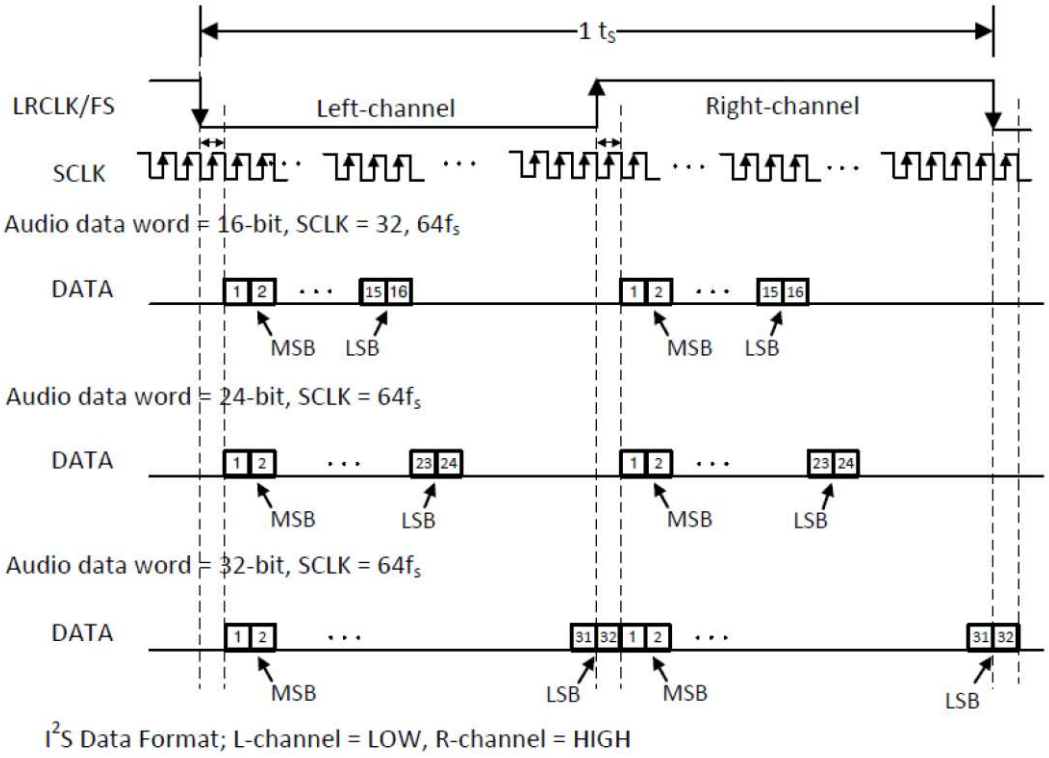


Figure 6 IIS Audio Data Format Timing

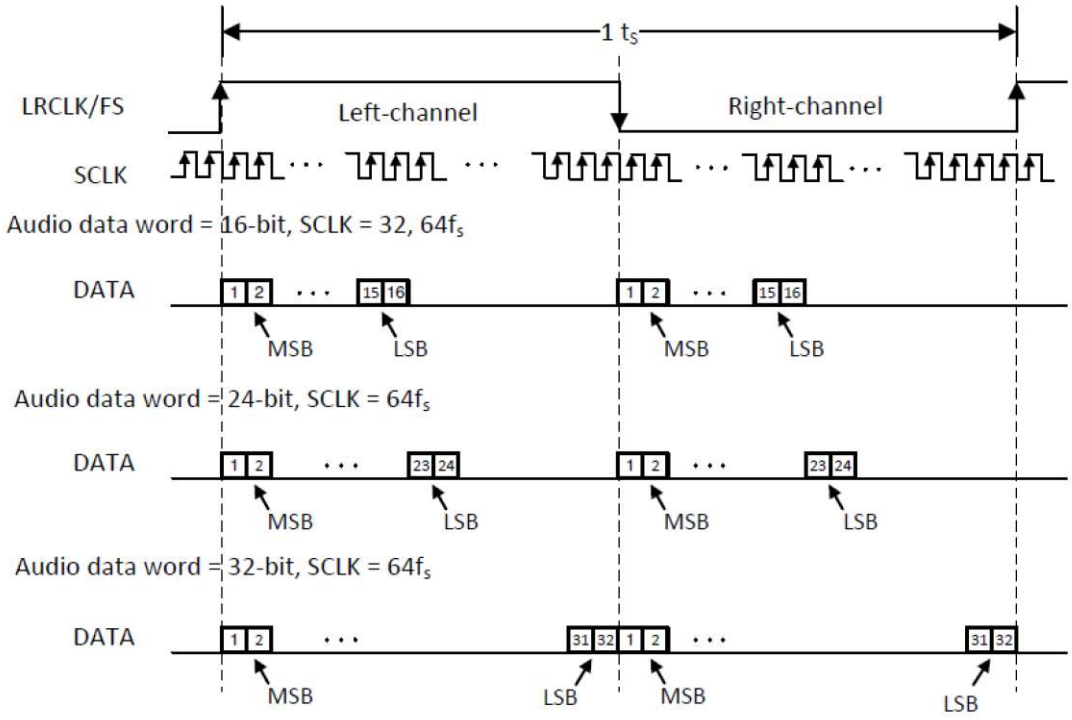


Figure 7 Left-Justified Audio Data Format Timing

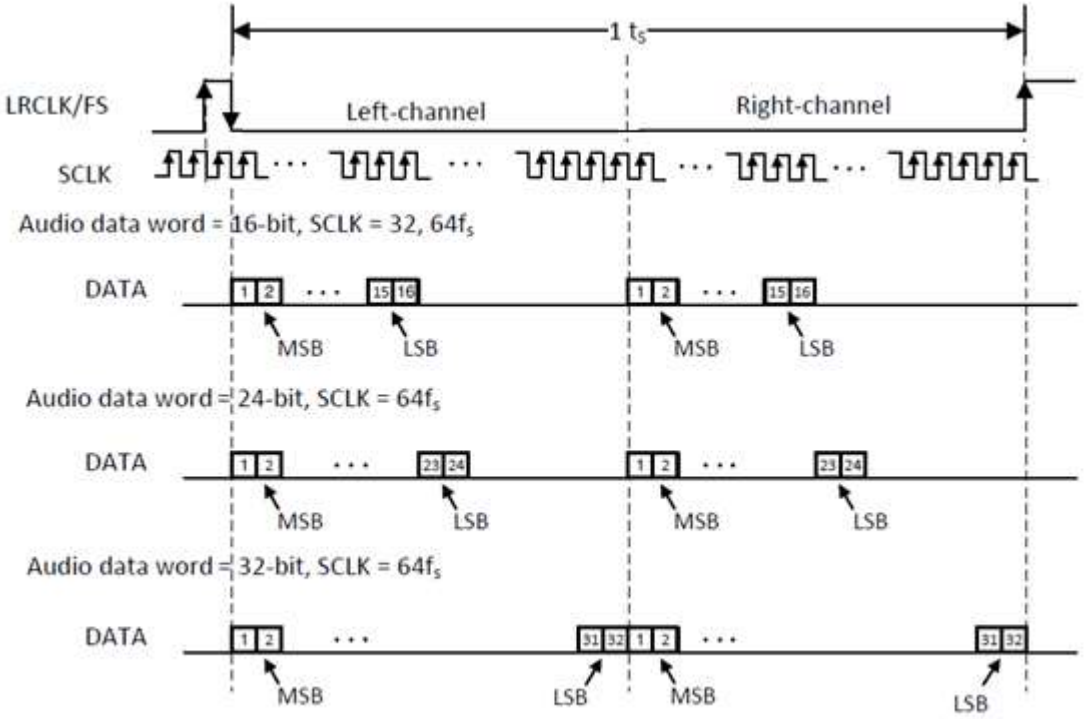


Figure 8 DSP/PCM Mode A Audio Data Format Timing

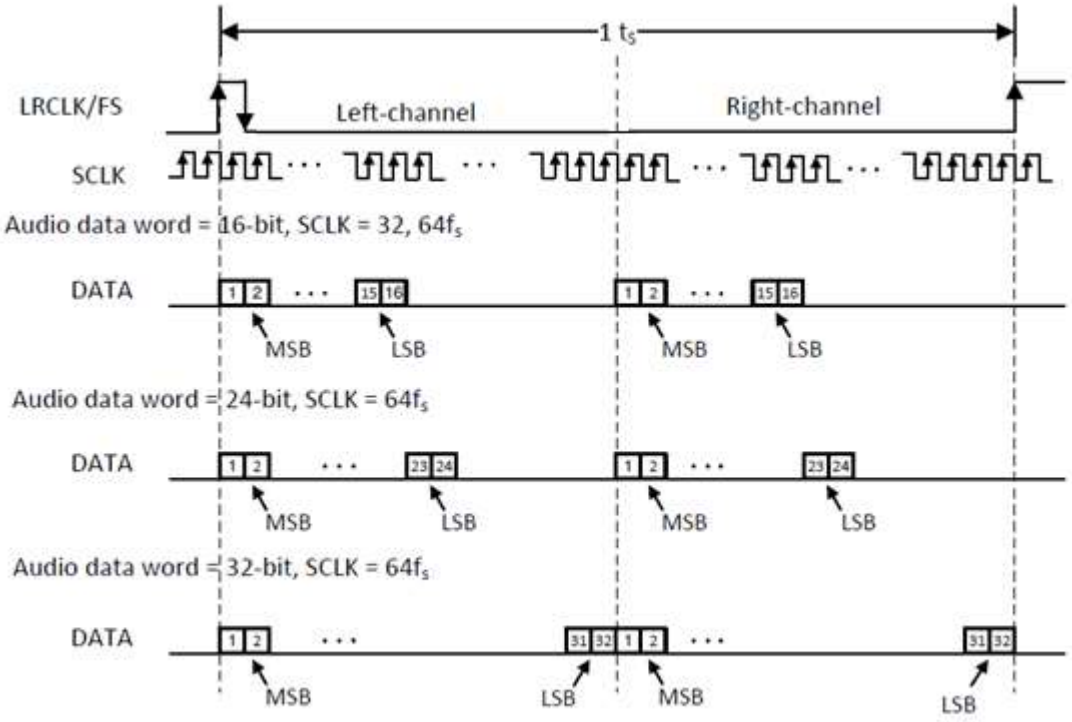


Figure 9 DSP/PCM Mode B Audio Data Format Timing

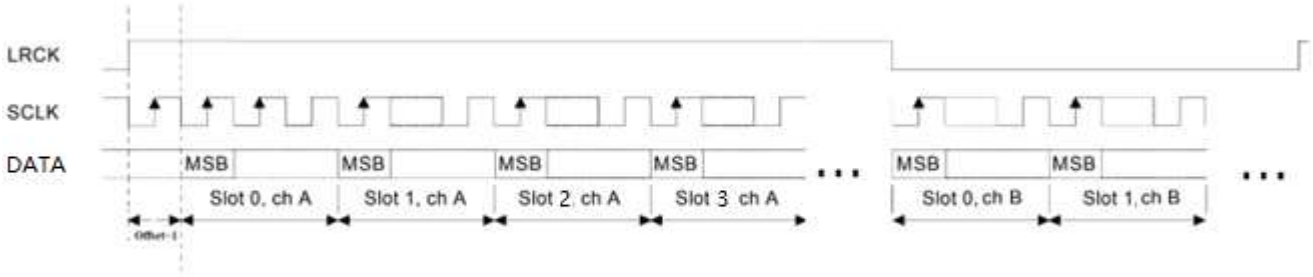


Figure 10 TDM I²SAudio Data Format Timing

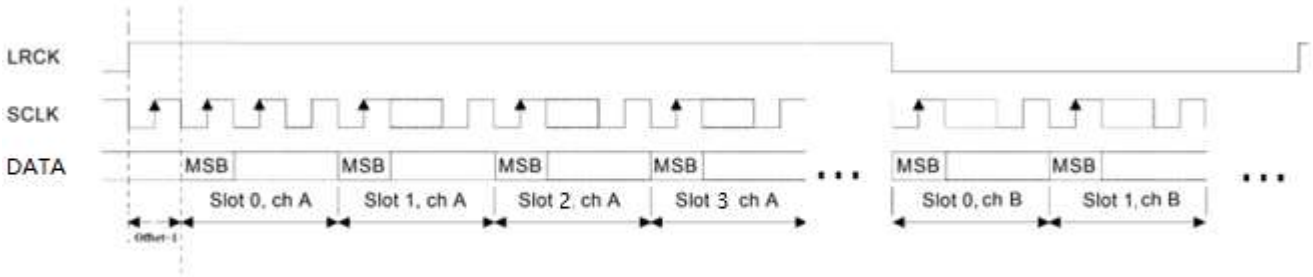


Figure 11 TDM DSP/PCM Mode A Audio Data Format Timing

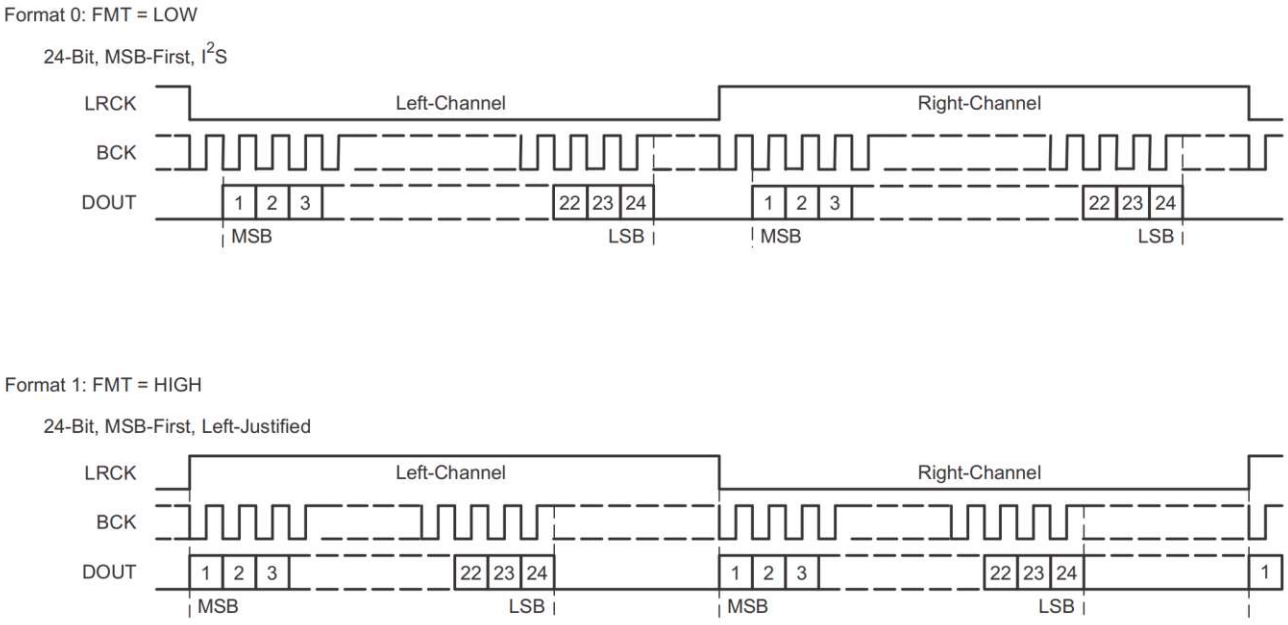


Figure 12 Audio Data Format (LRCK and BCK Work as Inputs in Slave Mode and as Outputs in Master Mode)

Typical Application

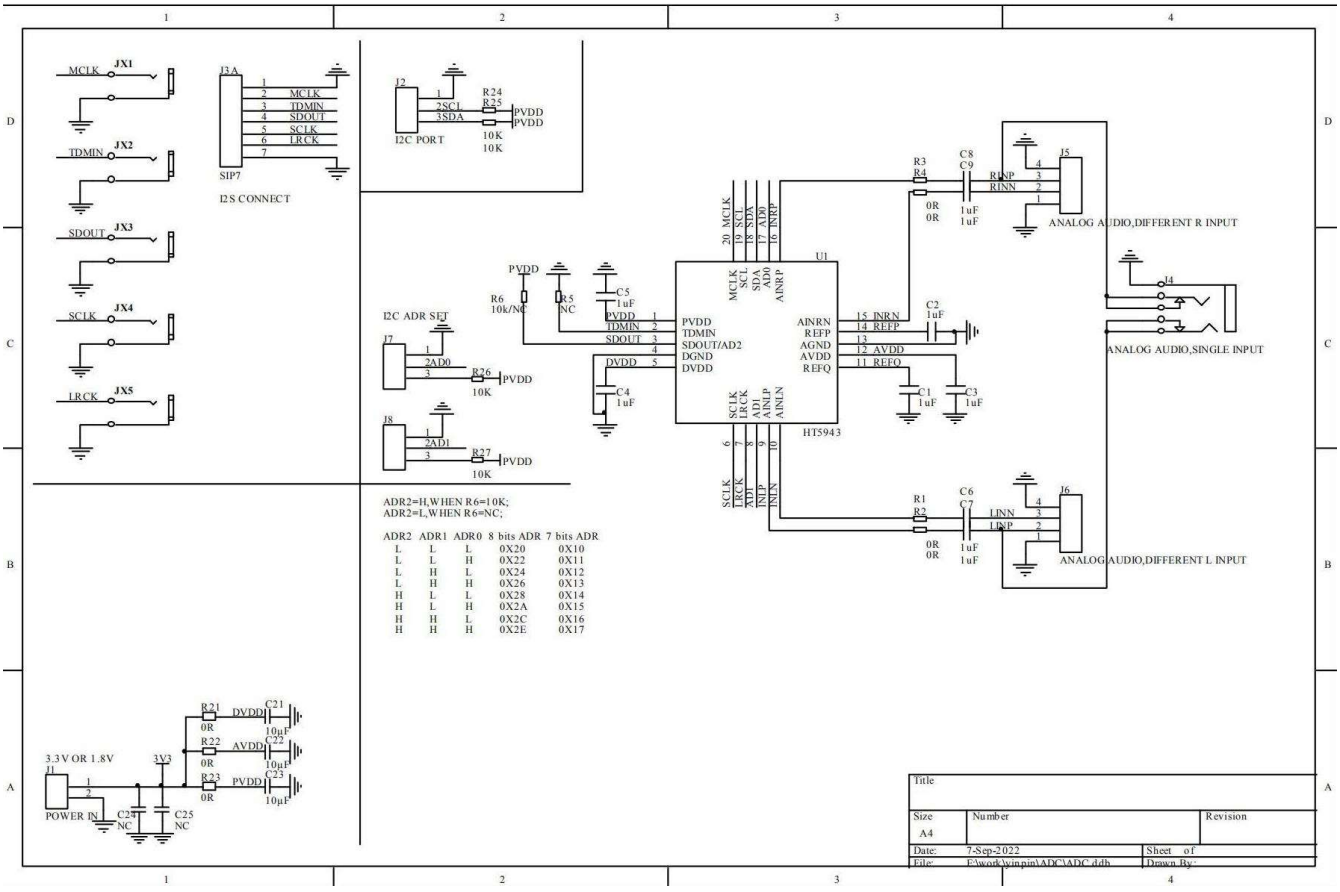


Figure 13 HT5943 Schematic Example

Register Information

REGISTER 0X00 –RESET, DEFAULT 0001 1110

Bit Name	Bit	Description
EN_CSM	7	Chip FSM control 0 - disable csm (default) 1 - enable csm
MS_SEL	6	Master/Slave select 0 - slave mode(default) 1 - master mode
ENB_SEQ	5	Power up sequence enable control 0 - power up sequence enable(default) 1 - power up sequence disable
RST_DIG	4	Digital circuits reset 0 - Not reset(default) 1 - Reset
RST_CM	3	Clock manager circuit reset 0 - Not reset (default) 1 - Reset
RST_MST	2	Master circuit reset 0 - Not reset (default) 1 - Reset
RST_ADC_DIG	1	ADC digital circuit reset 0 - Not reset (default) 1 - Reset
Reserved	0	0, do not change

REGISTER 0X01 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
Reserved	7:6	00, do not change
EN_MCLK	5	MCLK control 0 - disable MCLK(default) 1 - enable MCLK
EN_BCLK	4	BCLK control 0 - disable BCLK (default) 1 - enable BCLK
EN_CLKADC	3	Clock clk_adc control 0 - disable clk_adc (default) 1 - enable clk_adc
Reserved	2	0, do not change
EN_ANACLKADC	1	Clock anaclk_adc control 0 - disable anaclk_adc (default) 1 - enable anaclk_adc
Reserved	0	0, do not change

REGISTER 0X02 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
MCLK_SEL	7	Internal mclk select 0 - from MCLK PAD(default) 1 - from BCLK PAD
MSTBCLK_SEL	6	Master BCLK derive clocks 0 - from bclk_out[divided by DIV_BCLK](default) 1 - from anaclk_adc
MSTSRCCLK_SEL	5:4	At master mode, source clock select 00 - internal mclk(default) 01 - dig_mclk 10 - DSP_clk 11 - CF_clk
BCLK_FITBIT	2	BCLK out control when master mode 0 - continual bclk(default) 1 - master bclk stop after data transfer out
MCLK_INV	1	Internal mclk invert 0 - normal(default) 1 - invert
BCLK_INV	0	BCLK invert 0 - normal(default) 1 - BCLK invert

REGISTER 0X03 – CLOCK MANAGER, DEFAULT 0010 0000

Bit Name	Bit	Description
Reserved	7:6	00, do not change
ADC_OSR	5:0	ADC Over Sample Rate control 0~14 – reserved, do not use 15 - 60*fs 16 - 64*fs ... 31 - 124*fs 32 - 128*fs (default) ... 63 - 252*fs

REGISTER 0X04 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DIV_PRE	7:4	Pre-divided mclk Divide = DIV_PRE + 1
Reserved	3-2	00, do not change
MULT_PRE	1:0	Pre-multiplication mclk 0 - 1x(default) 1 - 2x 2 - 4x 3 - 8x

REGISTER 0X05 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DIV_CLKCF	7:4	CF clock divider Divide = DIV_CLKCF + 1
DIV_DSPCLK	3:0	DSP clock divider Divide = DIV_CLKDSP + 1

REGISTER 0X06 – CLOCK MANAGER, DEFAULT 0000 0011

Bit Name	Bit	Description
Reserved	7	0, do not change
DIV_BCLK	6:0	BCLK divider at master mode Divide = DIV_BCLK + 1

REGISTER 0X07 – CLOCK MANAGER, DEFAULT 0000 0001

Bit Name	Bit	Description
Reserved	7	0, do not change
TRI_BCLK	6	BCLK Tri-state control 0 - normal(default) 1 - Tri-state
TRI_LRCK	5	LRCK Tri-state 0 - normal(default) 1 - Tri-state
TRI_SDOUT	4	SDOUT Tri-state 0 - normal(default) 1 - Tri-state
DIV_LRCK[11:8]	3:0	Master LRCK divider bit 11 to bit 8 0~4095 - divide by 1~4096 511 - divide by 512(default)

REGISTER 0X08 – CLOCK MANAGER, DEFAULT 1111 1111

Bit Name	Bit	Description
DIV_LRCK[7:0]	7:0	Master LRCK divider bit 7 to bit 0 0~4095 - divide by 1~4096 511 - divide by 512(default)

REGISTER 0X09 – CLOCK MANAGER, DEFAULT 1100 0001

Bit Name	Bit	Description
S1_SEL	7:6	SEL S1 00 – NA 01 – default 10 – state2 11 – state3
S1_TIME	5:0	Timer for S1 For LRCK=48KHz: 0 - 21us 1 - 104us(default) 2 - 5ms … 63 - 167ms(max)

REGISTER 0X0A – SDP, DEFAULT 1000 0001

Bit Name	Bit	Description
S3_SEL	7:6	SEL S3 00 – NA 01 – default 10 – state2 11 – state3
S3_TIME	5:0	Timer for S3 For LRCK=48KHz: 0 - 21us 1 - 104us(default) 2 - 5ms … 63 - 167ms(max)

REGISTER 0X0B – SDP, DEFAULT 1100 0000

Bit Name	Bit	Description
I2S_OUT_MUTE	7:6	I2S out mute control 0 - not mute 1 - mute R channel 2 - mute L channel 3 - mute L/R channels(default)
I2S_LRP	5	I2S/Left Justify case: 0 - L/R normal polarity(default) Left/Right=High/Low (LJ) Left/Right=Low/High (I2S) 1 - L/R invert polarity Left/Right=Low/High (LJ) Left/Right=High/Low (I2S) DSP mode case: 0 - Mode A, MSB is available on 2nd SCLK rising edge after LRCK rising edge(default) 1 - Mode B, MSB is available on 1st SCLK rising edge after LRCK rising edge
I2S_WL	4:2	I2S word length 0 – 24-bit(default) 1 – 20-bit 2 – 18-bit 3 – 16-bit 4 – 32-bit others - 24-bit
I2S_FMT	1:0	I2S format - I2S(default) - LJ - reserved - DSP

REGISTER 0X0C – SDP, DEFAULT 0000 0000

Bit Name	Bit	Description
Reserved	7	0, do not change
TDM_FLAG	5:4	NFS flag at slot0/LSB 0 - no flag(default) 1 - first chip, generate flag '1' at slot0/LSB 2 - sync chip, get tdm flag '1' and sync, and send flag '1' at current slot 3 - all LSB is flag '0'
TDM_MODESEL	3:0	TDM mode selection 0 - ADC no TDM(default) 1 - 2FS 2 - 3FS 3 - 4FS 4 - 5FS 5 - 6FS 6 - 7Fs 7 - 8FS 8 - ADC + TDM shift (1FS) 9 - TDM loop other - not used

REGISTER 0X0D – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
ADC_DATAMUX	7:6	ADC data mux 0 - output L - R (default) 1 - output L - L 2 - output R - R 3 - output R - L
ADC_INV	5:4	ADC polarity inverted 0 - normal(default) 1 - ADCR invert 2 - ADCL invert 3 - ADCL/R invert
ADC_RAMCLR	3	ADC ram clear when lrck/adc_mclk active
ADC_SCALE	2:0	ADC gain scale up (normally used with ADC_OSR) 0 - 0dB (recommended when ADC_OSR=0x1C~0x20) (default) 1 - 6dB (recommended when ADC_OSR=0x18~0x1B) 2 - 12dB (recommended when ADC_OSR=0x14~0x17) 3 - 18dB (recommended when ADC_OSR=0x11~0x13) 4 - 24dB (recommended when ADC_OSR=0x10) 5 - 30dB 6 - 36dB 7 - 42dB

REGISTER 0X0E – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
ADC_VOLUME	7:0	ADC volume control 0x00 - '-95.5dB' (default) 0x01 - '-90.5dB' … 0.5dB/step 0xBE - '-0.5dB' 0xBF - '0dB' 0xC0 - '+0.5dB' … 0xFF - '+32dB' ADC_VOLUME is the maxgain when ALC on

REGISTER 0X0F – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
EN_ADCHPF	7	ADC HPF control 0 - disable(default) 1 - enable dynamic HPF
EN_ALC	6	ADC auto level control 0 - ALC disable(default) 1 - ALC enable
Reserved	5:4	00, do not change
ADCVC_RAMPRATE	3:0	ADC VC ramp rate 0 - disable (default) For LRCK=48KHz: 1 - 0.25dB/80us 2 - 0.25dB /160us 3 - 0.25dB /320us 4 - 0.25dB /640us 5 - 0.25dB /1.28ms 6 - 0.25dB /2.56ms 7 - 0.25dB /5.12ms 8 - 0.25dB /10.24ms 9 - 0.25dB /20.48ms 10 - 0.25dB /40.96ms 11 - 0.25dB /81.92ms 12 - 0.25dB /163.84ms 13 - 0.25dB /327.68ms 14 - 0.25dB /655.36ms 15 - 0.25dB /1.3s

REGISTER 0X10 – ADC CONTROL, DEFAULT 0000 0000，reserved, do not change

REGISTER 0X11 – ADC CONTROL, DEFAULT 0000 0000，reserved, do not change

REGISTER 0X12 – ADC CONTROL, DEFAULT 0000 0000，reserved, do not change

REGISTER 0X13 – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
ALC_RATE	7:4	ALC rate selection For LRCK=48KHz: 0001 - 0.25dB/40us 0010 - 0.25dB /80us 0011 - 0.25dB /160us 0100 - 0.25dB /320us 0101 - 0.25dB /640us 0110 - 0.25dB / 1.28ms 0111 - 0.25dB / 2.56ms 1000 - 0.25dB /5.12ms 1001 - 0.25dB /10.24ms 1010 - 0.25dB /20.48ms 1011 - 0.25dB /40.96ms 1100 - 0.25dB /81.92ms 1101 - 0.25dB /163.84ms 1110 - 0.25dB /327.68ms 1111 - 0.25dB /655.36ms
ALC_LEVEL	3:0	ALC target level 0000 - '-30.0dB' (default) 0001 - '-27.0dB' 0010 - '-24.0dB' 0011- '-22.0dB' 0100 - '-19.0dB' 0101 - '-17.0dB' 0110 - '-15.0dB' 0111 - '-13.5dB' 1000 - '-12.0dB' 1001 - '-10.5dB' 1010 - '-9.0 dB' 1011 - '-7.5 dB' 1100 - '-6.0 dB' 1101 - '-4.5 dB' 1110 - '-3.0 dB' 1111 - '-1.5 dB'

REGISTER 0X14 – ADC CONTROL, DEFAULT 0000 1100

Bit Name	Bit	Description
Reserved	7:5	000, do not change
ADC_HPFS1	4:0	ADCHPF stage1 coeff 0x0C (default)

REGISTER 0X15 – ADC CONTROL, DEFAULT 0000 1100

Bit Name	Bit	Description
Reserved	7:5	000, do not change
ADC_HPFS2	4:0	ADCHPF stage2 coeff 0x0C (default)

REGISTER 0X16 – ANALOG, DEFAULT 1111 1111

Bit Name	Bit	Description
ENB_ANA	7	0 – enable analog circuits 1 – disable analog circuits(default)

ENB_ANABIAS	6	0 – enable analog bias circuits 1 – disable analog bias circuits(default)
RST_MODL	5	0 – normal work(default) 1 – reset modulatorL
RST_MODR	4	0 – normal work(default) 1 – reset modulatorR
ENB_MODL	3	0 – enable analog modulatorIL 1 – disable analog modulatorL(default)
ENB_MODR	2	0 – enable analog modulatorR 1 – disable analog modulatorR(default)
ENB_PGAL	1	0 – enable analog PGAL 1 – disable analog PGAL(default)
ENB_PGAR	0	0 – enable analog PGAR 1 – disable analog PGAR(default)

REGISTER 0X17 – ANALOG, DEFAULT 0000 0000

Bit Name	Bit	Description
Reserved	7:2	0000 00, do not change
VRPCHARGE_SEL	1:0	00 - disable(default) 01 - fast charge operation 10 - normal operation 11 - faster charge operation(highest)

REGISTER 0X18 – ANALOG, DEFAULT 0010 0100

Bit Name	Bit	Description
Reserved	7:6	00, do not change
ANABIAS_SE	5:4	00 – bias setting level0, (default) 01 – bias setting level1 10 – bias setting level2 11 – bias setting level3(highest bias)
MODQCMP_SE	3:0	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X19 – ANALOG, DEFAULT 1000 1000

Bit Name	Bit	Description
PGALBIAS_SE	**7:4**	**0000 – not allowed** **0001 - bias setting level1(lowest)** **0010 - bias setting level2** **0011 - bias setting level3** **0100 - bias setting level4** **0101 - bias setting level5** **0110 - bias setting level6** **0111 - bias setting level7** **1000 - bias setting level8** **1001 - bias setting level9** **1010 - bias setting level10** **1011 - bias setting level11** **1100 - bias setting level12** **1101 - bias setting level13** **1110 - bias setting level14** **1111 - bias setting level15(highest)**
PGARBIAS_SE	**3:0**	**0000 – not allowed** **0001 - bias setting level1(lowest)** **0010 - bias setting level2** **0011 - bias setting level3** **0100 - bias setting level4** **0101 - bias setting level5** **0110 - bias setting level6** **0111 - bias setting level7** **1000 - bias setting level8** **1001 - bias setting level9** **1010 - bias setting level10** **1011 - bias setting level11** **1100 - bias setting level12** **1101 - bias setting level13** **1110 - bias setting level14** **1111 - bias setting level15(highest)**

REGISTER 0X1A – ANALOG, DEFAULT 0100 0100

Bit Name	Bit	Description
MODI1BIAS_SE	**7:4**	**0000 – not allowed** **0001 - bias setting level1(lowest)** **0010 - bias setting level2** **0011 - bias setting level3** **0100 - bias setting level4** **0101 - bias setting level5** **0110 - bias setting level6** **0111 - bias setting level7** **1000 - bias setting level8** **1001 - bias setting level9** **1010 - bias setting level10** **1011 - bias setting level11** **1100 - bias setting level12** **1101 - bias setting level13** **1110 - bias setting level14** **1111 - bias setting level15(highest)**
MODI23BIAS_SE	**3:0**	**0000 – not allowed** **0001 - bias setting level1(lowest)** **0010 - bias setting level2** **0011 - bias setting level3** **0100 - bias setting level4** **0101 - bias setting level5** **0110 - bias setting level6** **0111 - bias setting level7** **1000 - bias setting level8** **1001 - bias setting level9** **1010 - bias setting level10** **1011 - bias setting level11** **1100 - bias setting level12** **1101 - bias setting level13** **1110 - bias setting level14** **1111 - bias setting level15(highest)**

REGISTER 0X1B – ANALOG, DEFAULT 0100 0100

Bit Name	Bit	Description
MODSUMBIAS_SE	**7:4**	**0000 – not allowed** **0001 - bias setting level1(lowest)** **0010 - bias setting level2** **0011 - bias setting level3** **0100 - bias setting level4** **0101 - bias setting level5** **0110 - bias setting level6** **0111 - bias setting level7** **1000 - bias setting level8** **1001 - bias setting level9** **1010 - bias setting level10** **1011 - bias setting level11** **1100 - bias setting level12** **1101 - bias setting level13** **1110 - bias setting level14** **1111 - bias setting level15(highest)**

MODVRPBIAS_SE	3:0	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X1C – ANALOG, DEFAULT 0100 0100

Bit Name	Bit	Description
MODVRQBIAS_SE	7:4	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
MODQVFBIAS_SE	3:0	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X1D – ANALOG, DEFAULT 0000 0000

Bit Name	Bit	Description
LP_MODVRQ	7	0 – default 1 – low power
LP_MODVRQOUT	6	0 – default 1 – low power
LP_MODVRPL	5	0 – default 1 – low power
LP_MODVRPR	4	0 – default 1 – low power
LP_MODQCMPL	3	0 – default 1 – low power
LP_MODQCMPR	2	0 – default 1 – low power
LP_MODI1L	1	0 – default 1 – low power
LP_MODI1R	0	0 – default 1 – low power

REGISTER 0X1E – ANALOG, DEFAULT 0000 0101

Bit Name	Bit	Description
Reserved	7:6	00, do not change
LP_PGAL	5	0 – default 1 – low power
LP_PGAR	4	0 – default 1 – low power
LP_PGA1L	3	0 – default 1 – low power
LP_PGA1R	2	0 – default 1 – low power
LP_PGA2L	1	0 – default 1 – low power
LP_PGA2R	0	0 – default 1 – low power

REGISTER 0X1F – ANALOG, DEFAULT 0000 1100

Bit Name	Bit	Description
Reserved	7:6	00, do not change
EN_DMIC	5	0 – disable Dmic(default) 1 – enable Dmic
QVF_SEL	4	0 – default 1 – internal use
ENB_VCP	3	0 – enable internal charge pump 1 – disable(default)
VCP_SEL	2	0 – level1 1 – level2(default)
VRP_SEL	1:0	00 –'vdda/2' (default) 01 – level1 10 – level2 11 – level3

REGISTER 0X20 – ANALOG, DEFAULT 0000 0000

Bit Name	Bit	Description
Reserved	**7:5**	**000, do not change**
SELMICL	**4**	**0 – default** **1 – select MICL as PGAL input**
PGALGAIN_SEL	**3:0**	**PGA1 gain** **0000 – 0dB(default)** **0001 – 3dB** **0010 – 6dB** **0011 – 9dB** **0100 – 12dB** **0101 – 15dB** **0110 – 18dB** **0111 – 21dB** **1000 – 24dB** **1001 – 27dB** **1010 – 30dB** **1011 – 33dB** **1100 – 34.5dB** **1101 – 36dB** **1110 – 37.5dB** **1111 – 0dB**

REGISTER 0X21 – ANALOG, DEFAULT 0000 0000

Bit Name	Bit	Description
Reserved	**7:5**	**00, do not change**
SELMICR	**4**	**0 – default** **1 – select MICR as PGAR input**
PGARGAIN_SEL	**3:0**	**PGA2 gain** **0000 – 0dB(default)** **0001 – 3dB** **0010 – 6dB** **0011 – 9dB** **0100 – 12dB** **0101 – 15dB** **0110 – 18dB** **0111 – 21dB** **1000 – 24dB** **1001 – 27dB** **1010 – 30dB** **1011 – 33dB** **1100 – 34.5dB** **1101 – 36dB** **1110 – 37.5dB** **1111 – 0dB**

REGISTER 0XF7 – TEST MODE, DEFAULT 1111 0000

Bit Name	Bit	Description
PULLUP_BCLK	**7**	**BCLK pullup control** **0 - BCLK no pullup** **1 - BCLK pullup(default)**
PULLUP_LRCK	**6**	**LRCK pullup control** **0 - LRCK no pullup** **1 - LRCK pullup(default)**

PULLDN_TDMIN	5	TDMIN pulldown control 0 - TDMIN no pulldown 1 - TDMIN pulldown(default)
PULLDN_SDOUT	4	SDOUT pulldown control 0 - SDOUT no pulldown 1 - SDOUT pulldown(default)
Reserved	3	0, do not change
SDOUT_DRIVE	2	SDOUT driver select 0 - normal (default) 1 - weak
BCLK_DRIVE	1	BCLK driver select 0 - normal (default) 1 - weak
LRCK_DRIVE	0	LRCK driver select 0 - nromal (default) 1 - weak

REGISTER 0XF8 – TEST MODE, DEFAULT 0000 0000

Bit Name	Bit	Description
SDOUT_FAST	7	Internal use, do not change
PATHSEL	6	Internal use, do not change
DELYSEL	5:4	Internal use, do not change
ADC_DLY_SEL	3	Internal use, do not change
Reserved	2:0	000, do not change

REGISTER 0XF9 – TEST MODE, DEFAULT 0000 0000

Bit Name	Bit	Description
Reserved	7:1	0000 000, do not change
DLL_PWD	0	Internal use, do not change

REGISTER 0XFA – I2C CONFIGURE, DEFAULT 0000 0000

Bit Name	Bit	Description
Reserved	7:2	0000 00, do not change
I2C_RETIME	1	I2C signals retime 0 - normal(default) 1 - retime mode
RST_REG	0	Initial registers 0 - normal(default) 1 - reset registers to default

REGISTER 0XFC – FLAG, DEFAULT 0000 0000

Bit Name	Bit	Description
Reserved	7:6	00, do not change
FLAG_CSM	5:4	CSM flag, read only 00 - S0 01 - S1 10 - S2 11 - S3
Reserved	3:0	0000, do not change

REGISTER 0XFD – CHIP ID1, DEFAULT 0111 1010

Bit Name	Bit	Description
CHIP_ID1	**7:0**	**0X7A, read only**

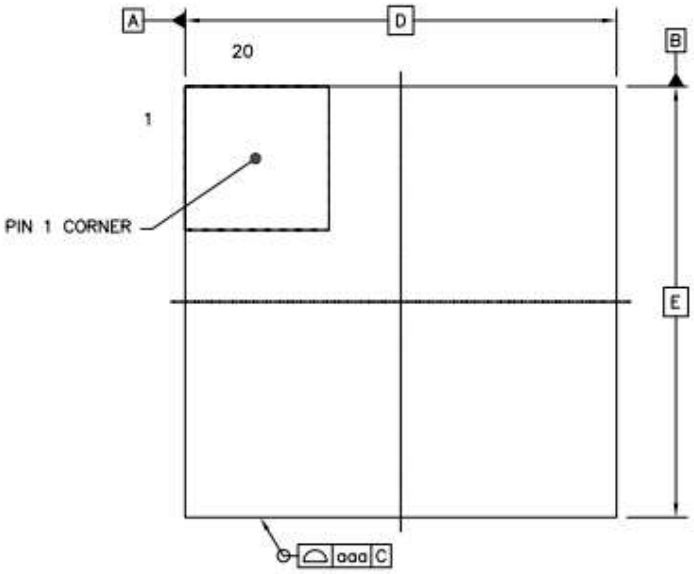
REGISTER 0XFE – CHIP ID2, DEFAULT 0100 0011

Bit Name	Bit	Description
CHIP_ID2	**7:0**	**0X43, read only**

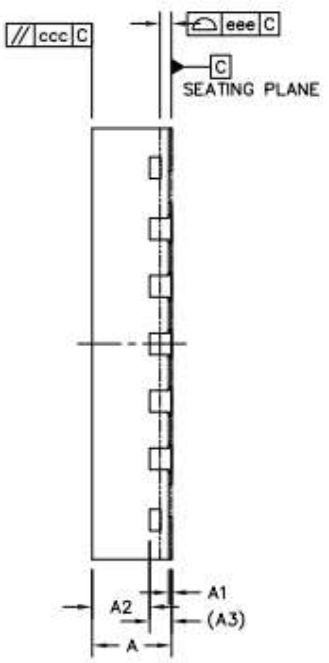
REGISTER 0XFF – CHIP VERSION, DEFAULT 0000 0000

Bit Name	Bit	Description
CHIP_VER	**7:0**	**0X00, read only**

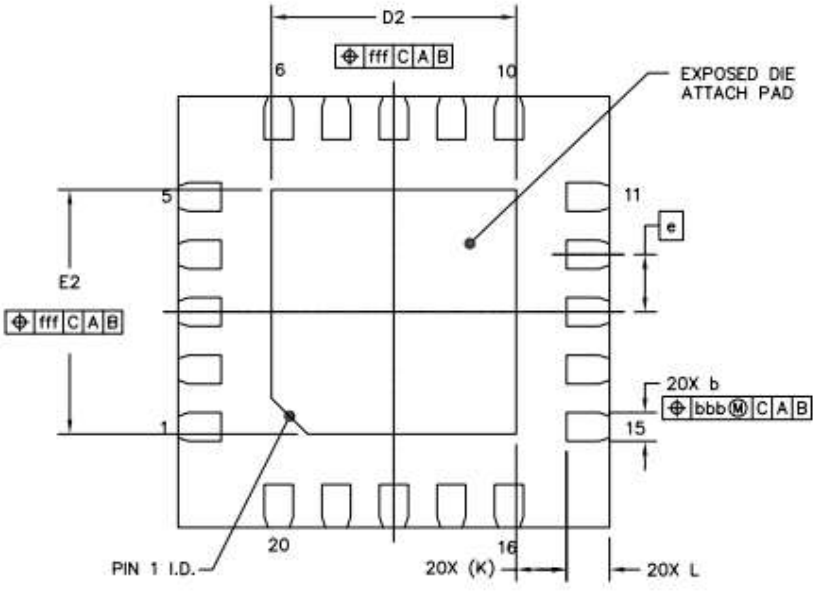
■ PACKAGE OUTLINE



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions in Millimeters		
	Min.	NOM	Max.
A	0.5	0.55	0.6
A1	0	0.02	0.05
A2	-	0.4	-
A3	0.152 REF		
b	0.15	0.2	0.25
D	3 BSC		
E	3 BSC		
e	0.4 BSC		
D2	1.6	1.7	1.8
E2	1.6	1.7	1.8
L	0.25	0.3	0.35
K	0.35REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		