HT6264-70
CMOS 8K×8-Bit SRAM

Features

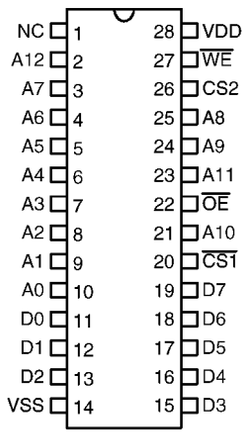
- Single 5V power supply
- Low power consumption
  - Operating: 200mW (Typ.)
  - Standby: 5μW (Typ.)
- 70ns (Max.) high speed access time
- Memory expansion by pin $\overline{OE}$
- Common I/O using tri-state outputs
- TTL compatible interface levels
- Fully static operation
- Pin-compatible with standard 8K×8 bits of EPROM/MASK ROM
- 28-pin DIP/SDIP/SOP package

General Description

The HT6264-70 is a 65,536-bit static random access memory organized as 8192 words by 8 bits and operates from a single 5-volt power supply. It is built with HOLTEK's high performance CMOS 0.8μm SPDM process.

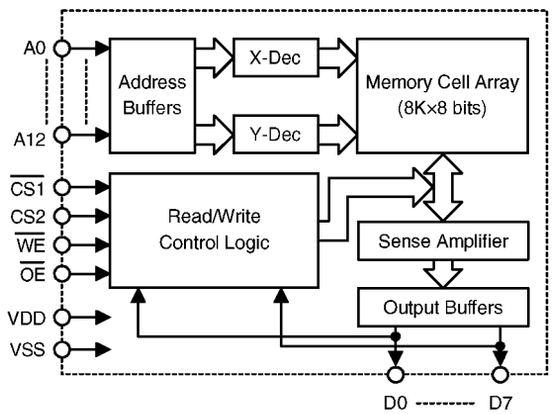
Six-transistor full COMS memory cell provides low standby current and high-reliability. Inputs and tri-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Pin Assignment



HT6264-70
– 28 DIP/SDIP/SOP

Block Diagram



Pin Description

Pin No.	Pin Name	I/O	Description
10~3, 25, 24, 21, 23, 2	A0~A12	I	Address input pins
11~13, 15~19	D0~D2, D3~D7	I/O	Data input and output signal pins
26, 20	CS2, $\overline{CS1}$	I	Chip select signal pin
22	$\overline{OE}$	I	Output enable signal pin
27	$\overline{WE}$	I	Write enable signal pin
28	VDD	I	Positive power supply pin
14	GND	I	Negative power supply pin
1	NC		No connection

Absolute Maximum Ratings*

VDD to GND .....–0.3V to +7.0V

IN, IN/OUT Voltage to GND, V_T.....–0.3V to V_{CC}+0.5V

Operating Temperature, T_{opr}.....–40°C to +85°C

Storage Temperature (Plastic), T_{stg}.....–55°C to +125°C

Temperature Under Bias, T_{bias}.....–10°C to +85°C

Power Dissipation, P_T 1.0W

* Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(VDD=5V±10%, GND=0V, Ta=–40°C to 85°C)

Symbol	Parameter		Min.	Typ.*	Max.	Unit
V_{DD}	Operating Voltage	—	4.5	5.0	5.5	V
I_{DD1}	Operating Current	T_{CYC}=Min. Cycle, I_{OUT}=0mA	—	—	45	mA
I_{DD2}		T_{CYC}=1μs, I_{OUT}=0mA	—	—	15	mA
I_{SB1}	Standby Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	—	—	10	mA
I_{SB2}		$\overline{CS1}$=CS2>=V_{DD}–0.2V, V_{IN}>=V_{DD}–0.2V or V_{IN}<=0.2V	—	—	50	μA
V_{OH}	Output High Voltage	I_{OH}=–1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=4mA	—	—	0.4	V

Symbol	Parameter		Min.	Typ.*	Max.	Unit
V_{IH}	Input High Voltage	—	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	—	–0.3	—	0.8	V
I_{LI}	Input Leakage Current	V_{DD}=5.5V, V_{IN}=GND to V_{DD}	—	—	1	μA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=GND to V_{DD}	—	—	1	μA

*V_{DD}=5V, Ta=25°C

A.C. Characteristics

Read cycle (V_{DD}=5V±10%, Ta=–40°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	70	—	—	ns
t_{AA}	Address Access Time	—	—	70	ns
t_{ACS}	Chip Selection Access Time	—	—	70	ns
t_{OE}	Output Enabled to Outputs Valid	—	—	40	ns
t_{OH}	Outputs Hold from Address Change	5	—	—	ns
t_{CLZ}	Chip select to Outputs in Low-Z	10	—	—	ns
t_{OLZ}	Output Enabled to Outputs in Low-Z	10	—	—	ns
t_{CHZ}	Chip Disabled to Outputs in High-Z	0	—	30	ns
t_{OHZ}	Output Disabled to Outputs in High-Z	0	—	30	ns

Notes: 1. A read occurs during the overlap of a low $\overline{CS1}$, a high CS2, a low $\overline{OE}$, and a high $\overline{WE}$.
2. t_{CLZ} is specified from $\overline{CS1}$ or CS2 whichever occurs last.
3. t_{CHZ} is specified from $\overline{CS1}$ or CS2 whichever occurs first.
4. t_{CHZ} and t_{OHZ} are specified by the time when DATA OUT is floating

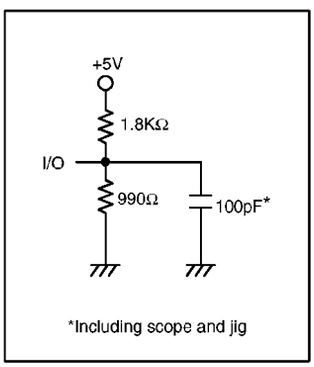
Write cycle (V_{DD}=5V±10%, Ta=–40°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WC}	Write Cycle Time	70	—	—	ns
t_{CW}	Chip Select to End of Write	35	—	—	ns
t_{AW}	Address Valid to End of Write	50	—	—	ns
t_{AS}	Address Setup Time	0	—	—	ns
t_{WP}	Write Pulse Width	25	—	—	ns
t_{WR}	Write Recovery Time	0	—	—	ns
t_{DW}	Data to Write Time Overlap	20	—	—	ns
t_{DH}	Data Hold from Write Time	0	—	—	ns
t_{OW}	Outputs Active from End of Write	5	—	—	ns
t_{OHZ}	Outputs Disable to Outputs in High-Z	0	—	40	ns
t_{WHZ}	Write to Outputs in High-Z	0	—	50	ns

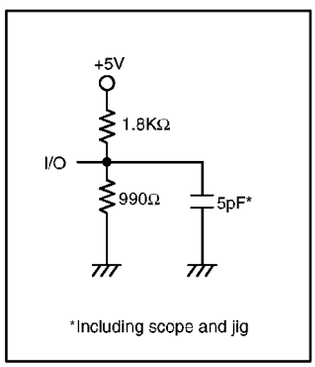
Notes: 1. A write cycle occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a write cycle.
3. t_{AS} is specified from $\overline{CS1}$, CS2, or $\overline{WE}$, whichever occurs last.
4. t_{WP} is an overlap time of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$.
5. t_{WR}, t_{DW} and t_{DH} is specified from $\overline{CS1}$, CS2, or $\overline{WE}$, whichever occurs first.
6. t_{WHZ} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are data output mode, don't force inverse signals to those pins.

A.C. Test Conditions

Item	Condition
Input Pluse Levels	0V to 3.0V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures below



Output Load



Output Load for
t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW}

Operation Truth Table

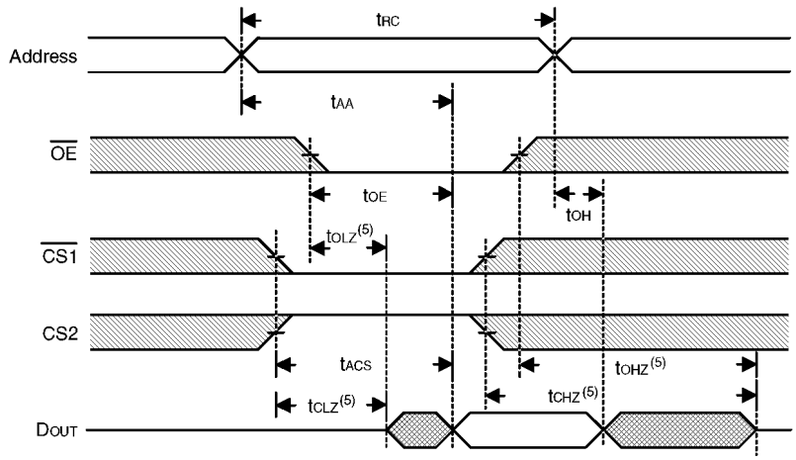
All relations between $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$ and CS2 can be described as the following truth table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	D0~D7
H X	X* L	X X	X X	Standby	High-Z
L	H	L	H	Read	Dout
L	H	H	H	Read	High-Z
L	H	X	L	Write	Din

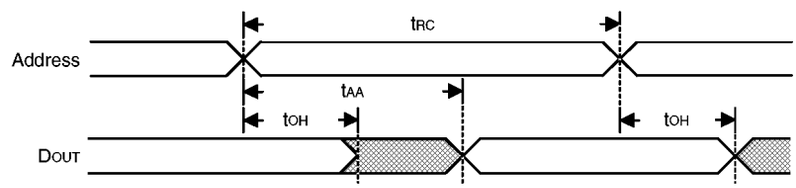
*X: Don't Care, Logical High or Low

Timing Diagrams

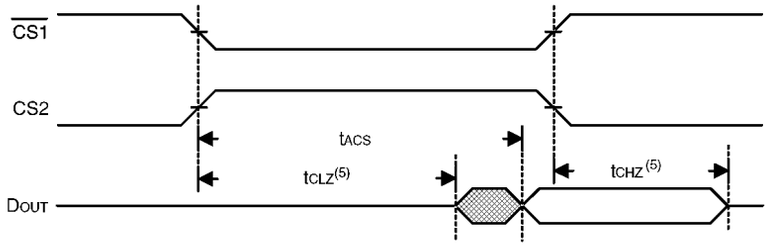
Read cycle 1(1)



Read cycle 2(1, 2, 4)

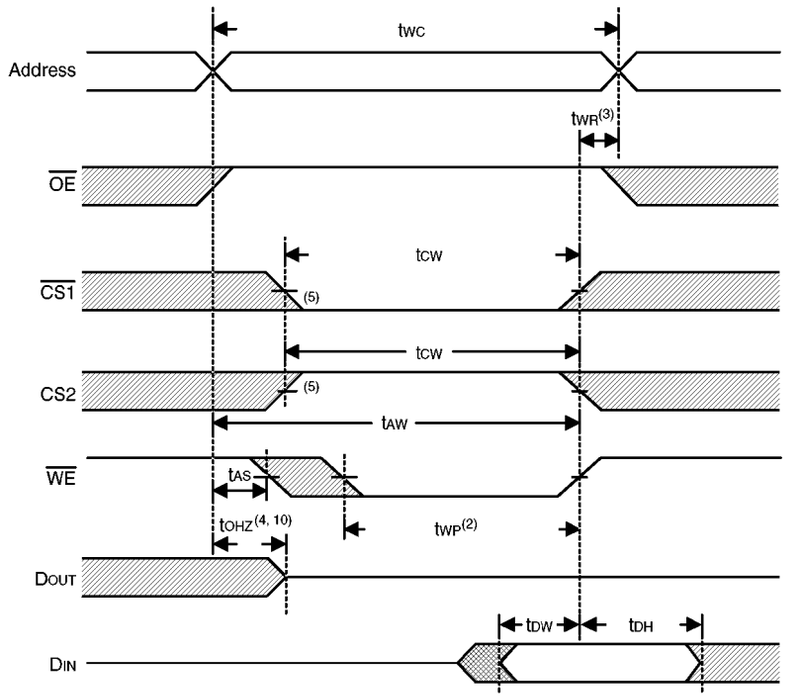


Read cycle 3(1, 3, 4)

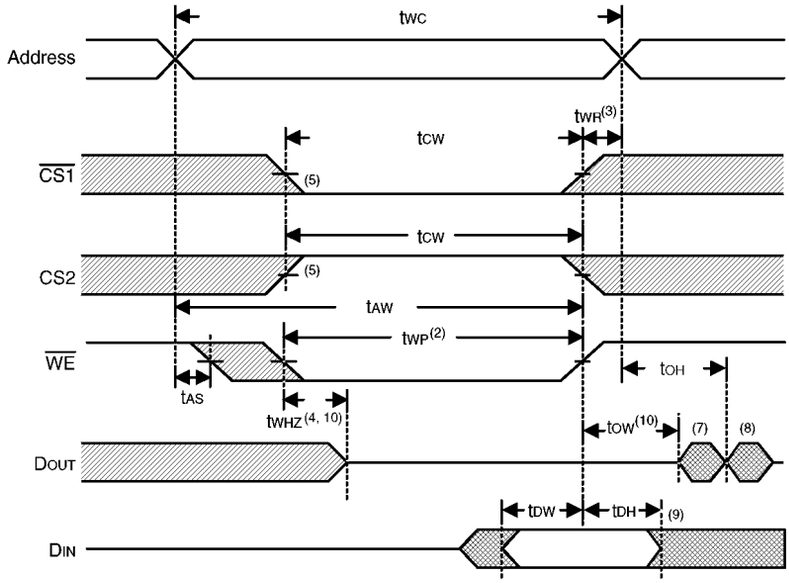


Notes:
1. $\overline{WE}$ is High for Read Cycle
2. Device is continuously enabled, $\overline{CS1}$=V_{IL} & CS2=V_{IH}
3. Address valid prior to or coincident with $\overline{CS1}$ transition low & CS2 transition high
4. $\overline{OE}$=V_{IL}
5. Transition is measured ± 500mV from steady state

Write cycle 1(1)



Write cycle 2[1, 6]



Notes:
1. $\overline{WE}$ must be high during all address transitions
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$
3. t_{WR} is measured from the earlier of $\overline{CS1}$ or $\overline{WE}$ going high and CS2 going low to the end of write cycle
4. During this period, I/O pins are in the output state so the input signals of oppsite phase to the outputs must not be applied
5. If the $\overline{CS1}$ low transition (or CS2 high transition) occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state
6. $\overline{OE}$ is continuously low ($\overline{OE}$=V_{IL})
7. D_{OUT} is the same phase of write data of this write cycle
8. D_{OUT} is the read data of next address
9. If $\overline{CS1}$ is low (or CS2 is high) during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them
10. Transition is measured ±500mV from steady state

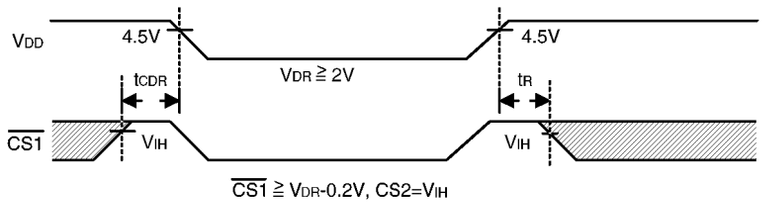
Data Rentention Characteristics

(Ta=–40°C to 85°C)

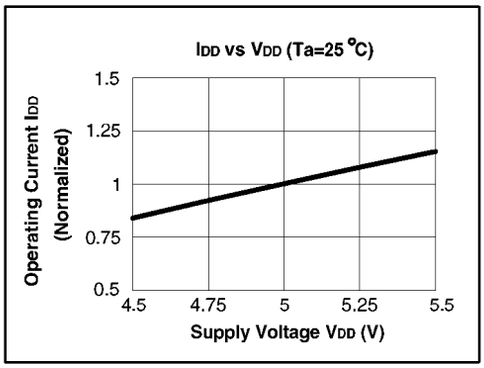
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{CS1}$=CS2≥V_{DD}–0.2V	2	5.5	V
I_{CCDR}	Data Retention Current	V_{DD}=3V, $\overline{CS1}$=CS2≥V_{DD}–0.2V V_{IN}≥V_{DD}–0.2V or V_{IN}≤0.2V	—	50	μA
t_{CDR}	Chip Disable Data Retention Time	See Retention Timing	0	—	ns
t_R	Operation Recovery Time	See Retention Timing	t_{RC}*	—	ns

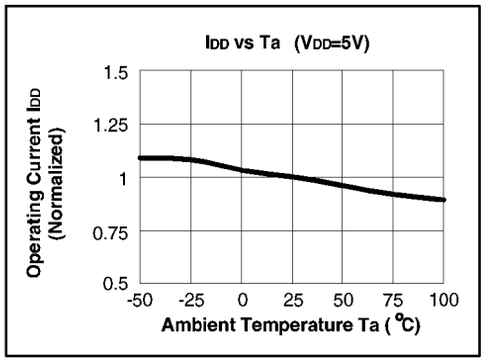
*t_{RC}=Read Cycle Time

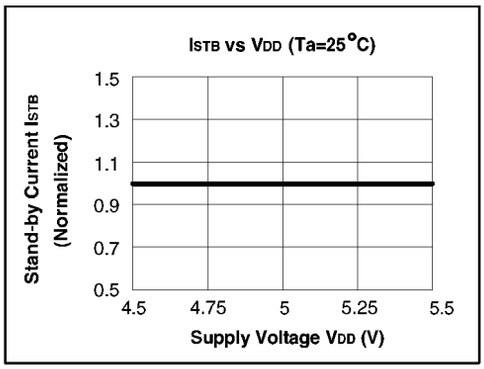
Low V_{DD} Data Retention Timing

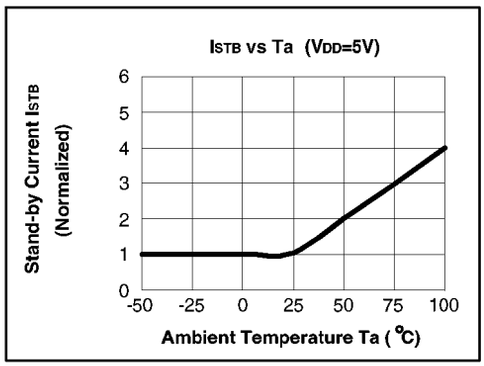


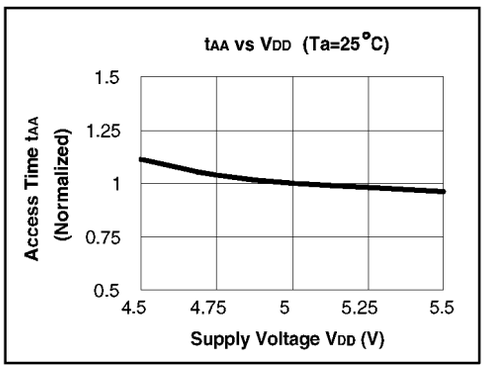
Characteristic Curves

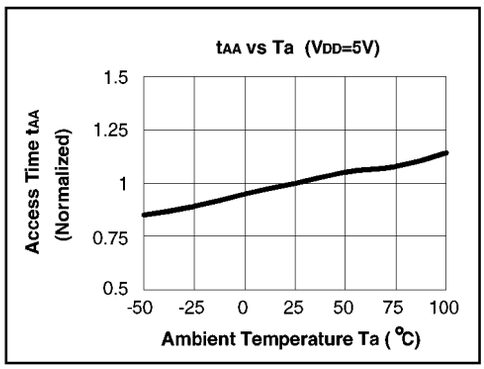


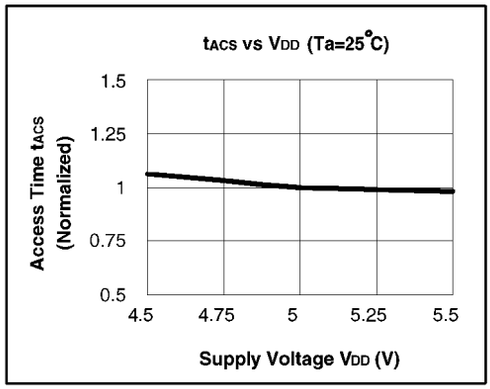


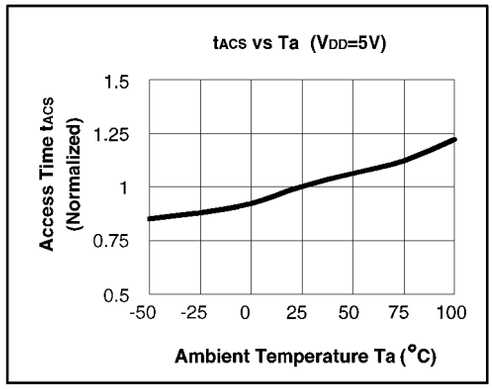


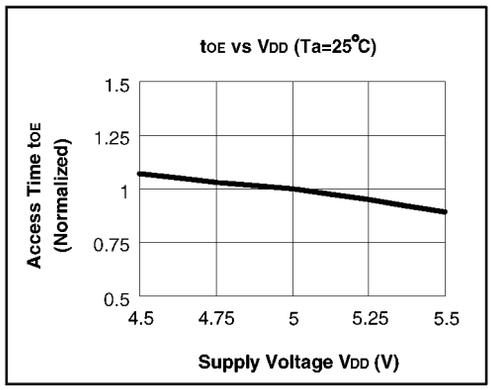


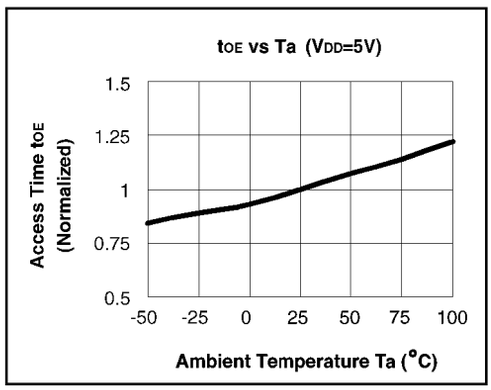





tACS vs VDD (Ta=25°C)
Access Time tACS (Normalized)
1.5
1.25
1
0.75
0.5
4.5
4.75
5
5.25
5.5
Supply Voltage VDD (V)


tACS vs Ta (VDD=5V)
Access Time tACS (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
100
Ambient Temperature Ta (°C)


tOE vs VDD (Ta=25°C)
Access Time tOE (Normalized)
1.5
1.25
1
0.75
0.5
4.5
4.75
5
5.25
5.5
Supply Voltage VDD (V)


tOE vs Ta (VDD=5V)
Access Time tOE (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
100
Ambient Temperature Ta (°C)