

# 2×20W I<sup>2</sup>S Input, Inductor Free, Stereo Class D Amplifier

## ■ FEATURE

- Power supply:
  - PVDD: 4.5V – 16V; -DVDD: 3.3V
- Audio Performance
  - BTL, 2×20W (PVDD=14.5V, R<sub>L</sub>=4Ω, THD+N=1%)
  - PBTL, 24W (PVDD=15V, R<sub>L</sub>=4Ω, THD+N=1%)
  - THD+N=0.04% (PVDD=12V, R<sub>L</sub>=4Ω, P<sub>o</sub>=1W)
  - Noise: 110uV (Gain = 19dBV, A weighted)
- Low Quiescent Current
  - 12mA at PVDD = 12V, no filter
- High efficiency in 1SPW mode (>90%)
- Inductor-free Operation (Ferrite Bead) and EMC compliant for most cases
- Flexible Audio I/O
  - I<sup>2</sup>S, LJ, RJ, TDM input
  - 8, 16, 32, 44.1, 48, 88.2, 96, 192kHz Sample Rates
- General Operational Features
  - Hardware or Software Control mode
  - 4 Programmable I<sup>2</sup>C Addresses
  - Spread Switching Frequency for Class D
- Robustness Features
  - Clock Error, DC, Over Current, Overvoltage, Undervoltage, and Overtemperature Protection
- Packages: Pb-free Packages, QFN36L-6×6

## ■ GENERAL DESCRIPTION

The HT660 is a stereo Class D audio amplifier with multiple audio format port (I<sup>2</sup>S, LJ, RJ, TDM). It supports a variety of audio clock configurations.

The outputs of the HT660 can be configured to drive two speakers in stereo BTL mode or mono PBTL mode.

The HT660 also includes hardware and software control modes, integrated digital clipper, and a wide power supply operating range to enable use in a multitude of applications.

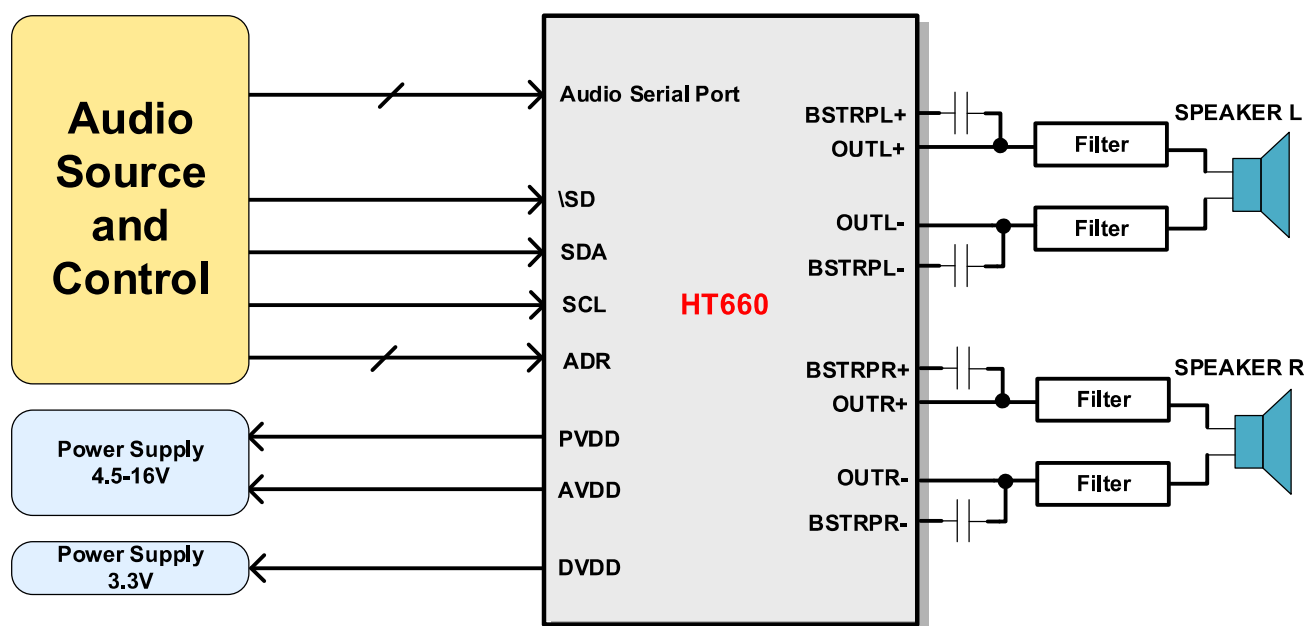
Advanced EMI Suppression with Spread Spectrum Control enables the use of inexpensive ferrite bead filters while meeting EMC requirements for system cost reduction.

An optimal mix of thermal performance and device cost is provided in the 150-mΩ R<sub>DS(ON)</sub> of the output MOSFETs. Additionally, a thermally enhanced 36-Pin QFN provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

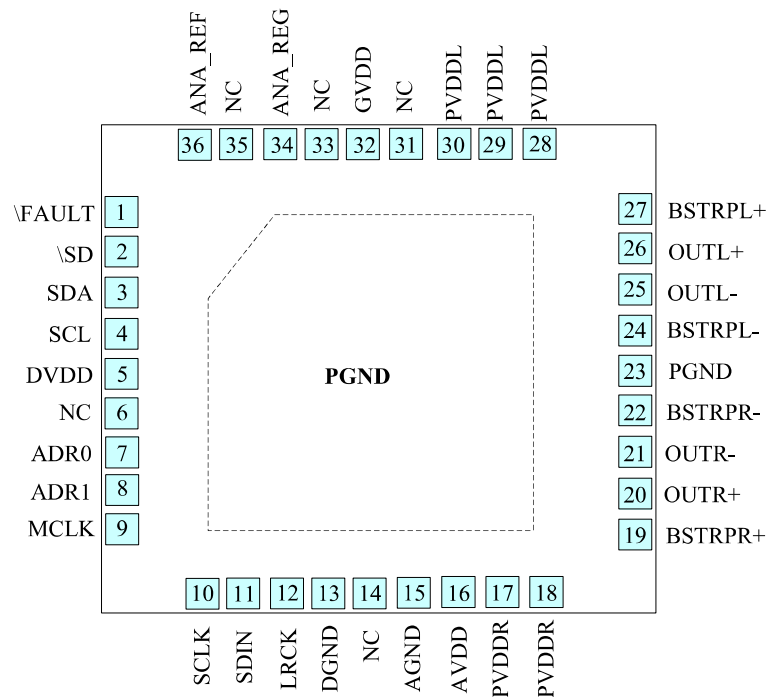
## ■ APPLICATIONS

- Bluetooth/Wi-Fi Speakers
- Portable Speakers
- Smart speakers
- LCD TV/Monitor
- Sound Bars, Docking stations, PC Audio

## ■ TYPICAL APPLICATION



## ■ TERMINAL CONFIGURATION



Top View

## ■ TERMINAL FUNCTION

Terminal No.	Name	I/O <sup>1</sup>	Description
1	\FAULT	OD	Speaker amplifier fault terminal, which is pulled LOW when an internal fault occurs, open-drain output.
2	\SD	I	Places the speaker amplifier in shutdown mode while pulled low level.
3	SDA	I	I <sup>2</sup> C data input pin.
4	SCL	I	I <sup>2</sup> C clock input terminal.
5	DVDD	P	Power supply for the internal digital circuitry
6, 14, 31, 33, 35	NC	-	Not connected inside the device (they be connected to ground for better thermal performance; however, they can be used as routing channels if required.)
7	ADR0	I	Determine the I <sup>2</sup> C Address of the device
8	ADR1	I	Determine the I <sup>2</sup> C Address of the device
9	MCLK	I	Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking
10	SCLK	I	Bit clock for the digital signal that is active on the serial data port's input data line
11	SDIN	I	Data line to the serial data port
12	LRCK	I	Word select clock for the digital signal that is active on the serial port's input data line
13	DGND	G	Ground for digital circuitry (NOTE: This pin should be connected to the system ground)
15	AGND	G	Ground for analog circuitry (NOTE: This pin should be connected to the system ground)

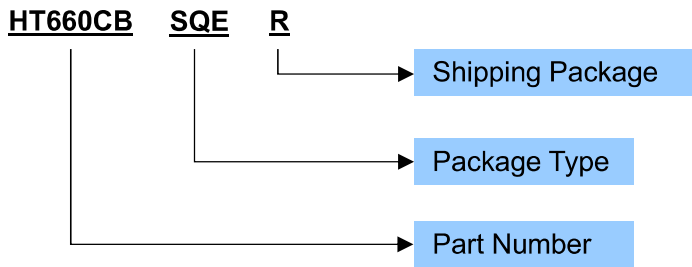
<sup>1</sup>: I: Input; O: Output; G: Ground; P: Power; BST: BOOT Strap; OD: Open drain

16	AVDD	P	Power supply for internal analog circuitry
17	PVDDR	P	Power Supply for internal power circuitry of Channel R
18	PVDDR	P	
19	BSBRPR+	BST	Connection point for the OUTR+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTR+
20	OUTR+	O	Positive pin for differential speaker amplifier output R
21	OUTR-	O	Negative pin for differential speaker amplifier output R
22	BSBRPR-	BST	Connection point for the OUTR- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTR-
23	PGND	G	Ground for power device circuitry (NOTE: This terminal should be connected to the system ground)
24	BSTRPL-	BST	Connection point for the OUTL- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTL-
25	OUTL-	O	Negative pin for differential speaker amplifier output L
26	OUTL+	O	Positive pin for differential speaker amplifier output L
27	BSBRPL+	BST	Connection point for the OUTL+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTL
28	PVDDL	P	Power Supply for internal power circuitry of Channel L
29	PVDDL	P	
30	PVDDL	P	
32	GVDD	O	Voltage regulator derived from PVDD supply (NOTE: This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
34	ANA_REG	P	Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
36	ANA_REF	P	Connection point for internal reference used by ANA_REG filter capacitors. <b>And connect to system GND.</b>
<b>EP</b>	<b>PGND</b>	<b>G</b>	Provides both <b>electrical and thermal connection</b> from the device to the board. <b>A matching ground pad must be provided on the PCB and the device connected to it via solder.</b> For proper electrical operation, this ground pad must be connected to the system ground.

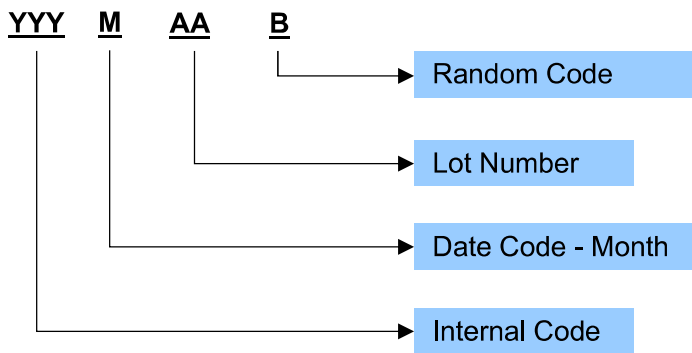
**ORDERING INFORMATION**

Ordering Number	Package Type	Marking	Operating Temperature Range	MOQ/Shipping Package
HT660CBSQER	QFN36L-6×6	HT660sq YYYYMAAB <sup>1</sup>	-25℃~85℃	Tape and Reel / 2500pcs

**Ordering Number**



**Production Tracking Code**



<sup>1</sup> YYYYMAAB is production tracking code

## ■ SPECIFICATIONS <sup>1</sup>

### ● Absolute Maximum Ratings <sup>2</sup>

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Power supply voltage for AVDD	AVDD	-0.3		18	V
Power supply voltage for PVDD	PVDD	-0.3		18	V
Power supply voltage for DVDD	DVDD	-0.3		4	V
DVDD Referenced Digital Input Voltages	V <sub>I</sub>	-0.3		DVDD+0.3	V
Moisture Sensitivity Level (MSL)			MSL3		
Ambient Operating Temperature	T <sub>A</sub>	-25		85	°C
Junction Temperature	T <sub>J</sub>	-40		125	°C
Storage Temperature	T <sub>STG</sub>	-40		125	°C

### ● Recommended Operating Conditions

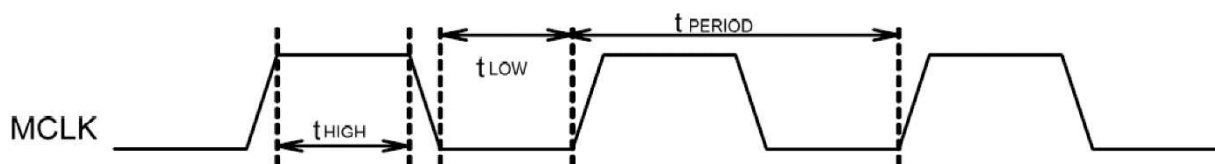
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage for AVDD	AVDD		4.5		16	V
Power supply voltage for PVDD	PVDD	BTL	4.5		16	V
		PBTL	6		16	
Power supply voltage for DVDD	DVDD		3.0	3.3	3.6	V
Ambient Operating Temperature	T <sub>a</sub>		-25	25	85	°C
DVDD Referenced Digital Input Voltages	V <sub>I</sub>		0		DVDD	V
Minimum Speaker Load in BTL Mode	R <sub>L</sub>		4			Ω
Minimum Speaker Load in PBTL Mode	R <sub>L</sub>		2			Ω

### ● I/O pins

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Input Logic High threshold for DVDD referenced digital inputs	V <sub>IH1</sub>	All Digital I/O pins including \FAULT, \SD, SDA, SCL, ADR0, ADR1, MCLK, SCLK, SDIN, LRCK	70			%DVDD
Input Logic LOW threshold for DVDD Referenced Digital Inputs	V <sub>IL1</sub>				30	%DVDD
Input Logic HIGH Current Level	I <sub>IH1</sub>				15	μA
Input Logic LOW Current Level	I <sub>IL1</sub>				-15	μA
Output Logic LOW Voltage Level	V <sub>OH</sub>		90			%DVDD
Output Logic LOW Voltage Level	V <sub>OL</sub>				10	%DVDD

### ● Master Clock

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable MCLK Duty Cycle	D <sub>MCLK</sub>		45	50	55	%
Supported MCLK Frequencies	f <sub>MCLK</sub>	Values include: 128, 192, 256, 384, 512.	128		512	f <sub>s</sub>
Pulse duration of MCLK high	t <sub>HIGH</sub>		10.1			ns
Pulse duration of MCLK low	t <sub>LOW</sub>		10.1			ns
Period of MCLK	t <sub>PERIOD</sub>		20.2			ns

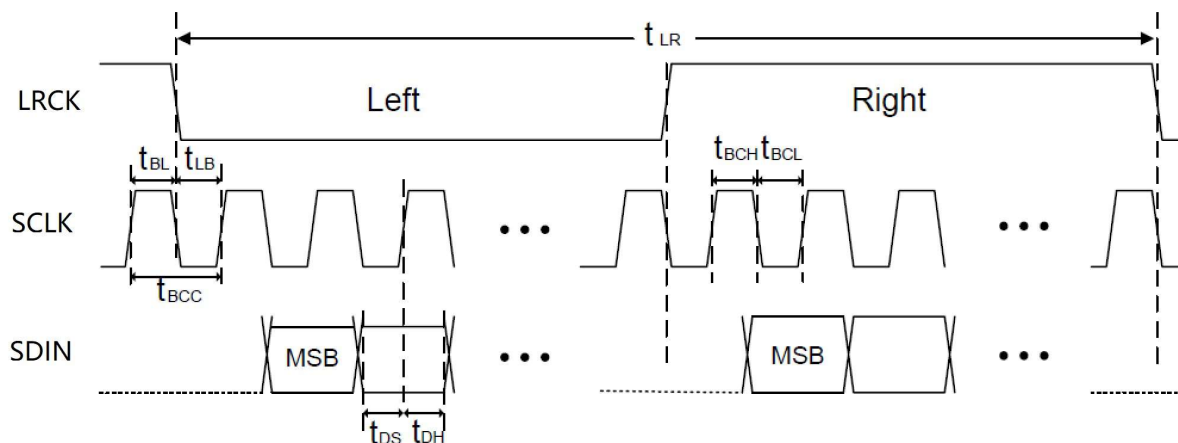


<sup>1</sup> Depending on parts and PCB layout, characteristics may be changed.

<sup>2</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

● **Serial Audio Port**

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable SCLK Duty Cycle	D <sub>SCLK</sub>		45	50	55	%
Supported Input Sample Rates (1/t <sub>LR</sub> )	f <sub>s</sub>		8		192	kHz
Required LRCK to SCLK Rising Edge	t <sub>LB</sub>		15			ns
Required SCLK Rising Edge to LRCK edge	t <sub>BL</sub>		15			ns
Supported SCLK Frequencies (1/t <sub>BCC</sub> ) for I2S	F <sub>SCLK</sub>	Values include: 32, 48, 64	32		64	f <sub>s</sub>
Supported SCLK Frequencies (1/t <sub>BCC</sub> ) for TDM	F <sub>SCLK</sub>	Values include: 128, 256, 512	128		512	f <sub>s</sub>
SCLK Pulse Width High	t <sub>BCL</sub>			t <sub>BCC</sub> /2		
SCLK Pulse Width Low	t <sub>BCH</sub>			t <sub>BCC</sub> /2		
Required SDIN Hold Time after SCLK, Rising Edge	t <sub>DH</sub>		15			ns
Required SDIN Setup Time before SCLK Rising Edge	t <sub>DS</sub>		15			ns



● **Protection Circuitry**

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
PVDD Overvoltage Error Threshold	OV <sub>ERTH</sub>	PVDD Rising		18		V
PVDD Overvoltage Error Threshold	OV <sub>FTH</sub>	PVDD Falling		17		V
PVDD Undervoltage Error Threshold	UV <sub>ERTH</sub>	PVDD Falling		4.2		V
PVDD Undervoltage Error Threshold	UV <sub>FTH</sub>	PVDD Rising		4.4		V
Overtemperature Error Threshold	OT <sub>ETH</sub>			150		°C
Overtemperature Error Hysteresis	OT <sub>EHYS</sub>			15		°C
Overcurrent Error Threshold for each BTL Output	OC <sub>ETH</sub>			7.5		A
DC Error Threshold	DC <sub>ETH</sub>			2.6		V
Speaker Amplifier Fault Time Out period	T <sub>fault</sub>	DCE or OTE or OCP		1.4		s

● **Speaker Amplifier in All Modes**

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Speaker Amplifier Gain	AV <sub>00</sub>			19		dBV
Speaker Amplifier DC Offset	V <sub>OS</sub>	BTL		1.5		mV
Speaker Amplifier Switching Frequency	f <sub>SPK_AMP(1)</sub>			360		kHz
On Resistance of Output MOSFET (both high-side and low-side)	R <sub>DS(ON)</sub>			150		mΩ
-3-dB Corner Frequency of High-Pass Filter	f <sub>c</sub>	f <sub>s</sub> = 44.1 kHz		3.7		Hz
		f <sub>s</sub> = 48 kHz		4		Hz
		f <sub>s</sub> = 88.2 kHz		7.4		Hz
		f <sub>s</sub> = 96 kHz		8		Hz

● **Speaker Amplifier in Stereo Bridge Tied Load (BTL) Mode**

TA = 25°, PVDD = 12V, DVDD= 3.3V, BTL mode, GAIN = 19dBV, BD mode, fs = 48kHz (unless otherwise noted)

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V <sub>N</sub>	PVDD = 12 V, GAIN = 19dBV, R <sub>SPK</sub> = 8 Ω or 4 Ω, 20-20kHz, A-Weighted		110		μV
Signal to Noise Ratio (Referenced to THD+N=1%)	SNR	PVDD = 12 V, R <sub>SPK</sub> = 8 Ω or 4Ω, 20-20kHz, A-Weighted		97		dB
Maximum Instantaneous Output Power Per. Ch.	P <sub>o</sub>	PVDD = 12 V, R <sub>SPK</sub> = 4 Ω, THD+N = 1%		14		W
		PVDD = 12 V, R <sub>SPK</sub> = 8 Ω, THD+N = 1%		8		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R <sub>SPK</sub> = 4 Ω, P <sub>o</sub> = 1 W		0.02		%
		PVDD = 12 V, R <sub>SPK</sub> = 8 Ω, P <sub>o</sub> = 1 W		0.02		%
Cross-talk (worst case between L->R and R->L coupling)	X-Talk	PVDD = 12 V, GAIN = 19dBV, R <sub>SPK</sub> = 4 Ω, P <sub>o</sub> = 1W		-85		dB

● **Speaker Amplifier in Mono Parallel Bridge Tied Load (PBTL) Mode**

TA = 25°, PVDD = 12V, DVDD= 3.3V, BTL mode, GAIN = 19dBV, BD mode, fs = 48kHz (unless otherwise noted)

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V <sub>N</sub>	PVDD = 12 V, GAIN = 19dBV, R <sub>SPK</sub> = 8 Ω or 4 Ω, 20-20kHz, A-Weighted		110		μV
Signal to Noise Ratio (Referenced to THD+N =1%)	SNR	PVDD = 12 V, R <sub>SPK</sub> = 8 Ω or 4Ω, 20-20kHz, A-Weighted		97		dB
Maximum Instantaneous Output Power.	P <sub>o</sub>	PVDD = 12 V, R <sub>SPK</sub> = 4 Ω, THD+N = 1%		16		W
		PVDD = 12 V, R <sub>SPK</sub> = 2 Ω, THD+N = 1%		26		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R <sub>SPK</sub> = 4 Ω, P <sub>o</sub> = 1 W		0.02		%
		PVDD = 12 V, R <sub>SPK</sub> = 2 Ω, P <sub>o</sub> = 1 W		0.03		%

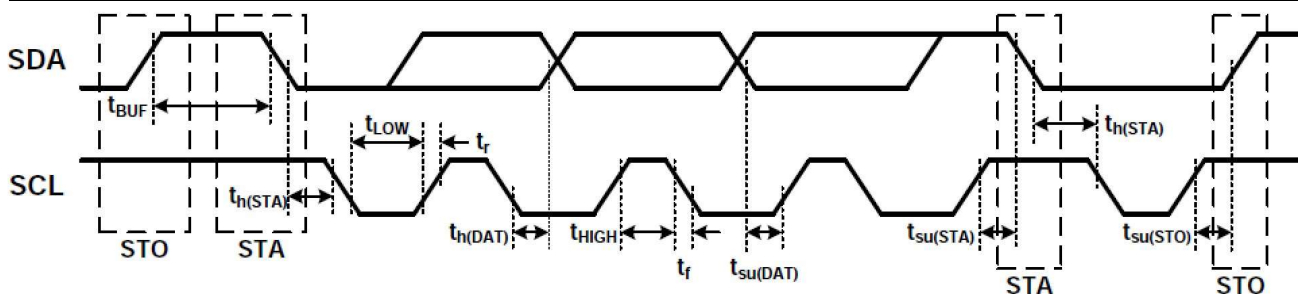
● **Typical current consumption**

TA = 25°, PVDD = 12V, DVDD= 3.3V, No Load, BTL mode, GAIN = 19dBV, BD mode, fs = 48kHz (unless otherwise noted)

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
<b>I<sub>DVDD</sub></b>						
Quiescent current in DVDD	I <sub>DVDD</sub>	fs=48kHz MCLK=128*fs		4.5		mA
		fs=48kHz MCLK=256*fs		5.3		mA
		fs=48kHz MCLK=512*fs		5.5		mA
		fs=96kHz MCLK=128*fs		6.7		mA
		fs=96kHz MCLK=256*fs		8.3		mA
		fs=96kHz MCLK=512*fs		8.8		mA
DVDD current consumption in sleep mode	I <sub>DVDD_SLEEP</sub>	SLEEP mode, fs=48kHz MCLK=256*fs		3.0		mA
		SLEEP mode, fs=96kHz MCLK=256*fs		3.5		mA
DVDD current consumption in SD mode	I <sub>DVDD_SD</sub>	∖SD = L, No clock		120		uA
<b>I<sub>PVDD</sub></b>						
Quiescent current in PVDD	I <sub>PVDD</sub>	PVDD=12V		12		mA
PVDD current consumption in Amplifier MUTEA Mode (MUTE_A)	I <sub>PVDD_MUTEA</sub>	PVDD=12V		6		mA
PVDD current consumption in SD mode	I <sub>PVDD_SD</sub>	PVDD=12V		11		uA

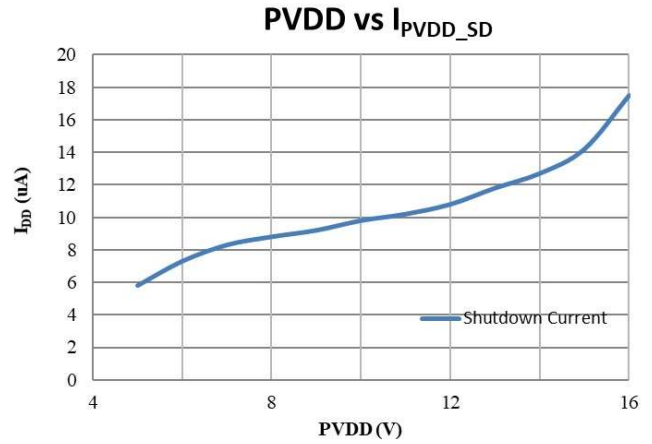
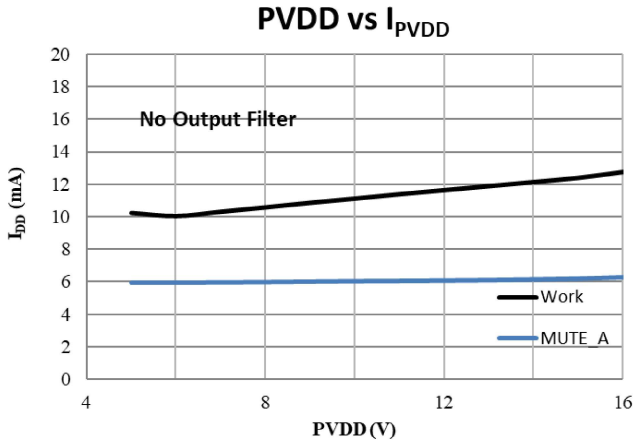
● **I<sup>2</sup>C Control Port**

PARAMETER	Symbol	Standard-Mode			Fast-Mode			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Allowable Load Capacitance for Each I <sup>2</sup> C Line	C <sub>b</sub>			400			400	pF
Support SCL frequency	f <sub>SCL</sub>			100			400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t <sub>h(STA)</sub>	4			0.6			us
Required Pulse Duration, SCL HIGH	t <sub>HIGH</sub>	4			0.6			us
Required Pulse Duration, SCL LOW	t <sub>LOW</sub>	4.7			1.3			us
Setup time for a repeated START condition	t <sub>su(STA)</sub>	4.7			0.6			us
Data hold time	t <sub>h(DAT)</sub>	0		3.45	0		0.9	us
Setup Time, SDA to SCL	t <sub>su(DAT)</sub>	250			100			ns
Rise Time, SCL	T <sub>r_SCL</sub>			1000			300	ns
Rise Time, SDA	T <sub>r_SDA</sub>			1/(4*f <sub>SCL</sub> )-0.25			1/(4*f <sub>SCL</sub> )-0.25	us
Fall Time, SCL and SDA	T <sub>f</sub>			300			300	ns
Setup Time, SCL to STOP condition	t <sub>su(STO)</sub>	4			0.6			us
Bus Free time between STOP and START conditions	t <sub>BUF</sub>	4.7			1.3			us

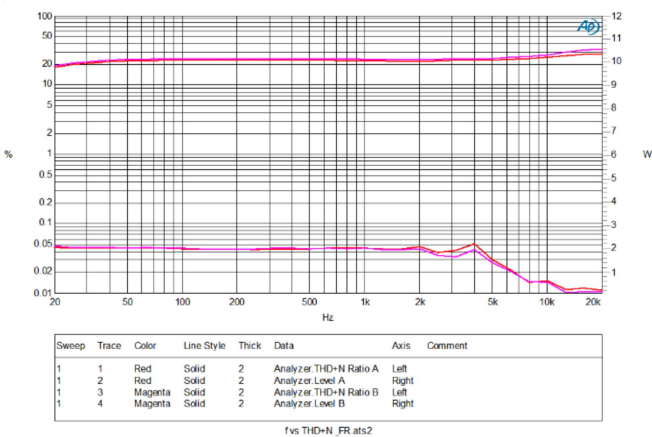
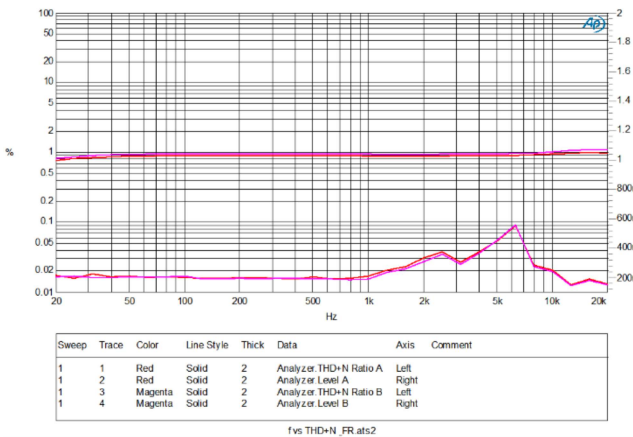
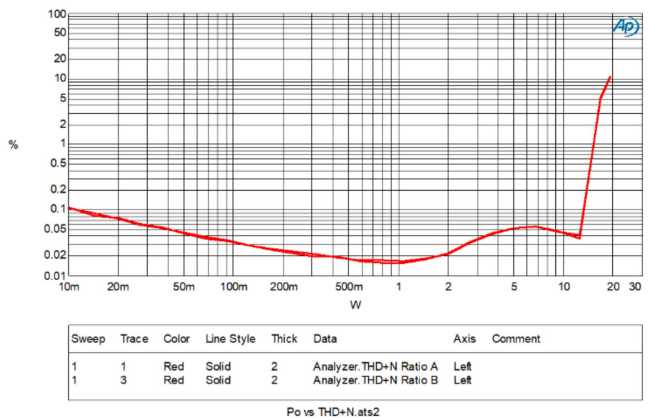
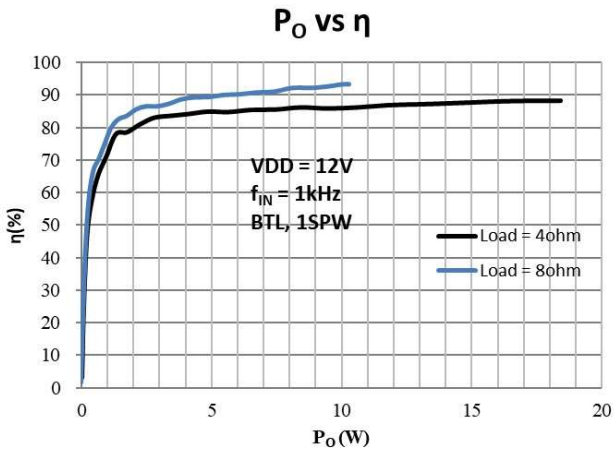




**TYPICAL OPERATING CHARACTERISTICS**

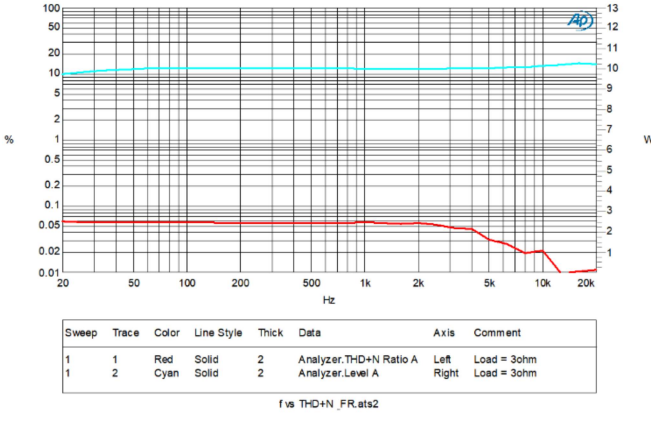
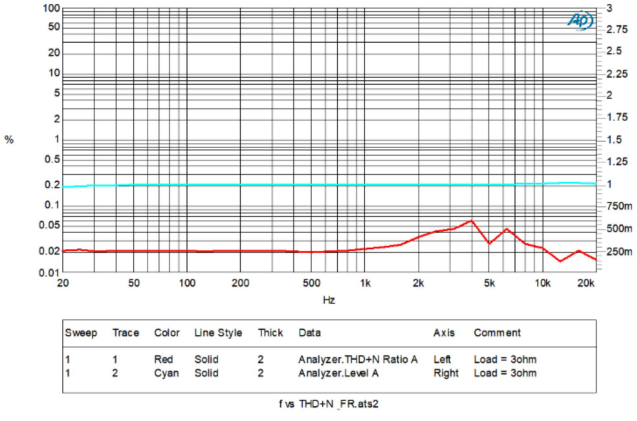
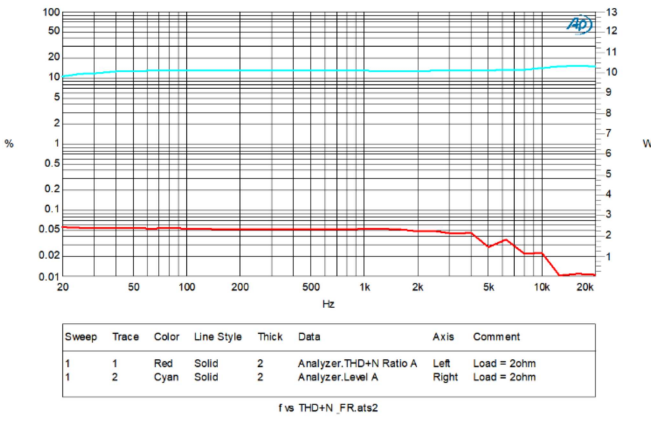
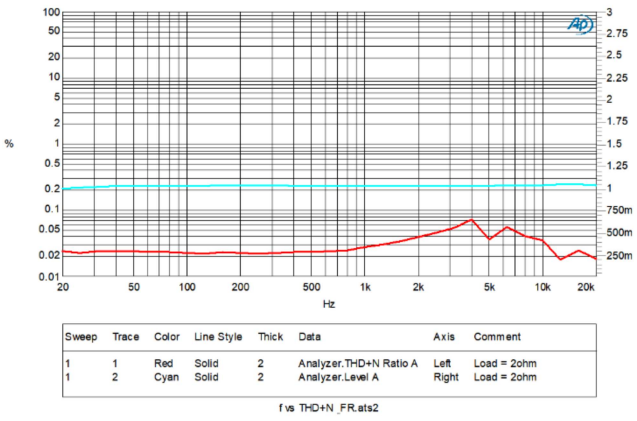
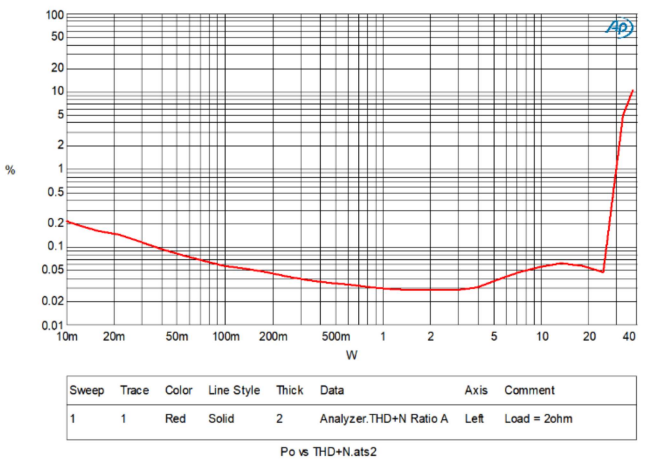
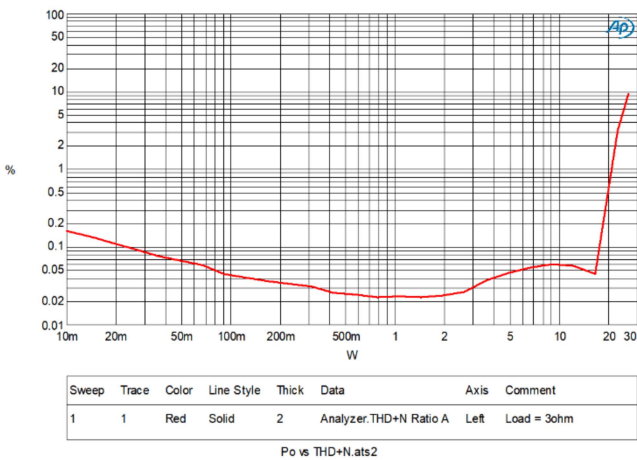
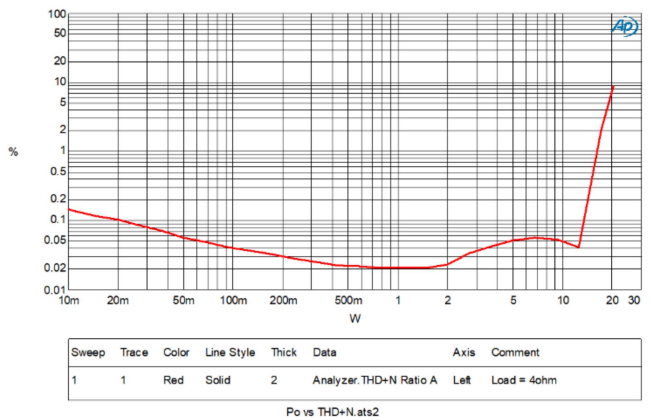
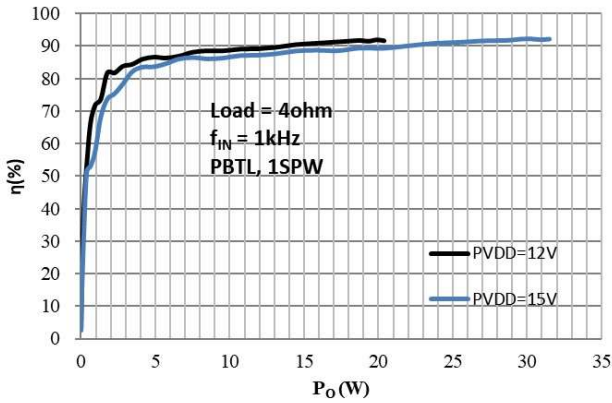


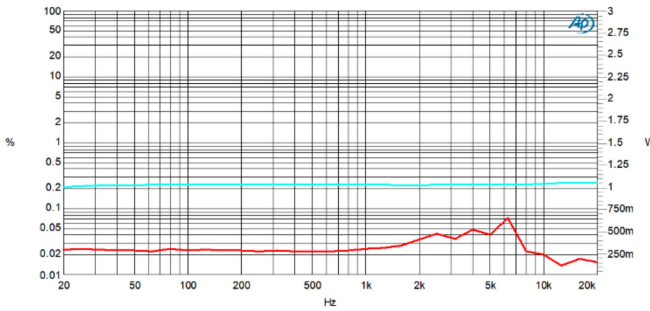
T<sub>A</sub> = 25°C, PVDD = 12V, DVDD = 3.3V, **BTL mode**, f<sub>IN</sub> = 1 kHz, BD mode, Load = 4ohm, No LC filter, unless otherwise noted.



T<sub>A</sub> = 25°C, PVDD = 12V, PBTL mode, f<sub>IN</sub> = 1 kHz, BD mode, Load = 4ohm, No LC filter, unless otherwise noted.

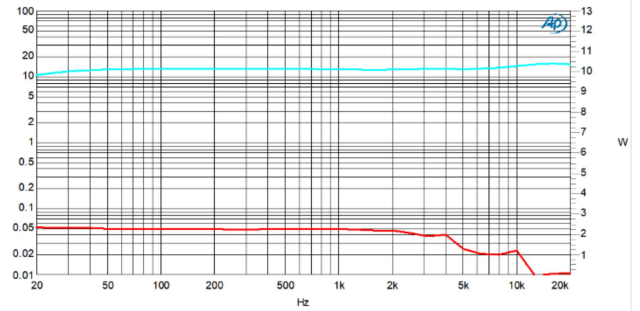
P<sub>O</sub> vs η





Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.TH+N Ratio A	Left	Load = 4ohm
1	2	Cyan	Solid	2	Analyzer.Level A	Right	Load = 4ohm

f vs THD+N\_FR.ats2



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.TH+N Ratio A	Left	Load = 4ohm
1	2	Cyan	Solid	2	Analyzer.Level A	Right	Load = 4ohm

f vs THD+N\_FR.ats2

**APPLICATION INFORMATION**

The HT660 is a flexible and easy-to-use stereo class-D speaker amplifier with an digital input serial audio port. The HT660 supports a variety of audio clock configurations between 8kHz to 192kHz sample rate. The outputs of the HT660 can be configured to drive two speakers in stereo Bridge Tied Load (BTL) mode or a single speaker in Parallel Bridge Tied Load (PBTL) mode.

**1 Power Supplies**

Only two power supplies are required for the HT660. They are a 3.3-V power supply, called DVDD, for the small signal analog and digital and a higher voltage power supply, called PVDD for the output stage of the speaker amplifier and AVDD for analog power supply. To enable use in a variety of applications, PVDD can be operated over a large range of voltages, which is 4.5V – 16V, and it is recommended to put paralleled capacitor of 100nF//1uF//220uF between each channel of PVDD and system ground.

**2 Speaker Amplifier Audio Signal Path**

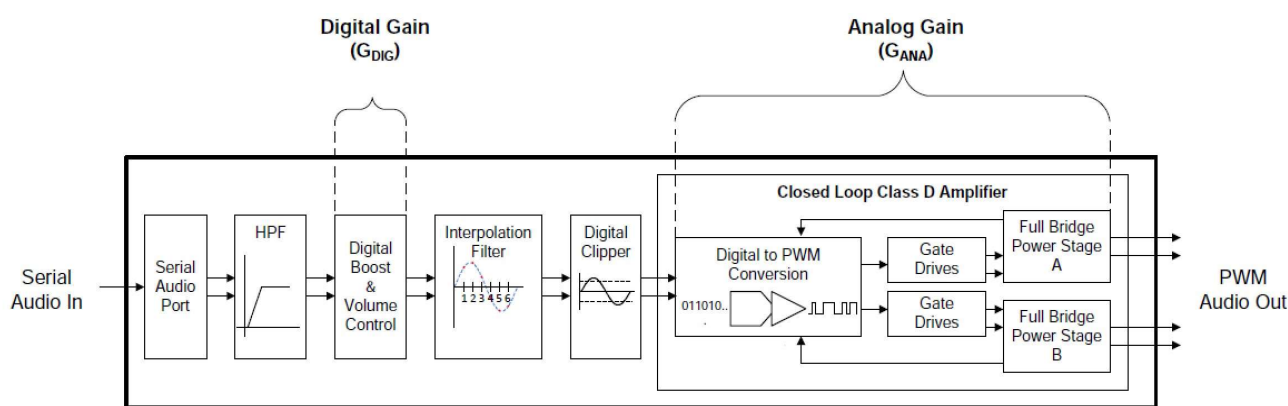


Figure 1 Speaker Amplifier Audio Signal Path

**2.1 Serial Audio Port**

The serial audio port receives audio in either I<sup>2</sup>S, Left Justified, Right Justified or TDM formats, up to 32-bit word length. Default setting is I<sup>2</sup>S and 32-bit word length. The supported clock rates and ratios are detailed below.

Table1 Supported SCLK rates for TDM

Maximum Sample Rate $f_s$ (kHz)	SCLK Rate (xfs)
8-48kHz	128, 256, 512
96kHz	128, 256
192kHz	128

Table2 Supported SCLK rates for IIS/LJ/RJ

Sample Rate $f_s$ (kHz)	MCLK rate ( $\times f_s$ )							
	128	192	256	384	512	768	1024	1152
	SCLK rate ( $\times f_s$ )							
8	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S
12	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S
16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
24	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
38	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
44.1	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S
88.2	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S
96	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S
128	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S
176.4	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S	N/S	N/S
192	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S	N/S	N/S

2.1.1 I<sup>2</sup>S

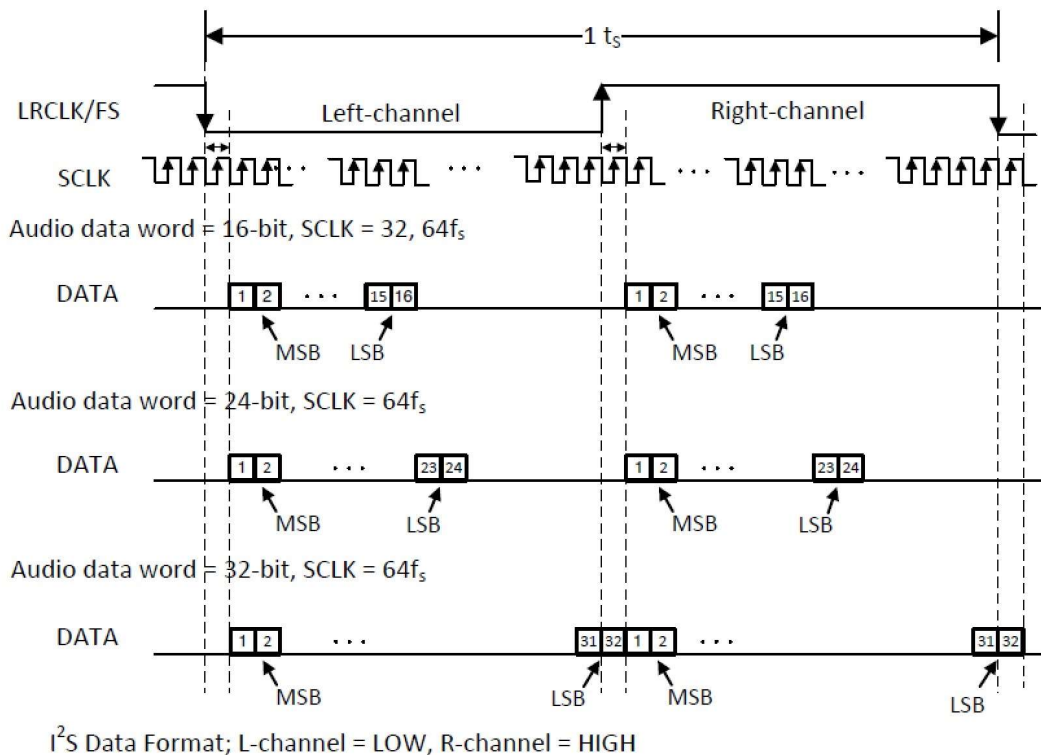


Figure 2 IIS Audio Data Format Timing

**2.1.2 Left-Justified**

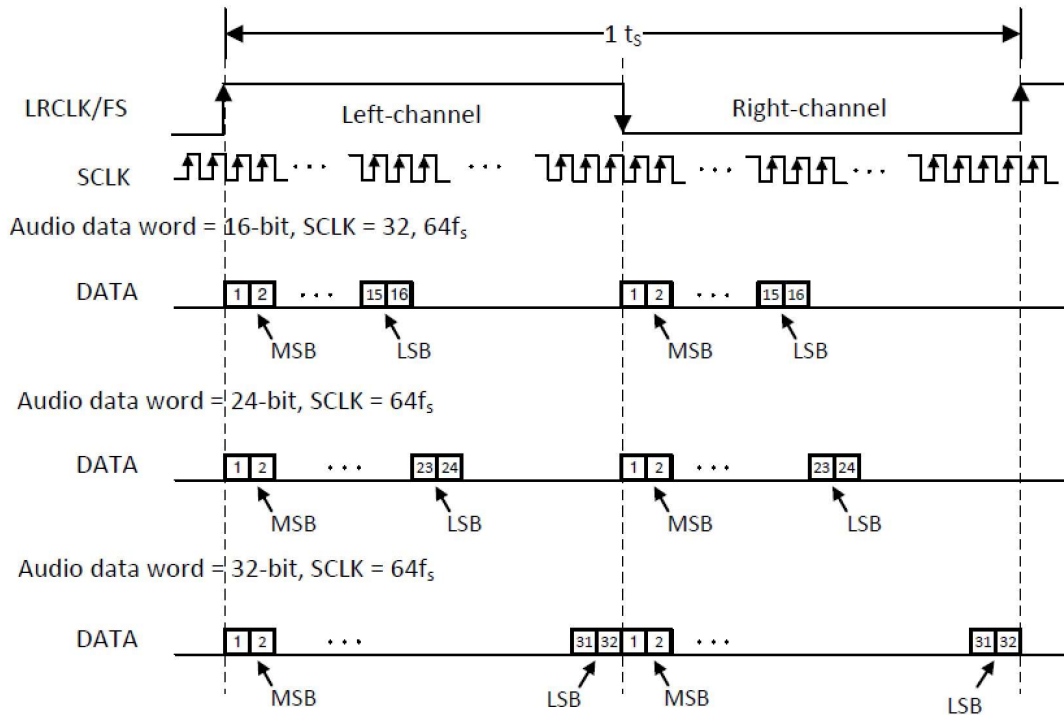


Figure 3 Left-Justified Audio Data Format Timing

**2.1.3 Right-Justified**

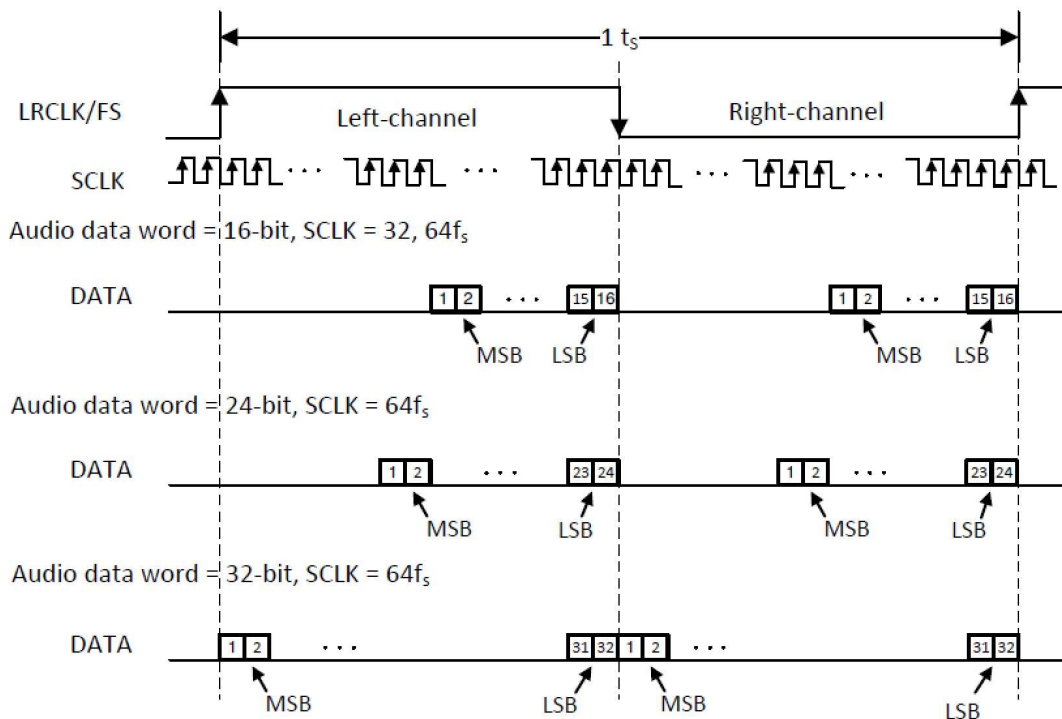


Figure 4 Right-Justified Audio Data Format Timing

### 2.1.4 TDM

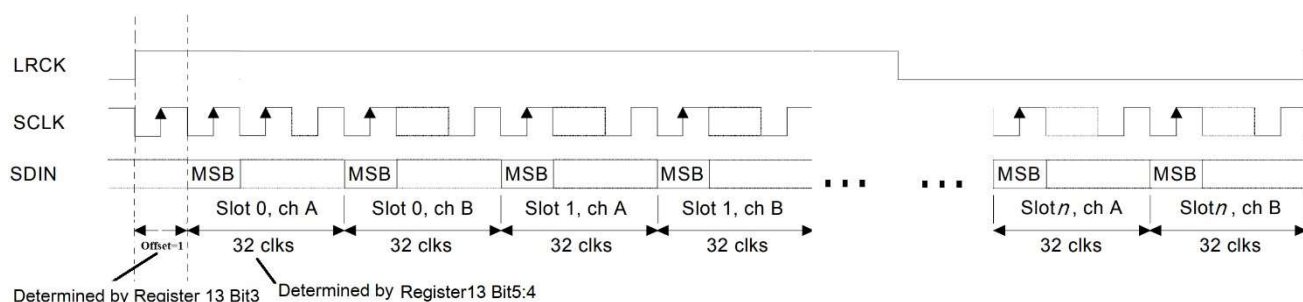


Figure 5 TDM Audio Data Format Timing

### 2.2 DC Blocking Filter

Excessive DC content in the audio signal can damage loudspeakers and even small amounts of DC offset in the signal path cause audible artifacts when muting and unmuting the speaker amplifier. For these reasons, the amplifier employs two separate DC blocking methods for the speaker amplifier. The first is a high-pass filter provided at the front of the data path to remove any DC from incoming audio data before it is presented to the audio path. The -3 dB corner frequencies for the filter are specified in the speaker amplifier electrical characteristics table. In Hardware Control mode, the DC blocking filter is active and cannot be disabled. In software Control mode, the filter can be bypassed by writing a 0 to bit 7 of register 0x14. The second method is a DC detection circuit that will shut down the power stage if DC is found to be present on the output due to some internal error of the device. This DC Error (DCE) protection is discussed in the 3 *Speaker Amplifier Protection Suite* section below.

### 2.3 Digital Boost and Volume Control

Following the high-pass filter, a digital boost block is included to provide additional digital gain if required for a given application as well as to set an appropriate clipping point for a given GAIN configuration. The digital boost block defaults to +0dB and is changeable through bit [1:0] of register 14. In most use cases, the digital boost block will remain unchanged, as the volume control offers sufficient digital gain for most applications. The HT660's digital volume control operates from Mute to 24 dB, in steps of 0.5 dB. The equation below illustrates how to set the 8-bit volume control register at address 0x15/0x16:  $DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB])$

Transitions between volume settings will occur at a rate of 0.5 dB every 8 LRCK cycles to ensure no audible artifacts occur during volume changes. This volume fade feature can be disabled via Bit 4 of Register 0x14.

### 2.4 Digital Clipper

A digital clipper is integrated in the oversampled domain to provide a component-free method to set the clip point of the speaker amplifier. Through the "Digital Clipper Level x" (at register address 0x10, 0x11, 0x12) controls in the I<sup>2</sup>C control port, the point at which the oversampled digital path clips can be set directly, which in turns sets the 10% THD+N operating point of the amplifier. This is useful for applications in which a single system is designed for use in several end applications that have different power rating specifications. Its place in the oversampled domain ensures that the digital clipper is acoustically appealing and reduces or eliminates tones which would otherwise foldback into the audio band during clipping events. Figure 6 shows a block diagram of the digital clipper.



Figure 6 Digital Clipper Simplified Block Diagram

It is important to note that the actual signal developed across the speaker will be determined not only by the digital clipper, but also the analog gain of the amplifier. Depending on the analog gain settings and the PVDD level applied, clipping could occur as a result of the voltage swing that is determined by the gain being larger than the available PVDD supply rail.

### 2.5 Closed-Loop Class-D Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed-Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device.

The switching rate of the amplifier is internally fixed around 360 kHz.

### 3 Speaker Amplifier Protection Suite

The speaker amplifier in the HT660 includes a robust suite of error handling and protection features. It is protected against Over-Current, Under-Voltage, Over-Voltage, Over-Temperature, DC, and Clock Errors. The status of some errors is reported via the \FAULT pin or/and the appropriate error status register in the I<sup>2</sup>C Control Port. Table3 details the types of errors protected by the HT660's Protection Suite and how each are handled.

Table3 Protection Suite Error Handling Summary

ERROR	CAUSE	Reported Method	The device resumes normal operation
Overvoltage Error (OVE)	PVDD level rises above that specified by OVE <sub>RTH</sub>	none	Immediately after PVDD level returning below OVE <sub>FTH</sub>
Undervoltage Error (UVE)	PVDD level drops below that specified by UVE <sub>RTH</sub>	none	Immediately after PVDD level returning above UVE <sub>RTH</sub>
Clock Error (CLKE)	One or more of the following errors has occurred: 1. Non-supported MCLK to LRCK and/or SCLK to LRCK Ratio; 2. Non-supported MCLK or LRCK rate 3. MCLK, SCLK, or LRCK has stopped	\FAULT and Register	Immediately after Clocks returning to valid state
Overcurrent Error (OCE)	Speaker Amplifier output current has increased above the level specified by OCE <sub>TH</sub>	\FAULT	T <sub>fault</sub> after \FAULT pin is pulled low
DC Detect Error (DCE)	DC offset voltage on the speaker amplifier output has increased above the level specified by the DCE <sub>TH</sub>	\FAULT	T <sub>fault</sub> after \FAULT pin is pulled low
Overtemperature Error (OTE)	The temperature of the die has increased above the level specified by the OTE <sub>TH</sub>	\FAULT	T <sub>fault</sub> after \FAULT pin is pulled low

#### 3.1 \FAULT pin

In both hardware and software Control mode, the \FAULT pin of the HT660 serves as a fault indicator to notify the system that a fault has occurred with the device by being actively pulled LOW. This pin is an open-drain output pin and, unless one is provided internal to the receiver, requires an external pullup to set the net to a known value. The behavior of this pin varies based upon the type of error which has occurred.

#### 3.2 Over-Current Protection

The HT660 features over-current conditions against the output stage short-circuit conditions. The short circuit



protection fault is reported on the \FAULT pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is triggered. The device will automatically attempt to resume after  $T_{\text{fault}}$ . If the over-current condition is still not cleared, the device will again go into protection.

### 3.3 Over-temperature Protection

Over-temperature protection on the HT660 device prevents damage to the device when the internal die temperature exceeds 150°C. This triggering point has a  $\pm 15^\circ\text{C}$  tolerance from device to device. Once the die temperature exceeds the thermal triggering point, the device is switched to the shutdown state and the outputs are disabled. Thermal protection faults are reported on the \FAULT pin. The device will automatically attempt to resume after  $T_{\text{fault}}$ . If the over-temperature condition is still not cleared, the device will again go into protection.

### 3.4 Over-voltage Protection

The HT660 device monitors the voltage on AVDD voltage threshold. When the voltage on AVDD pin exceeds the over-voltage threshold (18 V typ), the OVP circuit puts the device into shutdown mode. The device recovers automatically once the over-voltage condition has been removed.

### 3.5 Under-voltage Protection

When the voltage on AVDD pin falls below the under-voltage threshold (4.2 V typ), the UVP circuit puts the device into shutdown mode. The device recovers automatically once the under-voltage condition has been removed.

### 3.6 Clock error detection

When any clock of MCLK, SCLK, LRCK halt or shifted to a non-supported speed, the device reports Clock Error in bit [1:0] of Register 0x17 and \Fault pin. The device recovers automatically once the clock-error condition has been removed.

### 3.7 DC Detect Protection

The HT660 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. A DC detect fault is reported on the \FAULT pin as a low state. The DC Detect fault also causes the amplifier to shutdown by changing the state of the outputs to Hi-Z. The device will automatically attempt to resume after  $T_{\text{fault}}$ . If the over DC current condition is still not cleared, the device will again go into protection.

A DC Detect Fault is issued when the output DC voltage sustain for more than 420 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the \SD pin low at power-up until the signals at the inputs are stable.

## 4 Device Functional Modes

### 4.1 Software Control and Hardware Control

The HT660 device can be configured via an I<sup>2</sup>C communication port which is software control mode. Once all powers (PVDD, AVDD, DVDD) are brought up and stable, the device is ready for software control. Before the device is configured into operation (that is bring \SD pin to high, or write Bit “SD” into 1), configure the device via I<sup>2</sup>C in the manner required by the use case, e.g., bit “PBTL” and “Format”.

For systems which do not require the added flexibility of the I<sup>2</sup>C control port or do not have an I<sup>2</sup>C host controller, the HT660 can be used directly in Hardware Control Mode with default configurations. The only external I/O that can be controlled in Hardware Control Mode is the \SD pin.

### 4.2 Speaker Amplifier Shut Down (\SD pin)

The \SD pin is provided to place the speaker amplifier into shutdown. Driving this pin LOW will place the device into shutdown, while pulling it HIGH will bring the device into operation. The shutdown mode is the lowest power consumption mode that the device can be placed in while the power supplies are up.

However, when \SD pin is pulled low, the software control mode is ready, the device is still capable of being configured through I<sup>2</sup>C port. If the \SD pin is pulled low, and bit SD is written into 1, the device is in operation mode.

See as the following table.

Table4 \SD pin and Bit SD

\SD pin	Bit SD	Mode
LOW	1	Normal operation
LOW	0	Shutdown mode
High	0	Normal operation
High	1	Normal operation

### 4.3 Spread Spectrum and De-Phase

The HT660 device has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM output to improve EMI performance. The spread spectrum scheme is turned on as default, and can be turned off in bit 6:4 of Register 0x19.

De-phase inverts the phase of the output PWM such that the idle output PWM waveforms of the two audio channels are inverted. De-phase does not affect the audio signal, or its polarity. De-phase only works with BD mode; it is auto-disabled in 1SPW mode.

### 4.4 Speaker Amplifier Operating Modes

The HT660 device can be used with two different amplifier configurations, can be configured by Bit 3 of Register 0x18: BTL Mode and PBTL Mode.

#### 4.4.1 BTL Mode

In BTL mode, the HT660 amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUTL+ and OUTL-, the amplified right signal is presented on differential output pair shown as OUTF+ and OUTF-.

#### 4.4.2 PBTL

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel to increase the power sourcing capabilities of the device. In this mode, connect the OUTF+ and OUTF- together for the positive speaker terminal and OUTL+ and OUTL- together for the negative speaker terminal.

On the input side of the HT660 device, the input signal to the PBTL amplifier is left frame of I<sup>2</sup>S or TDM data (changeable in bit 7 of register 0x17).

### 4.5 Class D Amplifier Modulation

The HT660 device can be used with two different Class D amplifier modulations, can be configured by Bit 7 of Register 0x19.

#### 4.5.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTx+ and OUTx- are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTx+ is greater than 50% and OUTx- is less than 50% for positive output voltages. The duty cycle of OUTx+ is less than 50% and OUTx- is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I<sup>2</sup>R losses in the load.

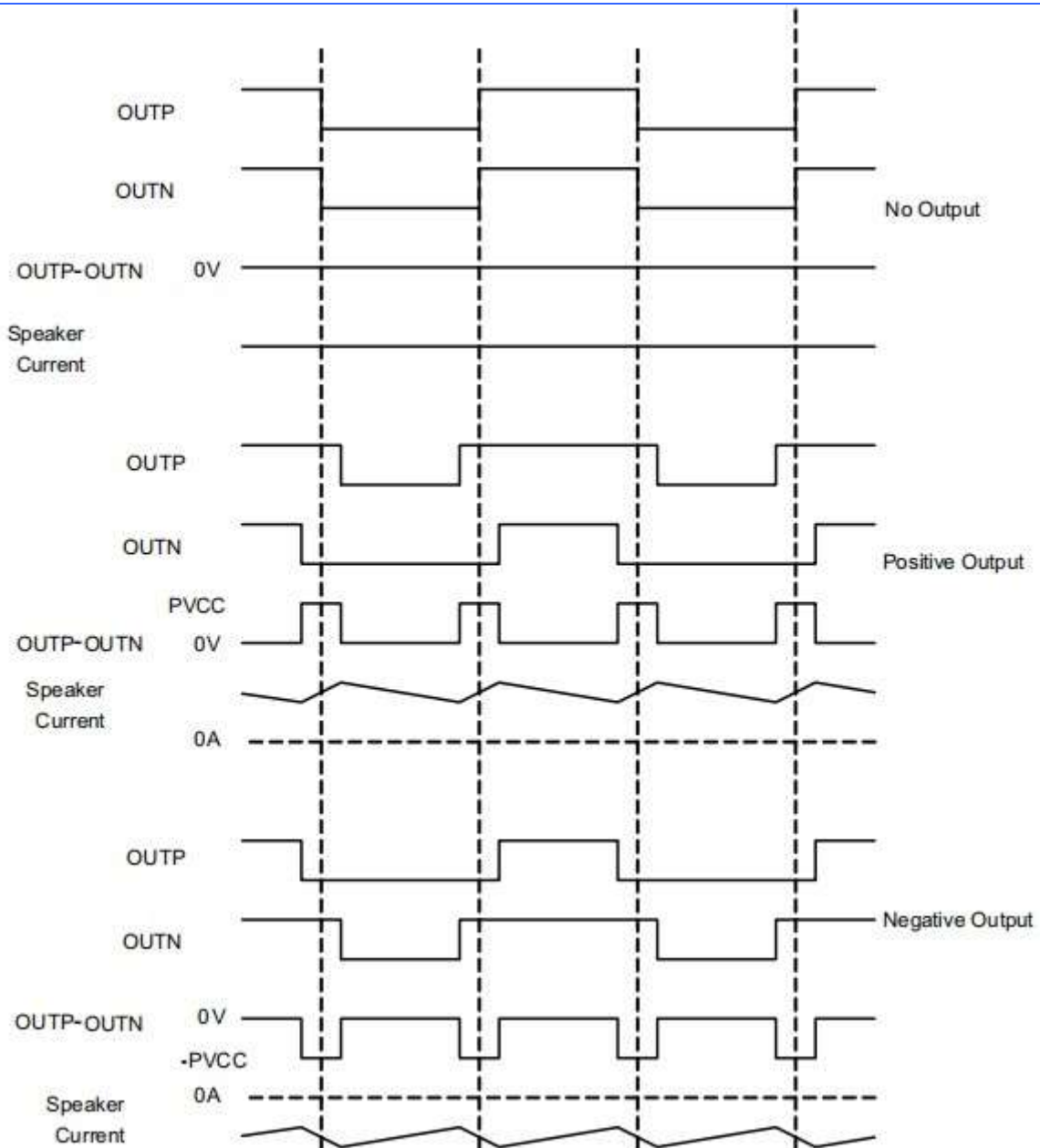


Figure 7 BD Modulation

#### 4.5.2 Low-Idle-Current 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an audio signal is applied one output decreases and the other output increases. The decreasing output signal rails to GND. At which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

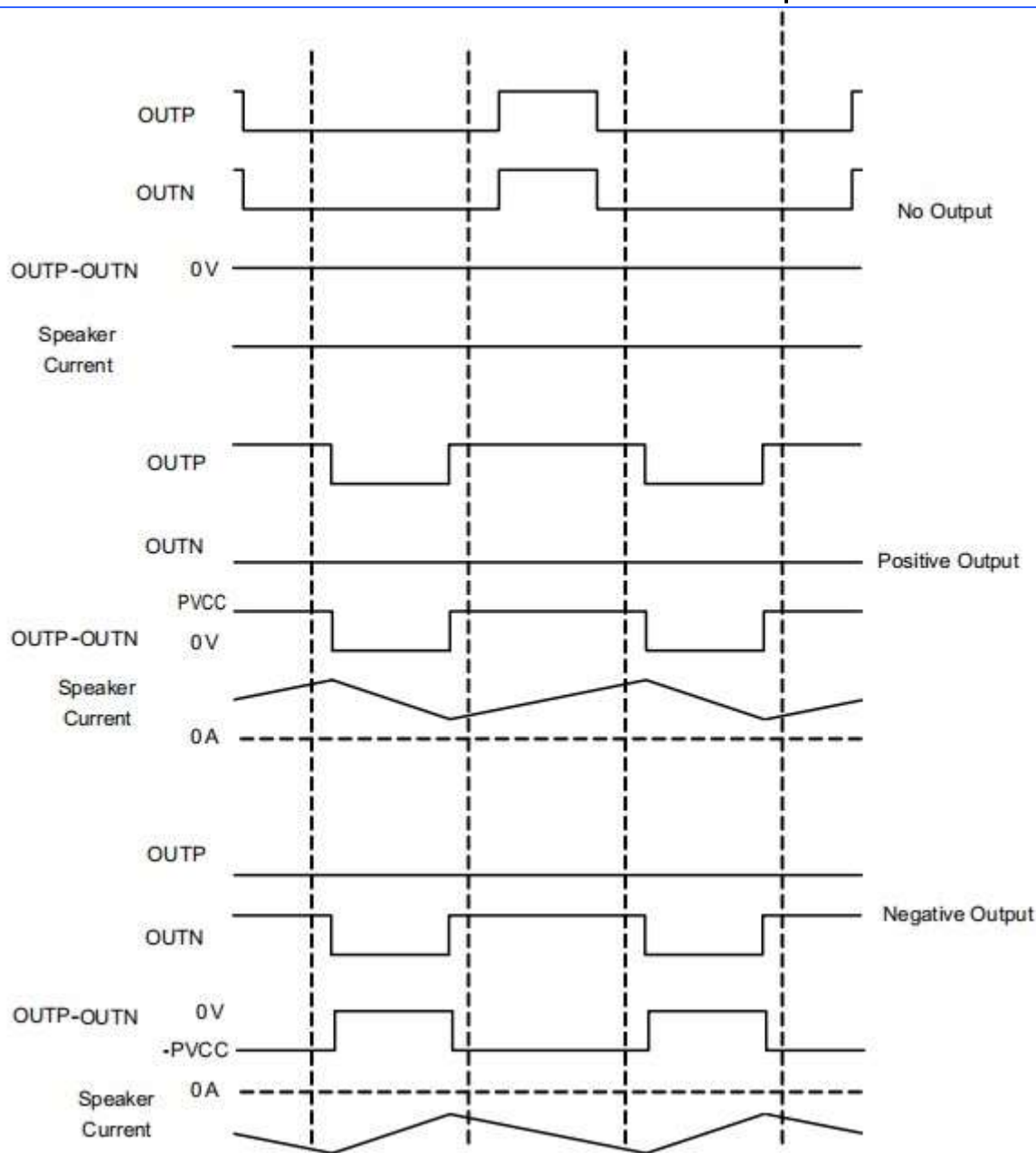


Figure 8 1SPW Modulation

## 4.6 I<sup>2</sup>C Control Port

### 4.6.1 I<sup>2</sup>C Device Address

Each device on the I<sup>2</sup>C bus has a unique address that allows it to appropriately transmit and receive data to and from the I<sup>2</sup>C master controller. As part of the I<sup>2</sup>C protocol, the I<sup>2</sup>C master broadcast an 8-bit word on the bus that contains a 7-bit device address in the upper 7 bits and a read or write bit for the LSB. The HT660 has a configurable I<sup>2</sup>C address. The ADR[1:0] can be used to set the device address of the HT660. The I<sup>2</sup>C device address is configured as “11011xx [R/W]”, where “xx” corresponds to the state of the ADR[1:0] pin at first power up sequence of the device. [R/W] represents 1 when writing, [R/W] represents 0 when reading.

Table5 IIC Address Configuration

ADR[1:0]	IIC Address for Reading	IIC Address for Writing
LL	0xD8	0xD9
LH	0xDA	0xDB
HL	0xDC	0xDD
HH	0xDE	0xDF

#### 4.6.2 General Operation of the I<sup>2</sup>C Control Port

The HT660 device has a bidirectional I<sup>2</sup>C interface that is compatible with the Inter IC (I<sup>2</sup>C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multi-master bus environment or wait-state insertion.

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus.

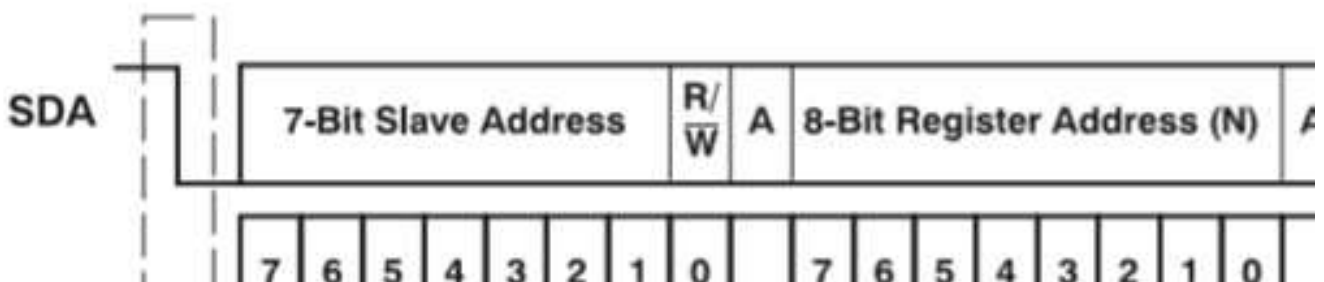


Figure 9 Typical I<sup>2</sup>C Sequence

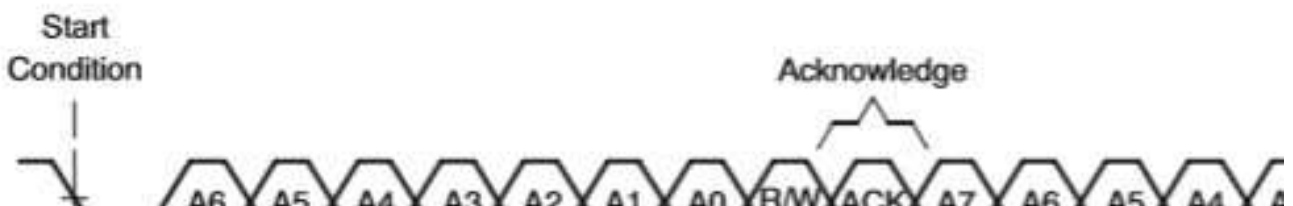


Figure 10 Single-Byte Write Transfer



Figure 11 Multiple-Byte Write Transfer



Figure 12 Single-Byte Read Transfer



Figure 13 Multiple-Byte Read Transfer

## 5 Register Map

Table6 Register Map

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
0x10	Digital Clipper Level DigClip[19:12]								FFh
0x11	Digital Clipper Level DigClip[11:4]								FFh
0x12	Digital Clipper Level DigClip[3:0]				SLEEP	SD	MUTE_A	SPEED	F0h
0x13	Data Format		Word_Length		TDM_Offset	TDM_Slot			00h
0x14	HPF Byps	Left_Mix	Right_Mix	Fade	MUTE_L	MUTE_R	Digital Boost		90h
0x15	Left channel volume control								CFh
0x16	Right channel volume control								CFh
0x17	ch_Shift	Fade_Mode	SCLK_DET_EN	CLK_DET_EN	Reserved		CLK_Error	SCLK_Error	33h
0x18	Reserved	Analog Gain			PBTL	Reserved			02h
0x19	Modulation	Spread Spectrum			Reserved			Gain_Group	70h

The register details are as follows. The **blue fonts** are the default settings when powering on.

### Register Address: 0x10 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[19:12]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

### Register Address: 0x11 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[11:4]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

The digital clipper level determined by DigClip[19:0] is the maximum output threshold level from DAC transferring to the analog Amplifier. The default value of the digital clipper level is the full scale of DAC output, and decreasing the value of DigClip[19:0] will decrease the digital clipper level as well.

### Register Address: 0x12 (default F0h)

Bit	R/W	Label	Default	Description
7:4	R/W	DigClip[3:0]	1111	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.
3	R/W	SLEEP	0	<b>0: the device is not in the SLEEP mode;</b> 1: the device is in the SLEEP mode. In sleep mode, the analog Amp is muted, and the digital circuit works with lower current dissipation.
2	R/W	SD	0	<b>0: the device is shut down;</b> 1: the device is not shut down; Notice that if the device is truly shutdown also depends on the $\overline{\text{SD}}$ pin, see 4.2.
1	R/W	MUTE_A	0	<b>0: The analog Amp output is not muted</b> 1: The analog Amp output is muted
0	R/W	SPEED	0	<b>0: Serial Audio Port will accept sample rates between 8k – 96kHz</b> 1: Serial Audio Port will accept sample rates between 96kHz-192kHz

**Register Address: 0x13 (default 00h)**

Bit	R/W	Label	Default	Description
7:6	R/W	Format	00	Control the Serial Audio Port data format 00: I <sup>2</sup> S 01 : Left justified 10: Right justified 11: TDM
5:4	R/W	Word_Length	00	Control the Serial Audio Port sample word length 00: 32bits 01: 24 bits 10: 20bits 11: 16bits
3	R/W	TDM_Offset	0	Control the offset of TDM data in the audio frame. The offset is defined as the number of SCLK from starting (MSB) of audio frame to the starting of the desired audio sample, see Figure 5 TDM Audio Data Format. 0: offset = 0 SCLK 1: offset = 1 SCLK
2:0	R/W	TDM_Slot	000	Control the slot number of TDM data in the audio frame. The slot number is defined as Figure 5 TDM Audio Data Format. 000: Slot0_A + Slot0_B; 001: Slot1_A + Slot1_B; ... 111: Slot7_A + Slot7_B;

**Register Address: 0x14 (default 90h)**

Bit	R/W	Label	Default	Description
7	R/W	HPF Byps	1	0: The internal high-pass filter in the digital path is bypassed 1: The internal high-pass filter in the digital path is not bypassed
6	R/W	Left_Mix	0	0: Left channel mixer is disabled 1: Left channel mixer is enabled, so that left = 1 / 2(left+right)
5	R/W	Right_Mix	0	0: Right channel mixer is disabled 1: Right channel mixer is enabled, so that right = 1 / 2(left+right)
4	R/W	Fade	1	0: Volume fading is disabled; 1: Volume fading is enabled
3	R/W	MUTE_L	0	MUTE the L channel digital output: 0: the left channel is not muted 1: the left channel is muted
2	R/W	MUTE_R	0	MUTE the R channel digital output: 0: the right channel is not muted 1: the right channel is muted
1:0	R/W	Dig Bst	00	Digital Boost setting 00: +0dB is added to the signal in the digital path 01: +6dB is added to the signal in the digital path 10: +12dB is added to the signal in the digital path 11: +18dB is added to the signal in the digital path



**Register Address: 0x15 (Default CFh)**

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_L	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB .....Gain decreased by 0.5dB every step <b>1100,1111: 0dB</b> .....Gain decreased by 0.5dB every step 0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

**Register Address: 0x16 (Default CFh)**

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_R	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB .....Gain decreased by 0.5dB every step <b>1100,1111: 0dB</b> .....Gain decreased by 0.5dB every step 0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

**Register Address: 0x17 (default 33h)**

Bit	R/W	Label	Default	Description
7	R/W	ch_Shift	0	<b>0: The left and right channels are not shifted</b> 1: The left and right channels are shifted
6	R/W	Fade_Mode	0	<b>0: The volume is fading by 0.5dB/8T<sub>LRCK</sub></b> 1: The volume is fading by 0.5dB/T <sub>LRCK</sub>
5	R/W	SCLK_DET_EN	1	SCLK error detection, such as SCLK missing detection, SCLK range detection, SCLK/LRCK detection. If error detection is enabled, once any such error is detected, the relevant error flag will change to 1. 0: SCLK error detection is disabled; <b>1: SCLK error detection is enabled.</b>
4	R/W	CLK_DET_EN	1	Audio serial port clock error detection, including SCLK, MCLK, LRCK. Once any error such as missing or wrong range of these clocks is detected, the relevant error flag will change to 1. 0: CLOCK error detection is disabled; <b>1: CLOCK error detection is enabled.</b>
3:2	R	Reserved	00	Unused, make it always 00
1	R	CLK_Error	1	Changes to 0 when Clock Error is detected; <b>back to 1 when Clock Error evacuated;</b>
0	R	SCLK_Error	1	Changes to 0 when SCLK Error is detected; <b>back to 1 when SCLK Error evacuated;</b>

**Register Address: 0x18 (Default 02h)**

Bit	R/W	Label	Default	Description
7	R	Reserved	0	Unused, make it always 0
6:4	R/W	A_GAIN	000	Set analog gain: <b>000: Gain0 = 19.3dB; Gain1 = 28.4dB</b> 001: Gain0 = 13.4dB; Gan1 = 16.7dB 010: Gain0 = 13.4dB; Gan1 = 16.7dB      011: Gain0 = 13.4dB; Gan1 = 16.7dB 100: Gain0 = 17.2dB; Gan1 = 23.2dB      101: Gain0 = 13.4dB; Gan1 = 16.7dB 110: Gain0 = 15.5dB; Gan1 = 20.0dB      111: Gain0 = 13.4dB; Gan1 = 16.7dB
3	R/W	PBTL	0	<b>0: BTL mode; 1: PBTL mode.</b>
2:0	R	Reserved	010	Unused, make it always 010

**Register Address: 0x19 (default 70h)**

Bit	R/W	Label	Default	Description
7	R/W	Modulation	0	<b>0: BD mode</b> ; 1: 1SPW mode The modulation is only changed when the device is brought from shutdown back into operation after this bit is changed.
6:4	R/W	Spread	111	<b>111: Spread Spectrum on</b> 011: Spread Spectrum off Spread Spectrum function is only switched when the device is brought from shutdown back into operation after this bit is changed.
3:1	R	Reserved	000	Unused, make it always 000
0	R/W	GAIN_Group	0	Select gain group for A_GAIN (register 0x18, bit [6:4]. <b>0: Gain0</b> ; 1: Gain1 The gain group is only changed when the device is brought from shutdown back into operation after this bit is changed.

## 6 Typical Applications

### 6.1 Startup Procedures

1. Configure I/O pins (ADR[1:0]);
2. \SD pin = Low;
3. Bring up power supplies (it does not matter if PVDD, AVDD or DVDD comes up first, provided the device is held in shutdown);
4. Once power supplies are stable, start MCLK, SCLK, LRCK;
5. Configure the device via the control port in the manner required by the use case; especially bit “PBTL”, “Format” (as “A” shown in the following figure)..
6. Once power supplies and clocks are stable and the control port has been programmed, bring \SD pin High, or write bit “SD” (Bit 2 of Register 0x12) as 1;
7. The device is now in normal operation. Fade in SDIN if needed. The device is still configurable through IIC port. (as “B” shown in the following figure)

The sequence diagram is shown in Figure 14 and Table 7.

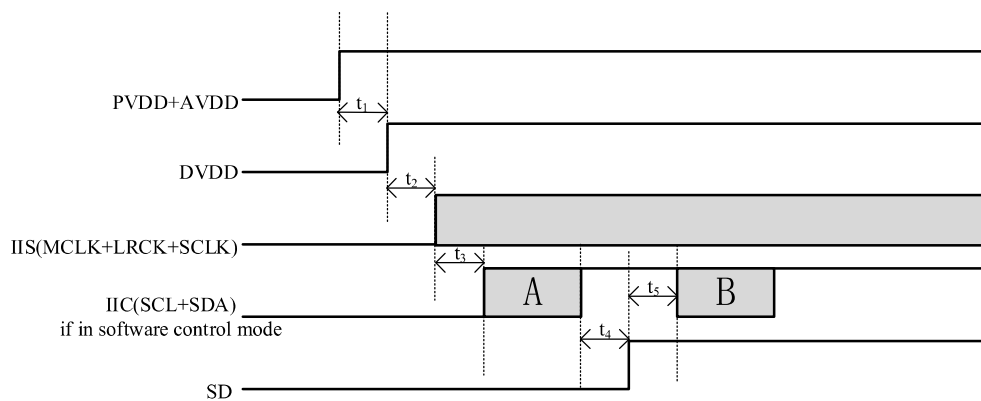


Figure 14 Power-on Sequence

Table 7 Recommendations for Power-on Timing

Symbol	CONDITION	MIN	TYP	MAX	UNIT
t1		0			ms
t2		0			ms
t3		1			ms
t4		1			ms
t5		200			ms

### 6.2 Power down Procedures

1. The device is in normal operation;
2. Fade out SDIN if needed. The device is configurable through IIC port before power off;
3. Pull \SD pin Low, or write bit “SD” (Bit 2 of Register 0x12) as 0;
4. The clocks can be stopped, and power supplies brought down;
5. The device is now fully shutdown and powered off.

The sequence diagram is shown in Figure 15 and Table8.

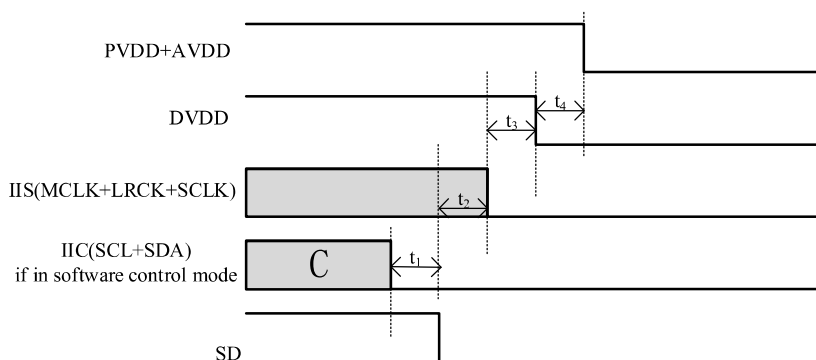


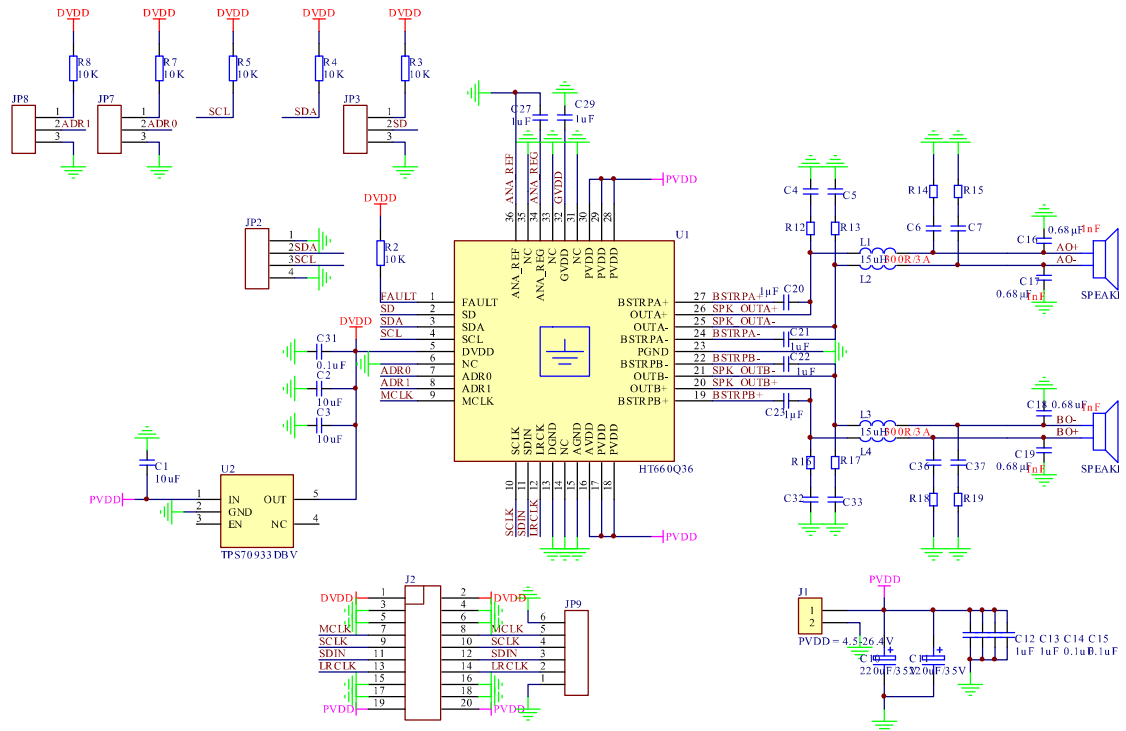
Figure 15 Power-off Sequence

Table8 Recommendations for Power-off Timing

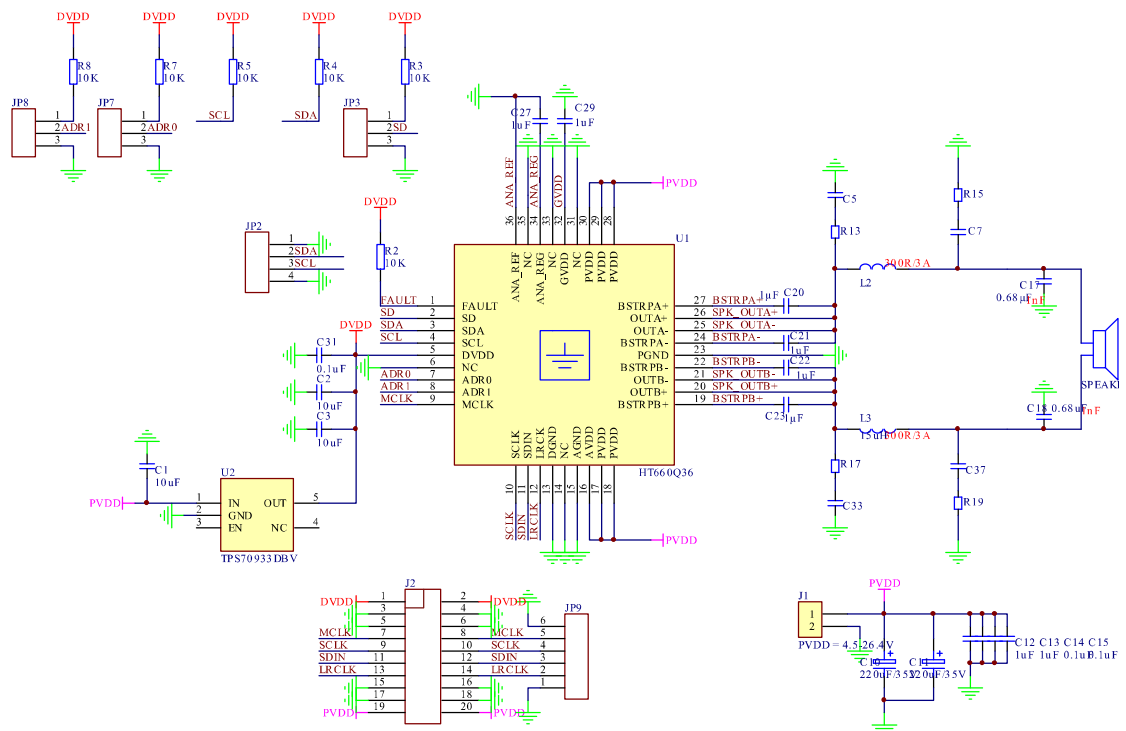
Symbol	CONDITION	MIN	TYP	MAX	UNIT
t <sub>1</sub>		1			ms
t <sub>2</sub>	Fade-out disabled	1			ms
	Fade-out enable	45			ms
t <sub>3</sub>		1			ms
t <sub>4</sub>		0			ms

### 6.3 Circuit Diagrams

#### BTL Mode

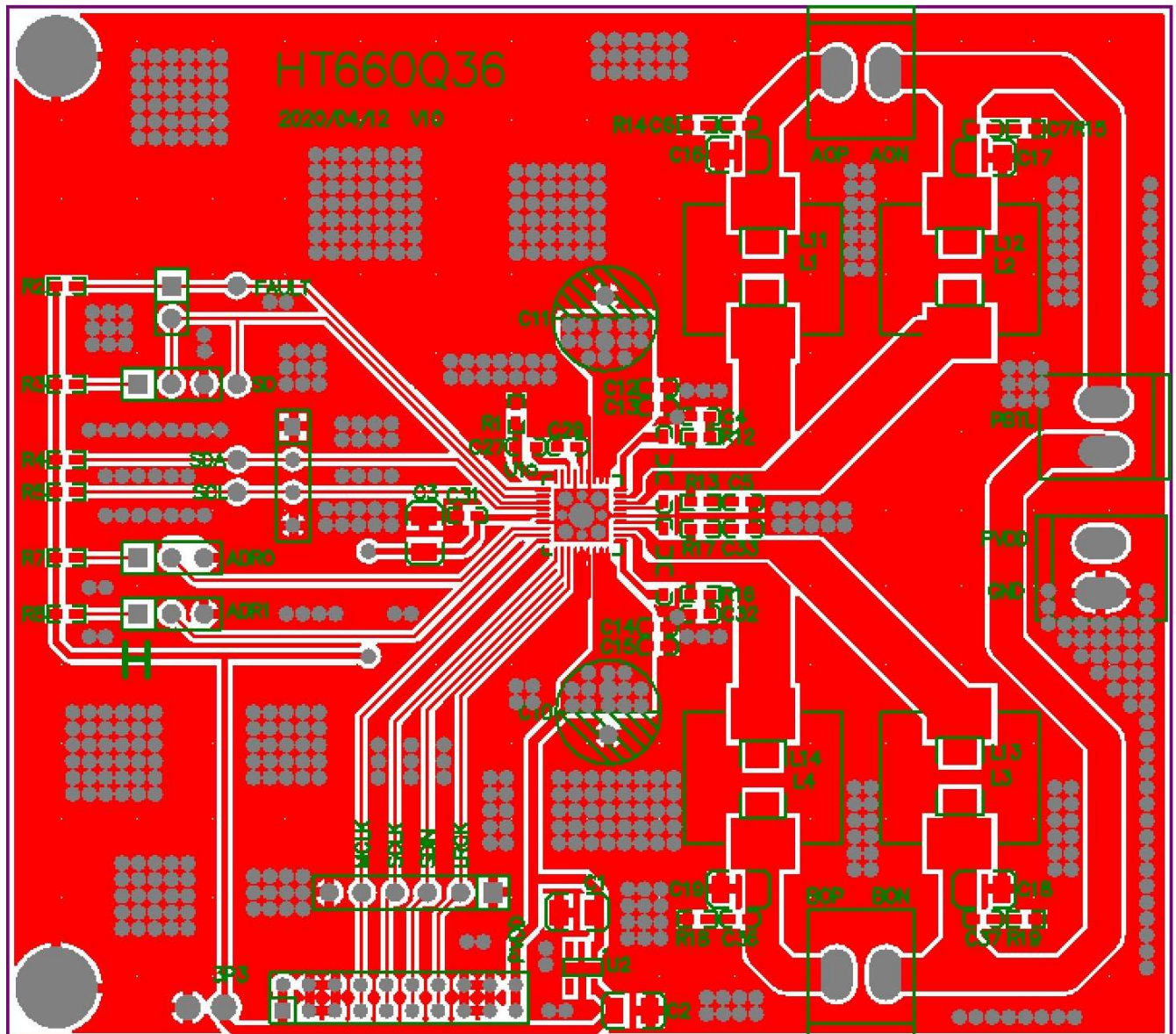


#### PBTL Mode

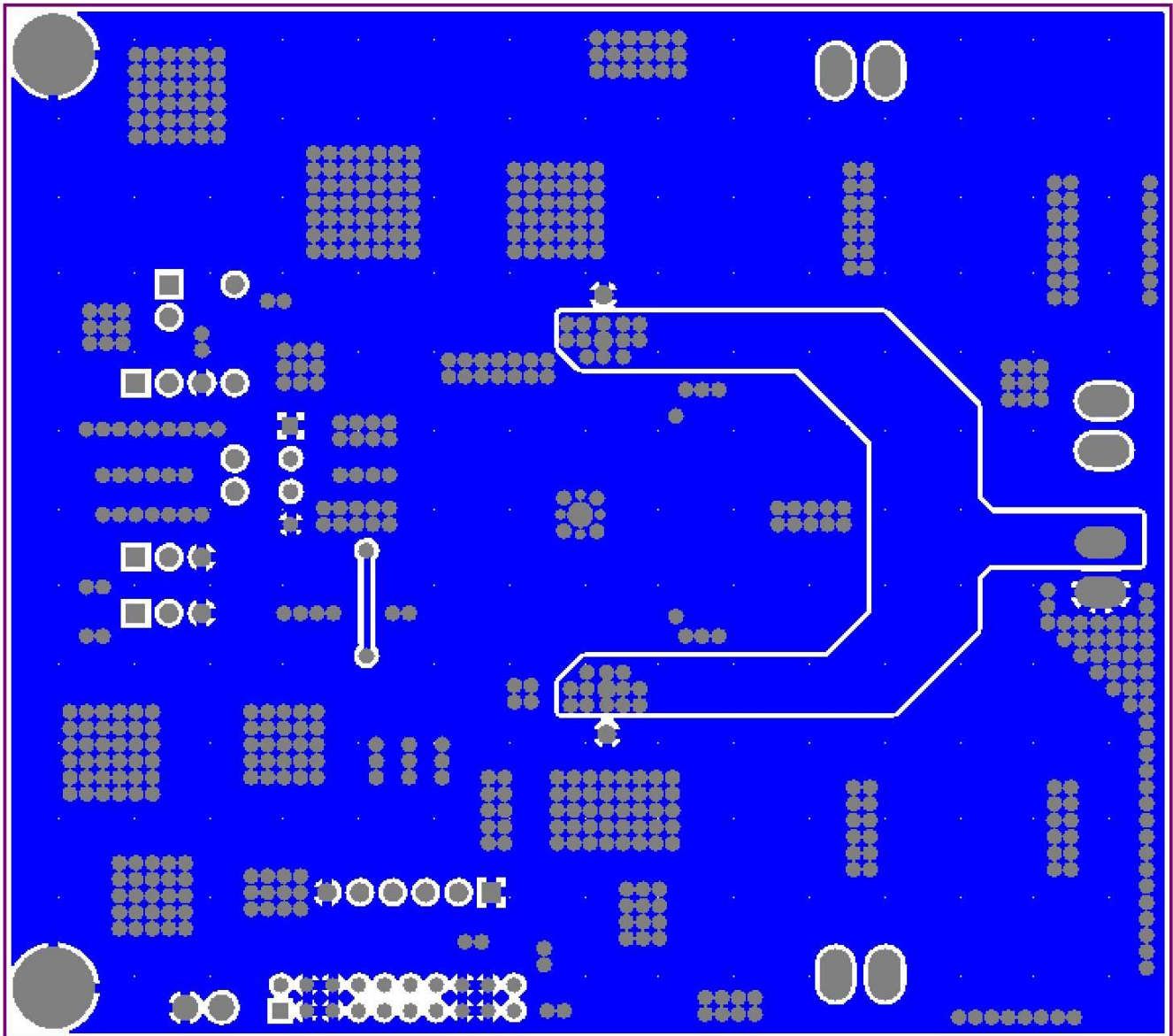


7 PCB Layout

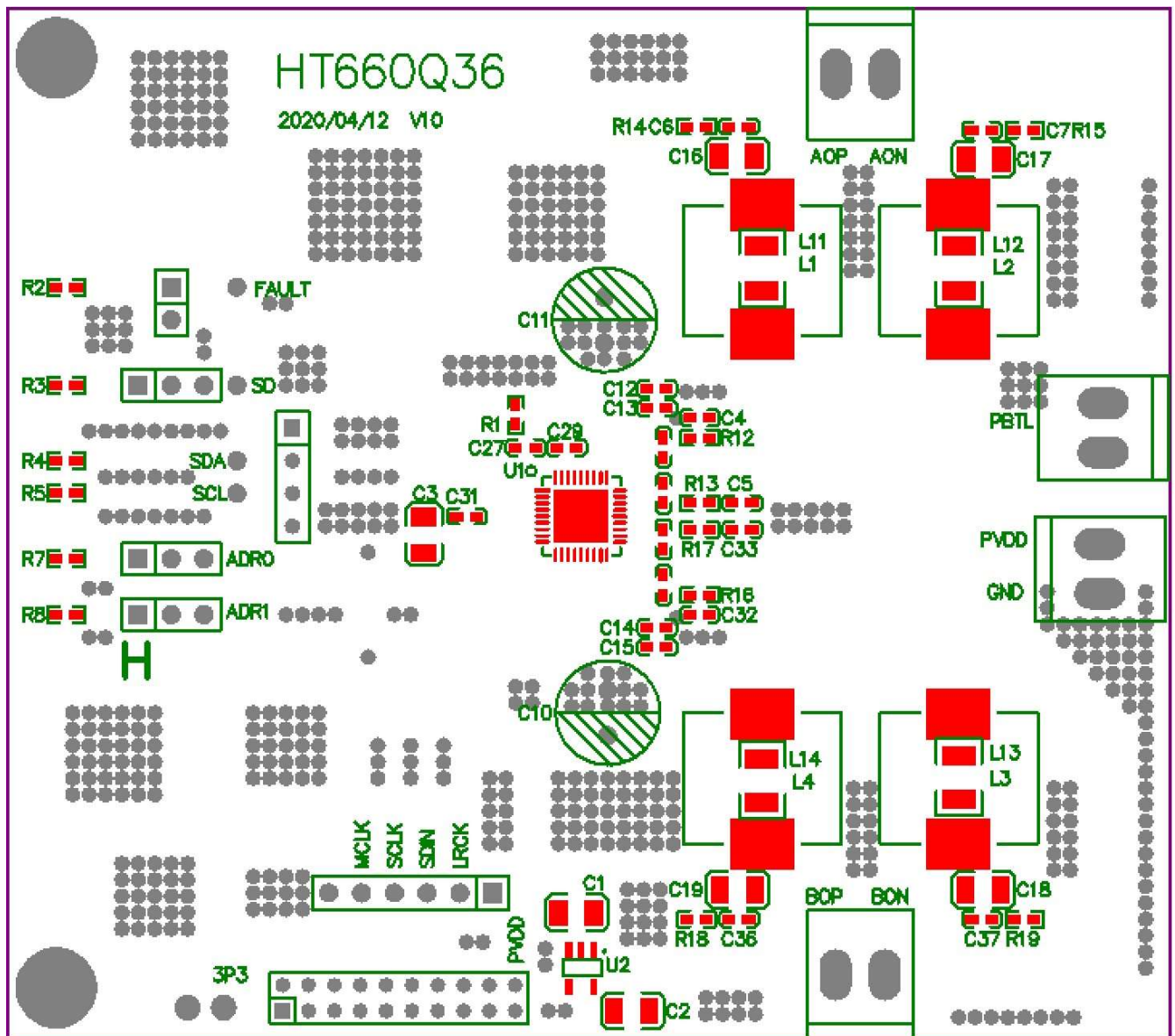
7.1 Top Layout



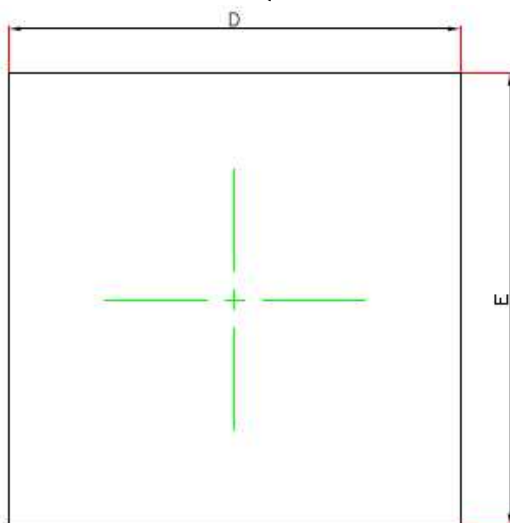
7.2 *Bottom Layout*



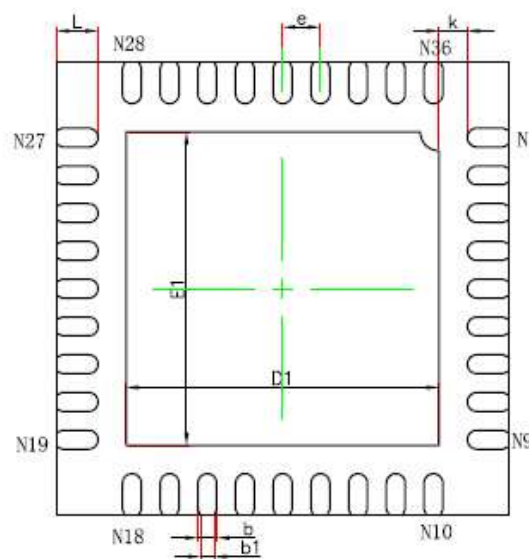
7.3 TopOverlayer



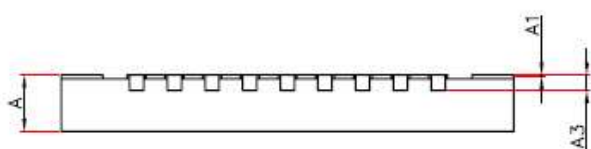


**PACKAGE OUTLINE**
**QFN36L 6\*6 with exposed thermal pad**


TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	5.900	6.100	0.232	0.240
E	5.900	6.100	0.232	0.240
D1	4.050	4.250	0.159	0.167
E1	4.050	4.250	0.159	0.167
b	0.180	0.300	0.007	0.012
b1	0.130	0.230	0.005	0.009
e	0.500TYP.		0.020TYP.	
k	0.200MIN.		0.008MIN.	
L	0.500	0.600	0.020	0.024