8-Bit Serial-In/Parallel-Out Shift Register

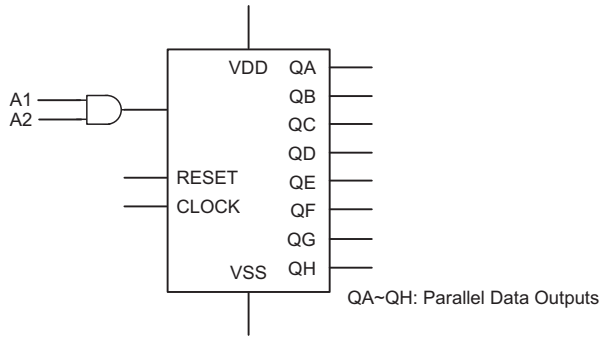
Features

- Operating voltage: 2.0V~6.0V
- A 8-bit, serial-input to parallel-output shift register
- Gated serial data inputs
- Asynchronous master reset
- Output drive capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS
- High noise immunity characteristic of CMOS Devices.
- 14-pin DIP/SOP package

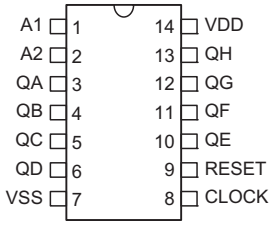
General Description

The HT74164 is identical in pin-out to the LS164. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. The HT74164 is a 8-bit, serial input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active low asynchronous reset overrides the Clock and Serial Data inputs.

Block Diagram



Pin Assignment



HT74164
14 DIP-A/SOP-A

Pin Description

Pad No.	Pad Name	I/O	Function
1, 2	A1, A2	I	Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register both A1 and A2 inputs must be high, thereby allowing one input to be used as a data enable input. When only one serial input is used, the other must be connected to VDD.
3~6, 10~13	QA~QD QE~QH	O	Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or non-inverted form.
7	VSS	—	Negative power supply, ground
8	CLOCK	I	Shift Register Clock. A positive going transition on this pin shifts the data at each stage to the next stage. The shift register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.
9	RESET	I	Active low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip flops and sets Outputs QA~QH to the low level state.
14	VDD	—	Positive power supply

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.5V to V_{SS}+7.0V

Input Voltage ..... V_{SS}–1.5V to V_{DD}+1.5V

Output Voltage ..... V_{SS}–0.5V to V_{DD}+0.5V

Output Current ..... ±25mA

Storage Temperature ..... –65°C to 150°C

Operating Temperature ..... –40°C to 85°C

Input Current ..... ±20mA

Supply Current ..... ±50mA

Power Dissipation in Still Air (Plastic or Ceramic DIP) 750mW

Lead Temperature, 1mm from Case for 10 Seconds (Plastic DIP Package) ..... 260°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

Derating: Plastic DIP: 10mW/°C from 65°C to 125°C

Recommended Operating Conditions

Supply Voltage ..... V_{SS}+2.0V to V_{SS}+6.0V

Input Voltage ..... 0V to V_{DD}

Operating Temperature ..... –40°C to 85°C

Input Rise and Fall Time (Figure 1): VDD=2.0V ..... 0 ~ 1000ns

Input Rise and Fall Time (Figure 1): VDD=4.5V ..... 0 ~ 500ns

Input Rise and Fall Time (Figure 1): VDD=6.0V ..... 0 ~ 400ns

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.0	—	6.0	V
I_{DD}	Operating Current	6.0V	$V_{IN}=V_{DD}$ or V_{SS}, $I_{OUT}=0\mu A$	—	—	8.0	μA
V_{IH}	Input High Voltage	2.0V	$V_{OUT}=0.1V$ or $V_{DD}-0.1V$, $I_{OUT} \le 30\mu A$	1.5	—	—	V
		4.5V		3.15	—	—	V
		6.0V		4.2	—	—	V
V_{IL}	Input Low Voltage	2.0V	$V_{OUT}=0.1V$ or $V_{DD}-0.1V$, $I_{OUT} \le 30\mu A$	—	—	0.5	V
		4.5V		—	—	1.35	V
		6.0V		—	—	1.8	V
V_{OH}	Input Level High Voltage	2.0V	$V_{IN}=V_{IH}$ or V_{IL}, $I_{OUT} \le 30\mu A$	1.9	—	—	V
		4.5V		4.4	—	—	V
		6.0V		5.9	—	—	V
		4.5V	$V_{IN}=V_{IH}$ or V_{IL}, $I_{OUT}=-6mA$	3.84	—	—	V
		6.0V	$V_{IN}=V_{IH}$ or V_{IL}, $I_{OUT}=-7.8mA$	5.34	—	—	V
V_{OL}	Input Level Low Voltage	2.0V	$V_{IN}=V_{IH}$ or V_{IL}, $I_{OUT}=0.02mA$	—	—	0.1	V
		4.5V		—	—	0.1	V
		6.0V		—	—	0.1	V
		4.5V	$V_{IN}=V_{IH}$ or V_{IL}, $I_{OUT}=6mA$	—	—	0.26	V
		6.0V	$V_{IN}=V_{IH}$ or V_{IL}, $I_{OUT}=7.8mA$	—	—	0.26	V

A.C. Characteristics

Ta=25°C

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit
f_{MAX}	Maximum clock Frequency (50% Duty cycle) (See figure 1, figure 4)	2.0V	—	—	5	MHz
		4.5V	—	—	24	MHz
		6.0V	—	—	28	MHz
f_{PLH}, f_{PLH}	Maximum Propagation Delay, Clock to Q (See figure 1, figure 4)	2.0V	—	—	175	ns
		4.5V	—	—	35	ns
		6.0V	—	—	30	ns
f_{PHL}	Maximum Propagation Delay, Reset to Q (See figure 2, figure 4)	2.0V	—	—	205	ns
		4.5V	—	—	41	ns
		6.0V	—	—	35	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (See figure 1, figure 4)	2.0V	—	—	75	ns
		4.5V	—	—	15	ns
		6.0V	—	—	13	ns
C_{IN}	Maximum Input Capacitance	—	—	—	10	pF

Note: For propagation delays with load other than 50pF.

Timing Requirements Ta=25°C

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit
t_{su}	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0V	75	—	—	ns
		4.5V	15	—	—	ns
		6.0V	13	—	—	ns
t_h	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0V	4	—	—	ns
		4.5V	4	—	—	ns
		6.0V	4	—	—	ns
t_{REC}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0V	5	—	—	ns
		4.5V	5	—	—	ns
		6.0V	5	—	—	ns
t_{W1}	Minimum Pulse Width, Clock (Figure 1)	2.0V	100	—	—	ns
		4.5V	20	—	—	ns
		6.0V	17	—	—	ns
t_{W2}	Minimum Pulse Width, Reset (Figure 1)	2.0V	75	—	—	ns
		4.5V	15	—	—	ns
		6.0V	13	—	—	ns
t_r, t_f	Rise/Fall Maximum Input Rise and Fall Times (Figure 1)	2.0V	—	—	1000	ns
		4.5V	—	—	500	ns
		6.0V	—	—	400	ns

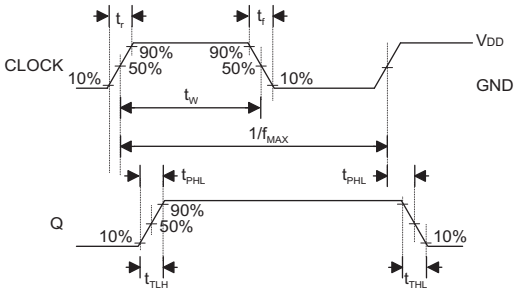


Figure 1

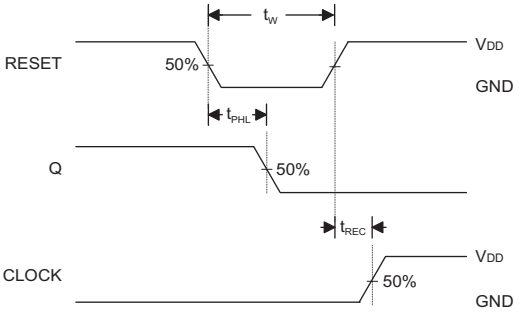


Figure 2

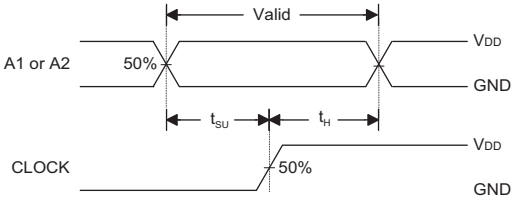
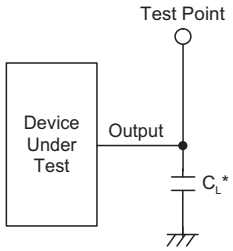


Figure 3



Note: * Including scope

Figure 4

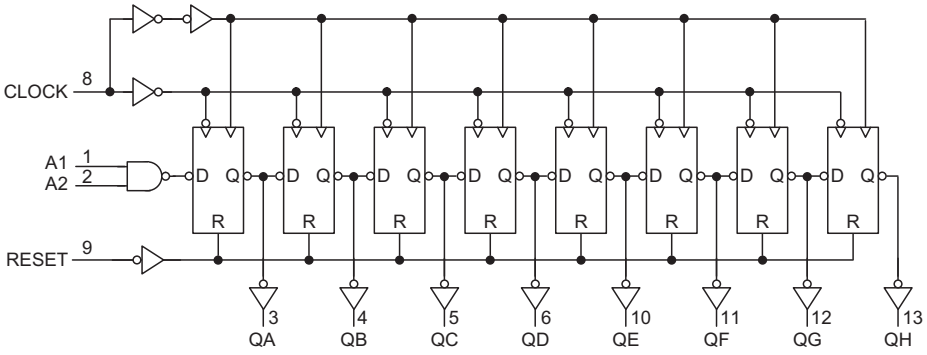
Functional Description

Input				Output			
Reset	**Clock**	**A1**	**A2**	**QA**	**QB**	**.....**	**QL**
L	X	X	X	L	L	.....	L
H	↓	X	X	X	X	.....	X
H	↑	H	D	D	QA	.....	QH
H	↑	D	H	D	QA	.....	QH

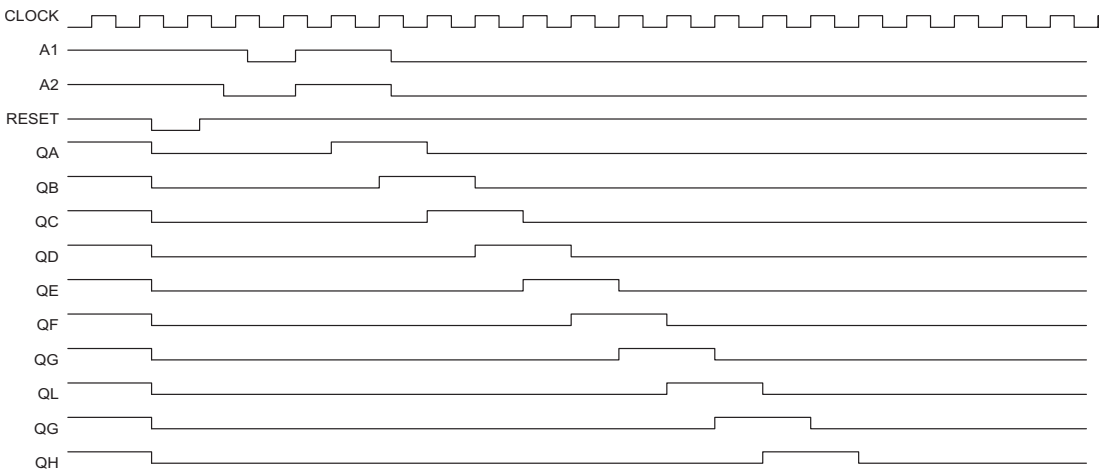
Note: ″D″ data input

″QA~QH″ data shifted from preceding stage on a rising edge at the clock input.

Expanded Logic Diagram

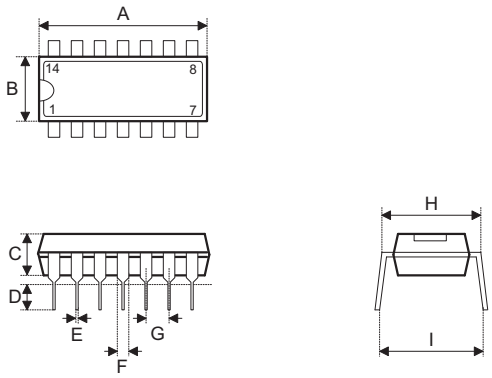


Timing Diagrams



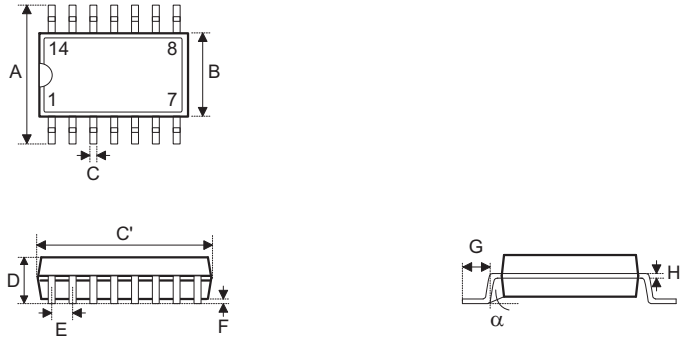
Package Information

14-pin DIP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	745	—	775
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	—	—	375

14-pin SOP (150mil) Outline Dimensions

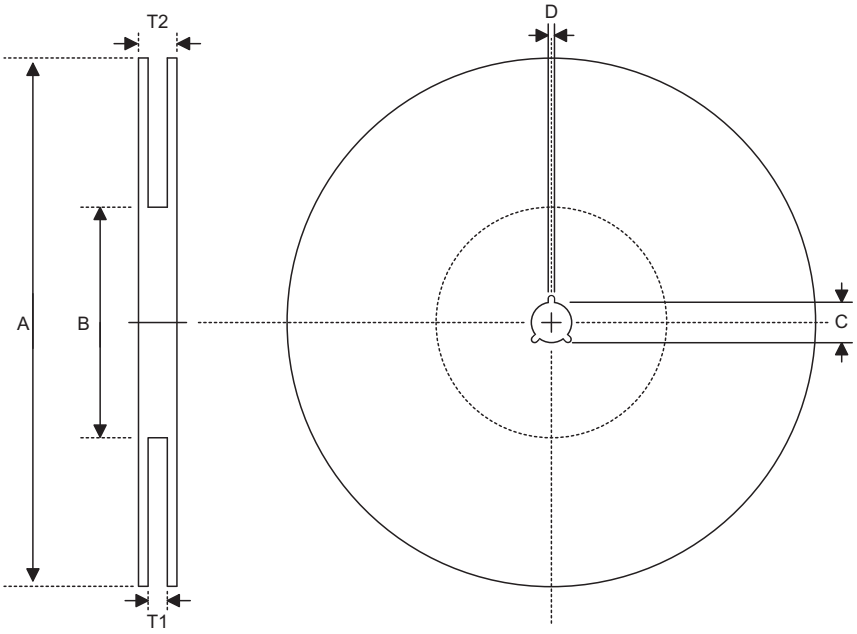


- MS-012

Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	150	—	157
C	12	—	20
C′	337	—	344
D	—	—	69
E	—	50	—
F	4	—	10
G	16	—	50
H	7	—	10
α	0°	—	8°

Product Tape and Reel Specifications

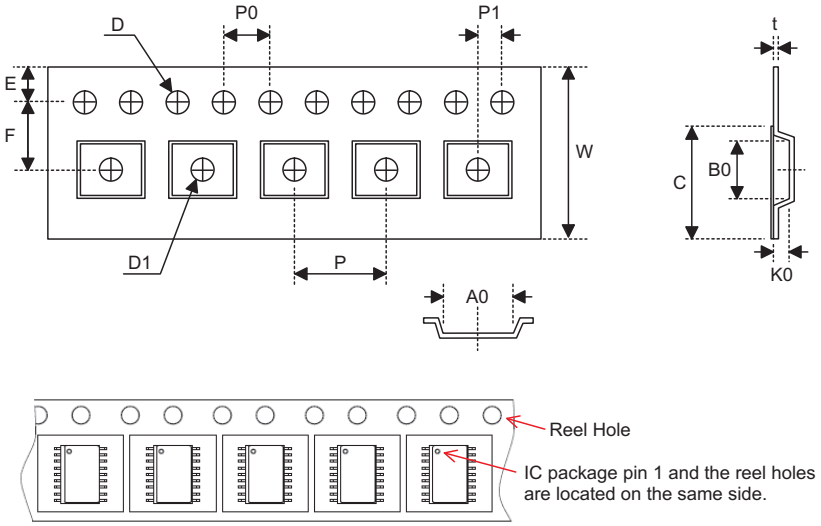
Reel Dimensions



SOP 14N

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	16.8 $^{+0.3/-0.2}$
T2	Reel Thickness	22.2±0.2

Carrier Tape Dimensions



SOP 14N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0 +0.3/-0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	1.5 +0.1/-0.0
D1	Cavity Hole Diameter	1.50 +0.25/-0.00
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.5±0.1
B0	Cavity Width	9.5±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	13.3±0.1