3 to 8 Cell Analog Front End for Li-Battery Protection

HT7Q2552

Revision: V1.30 Date: October 30, 2025

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Features

- V_{IN} input ranges from 7.5V to 36V
- Individual cell voltage monitor outputs 1/2 of battery cell voltage, when the analog output is 2.1V, it has an accuracy of ±7.5mV
- Internal cell balance switches
- Integrated voltage regulator with 5V/50mA and ±1% accuracy
- At Ta=-40°C~85°C, 2.5V reference voltage output with a maximum variation of 15mV in temperature drift
- Two Discharge N-type MOSFET gate drivers
- Single Charge N-type MOSFET gate driver
- Charge/Discharge differential current monitor:
    - IMON pin outputs amplified ISP-ISN differential voltage
    - Voltage amplifying rate selection: 10/50
- Discharge short-current detection:
    - Detection threshold voltage selection: 50mV/100mV/150mV/200mV/250mV/300mV/350mV/400mV
    - Detection debounce time selection: 0μs~992μs, 32 sections, 32μs per section
- Integrated Over-temperature protection selection: 85°C/100°C/125°C/150°C
- Sleep mode with 0.1μA ultra-low standby current
- Two High-voltage wake-up functions
- I^2C bus communication with host MCU
- Operating temperature range: -40°C to +85°C
- Package type: 32-pin QFN

Applications

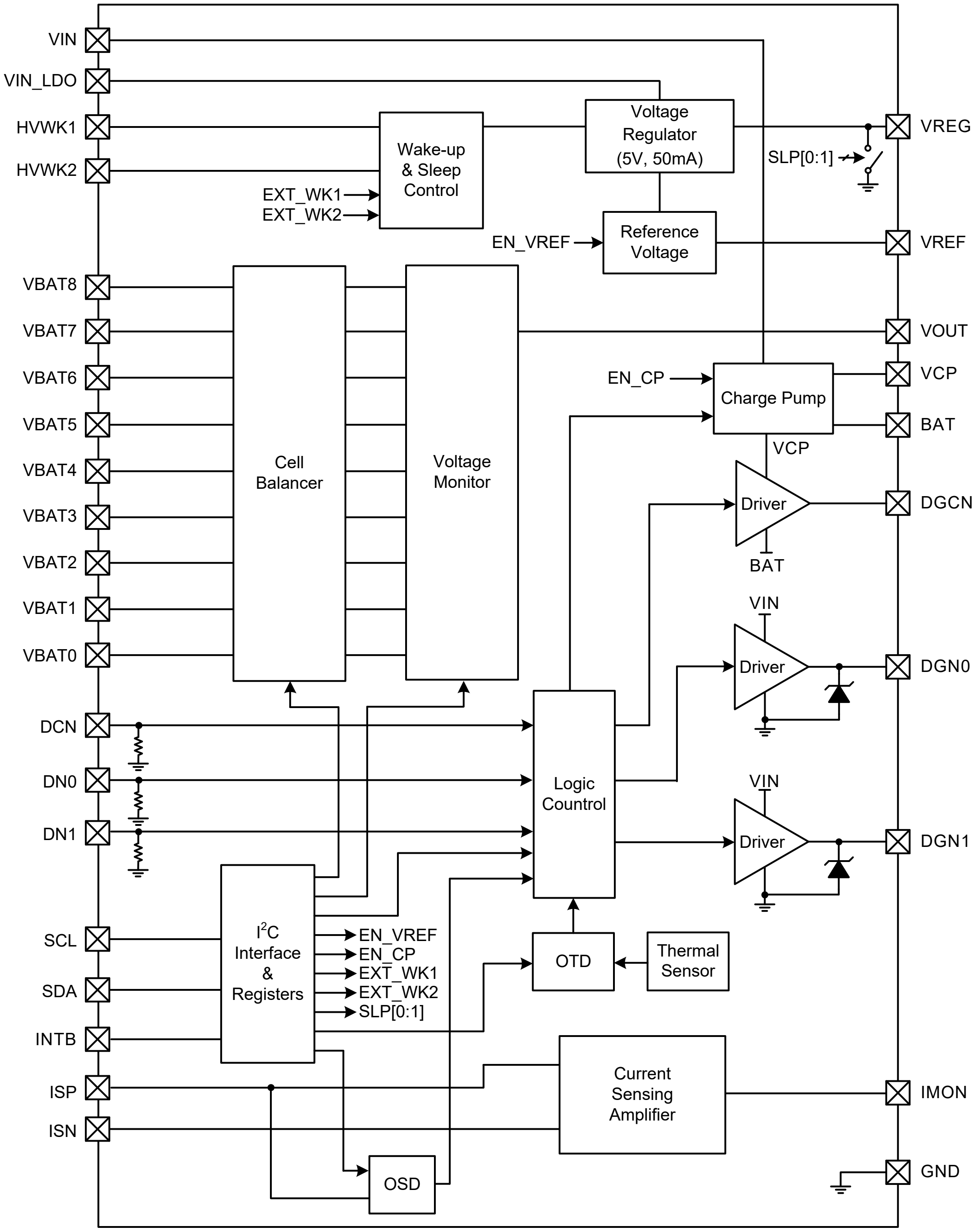
- Handheld vacuum cleaners
- Electric power tools

General Description

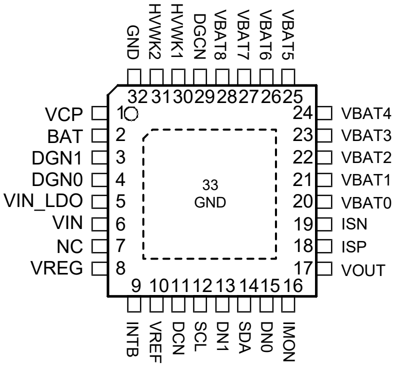
The HT7Q2552 is a high voltage analog-front-end IC for 3 to 8 cell Li-ion rechargeable battery protection. It consists of a 5V high accuracy regulator, an accuracy 2.5V reference voltage output, an individual cell voltage monitor, two discharge paths, i.e., low-side power switch gate drivers, a charge path, i.e., high-side power switch gate driver, a charge/discharge differential current monitor, and a discharge short-current protection. The cell voltage monitor is designed to monitor each battery cell voltage individually and outputs the divide-by-2 voltage to the analog multiplexer with ±7.5mV accuracy. The current monitor channel provides charge and discharge current monitoring and short-current protection. The device can directly drive external N-type MOSFETs to control charge and discharge by charge and discharge gate drivers. The internal battery balance circuitry provides a cell balance current without the need of external transistors. Each monitored battery cell voltage can be observed sequentially from VBAT1 to VBAT8 which benefits MCUs with a lower number of ADCs.

An integrated 5V regulator provides a 5V supply to the MCU with a 50mA driving current capability and which has ±1% accuracy. The voltage regulator, cell voltage monitor, current monitor, and gate drivers are shut down with an ultra-low standby current 0.1μA when the device is in the Sleep mode. When the HVWK1 or HVWK2 pin is triggered by a voltage greater than its threshold, the device will return to the normal operating status.

Functional Block Diagram



Pin Assignment



HT7Q2552
32 QFN-A

Pin Description

Pin No.	Name	Type	Pin Description
1	VCP	O	Charge pump capacitor for DGCN. Connect a capacitor between VCP and BAT
2	BAT	O	Charge pump capacitor for DGCN. Connect a capacitor between VCP and BAT
3	DGN1	O	Gate driver output 1 for driving discharge n-MOSFET. Recommended for applying on secondary loading path.
4	DGN0	O	Gate driver output 0 for driving discharge n-MOSFET. Recommended for applying on primary loading path.
5	VIN_LDO	P	Input supply voltage for regulator
6	VIN	P	Input supply voltage for gate drivers
7	NC	—	Not connected
8	VREG	O	Regulator 5V/50mA output. Connect 4.7μF capacitor typically
9	INTB	O	Interrupt output pin of short current detection for MCU. NMOS open drain output and output an ‘L’ level pulse when short-current event is detected.
10	VREF	O	Reference voltage 2.5V output pin
11	DCN	I	Gate driver DGCN control input*
12	SCL	I/O	I^2C serial clock line
13	DN1	I	Gate driver DGN1 control input*
14	SDA	I/O	I^2C data clock line
15	DN0	I	Gate driver DGN0 control input*
16	IMON	O	Current monitor output pin. Voltage of ISP-ISN multiplied by 10 or 50 is outputted.
17	VOUT	O	Voltage monitor output
18	ISP	I	Current monitor positive terminal voltage input pin. The voltage level of ISP pin should be higher than that of ISN in discharge state.
19	ISN	I	Current monitor negative terminal voltage input pin. Connected to the most negative terminal of battery cells.
20	VBAT0	I	Battery cell 1 negative terminal
21	VBAT1	I	Battery cell 1 positive terminal and battery cell 2 negative terminal
22	VBAT2	I	Battery cell 2 positive terminal and battery cell 3 negative terminal
23	VBAT3	I	Battery cell 3 positive terminal and battery cell 4 negative terminal
24	VBAT4	I	Battery cell 4 positive terminal and battery cell 5 negative terminal
25	VBAT5	I	Battery cell 5 positive terminal and battery cell 6 negative terminal
26	VBAT6	I	Battery cell 6 positive terminal and battery cell 7 negative terminal

Pin No.	Name	Type	Pin Description
27	VBAT7	I	Battery cell 7 positive terminal and battery cell 8 negative terminal
28	VBAT8	I	Battery cell 8 positive terminal
29	DGCN	O	Gate driver output for driving charge n-MOSFET
30	HVWK1	I	Sense and trigger pin of High voltage Wake-up function 1.
31	HVWK2	I	Sense and trigger pin of High voltage Wake-up function 2.
32	GND	G	Ground terminal
EP	GND	G	Connected to GND

Note: I: Input; O: Output; P: Power; G: Ground;
*: Internal pull down with 370kΩ.

Absolute Maximum Ratings

Pin/Parameter		Value	Unit
VIN, VIN_LDO, HVWK1, HVWK2, BAT		-0.3 to +48	V
DGCN, VCP		-0.3 to +60.0	V
VREG		-0.3 to +5.5	V
DGN0, DGN1		-0.3 to 18	V
VOUT, SCL, SDA, DN0, DN1, DCN, ISP, ISN, IMON, INTB, VREF		-0.3 to +5.5	V
∆[VBATi~VBAT(i-1)], i=8, 7, 6, 5, 4, 3, 2, 1		-0.3 to +5.5	V
Operating Temperature Range		-40 to +85	°C
Maximum Junction Temperature		+125	°C
Storage Temperature Range		-60 to +150	°C
Lead Temperature (Soldering 10sec)		+260	°C
ESD Susceptibility	Human Body Model	±2000	V
	Machine Model	±200	V
Junction-to-Ambient Thermal Resistance, θ_{JA}	32QFN (4×4)	47	°C/W

Recommended Operating Range

Pin / Parameter	Value	Unit
V_{IN}	7.5 to 36	V
T_A	-40 to +85	°C

Note that Absolute Maximum Ratings indicate limitations beyond which damage to the device may occur. Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specified performance limits.

Electrical Characteristics

V_{IN}=36V, C_{REG}=4.7μF, Ta=+25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply and Input						
V_{IN}	Supply Voltage	—	7.5	—	36.0	V
$I_{IN(STB)}$	Supply Current (Standby)	EN_S=EN_VREF=IMCE=ISCE='0' EN_OTD=EN_TS='0' DN0=DN1=DCN='0'	—	3.5	6.0	μA
$I_{IN(STB\_DSG)}$	VIN Supply Current with DGN0 and Short Current Detection is Activated	EN_S=EN_VREF=IMCE= EN_OTD=EN_TS='0' ISCE='1', DN0='1', DN1=DCN='0'	—	18	20	μA

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{OPR_DGNx}	VIN Operating Current when DGN0 and DGN1 Outputs are On	DN0=DN1='1', DCN='0'	—	15	—	μA
I_{SLP}	Standby Current in SLEEP Mode	SLP1='0', SLP0='1', V_{HVWK}=0V	—	0.1	0.2	μA
Voltage Regulator						
V_{REG}	Regulator Output Voltage	I_{LOAD}=10mA	4.95	5.00	5.05	V
I_{REG}	Regulator Maximum Output Current	V_{IN}=7.5V, Ta=-40~85°C	50	—	—	mA
ΔV_{REG}	Load Regulation	I_{LOAD}=0~50mA	—	—	50	mV
$\frac{\Delta V_{REG}}{(V_{REG}\times\Delta V_{IN})}$	Line Regulation	V_{IN}=7.5~36V, I_{LOAD}=10mA	—	0.02	—	%/V
$\frac{\Delta V_{REG}}{(V_{REG}\times\Delta Ta)}$	V_{REG} Temperature Coefficient	I_{LOAD}=1mA, Ta=-40~85°C	—	±100	—	ppm/°C
R_{DIS}	V_{REG} Discharge Resistance	SLP1='0', SLP0='1', V_{REG}=1V, I_{REG1} denotes VREG input current at V_{REG}=1V, $R_{DIS}=V_{REG}/I_{REG1}$	—	330	—	Ω
Cell Balancer						
R_{CB}	Cell Balance Resistance	V_{Bi}=4.5V (i=1~8), VBATi series resistors=0Ω	80	110	140	Ω
		V_{Bi}=2.5V (i=1~8), VBATi series resistors=0Ω	120	160	200	Ω
Reference Voltage						
V_{REF}	Reference Voltage	EN_VREF='1'	2.492	2.500	2.508	V
ΔV_{REF} (Note)	VREF Temperature Coefficient	I_{LOAD}=1μA, Ta=-40~85°C	—	—	±15	mV
I_{VREF_SOUR}	VREF Pin Output Source Current	C_{VREF}=0.1μF. Peak current at EN_VREF '0'→'1' rising edge	—	2	—	mA
I_{VREF_SINK}	VREF Pin Output Sink Current	C_{VREF}=0.1μF. Peak current at EN_VREF '1'→'0' falling edge	—	1	—	mA
t_{S_VREF}	VREF Pin Settling Time	Settling time from V_{REF}=0V to 2.475V, C_{VREF}=30pF	—	20	30	μs
Input/Output Logic						
V_{IL}	DN0, DN1, DCN Input Logic Low voltage	—	—	—	1.5	V
V_{IH}	DN0, DN1, DCN Input Logic High Holtage	—	3.5	—	—	V
R_{PD}	DN0, DN1, DCN Pull Down Resistance	—	—	370	—	kΩ
$V_{L(INTB)}$	INTB 'Low' Output Voltage	Load current=500μA, V_{REG}=5V	—	—	0.1	V
High Voltage Wake-Up						
V_{WKTH}	HVWK1 and HVWK2 Threshold Voltage	—	—	5.5	—	V
T_{WKDB}	HVWK1 and HVWK2 Debounce Time	—	1	—	—	ms
I_{WK}	HVWK1 and HVWK2 Input Current	V_{HVWK}=36V	—	50	—	μA

Note: Design guaranteed.

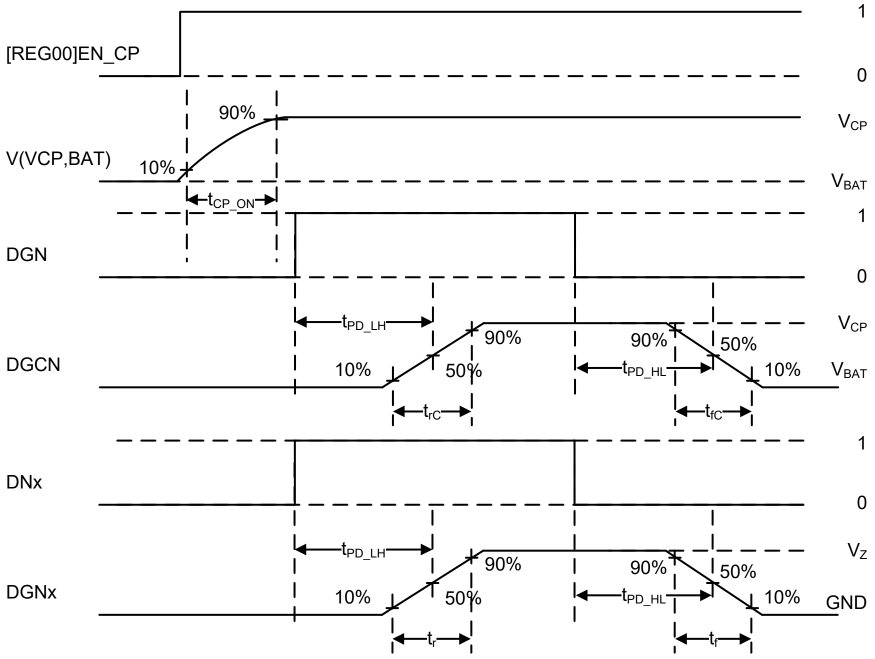
Electrical Characteristics (Continue)

V_{IN}=36V, C_{REG}=4.7μF and Ta=+25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Cell Voltage Monitor						
V_{Bi}	Cell Voltage	i=1~8	1.5	—	4.5	V
$V_{B(MIN)}$	Input Voltage between VBATi and VBATi-1 for Cell Voltage Monitoring	—	—	1.5	—	V
$I_{Bi(PWR)}$	Cell Input Leakage Current when VIN Powered	V_{Bi}=5V (i=1~8). EN_S=‘0’. V_{IN}=V_{BAT8}	-0.1	—	0.1	μA
$I_{Bi(ACT)}$	Cell Input Current when Voltage Monitoring	V_{Bi}=4.2V×i. EN_S bit=‘1’, V_{IN}=36V. i=1~8	—	15	—	μA
V_{OUT_VM}	Cell Voltage Monitor Output Accuracy	V_{Bi}–V_{Bi-1}=4.2V. i=1~8. Ta=25°C	2.094	2.100	2.106	V
		V_{Bi}–V_{Bi-1}=4.2V. i=1~8. Ta=-40~85°C	2.092	2.100	2.108	V
I_{VOUT_SOUR}	Cell Voltage Monitor Output Source Current	V_{Bi}–V_{Bi-1}=4.2V. i=1~8. C_{VOUT}=0.1μF. Peak current at EN_S ‘0’→‘1’ rising edge	—	2	—	mA
I_{VOUT_SINK}	Cell Voltage Monitor Output Sink Current	V_{Bi} – V_{Bi-1}=4.2V. i=1~8. C_{VOUT}=0.1μF. Peak current at EN_S ‘1’→‘0’ falling edge	—	1	—	mA
HS Gate Charge Pump						
V_{CP_UVLO+}	V(VCP, BAT) Turn On Level	V(VCP,BAT) rises	—	3	—	V
V_{CP_UVLO-}	V(VCP, BAT) Turn Off Level	V(VCP,BAT) falls	—	2.5	—	V
V_{CP}	VCP Output Voltage	EN_CP=‘1’, BAT=VIN>13V	V_{IN}+10	V_{IN}+12	V_{IN}+16	V
t_{CP_ON}	Rising Time of the Voltage Difference between VCP and VBAT	External capacitor 22nF between VCP and BAT. V_{IN}=36V, V(VCP, BAT) rises from 10% to 90% (V_{CP}-V_{BAT})(Note)	—	25	—	ms
f_{CP}	Charge Pump Switching Frequency	EN_CP=‘1’	—	600	—	kHz
Gate Drivers						
V_Z	DGNx Clamp Voltage	DNx=‘1’, V_{IN}>13V	10	12	16	V
		DNx=‘1’, V_{IN}≤13V	—	V_{IN}-0.7	—	V
t_r	DGNx Rising Time	C_{DGNx}=15nF(Note)	—	0.5	1.0	μs
t_f	DGNx Falling Time	C_{DGNx}=15nF(Note)	—	0.5	1.0	μs
t_{PD_HL}	DGNx Falling Propagation Delay Time	C_{DGNx}=15nF(Note)	—	0.5	1.0	μs
t_{PD_LH}	DGNx Rising Propagation Delay Time	C_{DGNx}=15nF(Note)	—	0.5	1.0	μs
t_{MM}	DGNx Delay Time Mismatch	C_{DGNx}=15nF. t_{MM} = |t_{PD_LHx} – t_{PD_HLx}|	—	0.5	1.0	μs
I_{SOURCE}	DGNx Source Current	C_{DGNx}=1μF, peak current at DNx ‘0’→‘1’ rising edge	—	850	—	mA
I_{SINK}	DGNx Sink Current	C_{DGNx}=1μF, peak current at DNx ‘1’→‘0’ falling edge	—	850	—	mA
I_{OPR_DGNx}	VIN Operating Current when DGN0 and DGN1 Outputs are On	DNx=‘1’	—	15	—	μA
R_{PL_S}	DGNx Pull Low Resistance at Sleep and Standby Mode	DNx=‘0’, SLP1=‘0’& SLP0=‘1’& HVWKx=‘0’ or HVWKx=‘1’, resistance between DGNx and GND	—	10	—	Ω
V_{DGCN_ON}	DGCN Gate Drive Turn-on Voltage	EN_CP=‘1’, DCN=‘1’	—	V_{CP}	—	V
V_{DGCN_OFF}	DGCN Gate Drive Turn-off Voltage	EN_CP=‘1’, DCN=‘0’	—	V_{IN}	—	V
R_{DGCN_ON}	DGCN Gate Drive Turn-on Resistance	EN_CP=‘1’, DCN=‘1’	—	2	—	kΩ
R_{DGCN_OFF}	DGCN Gate Drive Turn-off Resistance	EN_CP=‘1’, DCN=‘0’	—	150	—	Ω

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{rC}	Rising Time of the Voltage Difference between DGCN and BAT	EN_CP='1', $C_{DGCN-BAT}$=15nF, V_{IN}=36V, V(DGCN, BAT) rises from 10% to 90% (V_{DGCN} – V_{BAT}) (Note)	—	220	—	μs
t_{fC}	Falling Time of the Voltage Difference between DGCN and BAT	EN_CP='1', $C_{DGCN-BAT}$=15nF, V_{IN}=36V, V(DGCN, BAT) falls from 90% to 10% (V_{DGCN} – V_{BAT}) (Note)	—	5	—	μs

Note: These parameters are periodically sampled but not 100% tested.



Electrical Characteristics (Continue)

V_{IN}=36V, C_{REG}=4.7μF, ISP-to-ISN shunt resistor=5mΩ, Ta=+25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Current Monitor						
$G_{IM(R10)}$	IMON Output Voltage Amplify Rate	IMCE=‘1’, IAR=‘0’, Ta=25°C	9.7	10.0	10.3	V/V
		IMCE=‘1’, IAR=‘0’, Ta=-40~85°C	9.5	10.0	10.5	V/V
$G_{IM(R50)}$		IMCE=‘1’, IAR=‘1’, Ta=25°C	48.5	50.0	51.5	V/V
		IMCE=‘1’, IAR=‘1’, Ta=-40~85°C	47.5	50.0	52.5	V/V
$I_{MR(R10)}$	Current Monitor Range	IMCE=‘1’, IAR=‘0’, V_{REG}=5V, shunt resistor=5mΩ	-8	—	82	A
		IMCE=‘1’, IAR=‘0’, V_{REG}=5V, shunt resistor=2mΩ	-20	—	205	A
$I_{MR(R50)}$		IMCE=‘1’, IAR=‘1’, V_{REG}=5V, shunt resistor=5mΩ	-1.2	—	16	A
		IMCE=‘1’, IAR=‘1’, V_{REG}=5V, shunt resistor=2mΩ	-3	—	40	A
$V_{IMO(R10)}$	IMON Output Voltage at No Sensing Current	V_{ISP}-V_{ISN}=0V, IMCE=‘1’, ZERO=‘0’, IAR=‘0’	0.3	0.5	0.7	V
$V_{IMO(R50)}$		V_{ISP}-V_{ISN}=0V, IMCE=‘1’, ZERO=‘0’, IAR=‘1’	0.30	0.50	0.85	V
$V_{IMZ(R10)}$	IMON Output Voltage at ZERO State	IMCE=‘1’, ZERO=‘1’, IAR=‘0’	0.30	0.50	0.70	V
$V_{IMZ(R50)}$		IMCE=‘1’, ZERO=‘1’, IAR=‘1’	0.30	0.50	0.85	V
$I_{IMO(SOURCE)}$	IMON Output Source Current	—	100	—	—	μA
$I_{IMO(SINK)}$	IMON Output Sink Current	—	100	—	—	μA
$t_{IMZS(R10)}$	IMON Settling Time at ZERO State	IAR=‘0’, ZERO=‘1’, timing from IMCE=‘1’ to V_{IMON} settled at V_{IMZ}	—	—	100	μs
$t_{IMZS(R50)}$		IAR=‘1’, ZERO=‘1’, timing from IMCE=‘1’ to V_{IMON} settled at V_{IMZ}	—	—	500	μs
I_{IS}	ISP, ISN Input Current	V_{ISP}=V_{ISN}=0V, IAR=‘0’,ZERO=‘0’	—	-0.46	—	μA
$t_{IMR\_P(R10)}$	IMON Output Rising Time (V_{ISP}>V_{ISN})	IAR=‘0’, ZERO=‘0’, IMCE=‘1’, V_{ISN}=0V, V_{ISP} rises from 0V to 0.1V in 10μs	—	60	—	μs
$t_{IMR\_P(R50)}$		IAR=‘1’, ZERO=‘0’, IMCE=‘1’, V_{ISN}=0V, V_{ISP} rises from 0V to 0.1V in 10μs	—	300	—	μs
$t_{IMF\_P(R10)}$	IMON Output Falling Time (V_{ISP}>V_{ISN})	IAR=‘0’, ZERO=‘0’, IMCE=‘1’, V_{ISN}=0V, V_{ISP} falls from 0.1V to 0V in 10μs	—	60	—	μs
$t_{IMF\_P(R50)}$		IAR=‘1’, ZERO=‘0’, IMCE=‘1’, V_{ISN}=0V, V_{ISP} falls from 0.1V to 0V in 10μs	—	300	—	μs
$t_{IMR\_N(R10)}$	IMON Output Rising Time (V_{ISP}<V_{ISN})	IAR=‘0’, ZERO=‘0’, IMCE=‘1’, V_{ISP}=0V, V_{ISN} rises from 0V to 0.1V in 10μs	—	60	—	μs
$t_{IMR\_N(R50)}$		IAR=‘1’, ZERO=‘0’, IMCE=‘1’, V_{ISP}=0V, V_{ISN} rises from 0V to 0.1V in 10μs	—	300	—	μs
$t_{IMF\_N(R10)}$	IMON Output Falling Time (V_{ISP}<V_{ISN})	IAR=‘0’, ZERO=‘0’, IMCE=‘1’, V_{ISP}=0V, V_{ISN} falls from 0.1V to 0V in 10μs	—	30	—	μs
$t_{IMF\_N(R50)}$		IAR=‘1’, ZERO=‘0’, IMCE=‘1’, V_{ISP}=0V, V_{ISN} falls from 0.1V to 0V in 10μs	—	30	—	μs
Short-Current Detection						
V_{SCTH}	Short Circuit Detection Threshold voltage	ISCE=‘1’, SC_[2:0]=0b001	—	105	—	mV
t_{SCDB}	Short Circuit Detection Debounce Time	ISCE=‘1’, TD_[4:0]=0b00001 (default value)	—	6.32	—	μs
t_{SCPD}	Short Circuit Detection Propagation Delay Time	ISCE=‘1’, TD_[4:0]=0b00000 INTB sink current=50μA. Propagation delay time from V_{ISP}>V_{SCTH} to INTB pulled ‘Low’.	—	1	—	μs

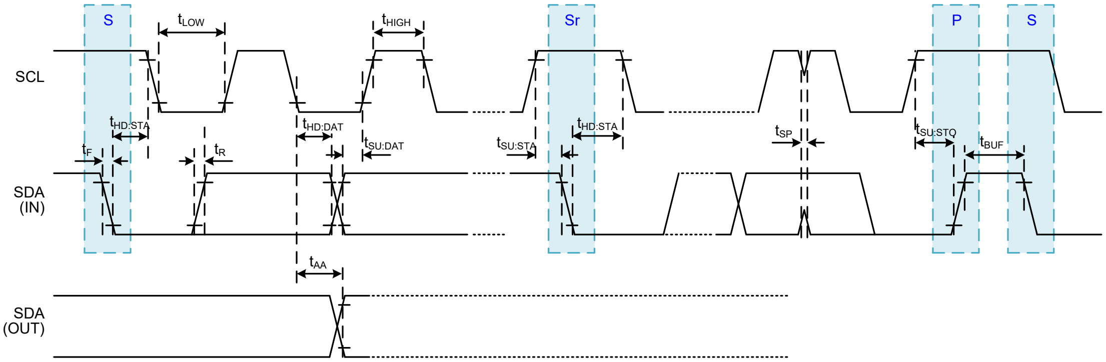
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Over-Temperature Detection						
T_{OTD}	Over-temperature Detection Threshold	EN_OTD='1', OTDTH[1:0]=0b00	—	85	—	°C
		EN_OTD='1', OTDTH[1:0]=0b01	—	100	—	°C
		EN_OTD='1', OTDTH[1:0]=0b10	—	125	—	°C
		EN_OTD='1', OTDTH[1:0]=0b11(default value)	—	150	—	°C
T_{HYS}	Over-temperature Detection Hysteresis	EN_OTD='1'	—	20	—	°C

I²C Interface Characteristic

V_{IN}=36V and Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC Characteristic						
V_{IH_I2C}	Input High Threshold Voltage	—	2.5	—	—	V
V_{IL_I2C}	Input Low Threshold Voltage	—	—	—	0.8	V
AC Characteristic						
f_{SCL}	Clock Frequency	—	—	—	400	kHz
t_{BUF}	Bus Free Time	Bus free time between STOP and START	1.3	—	—	μs
$t_{HD:STA}$	START Hold Time	After this period, the first clock pulse is generated	0.6	—	—	μs
t_{LOW}	SCL Low Time	—	1.3	—	—	μs
t_{HIGH}	SCL High Time	—	0.6	—	—	μs
$t_{SU:STA}$	START Setup Time	Only relevant for REPEATED START	0.6	—	—	μs
$t_{HD:DAT}$	Data Hold Time	—	0	—	—	ns
$t_{SU:DAT}$	Data Setup Time	—	100	—	—	ns
t_R	Rising Time	SDA and SCL	—	—	0.3	μs
t_F	Falling Time	SDA and SCL	—	—	0.3	μs
$t_{SU:STO}$	STOP Setup Time	—	0.6	—	—	μs
t_{AA}	Output Valid from Clock	—	—	—	0.9	μs
t_{SP}	Input Filter Time Constant	SDA and SCL noise suppression time	—	—	20	ns
t_{OUT}	I²C Time-out	—	—	32	—	ms

Note: These parameters are periodically sampled but not 100% tested.



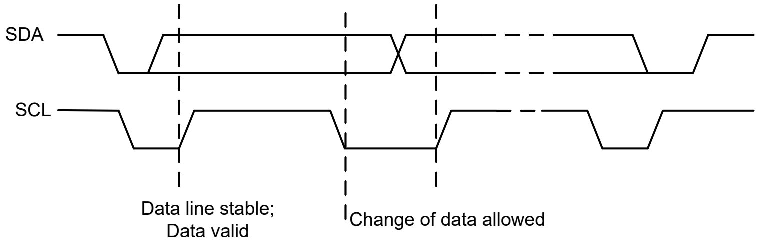
Functional Description

I²C Serial Interface

The HT7Q2552 supports I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). For the Standard Product, both lines are open-drain structure and two external pull-high resistors are required. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the Wired-AND function. Data transfer is initiated only when the bus is not busy.

Data Validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low.



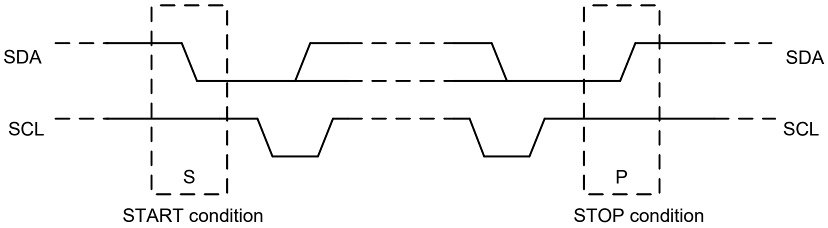
START and STOP

(1) A high to low signal transition on the SDA data line while SCL is high defines a START (S)

(2) A low to high signal transition on the SDA data line while SCL is high defines a STOP (P)

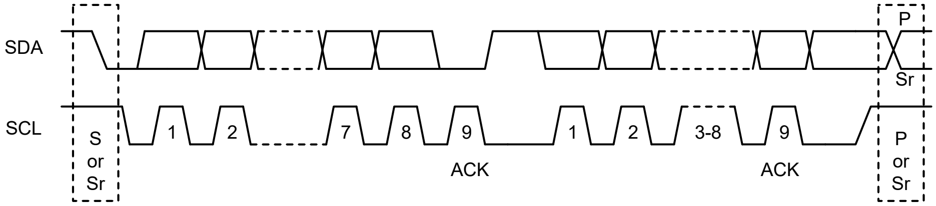
(3) START and STOP are always generated by the master. The bus is considered to be busy after the START. The bus is considered to be free again a certain time after the STOP.

(4) The bus stays busy if a REPEATED START (Sr) is generated instead of a STOP. In the respect, the START and REPEATED START are functionally identical.



Byte Format

Every byte put on the SDA data line signal must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



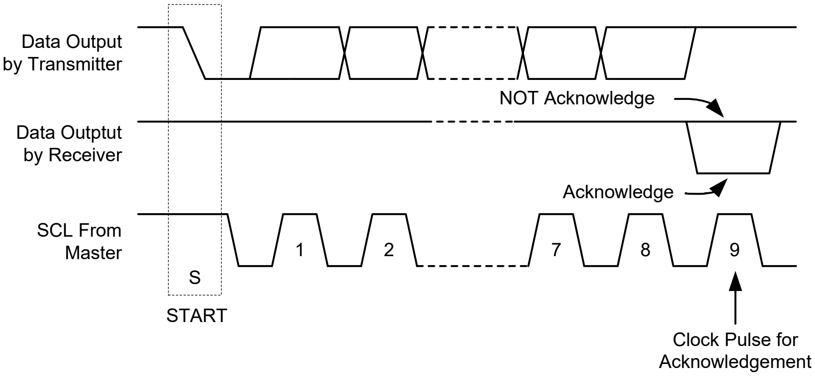
Acknowledge

(1) Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, the master generates an extra acknowledge related clock pulse.

(2) A slave receiver which is addressed must generate an Acknowledge response signal after the reception of each byte.

(3) The device that provides an acknowledge must pull down the SDA data line signal during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

(4) A master receiver must signal an end of data to the slave by generating a NOT Acknowledge response signal on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or Repeated START.



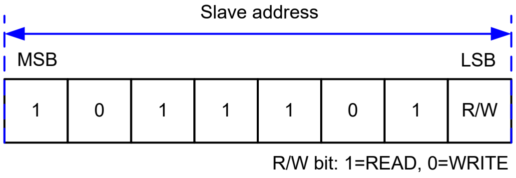
I²C Time-out Control

In order to reduce the I²C lockup problem due to reception of erroneous clock sources, a time-out function is provided. The I²C time-out function starts timing for the specified I²C time-out period (t_{OUT}) when receiving START (S) from I²C bus. The timer is reset by every falling edge of SCL data line signal and gets interrupted when receiving STOP (P). If the next falling edge of SCL data line signal or STOP (P) does not appear throughout the I²C time-out period (t_{OUT}), SDA and SCL data line signals are set to default states at the end of timing and meanwhile the registers remains unchanged. The I²C time-out is 32ms.

Slave Address

(1) The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When R/W bit is '1', then a READ operation is selected. When R/W bit is '0', it selects WRITE operation.

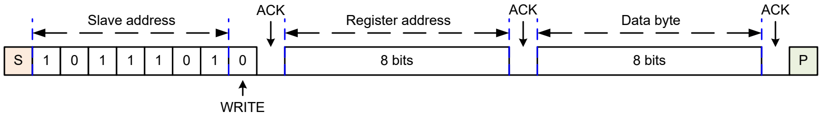
(2) The slave address of the HT7Q2552 is "1011101". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA data line signal.



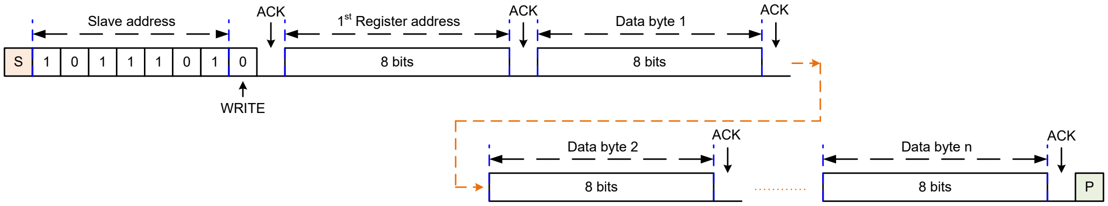
Write Operation

An I²C write operation combines a START bit, a Slave address byte with a Write bit, a Register address byte, single or multiple Data bytes, and a STOP bit.

Single Data Byte Write Sequence:

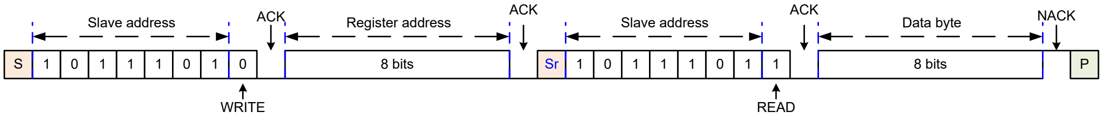


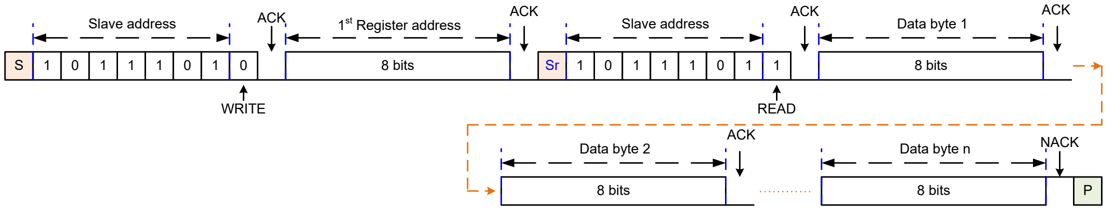
Multiple Data Bytes Write Sequence:



Read Sequence

The complete read mode consists of two stages. 1st stage: writes in the Register Address Byte to the device. 2nd state: reads out the single or multiple Data Bytes from the device.





I²C Register Map

The I²C register bit map is listed below.

Address	Acronym	Access Type	Value after POR	Register Description
00H	REG00	R/W	1000 0000	Sleep, Reference Voltage, Charge Pump and Voltage Monitor Control
01H	REG01	R/W	0000 0000	Cell Balance Control
02H	REG02	R/W	0000 0000	Current Monitor Setting
03H	REG03	R/W	1000 0001	Short-Current Detection Setting 1
04H	REG04	R/W	0000 0001	Short-Current Detection Setting 2
05H	REG05	R/W	0000 0011	Short-Current Detection Control
06H	REG06	R/W	1001 0010	Over-temperature Detection and Thermal Sensor
07H	REG07	R	0000 0000	Chip Status
08H	REG08	R/W	0000 0000	Interrupt Mask
09H	REG09	R	0000 0000	Interrupt Flag

- **Sleep, Reference Voltage, Charge Pump and Voltage Monitor Control Register (00H)**

Bit	7	6	5	4	3	2	1	0
Name	SLP1	SLP0	EN_VREF	EN_S	EN_CP	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	0	0	0	0	0	0	0

Bit 7~6 **SLP1, SLP0**: Sleep mode enable control

SLP1	SLP0	Action
0	0	Normal operation
0	1	Enter sleep mode
1	0	Normal operation
1	1	Normal operation

Bit 5 **EN_VREF**: Reference voltage output function enable control
0: Reference voltage output function is disabled, VREF pin output=0V
1: Reference voltage output function is enabled, VREF pin output=2.5V

Bit 4 **EN_S**: Voltage monitor function enable control
0: Voltage monitor function is disabled, VOUT pin output=0V
1: Voltage monitor function is enabled, VOUT pin output=$(V_{BAT1\sim8}-V_{BAT0\sim7})\times1/2$

Bit 3 **EN_CP**: Charge pump function enable control
0: Charge pump function is disabled
1: Charge pump function is enabled, VCP pin=V_{CP}

Bit 2~0 **B2, B1, B0**: 8-to-1 analog multiplexer selection bits (MSB: B2, LSB: B0)
Control B2~B0 to select which cell voltage to be outputted to VOUT.

EN_S	B2	B1	B0	V_{OUT} (V)
0	—	—	—	0
1	0	0	0	$(V_{BAT1}-V_{BAT0})\times1/2+V_{BAT0}$
1	0	0	1	$(V_{BAT2}-V_{BAT1})\times1/2$
1	0	1	0	$(V_{BAT3}-V_{BAT2})\times1/2$
1	0	1	1	$(V_{BAT4}-V_{BAT3})\times1/2$
1	1	0	0	$(V_{BAT5}-V_{BAT4})\times1/2$
1	1	0	1	$(V_{BAT6}-V_{BAT5})\times1/2$
1	1	1	0	$(V_{BAT7}-V_{BAT6})\times1/2$
1	1	1	1	$(V_{BAT8}-V_{BAT7})\times1/2$

*To avoid voltage drop caused by balance current, the cell balance function must be turned off during the voltage monitoring.

- **Cell Balance Control Register (01H)**

Bit	7	6	5	4	3	2	1	0
Name	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **CB8**: Enable control of the cell balance switch between VBAT8 and VBAT7
0: Balance switch Off
1: Balance switch On

Bit 6 **CB7**: Enable control of the cell balance switch between VBAT7 and VBAT6
0: Balance switch Off
1: Balance switch On

Bit 5 **CB6**: Enable control of the cell balance switch between VBAT6 and VBAT5
0: Balance switch Off
1: Balance switch On

Bit 4 **CB5**: Enable control of the cell balance switch between VBAT5 and VBAT4
0: Balance switch Off
1: Balance switch On

Bit 3 **CB4**: Enable control of the cell balance switch between VBAT4 and VBAT3
0: Balance switch Off
1: Balance switch On

Bit 2 **CB3**: Enable control of the cell balance switch between VBAT3 and VBAT2
0: Balance switch Off
1: Balance switch On

Bit 1 **CB2**: Enable control of the cell balance switch between VBAT2 and VBAT1
0: Balance switch Off
1: Balance switch On

Bit 0 **CB1**: Enable control of the cell balance switch between VBAT1 and VBAT0
0: Balance switch Off
1: Balance switch On

- **Current Monitor Setting Register (02H)**

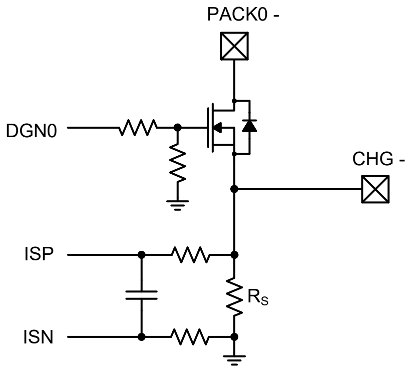
Bit	7	6	5	4	3	2	1	0
Name	IMCE	ZERO	IAR	Reserved	Reserved	Reserved	Reserved	Reserved
R/W	R/W	R/W	R/W	—	—	—	—	—
POR	0	0	0	0	0	0	0	0

Bit 7 **IMCE**: Enable current monitor
0: Disable current monitor
1: Enable current monitor

Bit 6 **ZERO**: Execute zero correction of current monitor
0: The input of internal differential voltage amplifier circuit are connected to ISP and ISN pin
1: Both input of internal differential voltage amplifier circuit are connected to GND

Bit 5 **IAR**: Select the voltage amplifying rate of current monitor
0: Voltage amplifying rate=10
1: Voltage amplifying rate=50

RS	IAR	Maximum Discharge Current (A)	Maximum Charge Current (A)
2mΩ	0	195	15
	1	38	2
5mΩ	0	78	6
	1	15	0.8



Bit 4~0 Reserved bits

- **Short-Current Detection Setting 1 Register (03H)**

Bit	7	6	5	4	3	2	1	0
Name	ISCE1	ISCE0	Reserved	Reserved	Reserved	SC_2	SC_1	SC_0
R/W	R/W	R/W	—	—	—	R/W	R/W	R/W
POR	1	0	0	0	0	0	0	1

Bit 7~6 **ISCE1, ISCE0**: Enable short-current detection

ISCE1	ISCE0	Action
0	0	Short current detection is off
0	1	Short current detection is activated
1	0	Short current detection is off
1	1	Short current detection is off

Bit 5~3 Reserved bits

Bit 2~0 **SC_2, SC_1, SC_0**: Select the short-current detection threshold voltage (V_{SCTH}) of short-current detection

If the voltage of V_{ISP} is greater than the threshold voltage, INTB is pulled low by internal switch.

SC_2	SC_1	SC_0	Threshold Voltage
0	0	0	50mV
0	0	1	100mV
0	1	0	150mV
0	1	1	200mV
1	0	0	250mV
1	0	1	300mV
1	1	0	350mV
1	1	1	400mV

- **Short-Current Detection Setting 2 Register (04H)**

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	TD_4	TD_3	TD_2	TD_1	TD_0
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	1

Bit 7~5 Reserved bits

Bit 4~0 **TD_4, TD_3, TD_2, TD_1, TD_0**: Select the debounce time of short-current detection

TD_4	TD_3	TD_2	TD_1	TD_0	Debounce Time
0	0	0	0	0	0μs
0	0	0	0	1	32μs
0	0	0	1	0	64μs
0	0	0	1	1	96μs
0	0	1	0	0	128μs
0	0	1	0	1	160μs
0	0	1	1	0	192μs
0	0	1	1	1	224μs
0	1	0	0	0	256μs
0	1	0	0	1	288μs
0	1	0	1	0	320μs
0	1	0	1	1	352μs
0	1	1	0	0	384μs

TD_4	TD_3	TD_2	TD_1	TD_0	Debounce Time
0	1	1	0	1	416µs
0	1	1	1	0	448µs
0	1	1	1	1	480µs
1	0	0	0	0	512µs
1	0	0	0	1	544µs
1	0	0	1	0	576µs
1	0	0	1	1	608µs
1	0	1	0	0	640µs
1	0	1	0	1	672µs
1	0	1	1	0	704µs
1	0	1	1	1	736µs
1	1	0	0	0	768µs
1	1	0	0	1	800µs
1	1	0	1	0	832µs
1	1	0	1	1	864µs
1	1	1	0	0	896µs
1	1	1	0	1	928µs
1	1	1	1	0	960µs
1	1	1	1	1	992µs

- **Short-Current detection Control Register (05H)**

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	IS_ACT_DGCN	IS_ACT_DGN1	IS_ACT_DGN0
R/W	—	—	—	—	—	R/W	R/W	R/W
POR	0	0	0	0	0	0	1	1

Bit 7~3 Reserved bits

Bit 2 **IS_ACT_DGCN**: Control actions of DGCN when short-current event is detected
IS_ACT_DGCN can be written only when V_{DCN}=0V
0: Remain present output status of DGCN when short-current event is detected
1: Shut down and lock the output of DGCN when short-current event is detected.
The locked output of DGCN is released by the falling edge of DCN input signal.

Bit 1 **IS_ACT_DGN1**: Control actions of DGN1 when short-current event is detected
IS_ACT_DGN1 can be written only when V_{DN1}=0V
0: Remain present output status of DGN1 when short-current event is detected.
1: Shut down and lock the output of DGN1 when short-current event is detected
The locked output of DGN1 is released by the falling edge of DN1 input signal.

Bit 0 **IS_ACT_DGN0**: Control actions of DGN0 when short-current event is detected
IS_ACT_DGN0 can be written only when V_{DN0}=0V
0: Remain present output status of DGN0 when short-current event is detected
1: Shut down and lock the output of DGN0 when short-current event is detected
The locked output of DGN0 is released by the falling edge of DN0 input signal.

• Over-temperature Detection and Thermal Sensor Register (06H)

Bit	7	6	5	4	3	2	1	0
Name	EN_OTD	Reserved	Reserved	OTD_ACT	Reserved	Reserved	OTDTH1	OTDTH0
R/W	R/W	—	—	R/W	—	—	R/W	R/W
POR	1	0	0	1	0	0	1	0

Bit 7 **EN_OTD**: Enable Over-temperature detection
0: Disable Over-temperature detection
1: Enable Over-temperature detection

Bit 6~5 Reserved bits

Bit 4 **OTD_ACT**: Control action of cell balance when internal over-temperature event is detected
0: Remain present turn-on status of cell balance when internal over-temperature event is detected
1: Turn off and lock all cell balance switches when internal over-temperature event is detected

The locked switches of cell balance can only turn on the cell balance function again after resetting the cell balance control register CB [8:1]=0x00.

Bit 3~2 Reserved bits

Bit 1~0 **OTDTH1, OTDTH0**: Select the over-temperature detection threshold

Symbol	OTDTH1	OTDTH0	OTD threshold
T_{OTD1}	0	0	85°C
T_{OTD2}	0	1	100°C
T_{OTD3}	1	0	125°C
T_{OTD4}	1	1	150°C

• Chip Status Register (07H)

Bit	7	6	5	4	3	2	1	0
Name	DGCN_ OUT	DGN1_ OUT	DGN0_ OUT	OTD_ST	EXT_ WK2	EXT_ WK1	Reserved	IS_SC_ ST
R/W	R	R	R	R	R	R	—	R
POR	0	0	0	0	0	0	0	0

Bit 7 **DGCN_OUT**: DGCN output status
0: DGCN output status is off ($V_{DGCN}= V_{BAT}$)
1: DGCN output status is on ($V_{DGCN}= V_{CP}$)

Bit 6 **DGN1_OUT**: DGN1 output status
0: DGN1 output status is off (V_{DGN1}=0V)
1: DGN1 output status is on ($V_{DGN1}=V_Z$)

Bit 5 **DGN0_OUT**: DGN0 output status
0: DGN0 output status is off (V_{DGN0}=0V)
1: DGN0 output status is on ($V_{DGN0}=V_Z$)

Bit 4 **OTD_ST**: OTD event status
0: Junction temperature is under T_{OTD}
1: Present junction temperature is higher than T_{OTD}.

OTD_ST goes to '0' when internal junction temperature drops under (T_{OTD}-T_{HYS}).

Bit 3 **EXT_WK2**: HVWK2 wake-up event status
0: Denotes that external wake-up event does not exist at HVWK2 pin
1: Denotes that external wake-up event exists at HVWK2 pin.

When V_{HVWK2} remains higher than V_{WKTH} over 1ms, EXT_WK2 will be set to '1', meanwhile SLP1 and SLP0 are reset to their POR values.

EXT_WK2 is cleared to '0' immediately when V_{HVWK2} drops under 1.5V.

Bit 2 **EXT_WK1**: HVWK1 wake-up event status
0: Denotes that external wake-up event does not exist at HVWK1 pin
1: Denotes that external wake-up event exists at HVWK1 pin or is written by MCU.

(1) When V_{HVWK1} remains higher than V_{WKTH} over 1ms, EXT_WK1 will be set to '1', meanwhile SLP1 and SLP0 are reset to their POR values.
EXT_WK1 is cleared to '0' immediately when V_{HVWK1} drops under 1.5V.

(2) EXT_WK1 can be written as '1' by MCU for the purpose of sending a wake-up signal. EXT_WK1 have to be written as '0' and SLP[1:0] have to be written as 0b10 through I^{2}C interface after EXT_WK1 is set as '1' by MCU, otherwise external wake-up event on HVWK1 pin cannot be recognized and the follow-up Sleep command will be failed.

(3) Writing both EXT_WK1 and SLP[1:0] as '1' and 0b01 is NOT permitted for avoiding unpredictable status.

(4) Reading EXT_WK1 reveals the external wake-up even status of HVWK1 pin only.

Bit 1 Reserved bit

Bit 0 **IS_SC_ST**: Short-current protection detecting status
0: V_{ISP} is under V_{SCTH}
1: Short-current event is happening at Short-current detection ($V_{ISP}>V_{SCTH}$)

• Interrupt Mask Register (08H)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	OTD_MSK	EXT_WK2_MSK	EXT_WK1_MSK	Reserved	IS_SC_MSK
R/W	—	—	—	R/W	R/W	R/W	—	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~5 Reserved bits

Bit 4 **OTD_MSK**: Over-temperature detection INTB mask
0: OTD_ST entry produces INTB pulse
1: OTD_ST entry does not produce INTB pulse but still trigger OTD_FLG

Bit 3 **EXT_WK2_MSK**: External wake-up event detection INTB mask
0: EXT_WK2 entry produces INTB pulse
1: EXT_WK2 entry does not produce INTB pulse but still trigger EXT_WK2_FLG

Bit 2 **EXT_WK1_MSK**: External wake-up event detection INTB mask
0: EXT_WK1 entry produces INTB pulse
1: EXT_WK1 entry does not produce INTB pulse but still trigger EXT_WK1_FLG

Bit 1 Reserved bit

Bit 0 **IS_SC_MSK**: Short-current detection INTB mask
0: IS_SC_ST entry produces INTB pulse
1: IS_SC_ST entry does not produce INTB pulse but still trigger IS_SC_FLG

• Interrupt Flag Register (09H)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	OTD_FLG	EXT_WK2_FLG	EXT_WK1_FLG	Reserved	IS_SC_FLG
R/W	—	—	—	R	R	R	—	R
POR	0	0	0	0	0	0	0	0

Bit 7~5 Reserved bits

Bit 4 **OTD_FLG**: Over-temperature detection INTB flag
0: Normal
1: OTD_ST rising edge detected

OTD_FLG is reset to '0' after I^{2}C master reads Interrupt Flag Register

Bit 3	**EXT_WK2_FLG**: HVWK2 external wake-up event detection INTB flag 0: Normal 1: EXT_WK2 rising edge detected EXT_WK2_FLG is reset to '0' after I²C master reads Interrupt Flag Register.
Bit 2	**EXT_WK1_FLG**: HVWK1 external wake-up event detection INTB flag 0: Normal 1: EXT_WK1 rising edge detected EXT_WK1_FLG is reset to '0' after I²C master reads Interrupt Flag Register
Bit 1	Reserved bit
Bit 0	**IS_SC_FLG**: Short-current detection INTB flag 0: Normal 1: IS_SC_ST rising edge detected IS_SC_FLG is reset to '0' after I²C master reads Interrupt Flag Register.

Cell Voltage Monitor

B2~B0 are 8-to-1 analog multiplexer selection bits (MSB: B2, LSB: B0). These bits control the selection of the battery voltage output to the VOUT pin only when EN_S = '1'. The control truth table is shown below. It transfers 1/2 of each battery cell's voltage to VOUT. It's recommended that to keep EN_S='0' when voltage scanning procedure is finish for power saving.

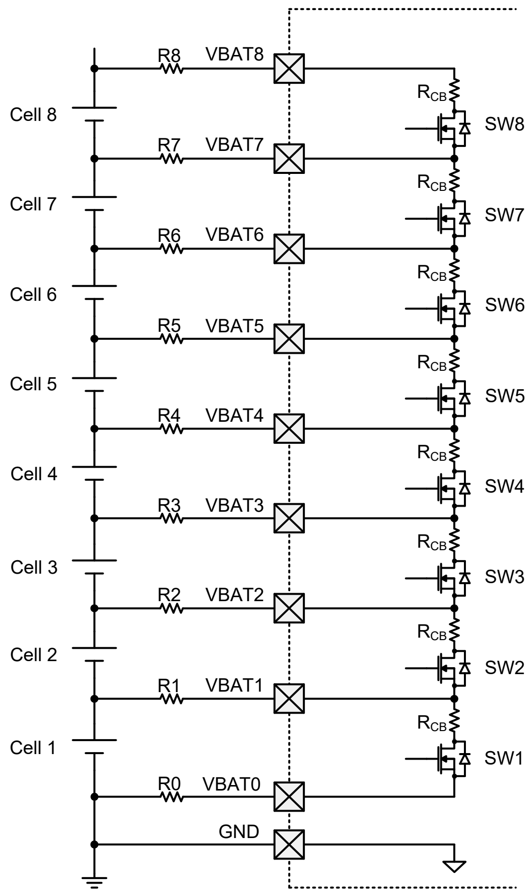
EN_S	B2	B1	B0	V_{OUT} (V)
0	X	X	X	0
1	0	0	0	$(V_{BAT1}-V_{BAT0})\times1/2+V_{BAT0}$
1	0	0	1	$(V_{BAT2} - V_{BAT1}) \times 1/2$
1	0	1	0	$(V_{BAT3} - V_{BAT2}) \times 1/2$
1	0	1	1	$(V_{BAT4} - V_{BAT3}) \times 1/2$
1	1	0	0	$(V_{BAT5} - V_{BAT4}) \times 1/2$
1	1	0	1	$(V_{BAT6} - V_{BAT5}) \times 1/2$
1	1	1	0	$(V_{BAT7} - V_{BAT6}) \times 1/2$
1	1	1	1	$(V_{BAT8} - V_{BAT7}) \times 1/2$

Cell Voltage Monitor Truth Table

Cell Balance

Multiple channels of cell balance switch can be turned on by host MCU via I²C interface. The register command byte of cell balance function is 01H, and the BIT7~BIT0 of Data byte correspond to the cell balance switch of each channel from SW8 to SW1, respectively. More than one switch can be turned on in the same time, but side-by-side cell balance switches are recommended NOT to be turned on simultaneously to ensure equal balance current between each channel. After receiving turn on command, cell balance switch remains turned on until it is turned off by a '0' data or get a command of SLP0='1'. By setting OTD_ACT='1', when internal junction temperature exceeds T_{OTD}, all balance switched are turned off and locked automatically and cannot be turned on again until the locked states are released. All locked switches are released by setting CB[8:1]=0x00.

The typical cell balance current is 10mA at battery cell voltage 4.2V with series resistance 100Ω, and the balance current can be adjusted by series resistors R0~R8. Note that for the reason of keeping voltage monitor accuracy, do not proceed voltage monitor while cell balance is activated.



CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	Balance Switch On/Off
1	0	0	0	0	0	0	0	SW1 On, others Off
0	1	0	0	0	0	0	0	SW2 On, others Off
0	0	1	0	0	0	0	0	SW3 On, others Off
0	0	0	1	0	0	0	0	SW4 On, others Off
0	0	0	0	1	0	0	0	SW5 On, others Off
0	0	0	0	0	1	0	0	SW6 On, others Off
0	0	0	0	0	0	1	0	SW7 On, others Off
0	0	0	0	0	0	0	1	SW8 On, others Off

Note: More than one switch can be turned On in the same time by the CB1~CB8 registers.

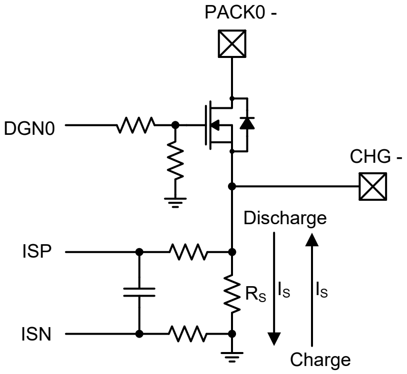
Current Monitor

A current monitor is fabricated for measuring battery discharge current. The current monitor with ISP and ISN input pins must be connected to the sense resistor on DGN0 or DGN1 pin discharge path. IMCE signal is the enable control of current monitor, and current monitors can be turned off by setting IMCE='0' for power saving purpose.

Current measurement is accomplished with placing current sensing resistors connected between ISP and ISN pins, and measure input voltage difference of these pins. The ISP pin level should be higher than the ISN pin level in discharge state for a wide discharge current sensing range. While there is no current on sensing resistor or ZERO='1', IMON pin outputs a center voltage of 0.5V (typ.). When ZERO pin is set to '0', voltage difference of (V_{ISP}-V_{ISN}) is multiplied by the gain of amplifier which is denoted as $G_{IM(R10)}$ for a gain of 10 or $G_{IM(R50)}$ for a gain of 50 and outputted to IMON pin. The IMON pin output voltage amplify rate (G_{IM}) is selected by IAR.

The current monitor allows to use one sense resistor for charge and discharge current sensing. In discharge state, the voltage of ISP pin is greater than the ISN pin, and the output voltage of IMON pin is in the range of 0.5V (typ.) to 2.5V (V_{REF}). In charge state, the voltage of ISP pin is smaller ISN pin, and the output voltage of IMON pin is in the range of 0V to 0.5V (typ.). IMON pin output voltage V_{IMON} is given by the following equation with the current sensing resistor R_S and its current I_S. The value of I_S is positive in discharge state and negative in charge state.

$$V_{IMON} = I_S \times R_S \times G_{IM} + 0.5$$



Short-current Detection

A short-current detection and protection circuit are fabricated for detecting loading short event. Short current detection with ISP and ISN input pins must be connected to the sense resistor on DGN0 or DGN1 pin discharge path. The ISCE signal is the enable control of short current protection, and short-current protection can be turned off by setting ISCE='0' for power saving purpose. By means of comparing V_{ISP} to short-current detection threshold voltage (V_{SCTH}), the exceeding current caused by loading shorted can be detected.

Sleep Mode

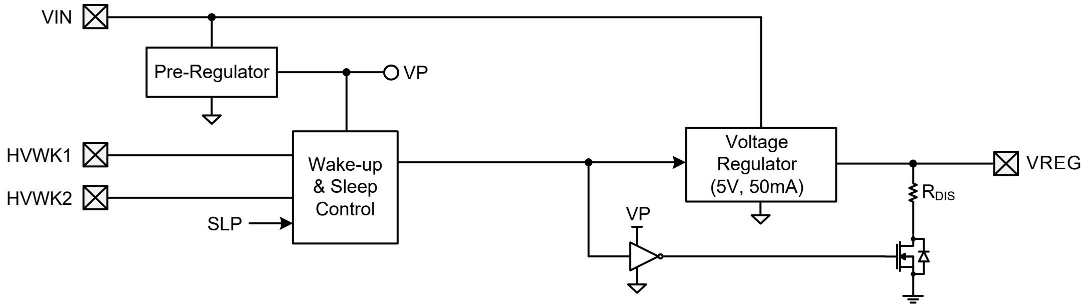
When EXT_WK1 and EXT_WK2 signals are all '0' and receiving a sleep command from I²C master, it indicates that high voltage applied on the HVWK1 or HVWK2 pin is not detected. The I²C master will set the SLP1 and SLP0 signals according to register (00H) Bit 7~6 to make the chip to enter the Sleep mode. During the sleep mode, all outputs are shut down and the capacitor of VREG is discharged through internal discharge resistor. The pre-regulator and high voltage wake-up circuit are the only blocks that are still working in the sleep mode and operates with an ultra-low standby current of 0.1μA (typical).

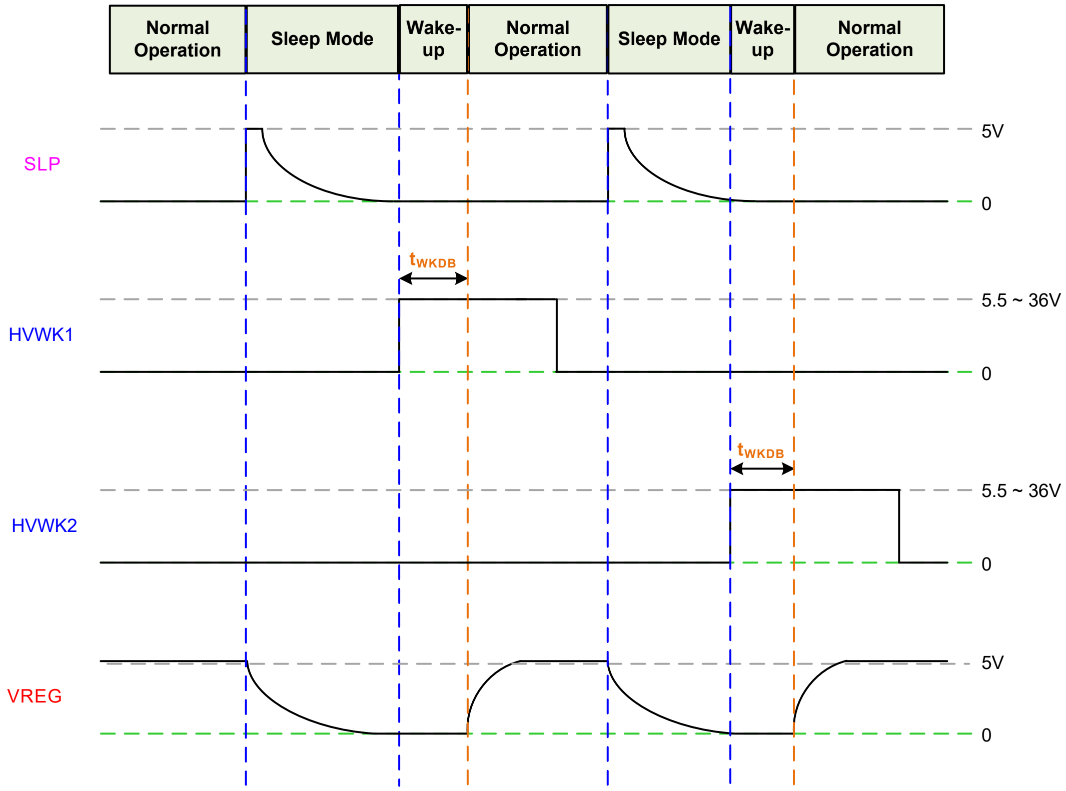
When either the EXT_WK or EXT_WK2 signal is '1', the I²C master will set the SLP1 and SLP0 signals according to register (00H) Bit 7~6 and abandon the sleep command until the EXT_WK and EXT_WK2 are cleared to '0'.

EXT_WK1 Status	EXT_WK2 Status	Sleep Mode Status
0	0	According to I²C master command or POR default value.
0	1	0
1	0	0
1	1	0

Wake up from Sleep Mode

The HVWK1 and HVWK2 pins can be used for detecting charger plugged-in, switch turned on, or load connected events. When the device is under the Sleep mode and the EXT_WK1 and EXT_WK2 signals are all ‘0’, it indicates that high voltage applied on the HVWK1 or HVWK2 pin is not detected. On the contrary, if either EXT_WK1 or EXT_WK2 signal is ‘1’, it indicates that a wake-up event has occurred. If it is detected that the HVWK1 or HVWK2 pin is triggered by a pulse with requiring at least 5.5V voltage and 1ms width, the output of VREG will resume and the whole chip is ready for normal operation. The reference timing diagram of entering sleep mode and waked up is listed below.





Discharge Path, i.e., Low-side Power Switch Gate Driver

The DGN0 and DGN1 are fabricated in the chip as discharge switch controllers. The output voltage of DGN0 and DGN1 pins are both clamped at 12V. A 370kΩ pull-down resistor is integrated at discharge gate control input pin DN0 and DN1. While operating in Normal Operation or sleep mode, DGN0 and DGN1 are pulled down by 10Ω resistors. The control logic and output status of DGN0 and DGN1 pins in each state are listed in the table below.

Operating Mode	DN0	V(DGN0)	Note
Normal Operation	0	0V	DGN0 output low to 0V
	1	12V	DGN0 output high clamp to 12V
Sleep Mode	X	0V	Pulled-low to GND by 10Ω.

Operating Mode	DN1	V(DGN1)	Note
Normal Operation	0	0V	DGN1 output low to 0V
	1	12V	DGN1 output high clamp to 12V
Sleep Mode	X	0V	Pulled-low to GND by 10Ω.

Charge Path, i.e., High-side Power Switch Gate Driver

A high-side power switch gate driver DGCN is provided as a charger switch controller. A charge pump circuit is fabricated to provide BAT or VCP voltage between the gate and source node of external charge power switch. When the DCN pin is‘0’, DGCN output low, the voltage level varies with the BAT pin. When the DCN pin is‘1’, DGCN output high, the voltage level varies with the VCP pin. A 370kΩ pull-down resistor is integrated at the control input pin DCN.

Input	Gate Driver Output	Note
DCN	V(DGCN)	
0	BAT	DGCN output low, the voltage level varies with the BAT pin
1	VCP	DGCN output high, the voltage level varies with the VCP pin

Over-temperature detection

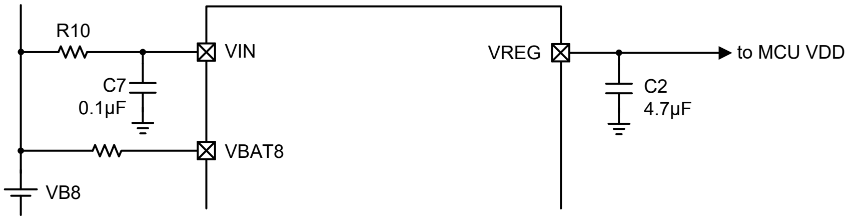
An over-temperature detection (OTD) is integrated in the HT7Q2552 to prevent from IC overheated while cell balance function is turned on. According to the setting of register (06H), the over-temperature detection function is active when EN_OTD=‘1’ and any of the Cell Balance switch is turned on. When internal junction temperature $T_J > T_{OTD}$, OTD_ST is set to ‘1’ and OTD_FLG is triggered as ‘1’ if OTD_MSK=‘0’. OTD_ST goes to ‘0’ when internal junction temperature drops under (T_{OTD}–T_{HYS}).

By setting OTD_ACT=‘1’, when internal junction temperature exceeds T_{OTD}, all balance switched are turned off and locked automatically. All locked switches cannot be turned on again until they are released by setting CB[8:1]=0x00.

Application Information

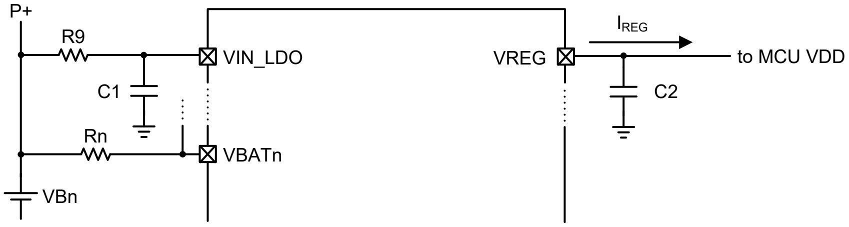
VIN, VREG Capacitors

It is recommended to connect a 0.1µF input capacitor C7 to the VIN pin and a 4.7µF output capacitor C2 to the VREG pin to improve input noise filtering and output load transient behavior.



VIN_LDO Filter Recommendation

The input capacitor C1 for VIN_LDO is used for lowering the input voltage ripple while the battery is supplying a highly inductive load in PWM mode. The recommanded value of VIN_LDO input capacitor C1 is 4.7μF. The input resistor R9 of VIN_LDO is able to reduce the inrush current during battery assembly, and also it shares the heat on chip while VREG outputs a large current in normal operation mode. The recommanded value for VIN_LDO input resistor R9 differs from different battery cell number applications. The recommended resistance values of VIN_LDO input resistor R9 with different battery cell numbers and the corresponding VREG maximum output current are listed in the table below.



Battery Cell Number	Input Resistor (R9)	VREG Maximum Output Current
3S	15Ω	50mA
4S	43Ω	50mA
5S	110Ω	40mA
6S	220Ω	35mA
7S	330Ω	30mA
8S	430Ω	30mA

It is necessary to select an appropriate package for VIN_LDO input resistor (R9) in order to prevent it being damaged from overheated. The maximum power of the resistor is easily calculated by:

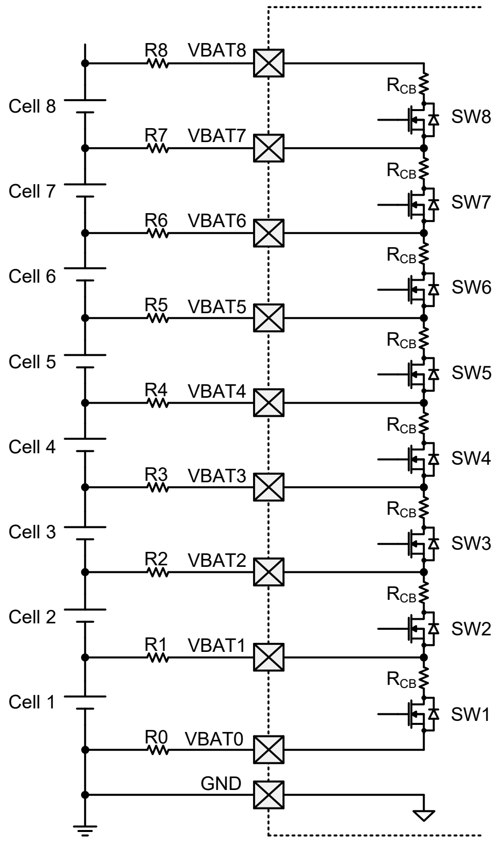
$$P_{R9.MAX}=(I_{REG})^2\times R9$$, where I_{REG} is the maximum VREG output current

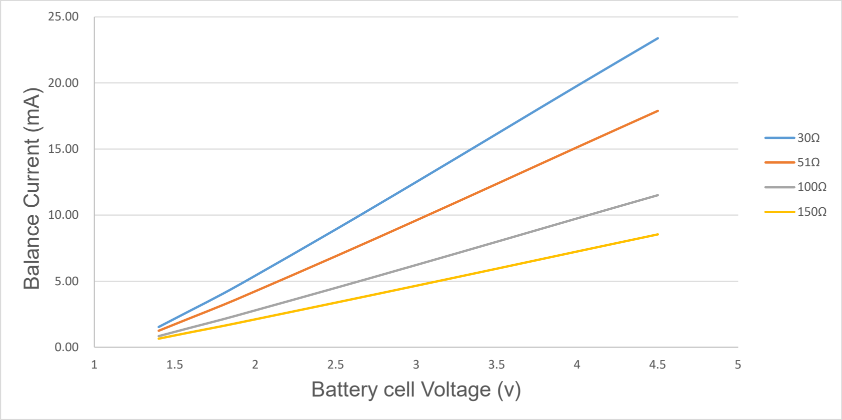
It is recommended to choose the resistor package that its maximum rated power is greater than twice the $P_{R9.MAX}$.

VBAT0~8 Protection and Balance Resistor Selection

The VBAT0~8 represents the VBAT0~VBAT8 pins. Series resistors RBn includes R0~R8, which not only suppress inrush and noise spikes applied to I/O pins, they affect cell balance current as well. Larger resistance of R0~R8 provide better protection to VBAT0~8 and other I/O pins, but they lower the cell balance current instead. The cell balance current of each channel is configured by internal balance resistors and external series resistors. Considering inrush spike protection to I/O pins and noise reduction of voltage monitor, the recommended typical values of resistor R0~R8 are 100Ω, and the cell balance current I_{CB} is 10mA while the voltage of battery cell is 4.2V. If larger balance current is needed, the recommended minimum values of resistors R0~R8 are 30Ω which provide 21mA while the voltage VBn of each cell is 4.2V. To ensure the internal balance circuit works properly, the minimum battery cell voltage to start the balance function is 3V. The recommended VBAT0~8 series resistors and their related cell balance current are listed in the table below.

Resistance of R0~R8 (RB_n)	Typical Balance Current (@V_{Bn}=4.2V) (I_{CB})	Note
30Ω	21mA	Minimum value of resistor R0~R8
51Ω	15.9mA	—
100Ω	10mA	—
150Ω	7.6mA	—


R8
VBAT8
Cell 8
R7
VBAT7
Cell 7
R6
VBAT6
Cell 6
R5
VBAT5
Cell 5
R4
VBAT4
Cell 4
R3
VBAT3
Cell 3
R2
VBAT2
Cell 2
R1
VBAT1
Cell 1
R0
VBAT0
GND
R_{CB}
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1

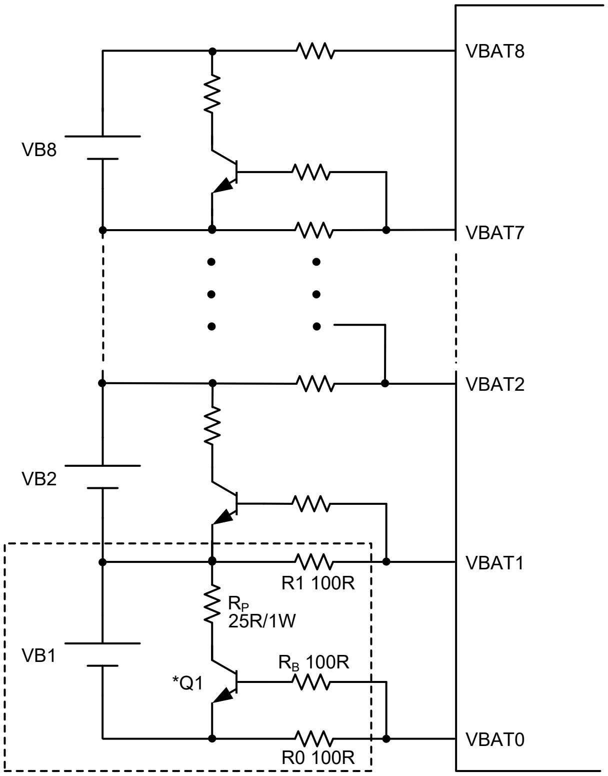

25.00
20.00
15.00
10.00
5.00
0.00
Balance Current (mA)
1
1.5
2
2.5
3
3.5
4
4.5
5
Battery cell Voltage (v)
30Ω
51Ω
100Ω
150Ω

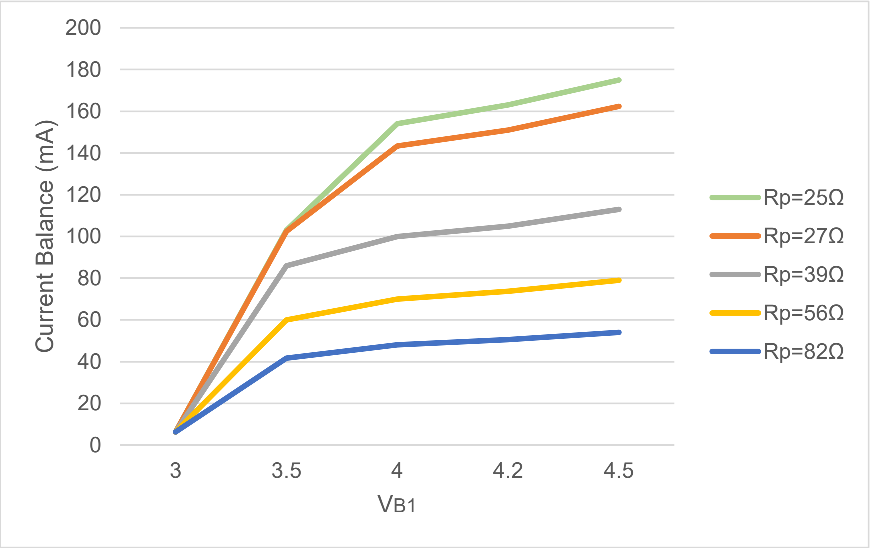
Increase Cell Balance Current

Refer to the following application circuits, when cell balance is turned on internally, the R0 will generate a voltage drop to make transistor Q1 conductive. Set the V_{B1}=4.2V, R0=R1=R_B=100R, balanced current (I_{CB}) is 150mA, it is recommended Q1 to choose NPN transient HFE≥85, $V_{CE(sat)} \leq 0.1V$, $V_{BE\ (sat)} \approx 0.7V$, and calculate R_P according to the following formula:

1. $R_P=(V_{B1}-V_{CE(sat)})/I_{CB}$
2. R_P selects resistance watts based on the calculation result

   $P_D=((V_{B1}-V_{CE(sat)})^2)/R_P$





Charger and Switch Status Detection for MCU

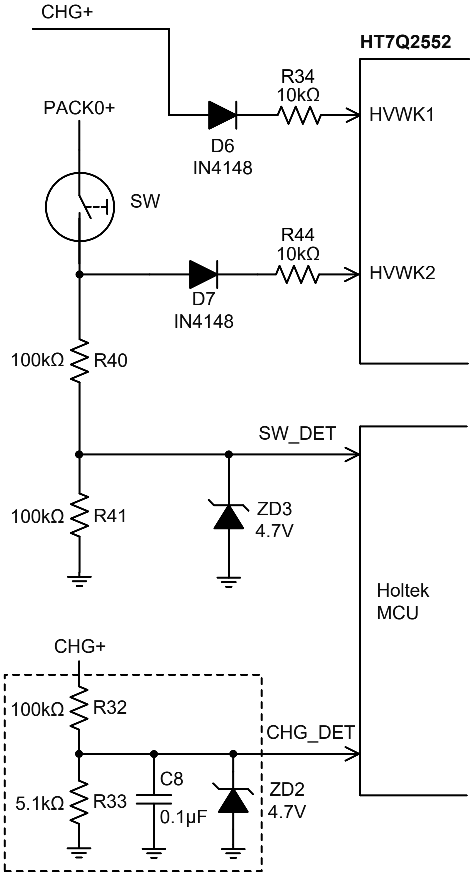
The High-voltage wake-up (HVWK) function is capable of detecting charger plugged in or load switched on. Two recommended HVWK external circuits are listed below, the main distinction is between switch high-voltage wake-up and switch low-voltage wake-up, whereas the chargers are both high-voltage wake-up.

The first circuit is a typical application for charger or switch high-voltage wake-up function, switch active high detection, charger plugged-in detection and charger voltage detection.

When a charger is plugged in or load switch is on, the voltage of HVWK is triggered to be larger than V_{WKTH} and set the EXT_WK bit as “1”. After the charger is removed or the switch is turned off, the EXT_WK bit is reset to “0”. An MCU can acquire the charger or switch status by reading the EXT_WK bit through the I^2C interface. Therefore, by the means of reading the EXT_WK bit status, additional charger or switch detection circuits for MCU are not necessary.

When the MCU requires to directly detect the switch status, a clamp circuit R40, R41 and ZD3 should be added to prevent the high voltage generated by pressing SW from entering the SW_DET directly. The typical values of R40 and R41 are 100kΩ and the ZD3 is 4.7V. When the battery is at a low voltage (PACK0+ = 7.5V), the voltage divided ratio of R40 and R41 should be adjusted according to the situation to ensure that the SW_DET voltage is higher than the MCU high level threshold.

In addition, the MCU can use its ADC to read the CHG_DET and then calculate the charger voltage using the voltage divided ratio of R32 and R33. The typical values of R32 and R33 are 100kΩ and 5.1kΩ respectively.



Charger plugged-in and charger voltage detection

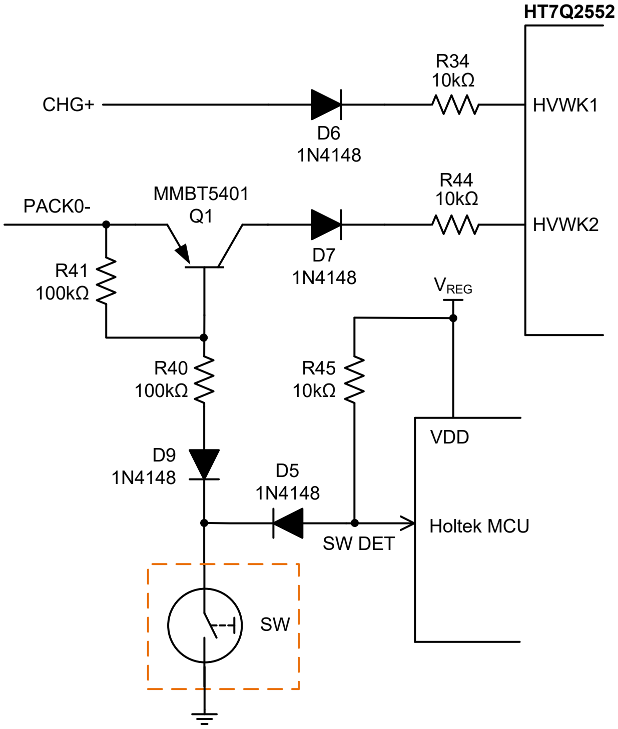
The second circuit is a typical application for charger high-voltage wake-up function, switch low-voltage wake-up function, switch active low detection, charger plugged-in detection and charger voltage detection. The charger detection parts are the same as the diagram above.

For the switch low-voltage wake-up function, the switch detection circuit needs to be changed, which can be obtained from the following application circuit. When the switch is turned on, the Q1 is switched on and the voltage of HVWK is triggered to be larger than V_{WKTH} and set the EXT_WK bit as "1". After the switch is turned off, the Q1 is switched off and the EXT_WK bit is reset to "0".

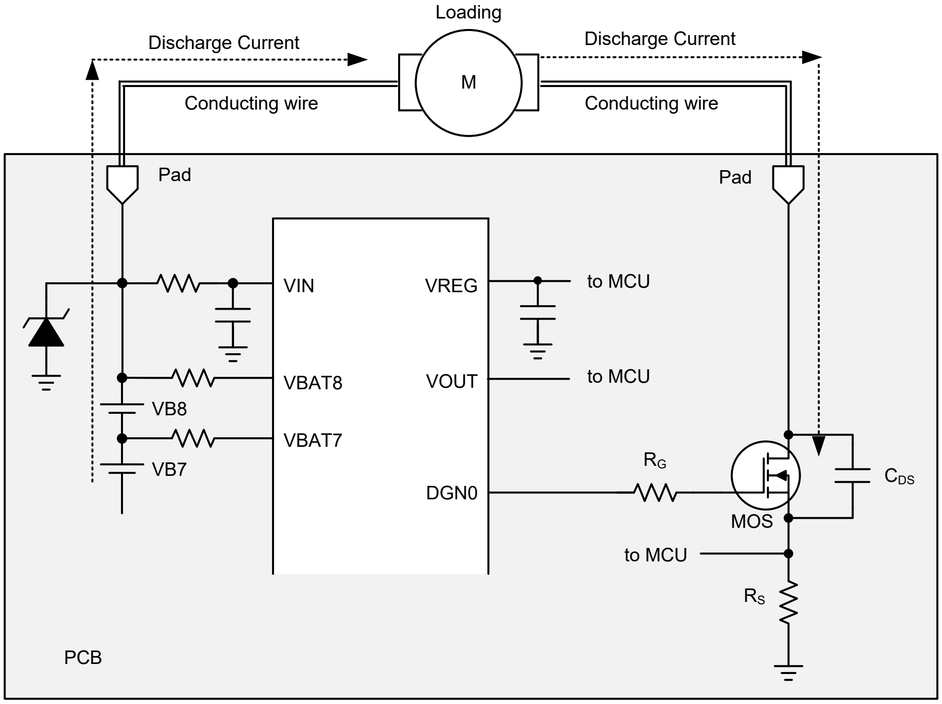
When the MCU requires to directly detect the switch status, a reverse diode D5 should be connected in series between the SW and SW_DET to prevent the high voltage when the switch is off from entering the MCU pin. The typical value of diode D5 is 1N4148.

In the switch off state, when the MCU has no internal pull-up resistor function, it is recommended to add R45, with a typical value of 10kΩ.

The resistance values of R41 and R40 should not be too small to avoid the current consumption after the switch is pressed. They must be matched with Q1. When Q1 is MMBT5401, the typical values of R41 and R40 are 100kΩ.



Voltage Spike Suppression Method



Simplified Typical BMS System Discharge Path Diagram

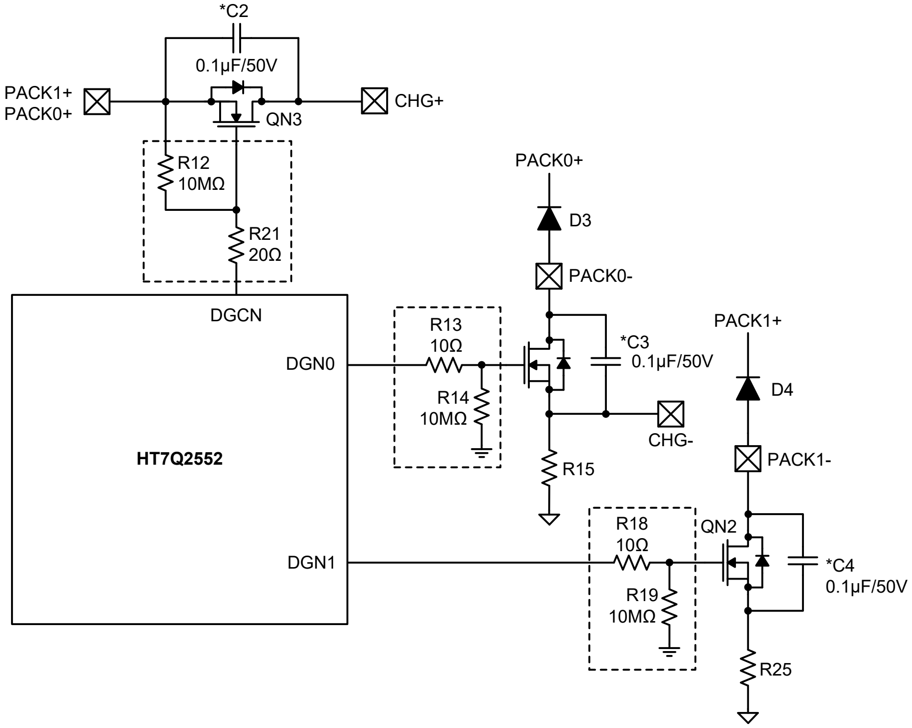
Most battery-management systems would monitor charge and discharge current to prevent over-current damage. Due to the parasitic inductance on conducting wires and PCB layout connections, large voltage spike may occurs while the MCU-controlled MOS rapidly shuts down the charge or discharge current, and this spike may damage the device VBAT0~8 or VIN pins. Any voltage spike on VBAT0~8 and VIN pins should not over the limitation in Absolute Maximum Ratings, which is 48V. Four recommended measures listed below would help to reduce the voltage spike.

1. Make the external conducting wire and PCB layout connections as short as possible where large charge or discharge current flows.
2. Adjust the slew rate of MOS switch with the gate resistor R_G. Turn off the MOS with slower slew rate for lower voltage spike, and the tradeoff is a slower protection response time.
3. Add a capacitor (C_{DS}) between drain and source node of the MOS switch as shown above. The recommended capacitance is 0.1μF to 0.22μF.
4. Add a 39V Zener diode between the highest voltage potential node of battery cells and GND.

System ESD/EFT Protection Circuit Description

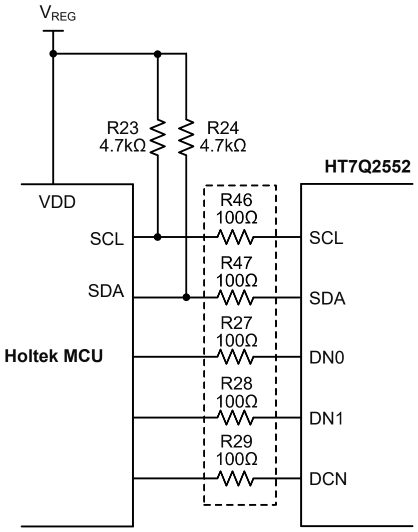
Charge/Discharge Circuit

With reference to the following application circuit, connect pull-down resistors R12, R14 and R19 to the device DGCN, DGN0 and DGN1 pins respectively, with typical values of 10MΩ. Connect resistors R21, R13 and R18 to the MOSFET gate nodes, with typical values of 20Ω, 10Ω and 10Ω. The typical values of C2, C3 and C4 capacitors are 0.1µF, which can reduce the external electrostatic energy of PACK+, CHG+, CHG- and PACK-. In the PCB layout, the above components should be placed close to the MOSFET pins.



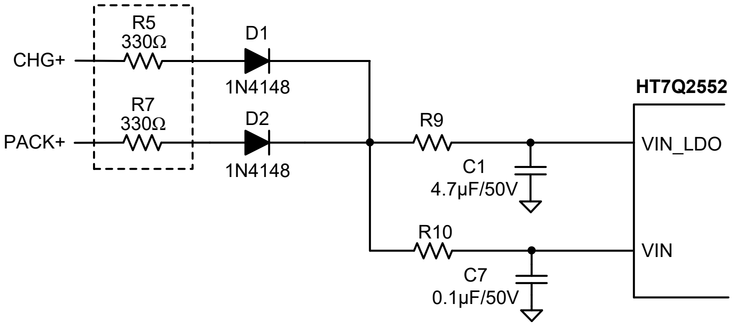
I/O Port

Connect series resistors between the device I/O pins and the MCU, which are used as limiting electrostatic energy components. The typical values of R46, R47, R27, R28 and R29 resistors are 100Ω. It is recommended that these components are placed close to the device I/O pins in the PCB layout.



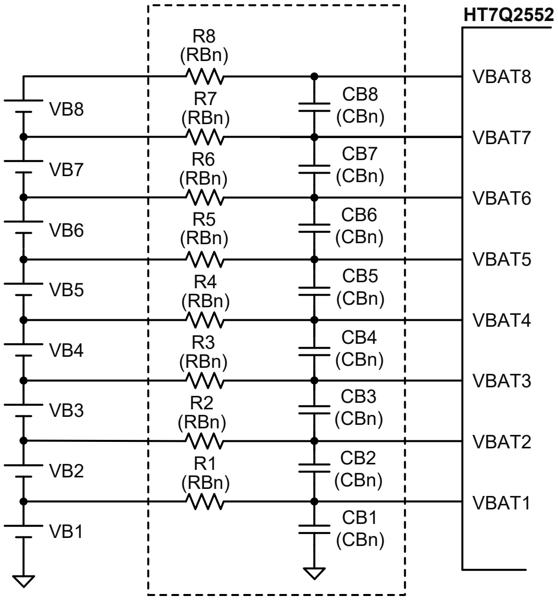
Power

The R5 and R7 resistors can reduce the external electrostatic energy of CHG+ and PACK+, which are typically 330Ω. They should be placed close to the CHG+ and PACK+ terminals in the PCB layout. It should be noted that R5, R7 and R9 limit the VREG maximum current output, and the resistance values of these resistors require to be adjusted according to the actual applications.



Battery Detection Circuit

Add an RBn resistor at each battery cell detection path and add a CBn capacitor to ground near the device VBAT pin, which can limit the reduced electrostatic energy. The typical value of the RBn resistor is 100Ω, and the typical value of the CBn capacitor is 0.1µF.



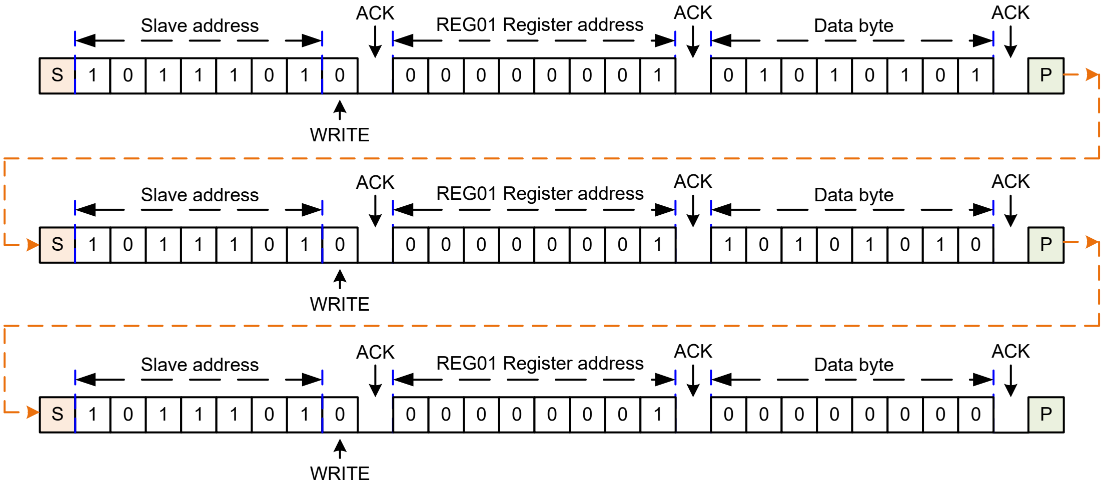
Cell Balance Register Off Method

Time to execute "Cell Balance Register Off":

1. Execute the operation once after the MCU is powered on.
2. When each battery cell measurement procedure is executed, if the difference between the battery cell lowest and highest voltage is greater than 200mV, it is necessary to execute the "Cell balance register off" once and then perform the measurement procedure for each battery cell again to ensure the measurement accuracy. If the voltage difference still exceeds 200mV, this indicates that the battery is unbalanced.

Considering that two adjacent cell balance registers cannot be on at the same time, it is necessary to turn off the cell balance register according to the following write logic:

1. Write 0x55 to the cell balance register (REG01)
2. Write 0xAA
3. Write 0x00

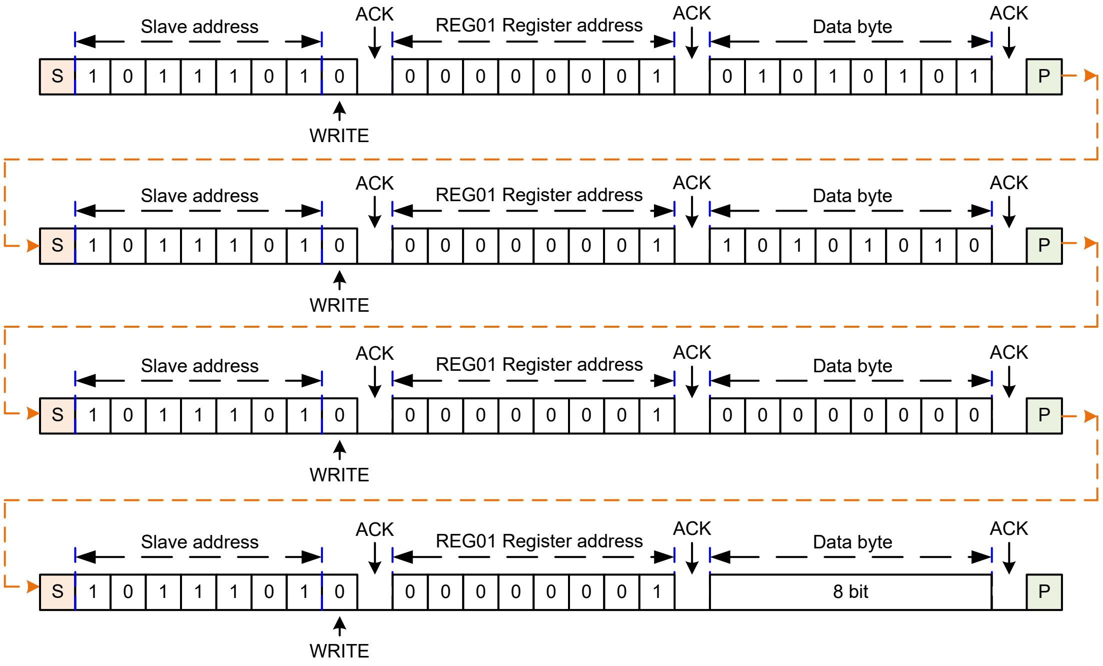


Cell Balance Register Off Method

Cell Balance Register On Method

Considering that two adjacent cell balance registers cannot be on at the same time, it is necessary to turn on the cell balance register according to the following write logic:

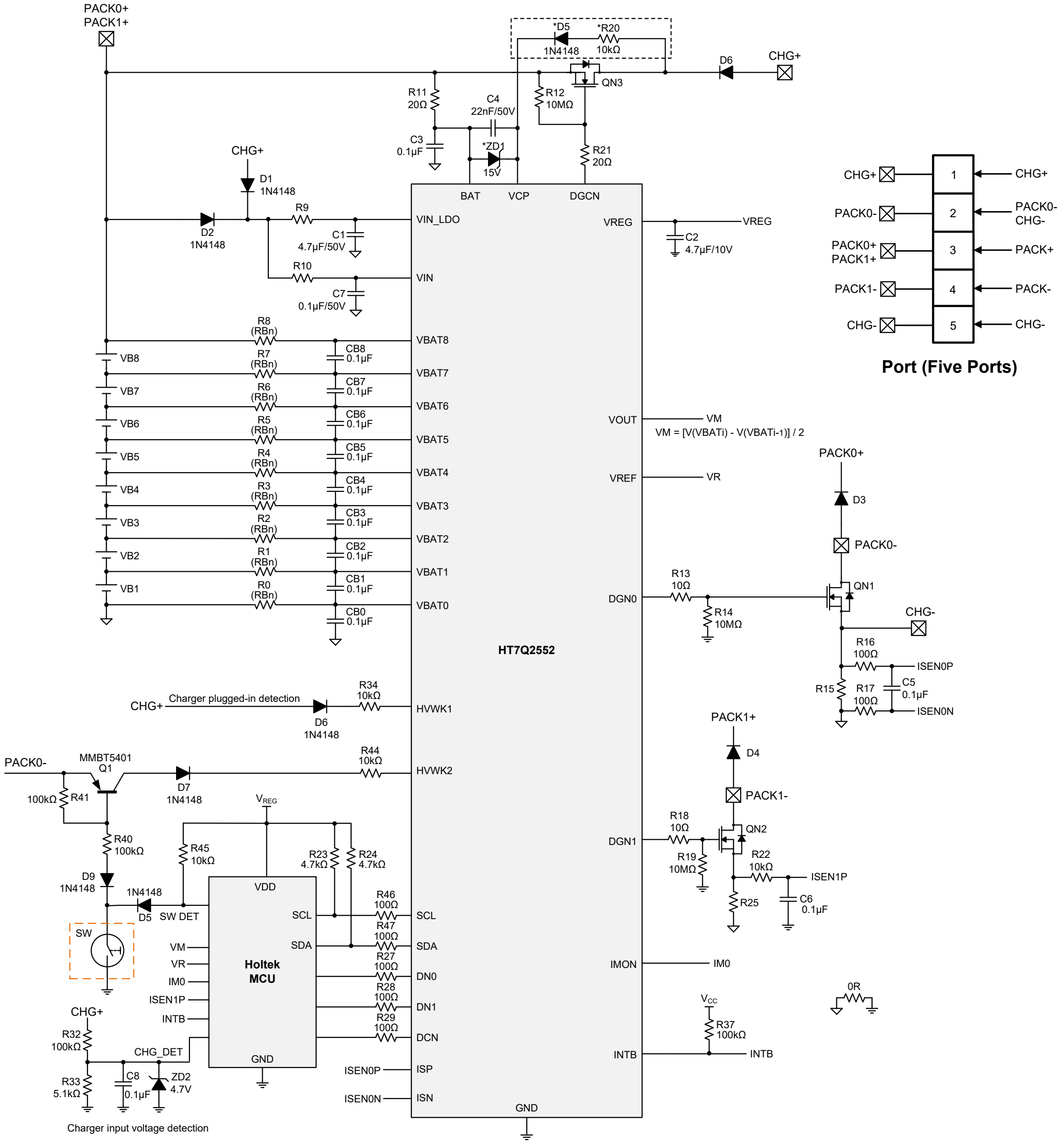
1. Write 0x55 to the cell balance register (REG01)
2. Write 0xAA
3. Write 0x00
4. Write to the battery cell that needs to be turned on



Cell Balance Register On Method

Typical Application Circuit

8S Battery Monitoring Typical Application Circuit



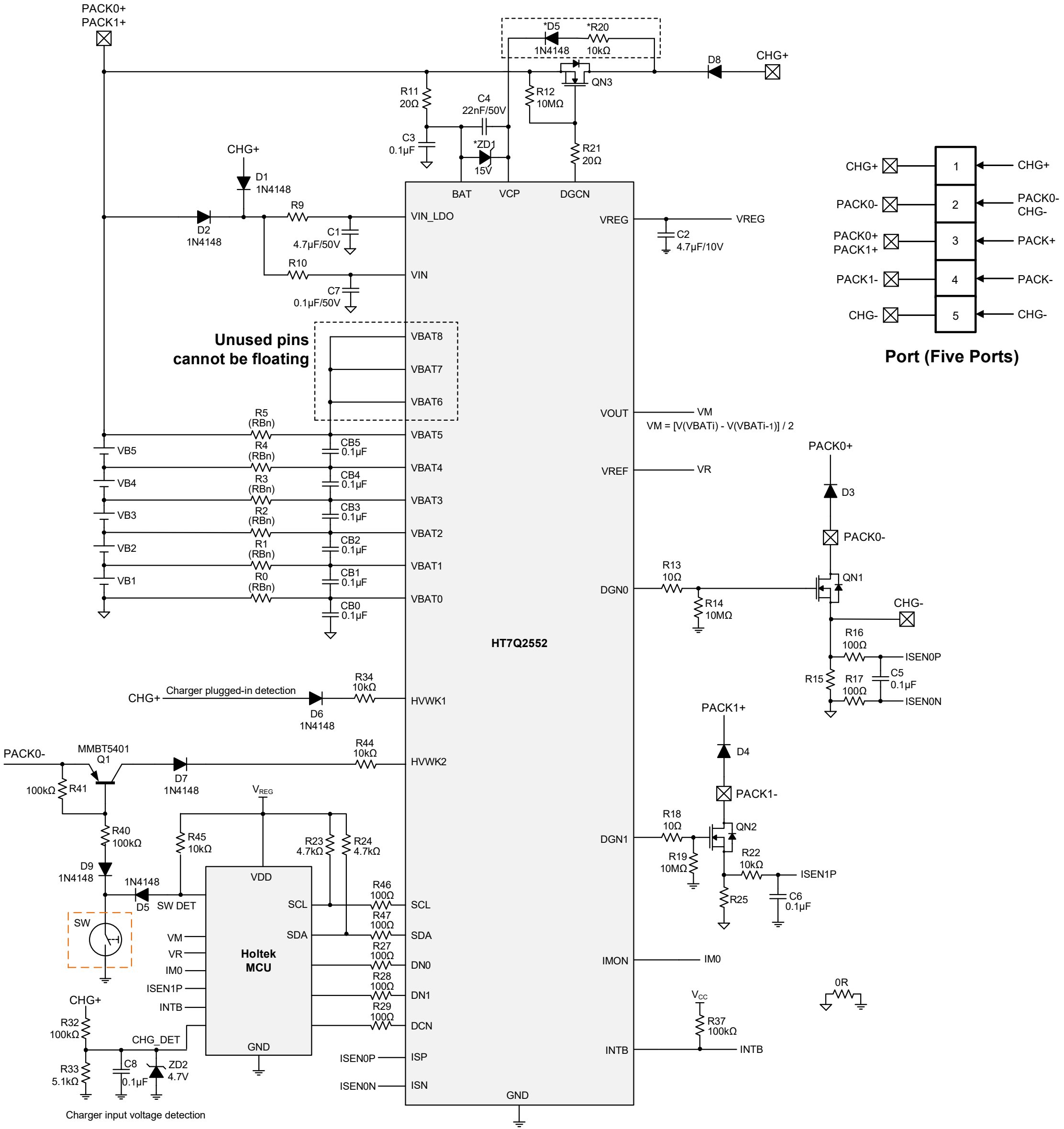
Note: 1. The resistance of R0~R8 can be adjusted to fit desired balance current. The recommended resistance of R0~R8 are listed in the ‘VBAT0~8 Protection and Balance Resistor Selection’ section.

2. If less than 8 serial batteries are used, connect the unused VBAT0~8 to the highest voltage potential. Do not leave any VBAT0~8 pin floating in order to prevent damage to the device.

3. The maximum capacitance of C2 is 4.7μF.

4. D5, R20 and ZD1 marked with * need to be added only when V_{IN}<7.5V, that is, charging is required. If this condition does not exist, there is no need to add the component.

5S Battery Monitoring Typical Application Circuit



Note: 1. The resistance of R0~R5 can be adjusted to fit desired balance current. The recommended resistance of R0~R5 are listed in the 'VBAT0~8 Protection and Balance Resistor Selection' section.

2. If less than 8 serial batteries are used, connect the unused VBAT0~8 to the highest voltage potential. Do not leave any VBAT0~8 pin floating in order to prevent damage to the device.

3. The maximum capacitance of C2 is 4.7μF.

4. D5, R20 and ZD1 marked with * need to be added only when V_{IN}<7.5V, that is, charging is required. If this condition does not exist, there is no need to add the component.

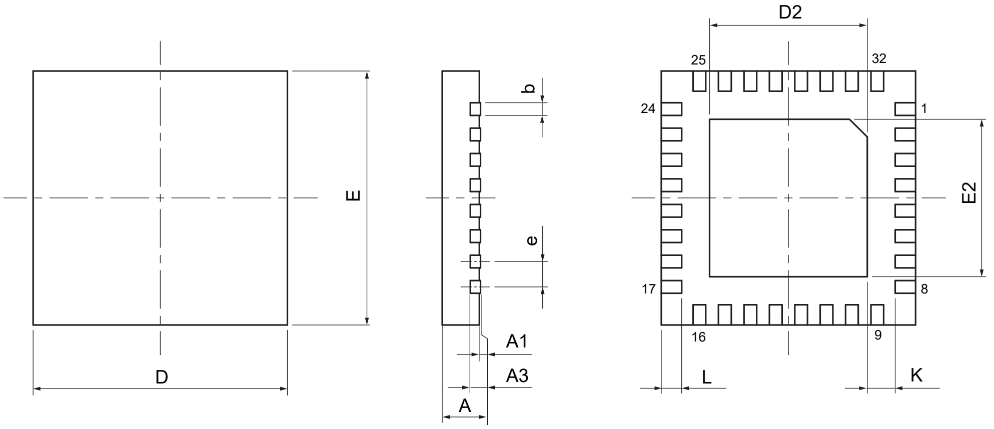
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

SAW Type 32-pin QFN (4mm×4mm×0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	0.008 REF		
b	0.006	0.008	0.010
D	0.157 BSC		
E	0.157 BSC		
e	0.016 BSC		
D2	0.100	—	0.108
E2	0.100	—	0.108
L	0.010	—	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	4.00 BSC		
E	4.00 BSC		
e	0.40 BSC		
D2	2.55	—	2.75
E2	2.55	—	2.75
L	0.25	—	0.45
K	0.20	—	—

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