

### Features

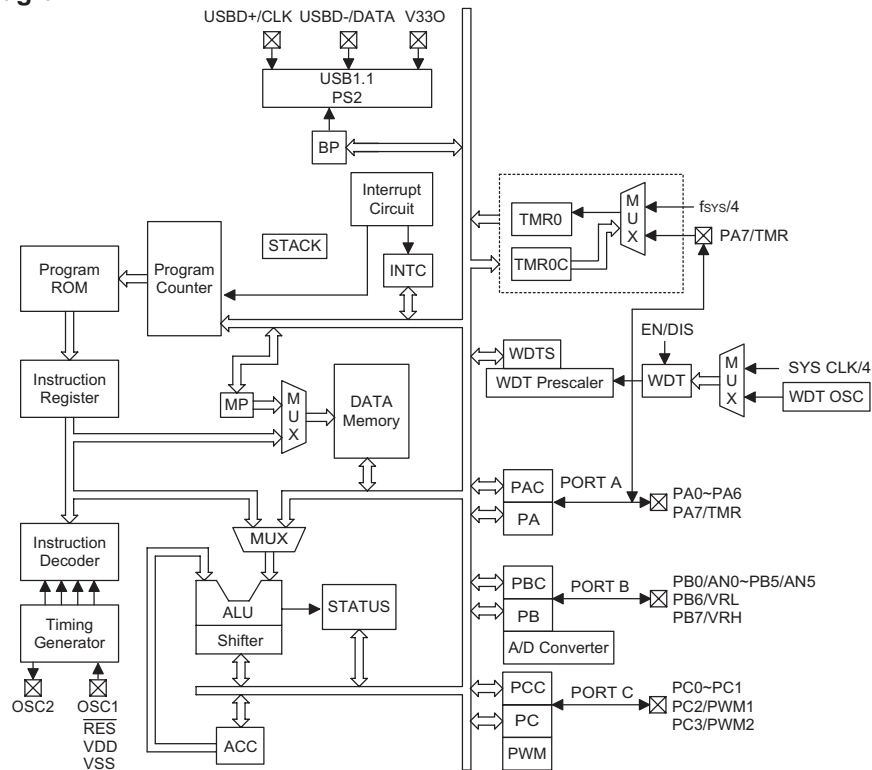
- Flexible total solution for applications that combine PS/2 and low-speed USB interface, such as mice, joysticks, and many others
- USB Specification Compliance
  - Conforms to USB specification V1.1
  - Conforms to USB HID specification V1.1
- Supports 1 Low-speed USB control endpoint and 1 interrupt endpoint
- Each endpoint has 8×8 bytes FIFO
- Integrated USB transceiver
- 3.3V regulator output
- External 6MHz or 12MHz ceramic resonator or crystal
- 8-bit RISC microcontroller, with 2K×14 EPROM (000H~7FFH)
- 96 bytes RAM (20H~7FH)
- 6MHz/12MHz internal CPU clock
- 4-level stacks
- Two 8-bit indirect addressing registers
- One 16-bit programmable timer counter with overflow interrupt (shared with PA7, vector 0CH)
- One USB interrupt input (vector 04H)
- HALT function and wake-up feature reduce power consumption
- PA0~PA7 support wake-up function
- Internal Power-On reset (POR)
- Watchdog Timer (WDT)
- 20 I/O ports (including 2-PWM output, PC2, PC3)
- 2 PWM output (PC2, PC3)
- Can produce PWM frequency range from 23Hz to 23kHz
- Built-in 8-bit Analog-to-Digital Converter, (6-channel for internal mode (PB0~PB5), 6-channel for external mode with VHL (PB7) and VRL (PB6))
- 20/28-pin SOP package

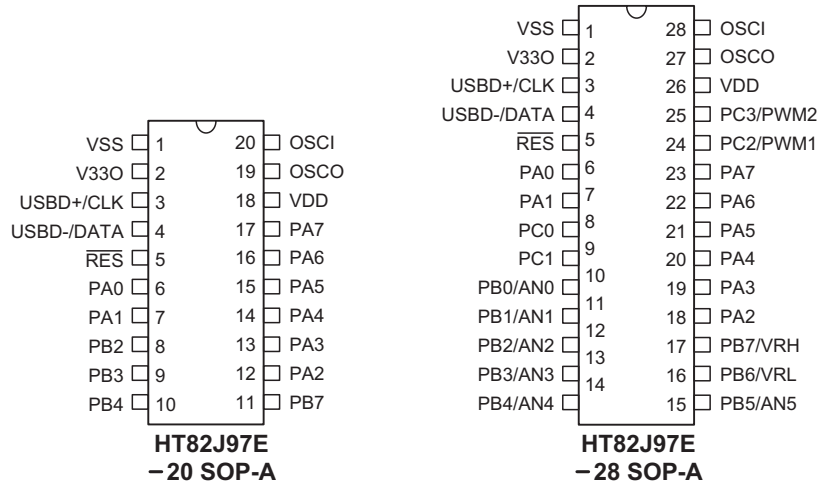
### General Description

The USB MCU OTP body is suitable for USB mouse and USB joystick devices. It consists of a Holtek high

performance 8-bit MCU core for control unit, built-in USB SIE, 2K×14 EPROM and 96 bytes data RAM.

### Block Diagram



**Pin Assignment**

**Pin Description**

| Pin Name   | I/O    | ROM Code Option                                    | Description   |
|--|--------|--|---|
| PA0~PA7  | I/O    | Pull-low<br>Pull-high<br>Wake-up<br>CMOS/NMOS/PMOS | Bidirectional 8-bit input/output port. Each bit can be configured as a wake-up input by ROM code option. The input or output mode is controlled by PAC (PA control register).<br>Pull-high resistor options: PA0~PA7<br>Pull-low resistor options: PA0~PA3<br>CMOS/NMOS/PMOS options: PA0~PA7<br>Wake-up options: PA0~PA7 |
| PB0/AN0<br>PB1/AN1<br>PB2/AN2<br>PB3/AN3<br>PB5/AN5<br>PB6/VRL | I/O    | Pull-high<br>Analog input                          | Bidirectional 8-bit input/output port. Software instructions determine the CMOS output or Schmitt trigger input with pull-high resistor (determined by pull-high options).<br>The PB can be used as analog input of the analog to digital converter (determined by options).<br>Pull-low resistor for options: PB2, PB3   |
| PB4/AN4<br>PB7/VRH   | I/O    | Pull-high<br>Analog input<br>Wake-up               | Bidirectional 8-bit input/output port. Software instructions determine the CMOS output or Schmitt trigger input with pull-high resistor (determined by pull-high options).<br>The PB can be used as analog input of the analog to digital converter (determined by options).<br>Wake-up options: PB4, PB7                 |
| VSS  | —      | —  | Negative power supply, ground   |
| PC0~PC3  | I/O    | Pull-high  | Bidirectional I/O lines. Software instructions determine the CMOS output or Schmitt trigger input with pull-high resistor (determined by pull-high options).<br>PC2 can be used as PWM1 output<br>PC3 can be used as PWM2 output  |
| RES  | I      | —  | Schmitt trigger reset input. Active low.  |
| VDD  | —      | —  | Positive power supply   |
| V33O   | O      | —  | 3.3V regulator output   |
| USBBD+/CLK   | I/O    | —  | USBBD+ or PS2 CLK I/O line<br>USB or PS2 function is controlled by software control register  |
| USBBD-/DATA  | I/O    | —  | USBBD- or PS2 DATA I/O line<br>USB or PS2 function is controlled by software control register   |
| OSC1<br>OSCO   | I<br>O | —  | OSC1, OSCO are connected to a 6MHz or 12MHz crystal/resonator (determined by software instructions) for the internal system clock.  |

**Absolute Maximum Ratings**

|                      |                                |                            |                                  |
|----------------------|--------------------------------|----------------------------|----------------------------------|
| Supply Voltage ..... | $V_{SS}-0.3V$ to $V_{SS}+6.0V$ | Storage Temperature .....  | $-50^{\circ}C$ to $125^{\circ}C$ |
| Input Voltage.....   | $V_{SS}-0.3V$ to $V_{DD}+0.3V$ | Operating Temperature..... | $0^{\circ}C$ to $70^{\circ}C$    |

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**D.C. Characteristics**

Ta=25°C

| Symbol           | Parameter  | Test Conditions |                                 | Min.               | Typ. | Max.               | Unit |
|------------------|--|-----------------|---------------------------------|--------------------|------|--------------------|------|
|                  |  | V <sub>DD</sub> | Conditions                      |                    |      |                    |      |
| V <sub>DD</sub>  | Operating Voltage  | —               | —                               | 4                  | —    | 5.5                | V    |
| I <sub>DD</sub>  | Operating Current (6MHz Crystal)                                 | 5V              | No load, f <sub>SYS</sub> =6MHz | —                  | 7    | 9                  | mA   |
| I <sub>STB</sub> | Standby Current  | 5V              | No load, system HALT            | —                  | 300  | 500                | μA   |
| V <sub>IL1</sub> | Input Low Voltage for I/O Ports                                  | 5V              | —                               | 0                  | —    | 0.8                | V    |
| V <sub>IH1</sub> | Input High Voltage for I/O Ports                                 | 5V              | —                               | 2                  | —    | 5                  | V    |
| V <sub>IL2</sub> | Input Low Voltage ( $\overline{RES}$ )                           | 5V              | —                               | 0                  | —    | 0.4V <sub>DD</sub> | V    |
| V <sub>IH2</sub> | Input High Voltage ( $\overline{RES}$ )                          | 5V              | —                               | 0.9V <sub>DD</sub> | —    | V <sub>DD</sub>    | V    |
| I <sub>OL</sub>  | Output Sink Current for Other Ports PA0~PA7, PB0~PB7 and PC0~PC3 | 5V              | V <sub>OL</sub> =0.4V           | 2                  | 4    | —                  | mA   |
| I <sub>OH</sub>  | Output Port Source Current                                       | 5V              | V <sub>OL</sub> =3.4V           | -2.5               | -4   | —                  | mA   |
| R <sub>PD</sub>  | Pull-down Resistance for PA0~PA3, PB2 and PB3                    | 5V              | —                               | 10                 | 30   | 50                 | kΩ   |
| R <sub>PH1</sub> | Pull-high Resistance for CLK and DATA                            | —               | —                               | 2                  | 4.7  | 6                  | kΩ   |
| R <sub>PH2</sub> | Pull-high Resistance for PA0~PA7, PB0~PB7 and PC0~PC3            | —               | —                               | 30                 | 50   | 70                 | kΩ   |
| V <sub>LVR</sub> | Low Voltage Reset  | 5V              | —                               | 2.4                | 2.7  | 3                  | V    |

**A.C. Characteristics**

Ta=25°C

| Symbol             | Parameter   | Test Conditions |                       | Min. | Typ. | Max. | Unit               |
|--------------------|---|-----------------|-----------------------|------|------|------|--------------------|
|                    |   | V <sub>DD</sub> | Conditions            |      |      |      |                    |
| f <sub>SYS</sub>   | System Clock (Crystal OSC)                                  | 5V              | —                     | 6    | —    | 12   | MHz                |
| f <sub>RCSYS</sub> | RC Clock with 8-bit Prescaler Register                      | 5V              | —                     | 0    | 32   | —    | kHz                |
| t <sub>WDT</sub>   | Watchdog Time-out Period (System Clock)                     | —               | Without WDT prescaler | 1024 | —    | —    | t <sub>RCSYS</sub> |
| t <sub>RF</sub>    | USB <sub>D+</sub> , USB <sub>D-</sub> Rising & falling Time | —               | —                     | 75   | —    | 300  | ns                 |
| t <sub>SST</sub>   | System Start-up Timer Period                                | —               | Wake-up from HALT     | —    | 1024 | —    | t <sub>SYS</sub>   |
| t <sub>OSC</sub>   | Crystal Setup   | —               | —                     | —    | 5    | 10   | ms                 |
| f <sub>PWM</sub>   | PWM Cycle Frequency   | —               | 6MHz or 12MHz         | 23   | —    | 2300 | Hz                 |

Note: Power-on period=t<sub>WDT</sub>+t<sub>SST</sub>+t<sub>OSC</sub>  
 WDT Time-out in normal mode=1/f<sub>RCSYS</sub>×256×WDTS+t<sub>WDT</sub>  
 WDT Time-out in HALT mode=1/f<sub>RCSYS</sub>×256×WDTS+t<sub>SST</sub>+t<sub>OSC</sub>

**Functional Description**

**Execution Flow**

The system clock for the microcontroller is derived from either 6MHz or 12MHz crystal oscillator, which used a frequency that is determined by the SCLKSEL bit of the SCC Register. The default system frequency is 12MHz. The system clock is internally divided into four non-overlapping clocks. One instruction cycle consists of four system clock cycles.

Instruction fetching and execution are pipelined in such a way that a fetch takes an instruction cycle while decoding and execution takes the next instruction cycle. However, the pipelining scheme causes each instruction to be effectively executed in a cycle. If an instruction changes the program counter, two cycles are required to complete the instruction.

**Program Counter – PC**

The program counter (PC) controls the sequence in which the instructions stored in the program ROM are executed and its contents specify a full range of program memory.

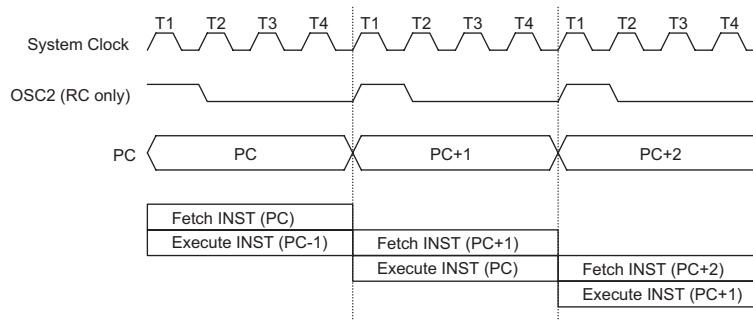
After accessing a program memory word to fetch an instruction code, the contents of the program counter are incremented by one. The program counter then points to the memory word containing the next instruction code.

When executing a jump instruction, conditional skip execution, loading to the PCL register, performing a sub-routine call or return from subroutine, initial reset, internal interrupt, external interrupt or return from interrupts, the PC manipulates the program transfer by loading the address corresponding to each instruction.

The conditional skip is activated by instructions. Once the condition is met, the next instruction, fetched during the current instruction execution, is discarded and a dummy cycle replaces it to get the proper instruction. Otherwise proceed with the next instruction.

The lower byte of the program counter (PCL) is a readable and writeable register (06H). Moving data into the PCL performs a short jump. The destination will be within the current program ROM page.

When a control transfer takes place, an additional dummy cycle is required.



**Execution Flow**

| Mode                         | Program Counter |    |    |    |    |    |    |    |    |    |    |
|------------------------------|-----------------|----|----|----|----|----|----|----|----|----|----|
|                              | *10             | *9 | *8 | *7 | *6 | *5 | *4 | *3 | *2 | *1 | *0 |
| Initial Reset                | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| USB Interrupt                | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| Timer/Event Counter Overflow | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  |
| Skip                         | PC+2            |    |    |    |    |    |    |    |    |    |    |
| Loading PCL                  | *10             | *9 | *8 | @7 | @6 | @5 | @4 | @3 | @2 | @1 | @0 |
| Jump, Call Branch            | #10             | #9 | #8 | #7 | #6 | #5 | #4 | #3 | #2 | #1 | #0 |
| Return from Subroutine       | S10             | S9 | S8 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

**Program Counter**

Note: \*10~\*0: Program counter bits  
#10~#0: Instruction code bits

S10~S0: Stack register bits  
@7~@0: PCL bits

**Program Memory – ROM**

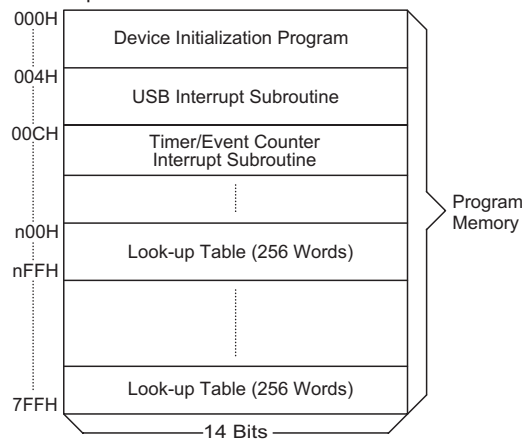
The program memory is used to store the program instructions which are to be executed. It also contains data, table, and interrupt entries, and is organized into 2048×14 bits, addressed by the program counter and table pointer.

Certain locations in the program memory are reserved for special usage:

- Location 000H  
This area is reserved for program initialization. After a chip reset, the program always begins execution at location 000H.
- Location 004H  
This area is reserved for the USB interrupt service program. If the USB interrupt is activated, the interrupt is enabled and the stack is not full, the program begins execution at location 004H.
- Location 00CH  
This location is reserved for the Timer/Event Counter interrupt service program. If a timer interrupt results from a Timer/Event Counter overflow, and the interrupt is enabled and the stack is not full, the program begins execution at location 00CH.

• Table location

Any location in the program memory can be used as look-up tables. There are three method to read the



Note: n ranges from 0 to 7

**Program Memory**

ROM data by two table read instructions: "TABRDC" and "TABRDL", transfer the contents of the lower-order byte to the specified data memory, and the higher-order byte to TBLH (08H).

The three methods are shown as follows:

- ♦ The instructions "TABRDC [m]" (the current page, one page=256words), where the table locations is defined by TBLP (07H) in the current page. And the ROM code option TBHP is disabled (default).
- ♦ The instructions "TABRDC [m]", where the table locations is defined by registers TBLP (07H) and TBHP (01FH). And the ROM code option TBHP is enabled.
- ♦ The instructions "TABRDL [m]", where the table locations is defined by Registers TBLP (07H) in the last page (0700H-07FFH).

Only the destination of the lower-order byte in the table is well-defined, the other bits of the table word are transferred to the lower portion of TBLH, and the remaining 1-bit words are read as "0". The Table Higher-order byte register (TBLH) is read only. The table pointer (TBLP, TBHP) is a read/write register (07H, 1FH), which indicates the table location. Before accessing the table, the location must be placed in the TBLP and TBHP (If the OTP option TBHP is disabled, the value in TBHP has no effect). The TBLH is read only and cannot be restored. If the main routine and the ISR (Interrupt Service Routine) both employ the table read instruction, the contents of the TBLH in the main routine are likely to be changed by the table read instruction used in the ISR. Errors can occur. In other words, using the table read instruction in the main routine and the ISR simultaneously should be avoided. However, if the table read instruction has to be applied in both the main routine and the ISR, the interrupt should be disabled prior to the table read instruction. It will not be enabled until the TBLH has been backed up. All table related instructions require two cycles to complete the operation. These areas may function as normal program memory depending on the requirements.

Once TBHP is enabled, the instruction "TABRDC [m]" reads the ROM data as defined by TBLP and TBHP value. Otherwise, the ROM code option TBHP is disabled, the instruction "TABRDC [m]" reads the ROM data as defined by TBLP and the current program counter bits.

| Instruction | Table Location |    |    |    |    |    |    |    |    |    |    |
|-------------|----------------|----|----|----|----|----|----|----|----|----|----|
|             | *10            | *9 | *8 | *7 | *6 | *5 | *4 | *3 | *2 | *1 | *0 |
| TABRDC [m]  | P10            | P9 | P8 | @7 | @6 | @5 | @4 | @3 | @2 | @1 | @0 |
| TABRDL [m]  | 1              | 1  | 1  | @7 | @6 | @5 | @4 | @3 | @2 | @1 | @0 |

**Table Location**

Note: \*10~\*0: Table location bits  
@7~@0: TBLP bits

P10~P8: Current program counter bits when TBHP is disabled  
TBHP register bit2~bit0 when TBHP is enabled

**Stack Register – STACK**

This is a special part of the memory which is used to save the contents of the program counter (PC) only. The stack is organized into 8 levels and is neither part of the data nor part of the program space, and is neither readable nor writeable. The activated level is indexed by the stack pointer (SP) and is neither readable nor writeable. At a subroutine call or interrupt acknowledge signal, the contents of the program counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled by a return instruction (RET or RETI), the program counter is restored to its previous value from the stack. After a chip reset, the SP will point to the top of the stack.

If the stack is full and a non-masked interrupt takes place, the interrupt request flag will be recorded but the acknowledge signal will be inhibited. When the stack pointer is decremented (by RET or RETI), the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. In a similar case, if the stack is full and a "CALL" is subsequently executed, stack overflow occurs and the first entry will be lost (only the most recent 8 return addresses are stored).

**Data Memory – RAM for Bank 0**

The data memory is designed with 96×8 bits. The data memory is divided into two functional groups: special function registers and general purpose data memory (96×8). Most are read/write, but some are read only.

The special function registers include the indirect addressing registers (R0;00H, R1;02H), Bank register (BP, 04H), PWM1 duty register (0DH), PWM2 duty register (0EH), Timer/Event Counter higher order byte register (TMRH;0FH), Timer/Event Counter lower order byte register (TMRL;10H), Timer/Event Counter control register (TMRC;11H), program counter lower-order byte register (PCL;06H), memory pointer registers (MP0;01H, MP1;03H), accumulator (ACC;05H), table pointers (TBLP;07H, TBHP;1FH), table higher-order byte register (TBLH;08H), status register (STATUS;0AH), interrupt control register (INTC;0BH), Watchdog Timer option setting register (WDTS;09H), I/O registers (PA;12H, PB;14H, PC;16H), PWM Base Period Register (18H), I/O control registers (PAC;13H, PBC;15H, PCC;17H). USB/PS2 status and control register (USC;1AH), USB endpoint interrupt status register (USR;1BH), system clock control register (SCC;1CH). A/D converter status and control register (ADSC;1DH) and A/D converter result register (ADR;1EH). The remaining space before the 20H is reserved for future ex-

| Bank 0 |  |
|--------|--|
| 00H    | Indirect Addressing Register 0               |
| 01H    | MP0  |
| 02H    | Indirect Addressing Register 1               |
| 03H    | MP1  |
| 04H    | BP   |
| 05H    | ACC  |
| 06H    | PCL  |
| 07H    | TBLP   |
| 08H    | TBLH   |
| 09H    | WDTS   |
| 0AH    | STATUS                                       |
| 0BH    | INTC   |
| 0CH    | PWM1 Duty Register                           |
| 0DH    | PWM2 Duty Register                           |
| 0EH    |  |
| 0FH    | TMRH   |
| 10H    | TMRL   |
| 11H    | TMRC   |
| 12H    | PA   |
| 13H    | PAC  |
| 14H    | PB   |
| 15H    | PBC  |
| 16H    | PC   |
| 17H    | PCC  |
| 18H    | PWM Base Period Register (PD)                |
| 19H    |  |
| 1AH    | USC  |
| 1BH    | USR  |
| 1CH    | SCC  |
| 1DH    | ADSC   |
| 1EH    | ADR  |
| 1FH    | TBHP   |
| 20H    | General Purpose<br>DATA MEMORY<br>(96 Bytes) |
| 21H    |  |
| 22H    |  |
| 23H    |  |
| 24H    |  |
| 25H    |  |
| 26H    |  |
| 27H    |  |
| 7FH    |  |

**Bank 0 RAM Mapping**

panded usage and reading these locations will get "00H". The general purpose data memory, addressed from 20H to 7FH, is used for data and control information under instruction commands.

All of the data memory areas can handle arithmetic, logic, increment, decrement and rotate operations directly. Except for some dedicated bits, each bit in the data memory can be set and reset by "SET [m].i" and "CLR [m].i". They are also indirectly accessible through memory pointer registers (MP0 or MP1).

**Data Memory – RAM for Bank 1**

The special function registers used in the USB interface are located in RAM Bank1. In order to access Bank1 register, only the Indirect addressing pointer MP1 can be used and the Bank register BP should be set to 1. The RAM bank 1 mapping is as shown.

| Bank 1 |                                |
|--------|--------------------------------|
| 00H    | Indirect Addressing Register 0 |
| 01H    | MP0                            |
| 02H    | Indirect Addressing Register 1 |
| 03H    | MP1                            |
| 04H    | BP                             |
| 05H    | ACC                            |
| 06H    | PCL                            |
| 07H    | TBLP                           |
| 08H    | TBLH                           |
| 09H    | WDT5                           |
| 0AH    | STATUS                         |
| 0BH    | INTC                           |
| 0CH    | PWM1 Duty Register             |
| 0DH    | PWM2 Duty Register             |
| 0EH    |                                |
| 0FH    | TMRH                           |
| 10H    | TMRL                           |
| 11H    | TMRC                           |
| 12H    | PA                             |
| 13H    | PAC                            |
| 14H    | PB                             |
| 15H    | PBC                            |
| 16H    | PC                             |
| 17H    | PCC                            |
| 18H    | PWM Base Period Register (PD)  |
| 19H    |                                |
| 1AH    | USC                            |
| 1BH    | USR                            |
| 1CH    | SCC                            |
| 1DH    | ADSC                           |
| 1EH    | ADR                            |
| 1FH    | TBHP                           |
| 20H    |                                |
| 41H    | Pipe_ctrl                      |
| 42H    | AWR                            |
| 43H    | STALL                          |
| 44H    | PIPE                           |
| 45H    | SIES                           |
| 46H    | MISC                           |
| 47H    |                                |
| 48H    | FIFO 0                         |
| 49H    | FIFO 1                         |

**RAM Bank 1**

Address 00~1FH in RAM Bank0 and Bank1 are located in the same Registers

**Indirect Addressing Register**

Locations 00H and 02H are indirect addressing registers that are not physically implemented. Any read/write operation on [00H] ([02H]) will access the data memory pointed to by MP0 (MP1). Reading location 00H (02H) indirectly will return the result 00H. Writing indirectly results in no operation.

The indirect addressing pointer (MP0) always points to Bank0 RAM addresses no matter the value of Bank Register (BP).

The indirect addressing pointer (MP1) can access Bank0 or Bank1 RAM data according to the value of BP which is set to 0 or 1 respectively.

The memory pointer registers (MP0 and MP1) are 8-bit registers.

**Accumulator**

The accumulator is closely related to ALU operations. It is also mapped to location 05H of the data memory and can carry out immediate data operations. The data movement between two data memory locations must pass through the accumulator.

**Arithmetic and Logic Unit – ALU**

This circuit performs 8-bit arithmetic and logic operations. The ALU provides the following functions:

- Arithmetic operations (ADD, ADC, SUB, SBC, DAA)
- Logic operations (AND, OR, XOR, CPL)
- Rotation (RL, RR, RLC, RRC)
- Increment and Decrement (INC, DEC)
- Branch decision (SZ, SNZ, SIZ, SDZ ....)

The ALU not only saves the results of a data operation but also changes the status register.

**Status Register – STATUS**

This 8-bit register (0AH) contains the zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). It also records the status information and controls the operation sequence.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition, operations related to the status register may give different results from those intended.

| Labels | Bits | Function  |
|--------|------|---|
| C      | 0    | C is set if an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction. |
| AC     | 1    | AC is set if an operation results in a carry out of the low nibbles in addition or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.  |
| Z      | 2    | Z is set if the result of an arithmetic or logic operation is zero; otherwise Z is cleared.   |
| OV     | 3    | OV is set if an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.   |
| PDF    | 4    | PDF is cleared by a system power-up or executing the "CLR WDT" instruction. PDF is set by executing the "HALT" instruction.   |
| TO     | 5    | TO is cleared by a system power-up or executing the "CLR WDT" or "HALT" instruction. TO is set by a WDT time-out.   |
| —      | 6    | Unused bit, read as "0"   |
| —      | 7    | Unused bit, read as "0"   |

### Status Register

The TO flag can be affected only by a system power-up, a WDT time-out or executing the "CLR WDT" or "HALT" instruction. The PDF flag can be affected only by executing the "HALT" or "CLR WDT" instruction or during a system power-up.

The Z, OV, AC and C flags generally reflect the status of the latest operations.

In addition, upon entering the interrupt sequence or executing a subroutine call, the status register will not be automatically pushed onto the stack. If the contents of the status are important and if the subroutine can corrupt the status register, precautions must be taken to save it properly.

### Interrupt

The device provides an external interrupt and internal timer/event counter interrupts. The Interrupt Control Register (INTC;0BH) contains the interrupt control bits to set the enable/disable and the interrupt request flags.

Once an interrupt subroutine is serviced, all the other interrupts will be blocked (by clearing the EMI bit). This scheme may prevent any further interrupt nesting. Other interrupt requests may occur during this interval but only the interrupt request flag is recorded. If a certain interrupt requires servicing within the service routine, the EMI bit and the corresponding bit of the INTC may be set to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the SP is decremented. If immediate service is desired, the stack must be prevented from becoming full.

All these kinds of interrupts have a wake-up capability. As an interrupt is serviced, a control transfer occurs by pushing the program counter onto the stack, followed by a branch to a subroutine at a specified location in the program memory. Only the program counter is pushed onto the stack. If the contents of the register or status register (STATUS) are altered by the interrupt service program which corrupts the desired control sequence, the contents should be saved in advance.

| Register      | Bit No. | Label | Function   |
|---------------|---------|-------|--|
| INTC<br>(0BH) | 0       | EMI   | Controls the master (global) interrupt (1=enable; 0=disable)     |
|               | 1       | EUI   | Controls the USB interrupt (1=enable; 0= disable)                |
|               | 2       | —     | Unused bit, read as "0"  |
|               | 3       | ETI   | Controls the Timer/Event Counter interrupt (1=enable; 0=disable) |
|               | 4       | USBF  | USB interrupt request flag (1=active; 0=inactive)                |
|               | 5       | —     | Unused bit, read as "0"  |
|               | 6       | TF    | Internal timer/event counter request flag (1:active; 0:inactive) |
|               | 7       | —     | Unused bit, read as "0"  |

### INTC Register



The USB interrupts are triggered by the following USB events and the related interrupt request flag (USBF; bit 4 of the INTC) will be set.

- Access of the corresponding USB FIFO from PC
- suspend signal from PC
- resume signal from PC
- USB Reset signal

When the interrupt is enabled, the stack is not full and the external interrupt is active, a subroutine call to location 04H will occur. The interrupt request flag (USBF) and EMI bits will be cleared to disable other interrupts.

When the PC Host access the FIFO of the HT82J97E, the corresponding request bit of the USR is set, and a USB interrupt is triggered. So user can easily decide which FIFO is accessed. When the interrupt has been served, the corresponding bit should be cleared by firmware. When the HT82J97E receives a USB Suspend signal from the Host PC, the suspend line (bit0 of the USC) of the HT82J97E is set and a USB interrupt is also triggered.

When the HT82J97E receives a Resume signal from the Host PC, the resume line (bit3 of the USC) of the HT82J97E is set and a USB interrupt is triggered.

Whenever a USB reset signal is detected, the USB interrupt is triggered and URST\_Flag bit of the USC register is set. When the interrupt has been served, the bit should be cleared by firmware.

The internal timer/event counter interrupt is initialized by setting the timer/event counter interrupt request flag (;bit 6 of the INTC), caused by a timer overflow. When the interrupt is enabled, the stack is not full and the TF is set, a subroutine call to location 0CH will occur. The related interrupt request flag (TF) will be reset and the EMI bit cleared to disable further interrupts.

During the execution of an interrupt subroutine, other interrupt acknowledge signals are held until the "RETI" instruction is executed or the EMI bit and the related interrupt control bit are set to 1 (if the stack is not full). To return from the interrupt subroutine, "RET" or "RETI" may be invoked. RETI will set the EMI bit to enable an interrupt service, but RET will not.

Interrupts, occurring in the interval between the rising edges of two consecutive T2 pulses, will be serviced on the latter of the two T2 pulses, if the corresponding interrupts are enabled. In the case of simultaneous requests the following table shows the priority that is applied. These can be masked by resetting the EMI bit.

| No. | Interrupt Source             | Priority | Vector |
|-----|------------------------------|----------|--------|
| a   | USB interrupt                | 1        | 04H    |
| b   | Timer/Event Counter overflow | 2        | 0CH    |

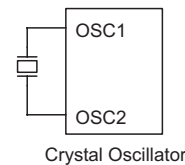
The timer/event counter interrupt request flag (TF), USB interrupt request flag (USBF), enable timer/event counter interrupt bit (ETI), enable USB interrupt bit (EUI) and

enable master interrupt bit (EMI) constitute an interrupt control register (INTC) which is located at 0BH in the data memory. EMI, EUI and ETI are used to control the enabling/disabling of interrupts. These bits prevent the requested interrupt from being serviced. Once the interrupt request flags (TF, USBF) are set, they will remain in the INTC register until the interrupts are serviced or cleared by a software instruction.

It is recommended that a program does not use the "CALL subroutine" within the interrupt subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately in some applications. If only one stack is left and enabling the interrupt is not well controlled, the original control sequence will be damaged once the "CALL" operates in the interrupt subroutine.

**Oscillator Configuration**

There is an oscillator circuit in the microcontroller.



**System Oscillator**

This oscillator is designed for system clocks. The HALT mode stops the system oscillator and ignores an external signal to conserve power.

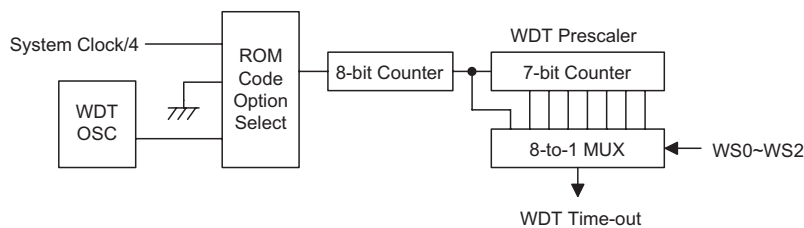
A crystal across OSC1 and OSC2 is needed to provide the feedback and phase shift required for the oscillator. No other external components are required. In stead of a crystal, a resonator can also be connected between OSC1 and OSC2 to get a frequency reference, but two external capacitors in OSC1 and OSC2 are required.

The HT82J97E can operate in 6MHz or 12MHz system clocks. In order to make sure that the USB SIE functions properly, user should correctly configure the SCLKSEL bit of the SCC Register. The default system clock is 12MHz.

The WDT oscillator is a free running on-chip RC oscillator, and no external components are required. Even if the system enters the power down mode, the system clock is stopped, but the WDT oscillator still works within a period of approximately 31µs. The WDT oscillator can be disabled by ROM code option to conserve power.

**Watchdog Timer – WDT**

The WDT clock source is implemented by a dedicated RC oscillator (WDT oscillator), or instruction clock (system clock divided by 4), determine by ROM code option. This timer is designed to prevent a software malfunction or sequence from jumping to an unknown location with unpredictable results. The Watchdog Timer can be disabled by ROM code option. If the Watchdog Timer is dis-



**Watchdog Timer**

abled, all the executions related to the WDT result in no operation.

Once the internal WDT oscillator (RC oscillator with a period of 31µs/5V normally) is selected, it is first divided by 256 (8-stage) to get the nominal time-out period of 8ms/5V. This time-out period may vary with temperatures, VDD and process variations. By invoking the WDT prescaler, longer time-out periods can be realized. Writing data to WS2, WS1, WS0 (bits 2, 1, 0 of the WDTS) can give different time-out periods. If WS2, WS1, and WS0 are all equal to 1, the division ratio is up to 1:128, and the maximum time-out period is 1s/5V. If the WDT oscillator is disabled, the WDT clock may still come from the instruction clock and operates in the same manner except that in the HALT state the WDT may stop counting and lose its protecting purpose. In this situation the logic can only be restarted by external logic. The high nibble and bit 3 of the WDTS are reserved for user defined flags, which can only be set to "10000" (WDTS.7~WDTS.3).

If the device operates in a noisy environment, using the on-chip 32kHz RC oscillator (WDT OSC) is strongly recommended, since the HALT will stop the system clock.

| WS2 | WS1 | WS0 | Division Ratio |
|-----|-----|-----|----------------|
| 0   | 0   | 0   | 1:1            |
| 0   | 0   | 1   | 1:2            |
| 0   | 1   | 0   | 1:4            |
| 0   | 1   | 1   | 1:8            |
| 1   | 0   | 0   | 1:16           |
| 1   | 0   | 1   | 1:32           |
| 1   | 1   | 0   | 1:64           |
| 1   | 1   | 1   | 1:128          |

**WDTS Register**

The WDT overflow under normal operation will initialize a "chip reset" and set the status bit "TO". But in the HALT mode, the overflow will initialize a "warm reset" and only the PC and SP are reset to zero. To clear the contents of the WDT (including the WDT prescaler), three methods are adopted; external reset (a low level to RES), software instruction and a "HALT" instruction. The software instruction include "CLR WDT" and the other set - "CLR WDT1" and "CLR WDT2". Of these two types of instruction, only one can be active depending on the ROM code option - "CLR WDT times selec-

tion option". If the "CLR WDT" is selected (i.e. CLRWDT times is equal to one), any execution of the "CLR WDT" instruction will clear the WDT. In the case that "CLR WDT" and "CLR WDT" are chosen (i.e. CLRWDT times is equal to two), these two instructions must be executed to clear the WDT; otherwise, the WDT may reset the chip as a result of time-out.

**Power Down Operation – HALT**

The HALT mode is initialized by the "HALT" instruction and results in the following:

- The system oscillator will be turned off but the WDT oscillator remains running (if the WDT oscillator is selected).
- The contents of the on-chip RAM and registers remain unchanged.
- The WDT and WDT prescaler will be cleared and recounted again (if the WDT clock is from the WDT oscillator).
- All of the I/O ports remain in their original status.
- The PDF flag is set and the TO flag is cleared.

The system can leave the HALT mode by means of an external reset, an interrupt, an external falling edge signal on port A or a WDT overflow. An external reset causes a device initialization and the WDT overflow performs a "warm reset". After the TO and PDF flags are examined, the cause for chip reset can be determined. The PDF flag is cleared by a system power-up or executing the "CLR WDT" instruction and is set when executing the "HALT" instruction. The TO flag is set if the WDT time-out occurs, and causes a wake-up that only resets the PC and SP; the others remain in their original status.

The port A wake-up and interrupt methods can be considered as a continuation of normal execution. Each bit in port A can be independently selected to wake-up the device by mask option. Awakening from an I/O port stimulus, the program will resume execution of the next instruction. If it awakens from an interrupt, two sequence may occur. If the related interrupt is disabled or the interrupt is enabled but the stack is full, the program will resume execution at the next instruction. If the interrupt is enabled and the stack is not full, the regular interrupt response takes place. If an interrupt request flag is set to "1" before entering the HALT mode, the wake-up function of the related interrupt will be disabled. Once a

wake-up event occurs, it takes  $1024 t_{SYS}$  (system clock period) to resume normal operation. In other words, a dummy period will be inserted after a wake-up. If the wake-up results from an interrupt acknowledge signal, the actual interrupt subroutine execution will be delayed by one or more cycles. If the wake-up results in the next instruction execution, this will be executed immediately after the dummy period is finished.

To minimize power consumption, all the I/O pins should be carefully managed before entering the HALT status.

**Reset**

There are four ways in which a reset can occur:

- $\overline{RES}$  reset during normal operation
- $\overline{RES}$  reset during HALT
- WDT time-out reset during normal operation
- USB reset

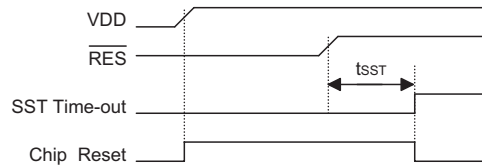
The WDT time-out during HALT is different from other chip reset conditions, since it can perform a "warm re-set" that resets only the PC and SP, leaving the other circuits in their original state. Some registers remain unchanged during other reset conditions. Most registers are reset to the "initial condition" when the reset conditions are met. By examining the PDF and TO flags, the program can distinguish between different "chip resets".

| TO | PDF | RESET Conditions                               |
|----|-----|--|
| 0  | 0   | $\overline{RES}$ reset during power-up         |
| u  | u   | $\overline{RES}$ reset during normal operation |
| 0  | 1   | $\overline{RES}$ wake-up HALT                  |
| 1  | u   | WDT time-out during normal operation           |
| 1  | 1   | WDT wake-up HALT                               |

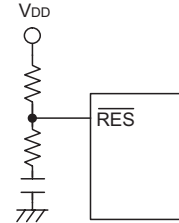
Note: "u" stands for "unchanged"

To guarantee that the system oscillator is started and stabilized, the SST (System Start-up Timer) provides an extra delay of 1024 system clock pulses when the system resets (power-up, WDT time-out or  $\overline{RES}$  reset) or the system awakes from the HALT state.

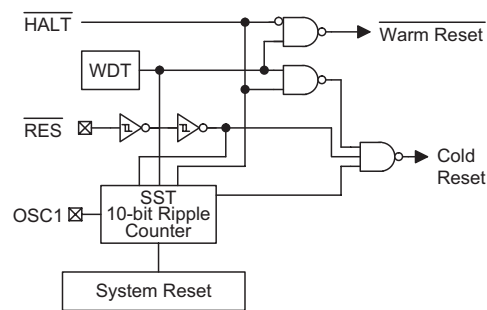
When a system reset occurs, the SST delay is added during the reset period. Any wake-up from HALT will enable the SST delay.



**Reset Timing Chart**



**Reset Circuit**



**Reset Configuration**

The functional unit chip reset status are shown below.

|                     |  |
|---------------------|--|
| PC                  | 000H   |
| Interrupt           | Disable  |
| Prescaler           | Clear  |
| WDT                 | Clear. After master reset, WDT begins counting |
| Timer/event Counter | Off  |
| Input/output Ports  | Input mode                                     |
| Stack Pointer       | Points to the top of the stack                 |

The registers status are summarized in the following table.

| Register        | Reset (Power On) | WDT Time-out (Normal Operation) | RES Reset (Normal Operation) | RES Reset (HALT) | WDT Time-Out (HALT)* | USB-Reset (Normal) | USB-Reset (HALT) |
|-----------------|------------------|---------------------------------|------------------------------|------------------|----------------------|--------------------|------------------|
| TMRH            | xxxx xxxx        | uuuu uuuu                       | uuuu uuuu                    | uuuu uuuu        | uuuu uuuu            | uuuu uuuu          | uuuu uuuu        |
| TMRL            | xxxx xxxx        | uuuu uuuu                       | uuuu uuuu                    | uuuu uuuu        | uuuu uuuu            | uuuu uuuu          | uuuu uuuu        |
| TMRC            | 00-0 1---        | 00-0 1---                       | 00-0 1---                    | 00-0 1---        | uu-u u---            | 00-0 1---          | 00-0 1---        |
| Program Counter | 000H             | 000H                            | 000H                         | 000H             | 000H                 | 000H               | 000H             |
| MP0             | 1xxx xxxx        | 1uuu uuuu                       | 1uuu uuuu                    | 1uuu uuuu        | 1uuu uuuu            | 1uuu uuuu          | 1uuu uuuu        |
| MP1             | 1xxx xxxx        | 1uuu uuuu                       | 1uuu uuuu                    | 1uuu uuuu        | 1uuu uuuu            | 1uuu uuuu          | 1uuu uuuu        |
| ACC             | xxxx xxxx        | uuuu uuuu                       | uuuu uuuu                    | uuuu uuuu        | uuuu uuuu            | uuuu uuuu          | uuuu uuuu        |
| TBLP            | xxxx xxxx        | uuuu uuuu                       | uuuu uuuu                    | uuuu uuuu        | uuuu uuuu            | uuuu uuuu          | uuuu uuuu        |
| TBLH            | -xxx xxxx        | -uuu uuuu                       | -uuu uuuu                    | -uuu uuuu        | -uuu uuuu            | -uuu uuuu          | -uuu uuuu        |
| STATUS          | --00 xxxx        | --1u uuuu                       | --uu uuuu                    | --01 uuuu        | --11 uuuu            | --uu uuuu          | --01 uuuu        |
| INTC            | -000 0000        | -000 0000                       | -000 0000                    | -000 0000        | -uuu uuuu            | -000 0000          | -000 0000        |
| WDTS            | 1000 0111        | 1000 0111                       | 1000 0111                    | 1000 0111        | uuuu uuuu            | 1000 0111          | 1000 0111        |
| PA              | 1111 1111        | 1111 1111                       | 1111 1111                    | 1111 1111        | uuuu uuuu            | 1111 1111          | 1111 1111        |
| PAC             | 1111 1111        | 1111 1111                       | 1111 1111                    | 1111 1111        | uuuu uuuu            | 1111 1111          | 1111 1111        |
| PB              | 1111 1111        | 1111 1111                       | 1111 1111                    | 1111 1111        | uuuu uuuu            | 1111 1111          | 1111 1111        |
| PBC             | 1111 1111        | 1111 1111                       | 1111 1111                    | 1111 1111        | uuuu uuuu            | 1111 1111          | 1111 1111        |
| PC              | 1111 1111        | 1111 1111                       | 1111 1111                    | 1111 1111        | uuuu uuuu            | 1111 1111          | 1111 1111        |
| PCC             | 1111 1111        | 1111 1111                       | 1111 1111                    | 1111 1111        | uuuu uuuu            | 1111 1111          | 1111 1111        |
| PD              | 1111 1111        | 1111 1111                       | 1111 1111                    | 1111 1111        | uuuu uuuu            | 1111 1111          | 1111 1111        |
| AWR             | 0000 0000        | uuuu uuuu                       | 0000 0000                    | 0000 0000        | uuuu uuuu            | 0000 0000          | 0000 0000        |
| PIPE            | 0000 0000        | uuuu uuuu                       | 0000 0000                    | 0000 0000        | uuuu uuuu            | 0000 0000          | 0000 0000        |
| STALL           | 0000 0000        | uuuu uuuu                       | 0000 0000                    | 0000 0000        | uuuu uuuu            | 0000 0000          | 0000 0000        |
| SIES            | 0000 0000        | uuuu uuuu                       | 0000 0000                    | 0000 0000        | uuuu uuuu            | 0000 0000          | 0000 0000        |
| MISC            | 0000 0000        | uuuu uuuu                       | 0000 0000                    | 0000 0000        | uuuu uuuu            | 0000 0000          | 0000 0000        |
| FIFO0           | xxxx xxxx        | uuuu uuuu                       | uuuu uuuu                    | uuuu uuuu        | uuuu uuuu            | 0000 0000          | 0000 0000        |
| FIFO1           | xxxx xxxx        | uuuu uuuu                       | uuuu uuuu                    | uuuu uuuu        | uuuu uuuu            | 0000 0000          | 0000 0000        |
| USC             | 11xx 0000        | uuxx uuuu                       | 11xx 0000                    | 11xx 0000        | uuxx uuuu            | 1100 0u00          | 1100 0u00        |
| USR             | 0100 0000        | uuuu uuuu                       | 0100 0000                    | 0100 0000        | uuuu uuuu            | u1uu 0000          | u1uu 0000        |
| SCC             | 0000 0000        | uuuu uuuu                       | 0000 0000                    | 0000 0000        | uuuu uuuu            | uu00 u000          | uu00 u000        |
| ADSC            | 1000 0000        | uuuu uuuu                       | 1000 0000                    | 1000 0000        | uuuu uuuu            | 1000 0000          | 1000 0000        |
| ADR             | xxxx xxxx        | uuuu uuuu                       | xxxx xxxx                    | xxxx xxxx        | uuuu uuuu            | xxxx xxxx          | xxxx xxxx        |

Note: "\*" stands for "warm reset"  
 "u" stands for "unchanged"  
 "x" stands for "unknown"

**Timer/Event Counter**

A timer/event counter (TMR) is implemented in the microcontroller.

The timer/event counter contains a 16-bit programmable count-up counter and the clock may come from an external source or from the system clock divided by 4.

Using the internal clock source, there is only 1 reference time-base for the timer/event counter. The internal clock source is coming from  $f_{SYS}/4$ . The external clock input allows the user to count external events, measure time intervals or pulse widths.

There are 3 registers related to the timer/event counter; TMRH (0FH), TMRL (10H), TMRC (11H). Writing TMRL will only put the written data to an internal lower-order byte buffer (8 bits) and writing TMRH will transfer the specified data and the contents of the lower-order byte buffer to TMRH and TMRL preload registers, respectively. The timer/event counter preload register is changed by each writing TMRH operations. Reading TMRH will latch the contents of TMRH and TMRL counters to the destination and the lower-order byte buffer, respectively. Reading the TMRL will read the contents of the lower-order byte buffer. The TMRC is the timer/event counter control register, which defines the operating mode, counting enable or disable and active edge.

The TM0, TM1 bits define the operating mode. The event count mode is used to count external events,

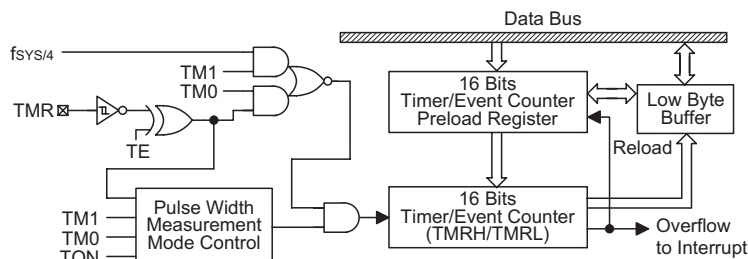
which means that the clock source comes from an external (TMR) pin. The timer mode functions as a normal timer with the clock source coming from the  $f_{SYS}/4$  (Timer). The pulse width measurement mode can be used to count the high or low level duration of the external signal (TMR). The counting is based on the  $f_{SYS}/4$ .

In the event count or timer mode, once the timer/event counter starts counting, it will count from the current contents in the timer/event counter to FFFFH. Once overflow occurs, the counter is reloaded from the timer/event counter preload register and generates the interrupt request flag (TF; bit 6 of the INTC) at the same time.

In the pulse width measurement mode with the TON and TE bits equal to one, once the TMR has received a transient from low to high (or high to low if the TE bit is "0") it will start counting until the TMR returns to the original level and resets the TON. The measured result will remain in the timer/event counter even if the activated transient occurs again. In other words, only one cycle measurement can be done. Until setting the TON, the cycle measurement will function again as long as it receives further transient pulse. Note that, in this operating mode, the timer/event counter starts counting not according to the logic level but according to the transient edges. In the case of counter overflows, the counter is reloaded from the timer/event counter preload register and issues the interrupt request just like the other two modes. To enable the counting operation, the timer ON

| Label (TMRC) | Bits   | Function   |
|--------------|--------|--|
| —            | 0~2    | Unused bit, read as "0"  |
| TE           | 3      | Defines the TMR active edge of the timer/event counter (0=active on low to high; 1=active on high to low)  |
| TON          | 4      | Enable/disable the timer counting (0=disable; 1=enable)  |
| —            | 5      | Unused bit, read as "0"  |
| TM0<br>TM1   | 6<br>7 | Defines the operating mode<br>01=Event count mode (external clock)<br>10=Timer mode (internal clock)<br>11=Pulse width measurement mode<br>00=Unused |

**TMRC Register**



**Timer/Event Counter**

bit (TON; bit 4 of TMRC) should be set to 1. In the pulse width measurement mode, the TON will be cleared automatically after the measurement cycle is completed. But in the other two modes the TON can only be reset by instructions. The overflow of the timer/event counter is one of the wake-up sources. No matter what the operation mode is, writing a 0 to ET can disable the corresponding interrupt services.

In the case of timer/event counter OFF condition, writing data to the timer/event counter preload register will also reload that data to the timer/event counter. But if the timer/event counter is turned on, data written to it will only be kept in the timer/event counter preload register. The timer/event counter will still operate until overflow occurs (a timer/event counter reloading will occur at the same time). When the timer/event counter (reading TMR) is read, the clock will be blocked to avoid errors. As clock blocking may result in a counting error, this must be taken into consideration by the programmer.

**Input/Output Ports**

There are 20 bidirectional input/output lines in the microcontroller, labeled from PA to PC, which are mapped to the data memory of [12H], [14H] and [16H] respectively. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, that is, the inputs must be ready at the T2 rising edge of instruction "MOV A,[m]" (m=12H, 14H or 16H). For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Each I/O line has its own control register (PAC, PBC, PCC) to control the input/output configuration. With this control register, CMOS/NMOS/PMOS output or Schmitt trigger input with or without pull-high/low resistor structures can be reconfigured dynamically under software

control. To function as an input, the corresponding latch of the control register must write a "1". The input source also depends on the control register. If the control register bit is "1", the input will read the pad state. If the control register bit is "0", the contents of the latches will move to the internal bus. The latter is possible in the "read-modify-write" instruction. For output function, CMOS/NMOS/PMOS configurations can be selected (NMOS and PMOS are available for PA only). These control registers are mapped to locations 13H, 15H and 17H.

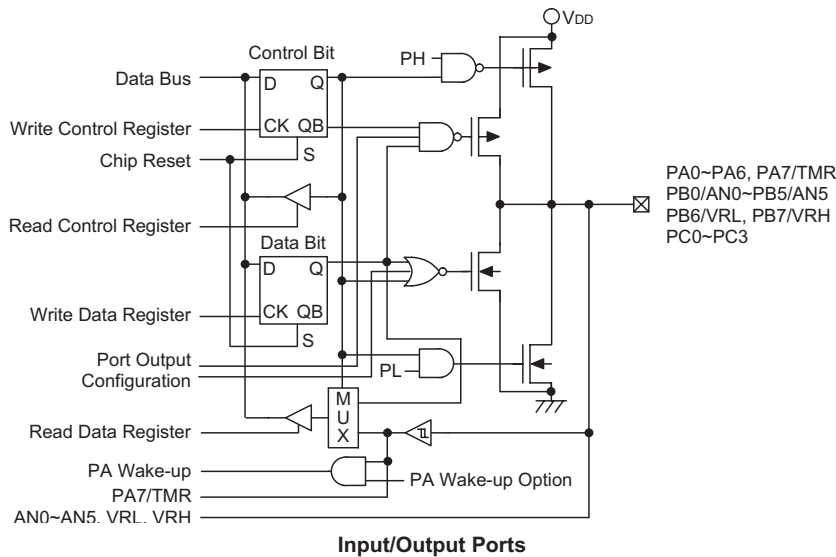
After a chip reset, these input/output lines remain at high levels or in a floating state (depending on the pull-high/low options). Each bit of these input/output latches can be set or cleared by "SET [m].i" and "CLR [m].i" (m=12H, 14H or 16H) instructions.

Some instructions first input data and then follow the output operations. For example, "SET [m].i", "CLR [m].i", "CPL [m]", "CPLA [m]" read the entire port states into the CPU, execute the defined operations (bit-operation), and then write the results back to the latches or the accumulator.

Each line of port A has the capability of waking-up the device.

There are pull-high/low (PA only) options available for I/O lines. Once the pull-high/low option of an I/O line is selected, the I/O line have pull-high/low resistor. Otherwise, the pull-high/low resistor is absent. It should be noted that a non-pull-high/low I/O line operating in input mode will cause a floating state.

It is recommended that unused or not bonded out I/O lines should be set as output pins by software instruction to avoid consuming power under input floating state.



Note: The outputs of PC2 and PC3 will be PWM outputs when PWM outputs are enabled.

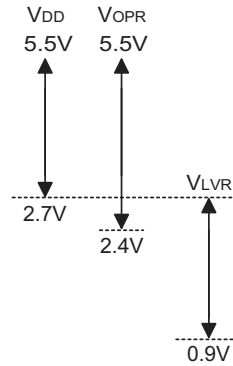
**Low Voltage Reset – LVR**

The microcontroller contains a low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device drops to within the range of  $0.9V \sim V_{LVR}$  such as might occur when changing the battery, the LVR will automatically reset the device internally.

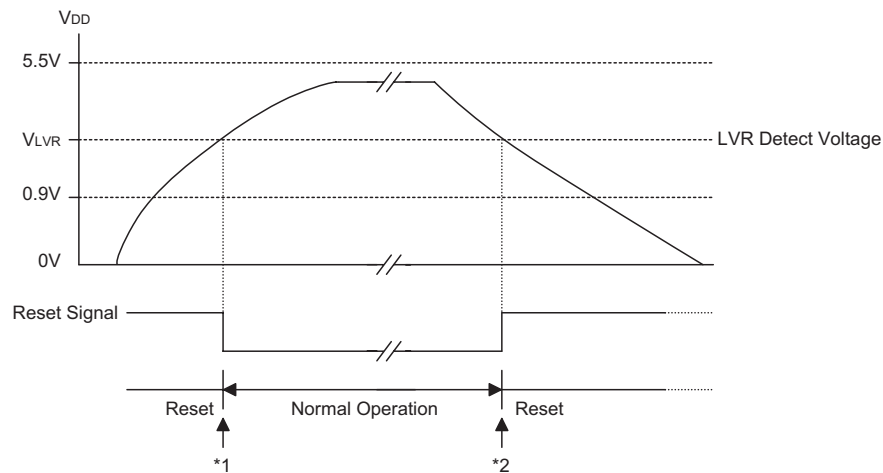
The LVR includes the following specifications:

- For a valid LVR signal, a low voltage ( $0.9V \sim V_{LVR}$ ) must exist for more than 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and will not perform a reset function.
- The LVR uses the "OR" function with the external RES signal to perform a chip reset.

The relationship between  $V_{DD}$  and  $V_{LVR}$  is shown below.



Note:  $V_{OPR}$  is the voltage range for proper chip operation at 6MHz or 12MHz system clock.



**Low Voltage Reset**

Note: \*1: To make sure that the system oscillator has stabilized, the SST provides an extra delay of 1024 system clock pulses before entering the normal operation.

\*2: A low voltage has to exist for more than 1ms, after that 1ms delay, the device enters a reset mode.

## USB with MCU Interface

There are eight registers, including Pipe\_ctrl, Address+Remote\_WakeUp, Stall, Pipe, SIES, Misc, FIFO 0 and FIFO 1 in this buffer function.

| Register Name  | Pipe_ctrl                     | Addr.+Remote | Stall | Pipe | SIES | Misc | FIFO 0 | FIFO 1 |
|----------------|-------------------------------|--------------|-------|------|------|------|--------|--------|
| Mem. Addr.     | 41H                           | 42H          | 43H   | 44H  | 45H  | 46H  | 48H    | 49H    |
| Reserved Addr. | Bank 1, Address 40H, 4AH, 4FH |              |       |      |      |      |        |        |

### Register Memory Mapping

Address+Remote\_WakeUp register represents current address and remote wake-up function. The initial value is "00000000" from MSB to LSB.

| Register Address | R/W | Bit 7                                   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0   |
|------------------|-----|---|-------|-------|-------|-------|-------|-------|---|
| 01000010B        | R/W | Address value<br>Default value=00000000 |       |       |       |       |       |       | Remote Wake-up Function<br>0: Not this function<br>1: The function exists |

### Address+Remote\_WakeUp Register

The PIPE\_ctrl, STALL and PIPE are bitmap ones. The Pipe\_ctrl Register is used for configuring IN (Bit=1) or OUT (Bit=0) Pipe. The default is defined as IN Pipe. The Pipe register represents whether the corresponding endpoint is accessed by host or not. After a USB interrupt signal is being sent out, the MCU can check which endpoint had been accessed. This register is set only after the host accessed the corresponding endpoint. The Stall register shows whether the corresponding endpoint works or not. As soon as the endpoint works improperly, the corresponding bit must be set. The bitmaps are listed as follows:

| Register Name | R/W | Register Address | Bit7~Bit2 Reserved | Bit 1  | Bit 0  | Default Value |
|---------------|-----|------------------|--------------------|--------|--------|---------------|
| Pipe_ctrl     | R/W | 01000001B        | —                  | Pipe 1 | Pipe 0 | 00000011      |
| Stall         | R/W | 01000011B        | —                  | Pipe 1 | Pipe 0 | 00000000      |
| Pipe          | R   | 01000100B        | —                  | Pipe 1 | Pipe 0 | 00000000      |

### Stall and Pipe Registers

The SIES Register is used to indicate the present signal state which the USB SIE received and also determines whether the USB SIE has to change the device address automatically.

| Bit No. | Function | Read/Write | Register Address |
|---------|----------|------------|------------------|
| 7       | MNI      | R/W        | 01000101B        |
| 6       | EOT      | R          |                  |
| 5       | CRC_ERR  | R/W        |                  |
| 4       | NAK      | R          |                  |
| 3       | IN       | R          |                  |
| 2       | OUT      | R/W        |                  |
| 1       | F0_ERR   | R/W        |                  |
| 0       | Adr_set  | R/W        |                  |

### SIES Registers Table



| Function Name | Read/Write | Description  |
|---------------|------------|--|
| Adr_set       | R/W        | This bit is used to configure the USB SIE to automatically change the device address with the value of the Address+Remote_WakeUp Register (42H).<br>When this bit is set to 1 by F/W, the USB SIE will update the device address with the value of the Address+Remote_WakeUp Register (42H) after the PC Host has successfully read the data from the device by the IN operation. The USB SIE will clear the bit after updating the device address.<br>Otherwise, when this bit is cleared to 0, the USB SIE will update the device address immediately after an address is written to the Address+Remote_WakeUp Register (42H). |
| F0_Err        | R/W        | This bit is used to indicate when there are some errors that occurred when the FIFO0 is accessed.<br>This bit is set by the USB SIE and cleared by F/W.  |
| Out           | R/W        | This bit is used to indicate that there are OUT token (except for the OUT zero) that has been received. The F/W clears the bit after the OUT data has been read. Also, this bit will be cleared by the USB SIE after the next valid SETUP token is received.   |
| IN            | R          | This bit is used to indicate that the current USB receiving signal from the PC Host is IN token.   |
| NAK           | R          | This bit is used to indicate that the USB SIE has transmitted the NAK signal to the Host in response to the PC Host IN or OUT token.   |
| CRC_err       | R/W        | This bit indicates that there are CRC error (bit=1). The programmer must do something to save the device and keep it alive.<br>This bit is set by the USB SIE and cleared by F/W.  |
| EOT           | R          | End of transient flag, normal status is 1. If suspend="1" line & EOT="0" indicates that something is wrong in the USB Interface. The programmer must do something to save the device and keep it alive.  |
| MNI           | R/W        | This bit is for masking the NAK interrupt when MNI="1", the default value="0"  |

**SIES Function Table**

The Misc register is actually a command + status to control the desired FIFO action and to show the status of the desired FIFO. Every bit's meaning and usage are listed as follows:

| Bit No. | Function  | Read/Write | Register Address |
|---------|-----------|------------|------------------|
| 7       | Len0      | R/W        | 01000110B        |
| 6       | Ready     | R          |                  |
| 5       | Set CMD   | R/W        |                  |
| 4       | Sel_pipe1 | R/W        |                  |
| 3       | Sel_pipe0 | R/W        |                  |
| 2       | Clear     | R/W        |                  |
| 1       | Tx        | R/W        |                  |
| 0       | Request   | R/W        |                  |

**Misc Registers Table**

| Function Name          | Read/Write | Description  |
|------------------------|------------|--|
| Request                | R/W        | After setting the other desired status, FIFO can be requested by setting this bit high active. After work has been done, this bit must be set low.   |
| Tx                     | R/W        | Represents the direction and transition end of the MCU accesses. When being set as logic 1, the MCU wants to write data to FIFO. After work has been done, this bit must be set to logic 0 before terminating the request to represent a transition end. For reading action, this bit must be set to logic 0 to indicate that the MCU wants to read and must be set to logic 1 after work is done. |
| Clear                  | R/W        | Represents MCU clear requested FIFO, even if FIFO is not ready.  |
| Sel_pipe1<br>Sel_pipe0 | R/W        | Determines which FIFO is desired, "00" for FIFO 0, "01" for FIFO 1   |
| Set CMD                | R/W        | Shows that the data in FIFO is setup as command. This bit will be cleared by firmware. So, even if the MCU is busy, nothing is missed by the SETUP command from the host.  |
| Ready                  | R          | Indicates that the desired FIFO is ready to work.  |
| Len0                   | R/W        | Indicates that the host sent a 0-sized packet to the MCU. This bit must be cleared by a read action to the corresponding FIFO. Also, this bit will be cleared by the USB SIE after the next valid SETUP token is received.   |

**Misc Function Table**

The HT82J97E has two 8x8 bidirectional FIFO for the two endpoints (control and Interrupt). User can easily read/write the FIFO data by accessing the corresponding FIFO pointer register (FIFO0, FIFO1). The following are two examples for reading and writing the FIFO data:

HT82J97E FIFO is read by packet. To read from FIFO, the following should be followed:

- Select one set of FIFO, set in the read mode (MISC TX bit = 0), and set the REQ bit to "1".
- Check the ready bit until the status = 1
- Read through the FIFO pointer register, and record the data number that has been read.
- Repeat steps 2 and 3 until the ready bit becomes 0 which indicates the end of the FIFO data reading.
- Set MISC TX bit = 1
- Clear the REQ bit to 0. Complete reading.

User reads the data through the FIFO pointer register, user has to record the number of bytes to be read. The

HT82J97E allows a maximum of 8 bytes of data in each packet.

The HT82J97E FIFO is written by packet. To write to FIFO, the following should be followed:

- Select a set of FIFO, set in the write mode (MISC TX bit = 1), and set the REQ bit to "1"
- Check the ready bit until the status = 1
- Write through the FIFO pointer register and take down the data number that has been written
- Repeat steps 2 and 3 until writing is complete or the ready bit becomes 0 which indicates that the FIFO no longer allows any data writing.
- Set MISC TX bit = 0
- Clear the REQ bit to 0. Complete writing.

User writes the data through the FIFO pointer register, user has to record the number of bytes that have been written. The HT82J97E allows a maximum of 8 bytes of data in each packet.

There are some timing constrains and usages illustrated here. By setting the MISC register, the MCU can perform reading, writing and clearing actions. There are some examples shown in the following table for endpoint FIFO reading, writing and clearing.

| Actions                                      | MISC Setting Flow and Status   |
|--|--|
| Read FIFO0 sequence                          | 00H→01H→delay of 2μs, check 41H→read* from FIFO0 register and check if not ready (01H)→03H→02H |
| Write FIFO1 sequence                         | 0AH→0BH→delay of 2μs, check 4BH→write* to FIFO1 register and check if not ready (0BH)→09H→08H  |
| Check whether FIFO0 can be read or not       | 00H→01H→delay of 2μs, check 41H (if ready) or 01H (if not ready)→00H                           |
| Check whether FIFO1 can be written to or not | 0AH→0BH→delay of 2μs, check 4BH (if ready) or 0BH (if not ready)→0AH                           |
| Write 0-sized packet sequence to FIFO 0      | 02H→03H→delay of 2μs, check 43H→01H→00H  |

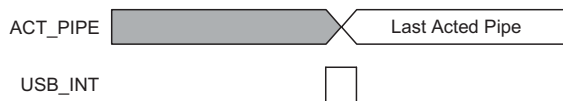
Note: \*: There are 2μs gap existing between 2 reading actions or between 2 writing actions

| Register Name | R/W | Register Address | Bit7~Bit0   |
|---------------|-----|------------------|-------------|
| FIFO 0        | R/W | 01001000B        | Data7~Data0 |
| FIFO 1        | R/W | 01001001B        | Data7~Data0 |

**FIFO Register Address Table**

**USB Active Pipe Timing**

The USB active pipe accessed by the host cannot be used by the MCU simultaneously. When the host finishes its work, the signal, a USB\_INT will be produced to tell the MCU that the pipe can be used and the acted pipe No. will be shown in the signal, ACT\_PIPE as well. The timing is illustrated in the Figure below.



**USB Active Pipe Timing**

**Suspend Wake-Up and Remote Wake-Up**

If there is no signal on the USB bus for over 3ms, the HT82J97E will go into a suspend mode. The Suspend line (bit 0 of the USC) will be set to 1 and a USB interrupt is triggered to indicate that the HT82J97E should jump to the suspend state to meet the 500μA USB suspend current spec.

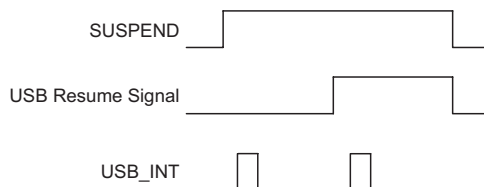
In order to meet the 500μA suspend current, the programmer should disable the USB clock by clearing the USBCKEN (bit3 of the SCC) to "0". The suspend current is 400μA.

The user can also further decrease the suspend current to 250μA by setting the SUSP2 (bit4 of the SCC). But if the SUSP2 is set, the user has to make sure not to enable the LVR OPT option, otherwise the HT82J97E will be reset.

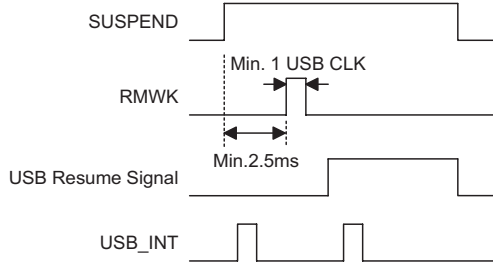
When the resume signal is sent out by the host, the HT82J97E will wake-up the MCU by USB interrupt and

the Resume line (bit 3 of the USC) is set. In order to make the HT82J97E function properly, the programmer must set the USBCKEN (bit 3 of the SCC) to 1 and clear the SUSP2 (bit4 of the SCC). Since the Resume signal will be cleared before the Idle signal is sent out by the host and the Suspend line (bit 0 of the USC) is going to "0". So when the MCU is detecting the Suspend line (bit0 of the USC), the Resume line should be remembered and taken into consideration.

After finishing the resume signal, the suspend line will go inactive and a USB interrupt is triggered. The following is the timing diagram:



The device with remote wake-up function can wake-up the USB Host by sending a wake-up pulse through RMWK (bit 1 of USC). Once the USB Host receive the wake-up signal from the HT82J97E, it will send a Resume signal to the device. The timing is as follows:



**To Configure the HT82J97E as PS2 Device**

The HT82J97E can be defined as a USB interface or a PS2 interface by configuring the SPS2 (bit 4 of the USR) and SUSB (bit 5 of the USR). If SPS2=1, and SUSB=0, the HT82J97E is defined as PS2 interface, pin USBD- is now defined as PS2 Data pin and USBD+ is now defined as PS2 Clk pin. The user can easily read or write to the PS2 Data or PS2 Clk pin by accessing the corresponding bit PS2DAI (bit 4 of the USC), PS2CKI (bit 5 of the USC), PS2DAO (bit 6 of the USC) and S2CKO (bit 7 of the USC) respectively.

The user should make sure that in order to read the data properly, the corresponding output bit must be set to "1". For example, if user wants to read the PS2 Data by reading PS2DAI, the PS2DAO should be set to "1". Otherwise it always read a "0".

If SPS2=0, and SUSB=1, the HT82J97E is defined as a USB interface. Both the USBD- and USBD+ are driven by the USB SIE of the HT82J97E. User only writes or reads the USB data through the corresponding FIFO.

Both SPS2 and SUSB default is "0".

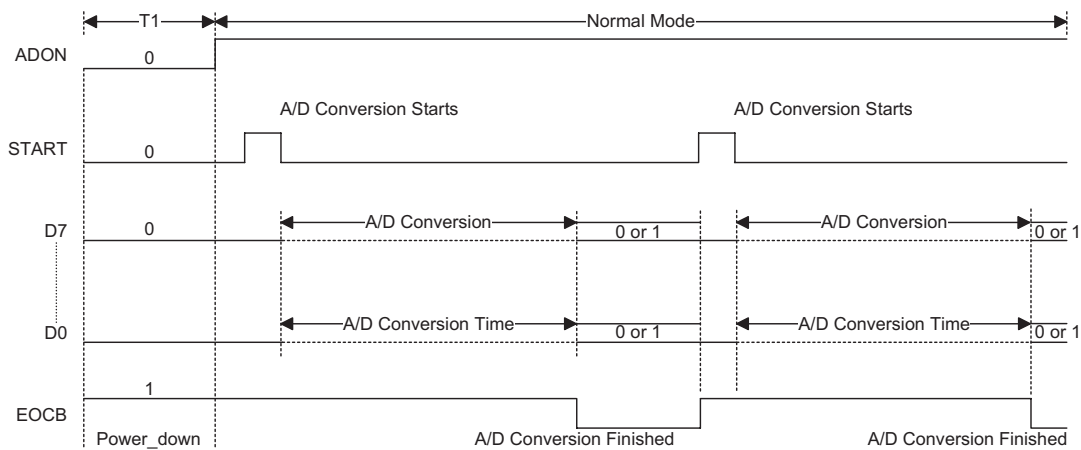
**To Configure the ADC Block**

The HT82J97E has built-in an 8-bit A/D converter with 6 channels (PB0~PB5). In order to make the A/D converter more flexible, there are two modes: External Reference voltage and Internal Reference voltage. It can be easily configured by setting the ADREF (bit 6 of the USR). For External Reference voltage, the reference voltage of the A/D converter comes from an external PB6/VRL and PB7/VRH pins. Otherwise, the reference voltage is coming from the VDD and VSS of the MCU.

PB0~PB5 is the 6-channel input of the A/D converter, it is easy to define which channel is converting by configuring ACS2~ACS0 (bit 2~0 of the ADSC). Also there are four converter clock sources to be selected by setting ADCS1 (bit 4 of the ADSC), ADCS0 (bit 3 of the ADSC).

Once the ADON (bit 6 of the ADSC) is set, it sends the start pulse through START (bit 5 of ADSC). The A/D converter will be in operation. There are EOCB (bit 7 of the ADSC) to indicate whether the A/D converter is busy or not. The EOCB is cleared when the conversion is completed. User can read the converter data by reading the register ADR. In order to meet 500µA suspend current spec., user should disable the A/D by clearing ADON before jumping to suspend mode.

The following is an A/D converter timing diagram:



**To Configure PWM Block**

The HT82J97E has two PWM outputs (PWM1 and PWM2), which are shared with PC2, PC3 and can be easily enabled or disabled by the PWM1\_EN or PWM2\_EN bit of PORT\_PC (16H) respectively.

Also there is a one 8-bit PWMBR (PWM Base Period Register, 18H) which defines both PWM output waveform cycle period.

PWM cycle period =  $256 \times 1/f_{SYS} \times (PWMBR+1)$ , or  $256 \times 4/f_{SYS} \times (PWMBR+1)$

where  $1/f_{SYS}$  or  $4/f_{SYS}$  is defined by PWM\_S bit of the PORT\_PC (16H)

For example if PWMBR = 17,  $4/f_{SYS}$  (T1) is selected and  $f_{SYS} = 6\text{MHz}$ .

So both output waveform cycle period is  $256 \times 4/6 \times (17+1) = \text{about } 3072\mu\text{s}$  (0.325kHz)

Now user can easily define the corresponding PWM duty by configuring the PWM1DR (for PWM1) or PWM2DR (for PWM2) duty registers

PWM1 duty (high pulse) =  $(PWM1DR+1)/256 \times 100\%$

PWM1 high pulse period = PWM1 duty  $\times$  PWM cycle period

PWM1 Low pulse period = PWM cycle period - high pulse period

PWM2 duty (high pulse) =  $(PWM2DR+1)/256 \times 100\%$

PWM2 high pulse period = PWM2 duty  $\times$  PWM cycle period

PWM2 Low pulse period = PWM cycle period - high pulse period

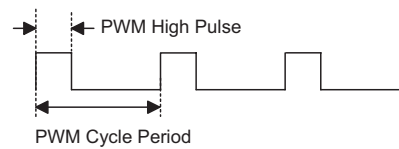
For example PWMBR=17, PWM1DR=63,  $4/f_{SYS}$  (T1) is selected and  $f_{SYS}=6\text{MHz}$

PWM cycle period =  $256 \times 4/6 \times (17+1) = \text{about } 3072\mu\text{s}$  (0.325kHz)

PWM1 duty =  $(63+1)/256 = 25\%$

PWM1 high pulse period =  $25\% \times 3072\mu\text{s} = 768\mu\text{s}$

PWM1 low pulse period =  $3072\mu\text{s} - 768\mu\text{s} = 2304\mu\text{s}$



**I/O Port Special Registers Definition**

- Port-A (12H) – PA

| Register | Bits | Labels | Read/Write | Option | Functions   |
|----------|------|--------|------------|--------|---|
| PA (12H) | 0    | PA0    | R/W        | —      | I/O (R/W) has pull-low and pull-high ROM code option. Has falling edge wake-up ROM code option.   |
|          | 1    | PA1    | R/W        | —      | I/O (R/W) has pull-low and pull-high option. Has falling edge wake-up option.                     |
|          | 2    | PA2    | R/W        | —      | I/O (R/W) has pull-low and pull-high option. Has falling edge and rising edge wake-up option.     |
|          | 3    | PA3    | R/W        | —      | I/O (R/W) has pull-low and pull-high option. Has falling edge and rising edge wake-up option.     |
|          | 4    | PA4    | R/W        | —      | I/O (R/W) has pull-high option. Has falling edge wake-up option.                                  |
|          | 5    | PA5    | R/W        | —      | I/O (R/W) has pull-high option. Has falling edge wake-up option.                                  |
|          | 6    | PA6    | R/W        | —      | I/O (R/W) has pull-high option. Has falling edge wake-up option.                                  |
|          | 7    | PA7    | R/W        | —      | I/O (R/W) has pull-high option. Has falling edge wake-up option, pin-shared with timer input pin. |

- Port-A Control (13H) – PAC

This port configure the input or output mode of Port-A

- Port-B Control (14H) – PB

| Register    | Bits | Labels | Read/Write | Option | Functions  |
|-------------|------|--------|------------|--------|--|
| PB<br>(14H) | 0    | PB0    | R/W        | —      | I/O (R/W), has pull-high option, ADC input.  |
|             | 1    | PB1    | R/W        | —      | I/O (R/W), has pull-high option, ADC input.  |
|             | 2    | PB2    | R/W        | —      | I/O (R/W), has pull-low and pull-high option, ADC input.   |
|             | 3    | PB3    | R/W        | —      | I/O (R/W), has pull-low and pull-high option, ADC input.   |
|             | 4    | PB4    | R/W        | —      | I/O (R/W), has pull-high option, can wake-up, ADC input.   |
|             | 5    | PB5    | R/W        | —      | I/O (R/W), has pull-high option, ADC input.  |
|             | 6    | PB6    | R/W        | —      | I/O (R/W), has pull-high option, ADC input, VRL input for ADC external mode.                         |
|             | 7    | PB7    | R/W        | —      | I/O (R/W), has pull-high option, ADC input, VRH input for ADC external mode, has wake-up capability. |

- Port-B Control (15H) – PBC

This port configures the input or output mode of Port-B for I/O mode

- Port-C Control (16H) – PC

| Register    | Bits | Labels | Read/Write | Option  | Functions   |
|-------------|------|--------|------------|---------|---|
| PC<br>(16H) | 0    | PC0    | R/W        | —       | I/O (R/W), has pull-high option   |
|             | 1    | PC1    | R/W        | —       | I/O (R/W), has pull-high option   |
|             | 2    | PC2    | R/W        | —       | I/O (R/W), has pull-high option, can be used as PWM1 output                         |
|             | 3    | PC3    | R/W        | —       | I/O (R/W), has pull-high option, can be used as PWM2 output                         |
|             | 4    | PC4    | —          | —       | Reserved bit  |
|             | 5    | PC5    | R/W        | PWM_S   | PWM base period register frequency source<br>0= T1 (default)<br>1= f <sub>sys</sub> |
|             | 6    | PC6    | R/W        | PWM1_EN | 1: Internal register bit, enable PWM1 output<br>0: Disable (default)                |
|             | 7    | PC7    | R/W        | PWM2_EN | 1: Internal register bit, enable output<br>0: Disable (default)                     |

- Port-C Control (17H) – PCC

This port is used to control whether the Port-C pin is input or output pin except PC4~PC7

**USB/PS2 Status and Control Register USC (Address 0X1A)**

| Register      | Bits | Labels | Read/Write | Option    | Functions  |
|---------------|------|--------|------------|-----------|--|
| USC<br>(0X1A) | 0    | PE0    | R          | SUSPEND   | USB suspend mode status bit. When 1, indicates that the USB system entry is in suspend mode.     |
|               | 1    | PE1    | W          | RMOT_WK   | USB remote wake-up signal. Default value is 0.   |
|               | 2    | PE2    | R/W        | URST_FLAG | USB bus reset event flag. Default value is 0.  |
|               | 3    | PE3    | R          | RESUME_O  | When RESUME_OUT EVENT, RESUME_O is set to 1. Default value is 0.                                 |
|               | 4    | PE4    | R          | PS2_DAI   | USBD-/DATA input   |
|               | 5    | PE5    | R          | PS2_CKI   | USBD+/CLK input  |
|               | 6    | PE6    | W          | PS2_DAO   | Output for driving USBD-/DATA pin, when working under 3D PS2 mouse function. Default value is 1. |
|               | 7    | PE7    | W          | PS2_CKO   | Output for driving USBD-/DATA pin, when working under 3D PS2 mouse function. Default value is 1. |

**Endpoint Interrupt Status Register USR (Address 0X1B)**

The USR (USB endpoint interrupt status register) register is used to indicate which endpoint is accessed and to select the serial bus (PS2 or USB) and A/D converter operation modes. The endpoint request flags (EP0IF, EP1IF) are used to indicate which endpoints are accessed. If an endpoint is accessed, the related endpoint request flag will be set to "1" and a USB interrupt will occur (If a USB interrupt is enabled and the stack is not full). When the active endpoint request flag is served, the endpoint request flag has to be cleared to "0".

| Register      | Bits | Labels | Read/Write | Option   | Functions   |
|---------------|------|--------|------------|----------|---|
| USR<br>(0X1B) | 0    | PEC0   | R/W        | EP0IF    | When set to "1", indicates an endpoint 0 interrupt event. Must wait for the MCU to process the interrupt event and clear this bit by firmware. This bit must be "0", then the next interrupt event will be processed. Default value is "0".   |
|               | 1    | PEC1   | R/W        | EP1IF    | When set to "1", indicates an endpoint 1 interrupt event. Must wait for the MCU to process the interrupt event, then clear this bit by firmware. This bit must be "0", then the next interrupt event will be processed. Default value is "0". |
|               | 2    | PEC2   | R/W        | —        | Reserved bit, set to "0"  |
|               | 3    | PEC3   | R/W        | —        | Reserved bit, set to "0"  |
|               | 4    | PEC4   | R/W        | SELPS2   | When set to "1", indicates that the chip is working under PS2 mode. Default value is "0".   |
|               | 5    | PEC5   | R/W        | SELUSB   | When set to "1", indicates that the chip is working under USB mode. Default value is 0.   |
|               | 6    | PEC6   | R/W        | VRSEL    | When set to "0", indicates the reference voltage of the 8-bit ADC from the external input pin. When set to "1", indicates that the reference voltage is from the internal power line. Default value is "1".                                   |
|               | 7    | PEC7   | R/W        | USB_flag | This flag is used to show that the MCU is in USB mode (Bit=1). This bit is R/W by FW and will be cleared to zero after power-on reset. The default is "0".  |

**Clock Control Register SCC (Address 0X1C)**

There is a system clock control register implemented to select the clock used in the MCU. This register consists of USB clock control bit (USBCKEN), second suspend mode control bit (SUSPEND2) and system clock selection (SCLKSEL).

| Register      | Bits | Labels  | Read/Write | Option   | Functions  |
|---------------|------|---------|------------|----------|--|
| SCC<br>(0X1C) | 2~0  | PF2~PF0 | R/W        | —        | Reserved   |
|               | 3    | PF3     | R/W        | USBCKEN  | USB clock control bit. When set to "1", indicates a USBCK ON, else USBCK OFF. Default value is "0".  |
|               | 4    | PF4     | R/W        | SUSPEND2 | When set to "1", enables a 7.5kΩ resistor connected to D-pin to 5V VDD. Default value is "0".  |
|               | 5    | PF5     | R/W        | —        | Reserved   |
|               | 6    | PF6     | R/W        | SCLKSEL  | System clock 6MHz or 12MHz option, when working on external oscillator mode. Default value is "0".<br>0: Operating at external 12MHz mode<br>1: Operating at external 6MHz mode<br>Default value is "0". |
|               | 7    | PF7     | R/W        | PS2_flag | This flag is used to show that the MCU is in PS2 mode (Bit=1). This bit is R/W by FW and will be cleared to zero after power-on reset. The default is "0".   |

**ADC Status and Control Register ADC (Address 0X1D)**

The A/D converter implemented in the MCU is a 6-channel 8-bit A/D converter. The reference voltage (high reference voltage and low reference voltage) can be selected as coming from external pins (PB6/VRL and PB7/VRH) or internal power supplies of the MCU (VDD and VSS). The VRL and VRH are used to set the minimal and maximal boundaries of the full-scale range of the A/D converter. If an analog input, VRL or VRH is not used for A/D conversion, it can also be used as a general purpose I/O line. The ADSC (A/D converter status and control register) register is used to set the configurations and A/D clock sources of the A/D converter and controls the operation of the A/D converter.

| Register      | Bits | Labels    | Read/Write | Option  | Functions  |
|---------------|------|-----------|------------|---------|--|
| ADC<br>(0X1D) | 2~0  | PFC2~PFC0 | R/W        | SEL_CH  | These four bits selects one of the eight ADC channels for conversion. Channels 0 to 5 correspond to inputs AD0~AD5 on port pins PB0~PB5 respectively. Channels 6 and 7 are the ADC reference inputs VRH and VRL, on port pins PB6 and PB7 respectively.<br>000: AD0 (PB0); 001: AD1 (PB1)<br>010: AD2 (PB2); 011: AD3 (PB3)<br>100: AD4 (PB4); 101: AD5 (PB5)<br>110: AD6 or VRL (PB6); 111: AD7 or VRH (PB7)<br>Default value is 000'B. |
|               | 4~3  | PFC4~PFC3 | R/W        | SEL_CLK | Selecting ADC operating clock.<br>00: 6MHz (Default clock)<br>01: 3MHz<br>10: 1.5MHz<br>11: 0.75MHz  |
|               | 5    | PFC5      | R/W        | START   | Start of ADC conversion. High active. Default value is "0"   |
|               | 6    | PFC6      | R/W        | ADON    | Enable pin. ADON=1, Enable ADC block. Default value is "0".  |
|               | 7    | PFC7      | R/W        | EOCB    | End of conversion. This read-only status bit is cleared when a conversion is completed, indicating that the ADC Data Register contains a valid result.   |



**ADC High-byte Data Register ADCR (Address 0X1E)**

| Register    | Bits | Labels  | Read/Write | Option | Functions  |
|-------------|------|---------|------------|--------|--|
| ADCR (0X1E) | 7~0  | PG7~PG0 | R          | ADCDR  | The ADCDR stores the result of a valid ADC conversion bit7~bit0. |

**Table High Byte Pointer for Current Table Read TBHP (Address 0X1F)**

| Register    | Bits | Labels   | Read/Write | Option | Functions                                |
|-------------|------|----------|------------|--------|--|
| TBHP (0X1F) | 2~0  | PGC2~PG0 | R          | —      | Store current table read bit10~bit8 data |

**PWM Base Period Register PWMBR (Address 0X18)**

This register is used to define the base period of the PWM cycle period. The period is defined according to the following equation:

$$\text{Base period} = (4/f_{\text{SYS}}) \times (\text{PWMBR} + 1) \text{ or } (1/f_{\text{SYS}}) \times (\text{PWMBR} + 1)$$

Where  $4/f_{\text{SYS}}$  or  $1/f_{\text{SYS}}$  is defined by PWM\_S bit of PORT\_PC

Where PWMBR = 1~255, PWMBR=0 is not available

$$\text{PWM cycle period} = 256 \times \text{Base period}$$

Base period equals to 1/256 duty cycle.

| Register     | Bits | Labels  | Read/Write | Option | Functions   |
|--------------|------|---------|------------|--------|---|
| PWMBR (0X18) | 7~0  | PD7~PD0 | R          | —      | Used to define the base period of the PWM<br>Range = 2~256×Base Period<br>Where PWMBR=1~255, PWMBR=0 is not available |

**PWM Duty Register PWM1DR (Address 0XCH) and PWM2DR (Address 0XDH)**

This register is used to define the duty of the PWM1 output (PC2) or PWM2 output (PC3) respectively. Both PWM cycle frequency is defined according to the following equation:

| Register                       | Bits | Read/Write | Option | Functions                   |
|--------------------------------|------|------------|--------|-----------------------------|
| PWM1DR (0XCH)<br>PWM2DR (0XDH) | 7~0  | R/W        | —      | Used to define the PWM duty |

$$\text{PWM1 duty} = (\text{PWM1DR} + 1) / \text{PWM cycle} \times 100\% \text{ period}$$

Where PWM1DR= 0~255

If the PWM function is enabled by setting the corresponding bit (PWM1\_EN or PWM2\_EN of Port C), the PWM output (PC2 or PC3) pins always output the PWM signal whether the corresponding control register bit (PCC2 or PCC3) is defined as in input or output mode.

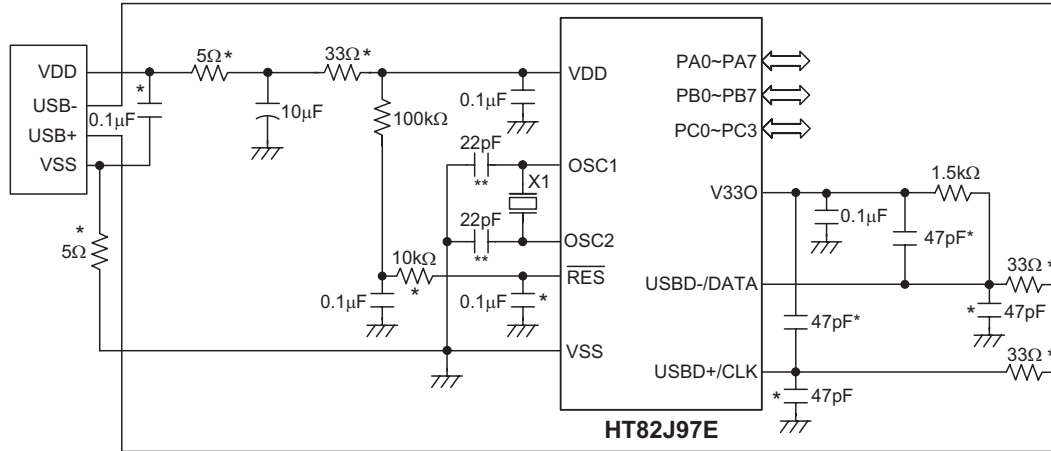
**OTP Options**

| No. | Option  |
|-----|---|
| 1   | WDT clock source: RC (system/4) (default: T1)   |
| 2   | WDT clock source: enable/disable for normal mode (default: disable)                                       |
| 3   | PA0~PA7, PB4, PB7 wake-up by bit (PA2, PA3 both wake-up by falling or rising edge) (default: non wake-up) |
| 4   | PA0~PA7 pull-high by bit (default: Pull-high)   |
| 5   | PC0~3, PB pull-high by nibble (default: Pull-high)  |
| 6   | 2.7 V (error 0.3V) LVR enable/disable (default: enable)   |
| 7   | PA0~PA3, PB2, PB3 Pull-low by bit (default: non pull-low 30kΩ)  |
| 8   | "CLR WDT", 1 or 2 instructions  |
| 9   | TBHP enable/disable (default: disable)  |
| 10  | PA output mode (CMOS/NMOS/PMOS) by bit (default: CMOS)  |

The LVR voltage is define as 2.7V±0.3V and default is enable.

**Application Circuits**

**Crystal or Ceramic Resonator for Multiple I/O Applications**



Note: The resistance and capacitance for the reset circuit should be designed in such a way as to ensure that the VDD is stable and remains within a valid operating voltage range before bringing RES to high.

X1 can use 6MHz or 12MHz, X1 as close OSC1 & OSC2 as possible

Components with \* are used for EMC issue.

Components with \*\* are used for resonator only.

**Instruction Set Summary**

| Mnemonic                         | Description  | Instruction Cycle | Flag Affected |
|----------------------------------|--|-------------------|---------------|
| <b>Arithmetic</b>                |  |                   |               |
| ADD A,[m]                        | Add data memory to ACC   | 1                 | Z,C,AC,OV     |
| ADDM A,[m]                       | Add ACC to data memory   | 1 <sup>(1)</sup>  | Z,C,AC,OV     |
| ADD A,x                          | Add immediate data to ACC  | 1                 | Z,C,AC,OV     |
| ADC A,[m]                        | Add data memory to ACC with carry                                  | 1                 | Z,C,AC,OV     |
| ADCM A,[m]                       | Add ACC to data memory with carry                                  | 1 <sup>(1)</sup>  | Z,C,AC,OV     |
| SUB A,x                          | Subtract immediate data from ACC                                   | 1                 | Z,C,AC,OV     |
| SUB A,[m]                        | Subtract data memory from ACC                                      | 1                 | Z,C,AC,OV     |
| SUBM A,[m]                       | Subtract data memory from ACC with result in data memory           | 1 <sup>(1)</sup>  | Z,C,AC,OV     |
| SBC A,[m]                        | Subtract data memory from ACC with carry                           | 1                 | Z,C,AC,OV     |
| SBCM A,[m]                       | Subtract data memory from ACC with carry and result in data memory | 1 <sup>(1)</sup>  | Z,C,AC,OV     |
| DAA [m]                          | Decimal adjust ACC for addition with result in data memory         | 1 <sup>(1)</sup>  | C             |
| <b>Logic Operation</b>           |  |                   |               |
| AND A,[m]                        | AND data memory to ACC   | 1                 | Z             |
| OR A,[m]                         | OR data memory to ACC  | 1                 | Z             |
| XOR A,[m]                        | Exclusive-OR data memory to ACC                                    | 1                 | Z             |
| ANDM A,[m]                       | AND ACC to data memory   | 1 <sup>(1)</sup>  | Z             |
| ORM A,[m]                        | OR ACC to data memory  | 1 <sup>(1)</sup>  | Z             |
| XORM A,[m]                       | Exclusive-OR ACC to data memory                                    | 1 <sup>(1)</sup>  | Z             |
| AND A,x                          | AND immediate data to ACC  | 1                 | Z             |
| OR A,x                           | OR immediate data to ACC   | 1                 | Z             |
| XOR A,x                          | Exclusive-OR immediate data to ACC                                 | 1                 | Z             |
| CPL [m]                          | Complement data memory   | 1 <sup>(1)</sup>  | Z             |
| CPLA [m]                         | Complement data memory with result in ACC                          | 1                 | Z             |
| <b>Increment &amp; Decrement</b> |  |                   |               |
| INCA [m]                         | Increment data memory with result in ACC                           | 1                 | Z             |
| INC [m]                          | Increment data memory  | 1 <sup>(1)</sup>  | Z             |
| DECA [m]                         | Decrement data memory with result in ACC                           | 1                 | Z             |
| DEC [m]                          | Decrement data memory  | 1 <sup>(1)</sup>  | Z             |
| <b>Rotate</b>                    |  |                   |               |
| RRA [m]                          | Rotate data memory right with result in ACC                        | 1                 | None          |
| RR [m]                           | Rotate data memory right   | 1 <sup>(1)</sup>  | None          |
| RRCA [m]                         | Rotate data memory right through carry with result in ACC          | 1                 | C             |
| RRC [m]                          | Rotate data memory right through carry                             | 1 <sup>(1)</sup>  | C             |
| RLA [m]                          | Rotate data memory left with result in ACC                         | 1                 | None          |
| RL [m]                           | Rotate data memory left  | 1 <sup>(1)</sup>  | None          |
| RLCA [m]                         | Rotate data memory left through carry with result in ACC           | 1                 | C             |
| RLC [m]                          | Rotate data memory left through carry                              | 1 <sup>(1)</sup>  | C             |
| <b>Data Move</b>                 |  |                   |               |
| MOV A,[m]                        | Move data memory to ACC  | 1                 | None          |
| MOV [m],A                        | Move ACC to data memory  | 1 <sup>(1)</sup>  | None          |
| MOV A,x                          | Move immediate data to ACC   | 1                 | None          |
| <b>Bit Operation</b>             |  |                   |               |
| CLR [m].i                        | Clear bit of data memory   | 1 <sup>(1)</sup>  | None          |
| SET [m].i                        | Set bit of data memory   | 1 <sup>(1)</sup>  | None          |

| Mnemonic                 | Description   | Instruction Cycle | Flag Affected                         |
|--------------------------|---|-------------------|---------------------------------------|
| <b>Branch</b>            |   |                   |                                       |
| JMP addr                 | Jump unconditionally  | 2                 | None                                  |
| SZ [m]                   | Skip if data memory is zero                                     | 1 <sup>(2)</sup>  | None                                  |
| SZA [m]                  | Skip if data memory is zero with data movement to ACC           | 1 <sup>(2)</sup>  | None                                  |
| SZ [m].i                 | Skip if bit i of data memory is zero                            | 1 <sup>(2)</sup>  | None                                  |
| SNZ [m].i                | Skip if bit i of data memory is not zero                        | 1 <sup>(2)</sup>  | None                                  |
| SIZ [m]                  | Skip if increment data memory is zero                           | 1 <sup>(3)</sup>  | None                                  |
| SDZ [m]                  | Skip if decrement data memory is zero                           | 1 <sup>(3)</sup>  | None                                  |
| SIZA [m]                 | Skip if increment data memory is zero with result in ACC        | 1 <sup>(2)</sup>  | None                                  |
| SDZA [m]                 | Skip if decrement data memory is zero with result in ACC        | 1 <sup>(2)</sup>  | None                                  |
| CALL addr                | Subroutine call   | 2                 | None                                  |
| RET                      | Return from subroutine  | 2                 | None                                  |
| RET A,x                  | Return from subroutine and load immediate data to ACC           | 2                 | None                                  |
| RETI                     | Return from interrupt   | 2                 | None                                  |
| <b>Table Read</b>        |   |                   |                                       |
| TABRDC[M] <sup>(5)</sup> | Read ROM code (locate by TBLP and TBHP) to data memory and TBLH | 2 <sup>(1)</sup>  | None                                  |
| TABRDC[m] <sup>(6)</sup> | Read ROM code (current page) to data memory and TBLH            | 2 <sup>(1)</sup>  | None                                  |
| TABRDL [m]               | Read ROM code (last page) to data memory and TBLH               | 2 <sup>(1)</sup>  | None                                  |
| <b>Miscellaneous</b>     |   |                   |                                       |
| NOP                      | No operation  | 1                 | None                                  |
| CLR [m]                  | Clear data memory   | 1 <sup>(1)</sup>  | None                                  |
| SET [m]                  | Set data memory   | 1 <sup>(1)</sup>  | None                                  |
| CLR WDT                  | Clear Watchdog Timer  | 1                 | TO,PDF                                |
| CLR WDT1                 | Pre-clear Watchdog Timer  | 1                 | TO <sup>(4)</sup> ,PDF <sup>(4)</sup> |
| CLR WDT2                 | Pre-clear Watchdog Timer  | 1                 | TO <sup>(4)</sup> ,PDF <sup>(4)</sup> |
| SWAP [m]                 | Swap nibbles of data memory                                     | 1 <sup>(1)</sup>  | None                                  |
| SWAPA [m]                | Swap nibbles of data memory with result in ACC                  | 1                 | None                                  |
| HALT                     | Enter power down mode   | 1                 | TO,PDF                                |

Note: x: Immediate data

m: Data memory address

A: Accumulator

i: 0~7 number of bits

addr: Program memory address

√: Flag is affected

–: Flag is not affected

<sup>(1)</sup>: If a loading to the PCL register occurs, the execution cycle of instructions will be delayed for one more cycle (four system clocks).

<sup>(2)</sup>: If a skipping to the next instruction occurs, the execution cycle of instructions will be delayed for one more cycle (four system clocks). Otherwise the original instruction cycle is unchanged.

<sup>(3)</sup>: <sup>(1)</sup> and <sup>(2)</sup>

<sup>(4)</sup>: The flags may be affected by the execution status. If the Watchdog Timer is cleared by executing the "CLR WDT1" or "CLR WDT2" instruction, the TO and PDF are cleared. Otherwise the TO and PDF flags remain unchanged.

<sup>(5)</sup>: "ROM code TBHP option" is enabled

<sup>(6)</sup>: "ROM code TBHP option" is disabled

**Instruction Definition**

**ADC A,[m]** Add data memory and carry to the accumulator  
 Description The contents of the specified data memory, accumulator and the carry flag are added simultaneously, leaving the result in the accumulator.

Operation  $ACC \leftarrow ACC+[m]+C$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**ADCM A,[m]** Add the accumulator and carry to data memory  
 Description The contents of the specified data memory, accumulator and the carry flag are added simultaneously, leaving the result in the specified data memory.

Operation  $[m] \leftarrow ACC+[m]+C$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**ADD A,[m]** Add data memory to the accumulator  
 Description The contents of the specified data memory and the accumulator are added. The result is stored in the accumulator.

Operation  $ACC \leftarrow ACC+[m]$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**ADD A,x** Add immediate data to the accumulator  
 Description The contents of the accumulator and the specified data are added, leaving the result in the accumulator.

Operation  $ACC \leftarrow ACC+x$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**ADDM A,[m]** Add the accumulator to the data memory  
 Description The contents of the specified data memory and the accumulator are added. The result is stored in the data memory.

Operation  $[m] \leftarrow ACC+[m]$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**AND A,[m]**

Logical AND accumulator with data memory

Description

Data in the accumulator and the specified data memory perform a bitwise logical\_AND operation. The result is stored in the accumulator.

Operation

 $ACC \leftarrow ACC \text{ "AND" } [m]$ 

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**AND A,x**

Logical AND immediate data to the accumulator

Description

Data in the accumulator and the specified data perform a bitwise logical\_AND operation. The result is stored in the accumulator.

Operation

 $ACC \leftarrow ACC \text{ "AND" } x$ 

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**ANDM A,[m]**

Logical AND data memory with the accumulator

Description

Data in the specified data memory and the accumulator perform a bitwise logical\_AND operation. The result is stored in the data memory.

Operation

 $[m] \leftarrow ACC \text{ "AND" } [m]$ 

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**CALL addr**

Subroutine call

Description

The instruction unconditionally calls a subroutine located at the indicated address. The program counter increments once to obtain the address of the next instruction, and pushes this onto the stack. The indicated address is then loaded. Program execution continues with the instruction at this address.

Operation

 $Stack \leftarrow PC+1$   
 $PC \leftarrow addr$ 

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**CLR [m]**

Clear data memory

Description

The contents of the specified data memory are cleared to 0.

Operation

 $[m] \leftarrow 00H$ 

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**CLR [m].i** Clear bit of data memory  
 Description The bit i of the specified data memory is cleared to 0.  
 Operation  $[m].i \leftarrow 0$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**CLR WDT** Clear Watchdog Timer  
 Description The WDT is cleared (clears the WDT). The power down bit (PDF) and time-out bit (TO) are cleared.  
 Operation  $WDT \leftarrow 00H$   
 $PDF \text{ and } TO \leftarrow 0$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| 0  | 0   | —  | — | —  | — |

**CLR WDT1** Preclear Watchdog Timer  
 Description Together with CLR WDT2, clears the WDT. PDF and TO are also cleared. Only execution of this instruction without the other preclear instruction just sets the indicated flag which implies this instruction has been executed and the TO and PDF flags remain unchanged.  
 Operation  $WDT \leftarrow 00H^*$   
 $PDF \text{ and } TO \leftarrow 0^*$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| 0* | 0*  | —  | — | —  | — |

**CLR WDT2** Preclear Watchdog Timer  
 Description Together with CLR WDT1, clears the WDT. PDF and TO are also cleared. Only execution of this instruction without the other preclear instruction, sets the indicated flag which implies this instruction has been executed and the TO and PDF flags remain unchanged.  
 Operation  $WDT \leftarrow 00H^*$   
 $PDF \text{ and } TO \leftarrow 0^*$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| 0* | 0*  | —  | — | —  | — |

**CPL [m]** Complement data memory  
 Description Each bit of the specified data memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice-versa.  
 Operation  $[m] \leftarrow \overline{[m]}$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**CPLA [m]**

Complement data memory and place result in the accumulator

Description

Each bit of the specified data memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice-versa. The complemented result is stored in the accumulator and the contents of the data memory remain unchanged.

Operation

$$ACC \leftarrow \overline{[m]}$$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**DAA [m]**

Decimal-Adjust accumulator for addition

Description

The accumulator value is adjusted to the BCD (Binary Coded Decimal) code. The accumulator is divided into two nibbles. Each nibble is adjusted to the BCD code and an internal carry (AC1) will be done if the low nibble of the accumulator is greater than 9. The BCD adjustment is done by adding 6 to the original value if the original value is greater than 9 or a carry (AC or C) is set; otherwise the original value remains unchanged. The result is stored in the data memory and only the carry flag (C) may be affected.

Operation

If  $ACC.3 \sim ACC.0 > 9$  or  $AC=1$   
 then  $[m].3 \sim [m].0 \leftarrow (ACC.3 \sim ACC.0) + 6$ ,  $AC1 = \overline{AC}$   
 else  $[m].3 \sim [m].0 \leftarrow (ACC.3 \sim ACC.0)$ ,  $AC1 = 0$   
 and  
 If  $ACC.7 \sim ACC.4 + AC1 > 9$  or  $C=1$   
 then  $[m].7 \sim [m].4 \leftarrow ACC.7 \sim ACC.4 + 6 + AC1$ ,  $C=1$   
 else  $[m].7 \sim [m].4 \leftarrow ACC.7 \sim ACC.4$ ,  $C=C$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | √ |

**DEC [m]**

Decrement data memory

Description

Data in the specified data memory is decremented by 1.

Operation

$$[m] \leftarrow [m] - 1$$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**DECA [m]**

Decrement data memory and place result in the accumulator

Description

Data in the specified data memory is decremented by 1, leaving the result in the accumulator. The contents of the data memory remain unchanged.

Operation

$$ACC \leftarrow [m] - 1$$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |



**HALT** Enter power down mode

Description This instruction stops program execution and turns off the system clock. The contents of the RAM and registers are retained. The WDT and prescaler are cleared. The power down bit (PDF) is set and the WDT time-out bit (TO) is cleared.

Operation  
 $PC \leftarrow PC+1$   
 $PDF \leftarrow 1$   
 $TO \leftarrow 0$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| 0  | 1   | —  | — | —  | — |

**INC [m]** Increment data memory

Description Data in the specified data memory is incremented by 1

Operation  
 $[m] \leftarrow [m]+1$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**INCA [m]** Increment data memory and place result in the accumulator

Description Data in the specified data memory is incremented by 1, leaving the result in the accumulator. The contents of the data memory remain unchanged.

Operation  
 $ACC \leftarrow [m]+1$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**JMP addr** Directly jump

Description The program counter are replaced with the directly-specified address unconditionally, and control is passed to this destination.

Operation  
 $PC \leftarrow \text{addr}$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**MOV A,[m]** Move data memory to the accumulator

Description The contents of the specified data memory are copied to the accumulator.

Operation  
 $ACC \leftarrow [m]$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**MOV A,x** Move immediate data to the accumulator  
 Description The 8-bit data specified by the code is loaded into the accumulator.  
 Operation  $ACC \leftarrow x$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**MOV [m],A** Move the accumulator to data memory  
 Description The contents of the accumulator are copied to the specified data memory (one of the data memories).  
 Operation  $[m] \leftarrow ACC$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**NOP** No operation  
 Description No operation is performed. Execution continues with the next instruction.  
 Operation  $PC \leftarrow PC+1$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**OR A,[m]** Logical OR accumulator with data memory  
 Description Data in the accumulator and the specified data memory (one of the data memories) perform a bitwise logical\_OR operation. The result is stored in the accumulator.  
 Operation  $ACC \leftarrow ACC \text{ "OR" } [m]$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**OR A,x** Logical OR immediate data to the accumulator  
 Description Data in the accumulator and the specified data perform a bitwise logical\_OR operation. The result is stored in the accumulator.  
 Operation  $ACC \leftarrow ACC \text{ "OR" } x$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**ORM A,[m]** Logical OR data memory with the accumulator  
 Description Data in the data memory (one of the data memories) and the accumulator perform a bitwise logical\_OR operation. The result is stored in the data memory.  
 Operation  $[m] \leftarrow ACC \text{ "OR" } [m]$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**RET** Return from subroutine  
 Description The program counter is restored from the stack. This is a 2-cycle instruction.  
 Operation  $PC \leftarrow Stack$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**RET A,x** Return and place immediate data in the accumulator  
 Description The program counter is restored from the stack and the accumulator loaded with the specified 8-bit immediate data.  
 Operation  $PC \leftarrow Stack$   
 $ACC \leftarrow x$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**RETI** Return from interrupt  
 Description The program counter is restored from the stack, and interrupts are enabled by setting the EMI bit. EMI is the enable master (global) interrupt bit.  
 Operation  $PC \leftarrow Stack$   
 $EMI \leftarrow 1$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**RL [m]** Rotate data memory left  
 Description The contents of the specified data memory are rotated 1 bit left with bit 7 rotated into bit 0.  
 Operation  $[m].(i+1) \leftarrow [m].i$ ;  $[m].i$ :bit i of the data memory ( $i=0\sim 6$ )  
 $[m].0 \leftarrow [m].7$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**RLA [m]** Rotate data memory left and place result in the accumulator  
 Description Data in the specified data memory is rotated 1 bit left with bit 7 rotated into bit 0, leaving the rotated result in the accumulator. The contents of the data memory remain unchanged.  
 Operation  $ACC.(i+1) \leftarrow [m].i$ ;  $[m].i$ :bit i of the data memory ( $i=0\sim 6$ )  
 $ACC.0 \leftarrow [m].7$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**RLC [m]** Rotate data memory left through carry  
 Description The contents of the specified data memory and the carry flag are rotated 1 bit left. Bit 7 replaces the carry bit; the original carry flag is rotated into the bit 0 position.  
 Operation  $[m].(i+1) \leftarrow [m].i$ ;  $[m].i$ :bit i of the data memory (i=0~6)  
 $[m].0 \leftarrow C$   
 $C \leftarrow [m].7$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | √ |

**RLCA [m]** Rotate left through carry and place result in the accumulator  
 Description Data in the specified data memory and the carry flag are rotated 1 bit left. Bit 7 replaces the carry bit and the original carry flag is rotated into bit 0 position. The rotated result is stored in the accumulator but the contents of the data memory remain unchanged.  
 Operation  $ACC.(i+1) \leftarrow [m].i$ ;  $[m].i$ :bit i of the data memory (i=0~6)  
 $ACC.0 \leftarrow C$   
 $C \leftarrow [m].7$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | √ |

**RR [m]** Rotate data memory right  
 Description The contents of the specified data memory are rotated 1 bit right with bit 0 rotated to bit 7.  
 Operation  $[m].i \leftarrow [m].(i+1)$ ;  $[m].i$ :bit i of the data memory (i=0~6)  
 $[m].7 \leftarrow [m].0$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**RRA [m]** Rotate right and place result in the accumulator  
 Description Data in the specified data memory is rotated 1 bit right with bit 0 rotated into bit 7, leaving the rotated result in the accumulator. The contents of the data memory remain unchanged.  
 Operation  $ACC.(i) \leftarrow [m].(i+1)$ ;  $[m].i$ :bit i of the data memory (i=0~6)  
 $ACC.7 \leftarrow [m].0$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**RRC [m]** Rotate data memory right through carry  
 Description The contents of the specified data memory and the carry flag are together rotated 1 bit right. Bit 0 replaces the carry bit; the original carry flag is rotated into the bit 7 position.  
 Operation  $[m].i \leftarrow [m].(i+1)$ ;  $[m].i$ :bit i of the data memory (i=0~6)  
 $[m].7 \leftarrow C$   
 $C \leftarrow [m].0$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | √ |

**RRCA [m]** Rotate right through carry and place result in the accumulator

Description Data of the specified data memory and the carry flag are rotated 1 bit right. Bit 0 replaces the carry bit and the original carry flag is rotated into the bit 7 position. The rotated result is stored in the accumulator. The contents of the data memory remain unchanged.

Operation  $ACC.i \leftarrow [m].(i+1)$ ;  $[m].i$ :bit i of the data memory (i=0~6)  
 $ACC.7 \leftarrow C$   
 $C \leftarrow [m].0$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | √ |

**SBC A,[m]** Subtract data memory and carry from the accumulator

Description The contents of the specified data memory and the complement of the carry flag are subtracted from the accumulator, leaving the result in the accumulator.

Operation  $ACC \leftarrow ACC + \overline{[m]} + C$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**SBCM A,[m]** Subtract data memory and carry from the accumulator

Description The contents of the specified data memory and the complement of the carry flag are subtracted from the accumulator, leaving the result in the data memory.

Operation  $[m] \leftarrow ACC + \overline{[m]} + C$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**SDZ [m]** Skip if decrement data memory is 0

Description The contents of the specified data memory are decremented by 1. If the result is 0, the next instruction is skipped. If the result is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if  $([m]-1)=0$ ,  $[m] \leftarrow ([m]-1)$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SDZA [m]** Decrement data memory and place result in ACC, skip if 0

Description The contents of the specified data memory are decremented by 1. If the result is 0, the next instruction is skipped. The result is stored in the accumulator but the data memory remains unchanged. If the result is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if  $([m]-1)=0$ ,  $ACC \leftarrow ([m]-1)$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SET [m]** Set data memory  
 Description Each bit of the specified data memory is set to 1.  
 Operation  $[m] \leftarrow FFH$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SET [m]. i** Set bit of data memory  
 Description Bit i of the specified data memory is set to 1.  
 Operation  $[m].i \leftarrow 1$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SIZ [m]** Skip if increment data memory is 0  
 Description The contents of the specified data memory are incremented by 1. If the result is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).  
 Operation Skip if  $([m]+1)=0$ ,  $[m] \leftarrow ([m]+1)$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SIZA [m]** Increment data memory and place result in ACC, skip if 0  
 Description The contents of the specified data memory are incremented by 1. If the result is 0, the next instruction is skipped and the result is stored in the accumulator. The data memory remains unchanged. If the result is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).  
 Operation Skip if  $([m]+1)=0$ ,  $ACC \leftarrow ([m]+1)$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SNZ [m].i** Skip if bit i of the data memory is not 0  
 Description If bit i of the specified data memory is not 0, the next instruction is skipped. If bit i of the data memory is not 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).  
 Operation Skip if  $[m].i \neq 0$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SUB A,[m]** Subtract data memory from the accumulator  
 Description The specified data memory is subtracted from the contents of the accumulator, leaving the result in the accumulator.  
 Operation  $ACC \leftarrow ACC + \overline{[m]} + 1$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**SUBM A,[m]** Subtract data memory from the accumulator  
 Description The specified data memory is subtracted from the contents of the accumulator, leaving the result in the data memory.  
 Operation  $[m] \leftarrow ACC + \overline{[m]} + 1$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**SUB A,x** Subtract immediate data from the accumulator  
 Description The immediate data specified by the code is subtracted from the contents of the accumulator, leaving the result in the accumulator.  
 Operation  $ACC \leftarrow ACC + \overline{x} + 1$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | √  | √ | √  | √ |

**SWAP [m]** Swap nibbles within the data memory  
 Description The low-order and high-order nibbles of the specified data memory (1 of the data memories) are interchanged.  
 Operation  $[m].3 \sim [m].0 \leftrightarrow [m].7 \sim [m].4$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SWAPA [m]** Swap data memory and place result in the accumulator  
 Description The low-order and high-order nibbles of the specified data memory are interchanged, writing the result to the accumulator. The contents of the data memory remain unchanged.  
 Operation  $ACC.3 \sim ACC.0 \leftarrow [m].7 \sim [m].4$   
 $ACC.7 \sim ACC.4 \leftarrow [m].3 \sim [m].0$   
 Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SZ [m]** Skip if data memory is 0  
 Description If the contents of the specified data memory are 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if [m]=0

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SZA [m]** Move data memory to ACC, skip if 0  
 Description The contents of the specified data memory are copied to the accumulator. If the contents is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if [m]=0

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**SZ [m].i** Skip if bit i of the data memory is 0  
 Description If bit i of the specified data memory is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if [m].i=0

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**TABRDC [m]** Move the ROM code (locate by TBLP and TBHP) to TBLH and data memory (ROM code TBHP is enabled)

Description The low byte of ROM code addressed by the table pointers (TBLP and TBHP) is moved to the specified data memory and the high byte transferred to TBLH directly.

Operation [m] ← ROM code (low byte)  
 TBLH ← ROM code (high byte)

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**TABRDC [m]** Move the ROM code (current page) to TBLH and data memory (ROM code TBHP is disabled)

Description The low byte of ROM code (current page) addressed by the table pointer (TBLP) is moved to the specified data memory and the high byte transferred to TBLH directly.

Operation [m] ← ROM code (low byte)  
 TBLH ← ROM code (high byte)

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |



**TABRDL [m]** Move the ROM code (last page) to TBLH and data memory  
 Description The low byte of ROM code (last page) addressed by the table pointer (TBLP) is moved to the data memory and the high byte transferred to TBLH directly.  
 Operation  $[m] \leftarrow \text{ROM code (low byte)}$   
 $\text{TBLH} \leftarrow \text{ROM code (high byte)}$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | — | —  | — |

**XOR A,[m]** Logical XOR accumulator with data memory  
 Description Data in the accumulator and the indicated data memory perform a bitwise logical Exclusive\_OR operation and the result is stored in the accumulator.  
 Operation  $\text{ACC} \leftarrow \text{ACC "XOR" [m]}$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

**XORM A,[m]** Logical XOR data memory with the accumulator  
 Description Data in the indicated data memory and the accumulator perform a bitwise logical Exclusive\_OR operation. The result is stored in the data memory. The 0 flag is affected.  
 Operation  $[m] \leftarrow \text{ACC "XOR" [m]}$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

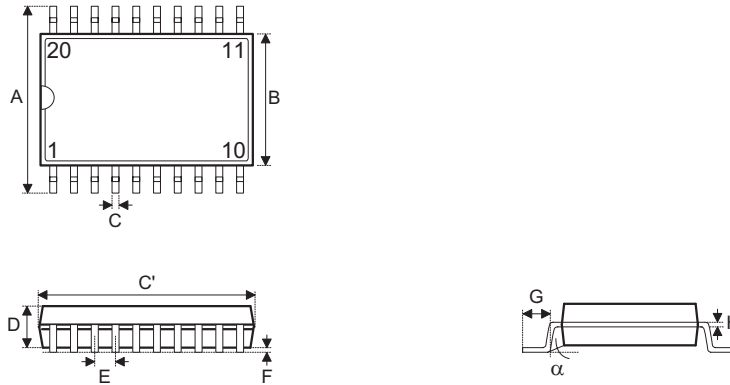
**XOR A,x** Logical XOR immediate data to the accumulator  
 Description Data in the accumulator and the specified data perform a bitwise logical Exclusive\_OR operation. The result is stored in the accumulator. The 0 flag is affected.  
 Operation  $\text{ACC} \leftarrow \text{ACC "XOR" x}$

Affected flag(s)

| TO | PDF | OV | Z | AC | C |
|----|-----|----|---|----|---|
| —  | —   | —  | √ | —  | — |

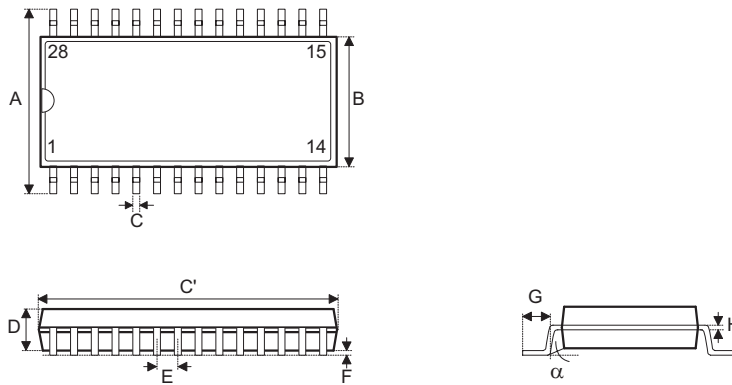
**Package Information**

**20-pin SOP (300mil) Outline Dimensions**



| Symbol   | Dimensions in mil |      |      |
|----------|-------------------|------|------|
|          | Min.              | Nom. | Max. |
| A        | 394               | —    | 419  |
| B        | 290               | —    | 300  |
| C        | 14                | —    | 20   |
| C'       | 490               | —    | 510  |
| D        | 92                | —    | 104  |
| E        | —                 | 50   | —    |
| F        | 4                 | —    | —    |
| G        | 32                | —    | 38   |
| H        | 4                 | —    | 12   |
| $\alpha$ | 0°                | —    | 10°  |

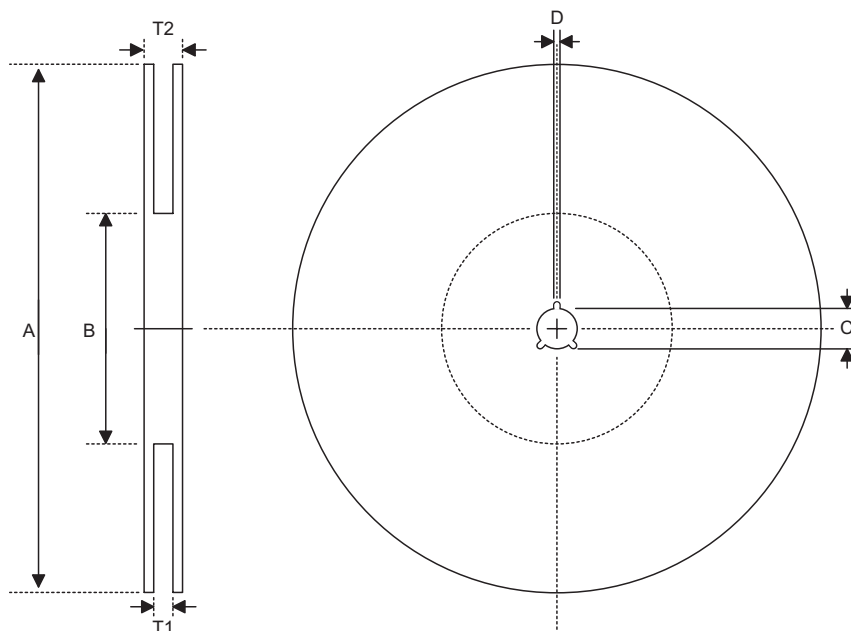
28-pin SOP (300mil) Outline Dimensions



| Symbol   | Dimensions in mil |      |      |
|----------|-------------------|------|------|
|          | Min.              | Nom. | Max. |
| A        | 394               | —    | 419  |
| B        | 290               | —    | 300  |
| C        | 14                | —    | 20   |
| C'       | 697               | —    | 713  |
| D        | 92                | —    | 104  |
| E        | —                 | 50   | —    |
| F        | 4                 | —    | —    |
| G        | 32                | —    | 38   |
| H        | 4                 | —    | 12   |
| $\alpha$ | 0°                | —    | 10°  |

**Product Tape and Reel Specifications**

**Reel Dimensions**

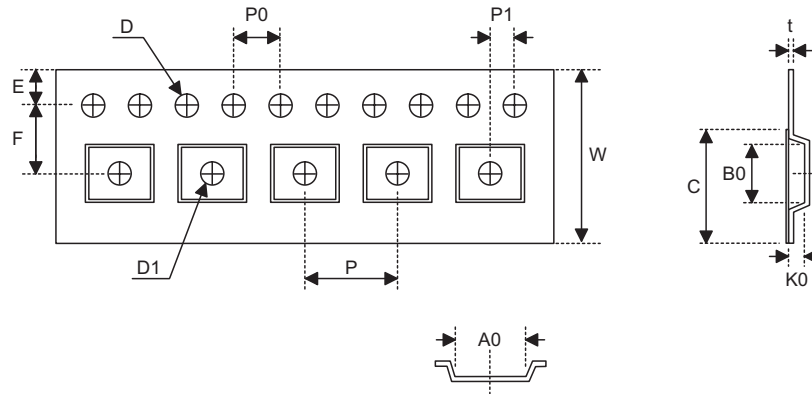


**SOP 20W**

| Symbol | Description           | Dimensions in mm |
|--------|-----------------------|------------------|
| A      | Reel Outer Diameter   | 330±1.0          |
| B      | Reel Inner Diameter   | 62±1.5           |
| C      | Spindle Hole Diameter | 13.0+0.5<br>-0.2 |
| D      | Key Slit Width        | 2.0±0.5          |
| T1     | Space Between Flange  | 24.8+0.3<br>-0.2 |
| T2     | Reel Thickness        | 30.2±0.2         |

**SOP 28W (300mil)**

| Symbol | Description           | Dimensions in mm |
|--------|-----------------------|------------------|
| A      | Reel Outer Diameter   | 330±1.0          |
| B      | Reel Inner Diameter   | 62±1.5           |
| C      | Spindle Hole Diameter | 13.0+0.5<br>-0.2 |
| D      | Key Slit Width        | 2.0±0.5          |
| T1     | Space Between Flange  | 24.8+0.3<br>-0.2 |
| T2     | Reel Thickness        | 30.2±0.2         |

**Carrier Tape Dimensions**

**SOP 20W**

| Symbol | Description                              | Dimensions in mm |
|--------|--|------------------|
| W      | Carrier Tape Width                       | 24.0+0.3<br>-0.1 |
| P      | Cavity Pitch                             | 12.0±0.1         |
| E      | Perforation Position                     | 1.75±0.1         |
| F      | Cavity to Perforation (Width Direction)  | 11.5±0.1         |
| D      | Perforation Diameter                     | 1.5+0.1          |
| D1     | Cavity Hole Diameter                     | 1.5+0.25         |
| P0     | Perforation Pitch                        | 4.0±0.1          |
| P1     | Cavity to Perforation (Length Direction) | 2.0±0.1          |
| A0     | Cavity Length                            | 10.8±0.1         |
| B0     | Cavity Width                             | 13.3±0.1         |
| K0     | Cavity Depth                             | 3.2±0.1          |
| t      | Carrier Tape Thickness                   | 0.3±0.05         |
| C      | Cover Tape Width                         | 21.3             |

**SOP 28W (300mil)**

| Symbol | Description                              | Dimensions in mm |
|--------|--|------------------|
| W      | Carrier Tape Width                       | 24.0±0.3         |
| P      | Cavity Pitch                             | 12.0±0.1         |
| E      | Perforation Position                     | 1.75±0.1         |
| F      | Cavity to Perforation (Width Direction)  | 11.5±0.1         |
| D      | Perforation Diameter                     | 1.5+0.1          |
| D1     | Cavity Hole Diameter                     | 1.5+0.25         |
| P0     | Perforation Pitch                        | 4.0±0.1          |
| P1     | Cavity to Perforation (Length Direction) | 2.0±0.1          |
| A0     | Cavity Length                            | 10.85±0.1        |
| B0     | Cavity Width                             | 18.34±0.1        |
| K0     | Cavity Depth                             | 2.97±0.1         |
| t      | Carrier Tape Thickness                   | 0.35±0.01        |
| C      | Cover Tape Width                         | 21.3             |

**Holtek Semiconductor Inc. (Headquarters)**

No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan  
Tel: 886-3-563-1999  
Fax: 886-3-563-1189  
<http://www.holtek.com.tw>

**Holtek Semiconductor Inc. (Taipei Sales Office)**

4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan  
Tel: 886-2-2655-7070  
Fax: 886-2-2655-7373  
Fax: 886-2-2655-7383 (International sales hotline)

**Holtek Semiconductor Inc. (Shanghai Sales Office)**

7th Floor, Building 2, No.889, Yi Shan Rd., Shanghai, China 200233  
Tel: 021-6485-5560  
Fax: 021-6485-0313  
<http://www.holtek.com.cn>

**Holtek Semiconductor Inc. (Shenzhen Sales Office)**

43F, SEG Plaza, Shen Nan Zhong Road, Shenzhen, China 518031  
Tel: 0755-8346-5589  
Fax: 0755-8346-5590  
ISDN: 0755-8346-5591

**Holtek Semiconductor Inc. (Beijing Sales Office)**

Suite 1721, Jinyu Tower, A129 West Xuan Wu Men Street, Xicheng District, Beijing, China 100031  
Tel: 010-6641-0030, 6641-7751, 6641-7752  
Fax: 010-6641-0125

**Holmate Semiconductor, Inc. (North America Sales Office)**

46712 Fremont Blvd., Fremont, CA 94538  
Tel: 510-252-9880  
Fax: 510-252-9885  
<http://www.holmate.com>

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