HT82V42
CIS Analog Signal Processor

Features

- 3.3V single power supply
- Low power consumption: 188mW (Typ.)
- Power-down mode: 300uA (Typ.)
- 16-bit 15 MSPS A/D converter
- Guaranteed won't miss codes
- 8-bit programmable gain
- Correlated Double Sampling
- ±315mV 8-bit programmable offset
- Programmable clamp voltage
- Internal voltage reference
- Programmable 4-wire serial interface
- 4-bit multiplexed nibble mode
- 20-pin SSOP/TSSOP package

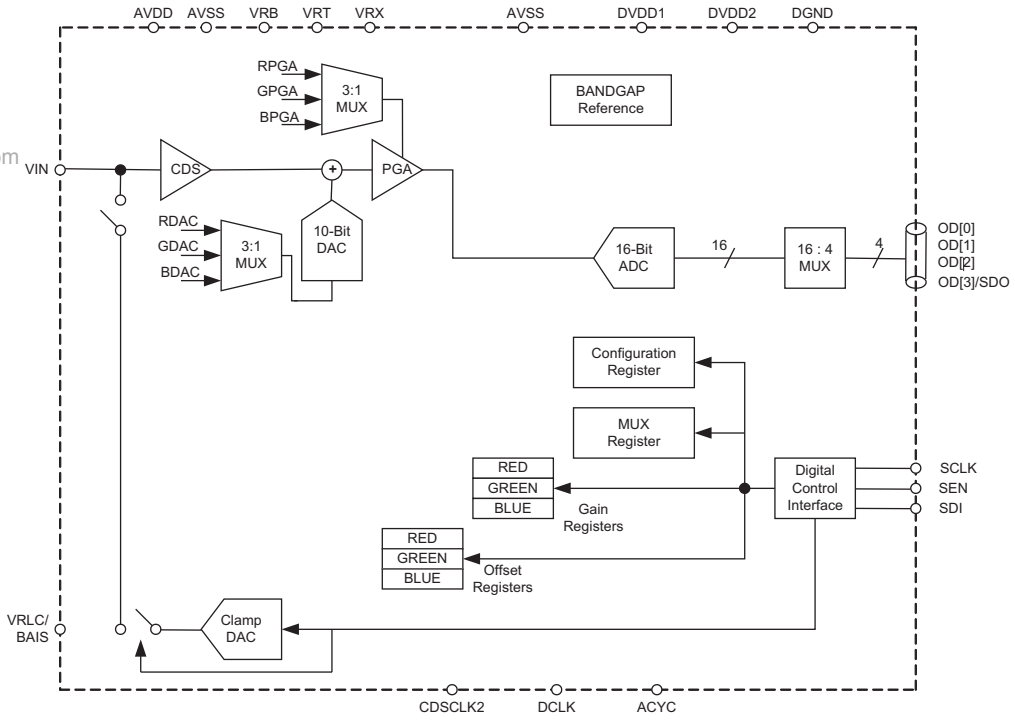
Applications

- Flatbed document scanners
- Film scanners
- Digital color copiers
- Multifunction peripherals

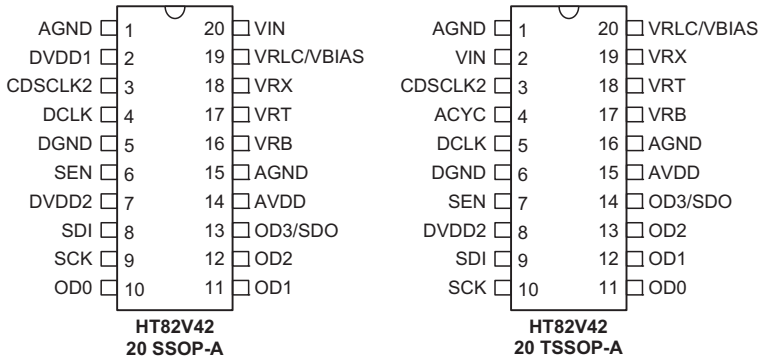
General Description

The HT82V42 is a complete analog signal processor for CCD imaging applications. It features a 1-channel architecture designed to sample and condition the outputs of tri-linear color CCD arrays. The channel consists of an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA) and a high performance 16-bit A/D converter. The CDS amplifiers may be disabled for use with sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, which do not require CDS. The 16-bit digital output is available in 4-bit wide multiplexed format. The internal registers are programmed through a 4-wire serial interface, which provides gain, offset and operating mode adjustments. The HT82V42 operates from a single 3.3V power supply and typically consumes 188mW of power.

Block Diagram



Pin Assignment



Pin Description

Pin Name	I/O	Description
AGND	P	Negative power supply for analog circuit
DVDD1	P	Digital Driver Power (3.3V).
CDSCLK2	DI	CDS Video Sample Clock Pulse Input
RLC/ACYC	DI	ACYC auto cycles between R, G, B inputs.
DCLK	DI	ADC Clock. This clock is applied at N times the input pixel rate (N = 2, 3, 6, 8 or any multiple of 2 thereafter depending on input sample mode).
DGND	P	Digital Driver Ground
SEN	DI	Serial Interface Enable Pulse (High Active)
DVDD2	P	Digital Driver Power(3.3V).
SDI	DI	Serial Data Input
SCK	DI	Clock Input for Serial Interface
OD0~OD2 OD3/SDO	DO	Digital multiplexed output data bus. ADC output data D[15:0] is available in two multiplexed formats as shown. When register bit OEB = 0, address bit4 = 1 and SEN has been pulsed high, this pin use as SDO for register data read-back. Otherwise, this pin use as Digital Data Output.
AVDD	P	Analog Supply (3.3V).
VRB	AO	Reference Decoupling, this pin must be connected to AGND via a decoupling capacitor.
VRT	AO	Reference Decoupling, this pin must be connected to AGND via a decoupling capacitor.
VRX	AO	Reference Decoupling, this pin must be connected to AGND via a decoupling capacitor.
VRLC/VBIAS	AO	Selectable analog output voltage for RLC or single-ended bias reference. This pin would typically be connected to AGND via a decoupling capacitor. VRLC can be externally driven if programmed Hi-z.
VIN	AI	Analog Input

A	B	C	D
D12	D8	D4	D0
D13	D9	D5	D1
D14	D10	D6	D2
D15	D11	D7	D3

Note: AI=Analog Input; AO=Analog Output; AIO=Analog Inout
DI=Digital Input; DO=Digital Output; P=Power

Absolute Maximum Ratings

Supply Voltage .....V_{SS}–0.3V to V_{SS}+4.3V

Input Voltage .....V_{SS}–0.3V to V_{CC}+0.3V

Analogue Supply Power .....3.0V~3.6V

Storage Temperature .....–50°C to 125°C

Operating Temperature .....0°C to 70°C

Digital supply power.....3.0V~3.6V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

AV_{DD}=DV_{DD1}=DV_{DD2}=3.3V, AGND=DGND=0V, Ta=25°C, DCLK=30MHz unless otherwise stated.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Overall System Specification (including 16-bit ADC, PGA, Offset and CDS Functions)							
	Full-scale Input Voltage Range (see Note 1)	3.3V	—	—	0.27	—	V_{P-P}
				—	3.0	—	V_{P-P}
V_{IN}	Input Signal Limits (see Note 2)	3.3V	—	0		AV_{DD}	V
	Full-scale Transition Error	3.3V	Gain = 0dB; PGA[7:0] = 54(hex)	—	50	—	mV
	Zero-scale Transition Error	3.3V	Gain = 0dB; PGA[7:0] = 54(hex)	—	50	—	mV
DNL	Differential non-Linearity	3.3V	—	—	1.5	—	LSB
INL	Integral non-Linearity	3.3V	—	—	50	—	LSB
	Total Output Noise	3.3V	Min Gain	—	7	—	LSB rms
			Max Gain	—	18	—	
References							
VRT	Upper Reference Voltage		—	1.90	2.00	2.20	V
VRB	Lower Reference Voltage		—	0.90	1.00	1.20	V
VRX	Input Return Bias Voltage		—	—	1.70	—	V
V_{RTB}	Diff. Reference Voltage (VRT-VRB)		—	0.9	1.0	1.1	V
Reset-Level Clamp (RLC) circuit/ Reference Level DAC							
	Reference RLCDAC Resolution		—	—	4	—	bits
$V_{RLCSTEP}$	Reference RLCDAC Step Size RLCDACRNG=0	3.3V	—	0.159	0.173	0.187	V/step
V_{RLCBOT}	Reference RLCDAC Step Size RLCDACRNG=1		—	0.096	0.11	0.124	V/step
V_{RLCBOT}	Reference RLCDAC Output Voltage at Code 0(hex), RLCDACRNG=0	3.3V	—	0.35	0.4	0.45	V
V_{RLCTOP}	Reference RLCDAC Output Voltage at Code 0(hex), RLCDACRNG=1		—	0.35	0.40	0.45	V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{RLCTOP}	Reference RLCLDAC Output Voltage at Code F(hex), RLCDACRNG=0	3.3V		2.8	3.0	3.10	V
$V_{RLCSTEP}$	Reference RLCDAC Output Voltage at Code F(hex), RLCDACRNG=1			1.90	2.00	2.10	V
Offset DAC, Monotonicity Guaranteed							
	Resolution			—	8	—	bits
DNL	Differential Non-Linearity			—	0.1	0.5	LSB
INL	Integral Non-Linearity			—	0.25	1.00	LSB
	Step Size			—	2.46	—	mV/step
	Output Voltage			—	–315	—	mV
				—	+315	—	mV
Programmable Gain Amplifier							
	Resolution			—	8	—	bits
	Gain Equation			186/(278-PGA[7:0])			V/V
G_{MAX}	Max Gain			6.50	8.00	8.40	V/V
G_{MIN}	Min Gain			0.65	0.68	0.75	V/V
	Gain Error			—	2	—	%
Analogue to Digital Converter							
	Resolution			—	16	—	bits
	Speed			—	—	15	MSPS
	Full-scale Input Range (2*(VRT–VRB))			—	2	—	V
Digital Inputs							
V_{IH}	High Level Input Voltage			$0.7V_{DD}$	—	—	V
V_{IL}	Low Level Input Voltage			—	—	$0.2V_{DD}$	V
I_{IH}	High Level Input Current			—	—	1	μA
I_{IL}	Low Level Input Current			—	—	1	μA
C_I	Input Capacitance			—	5	—	pF
Digital Outputs							
V_{OH}	High Level Output Voltage		I_{OH}=1mA	DV_{DD}-0.5	—	—	V
V_{OL}	Low Level Output Voltage		I_{OL}=1mA	—	—	0.5	V
I_{OZ}	High Impedance Output Current			—	—	1	μA
Supply Currents							
	Total Supply Current – Active (Signal Channel Mode)		LINEBYLINE=1 DCLK=30MHz	—	57	—	mA
	Total Analog Supply Current – Active (Signal Channel Mode)		LINEBYLINE=1 DCLK=30MHz	—	36	—	mA
	Digital Supply Current – Active (DV_{DD1})		DCLK=30MHz	—	14	—	mA

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
	Digital Supply Current – Active (DV_{DD2})		DCLK=30MHz	—	7	—	mA
	Supply Current – Full Power Down Mode			—	300	—	μA

Note: 1. Full-scale input voltage denotes the peak input signal amplitude that can be gained to match the ADC full-scale input range.

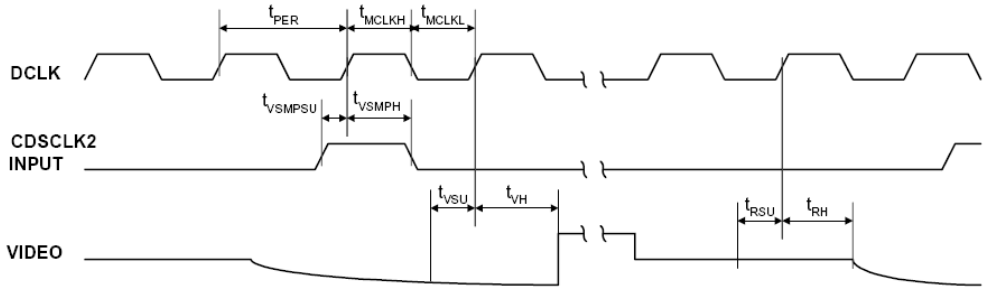
2. Input signal limits are the limits within which the full-scale input voltage signal must lie.

A.C. Characteristics

$AV_{DD}=DV_{DD1}=DV_{DD2}=3.3V$, AGND=DGND=0V, Ta=25°C, DCLK=30MHz unless otherwise stated.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
	Conversion Rate	3.3V	—	—	—	15	MSPS

Input Video Timing



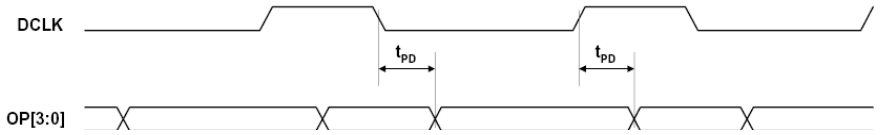
$AV_{DD}=DV_{DD1}=DV_{DD2}=3.3V$, AGND=DGND=0V, Ta=25°C, DCLK=30MHz unless otherwise stated.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PER}	DCLK period	33.3	—	—	ns
t_{DCLKH}	DCLK high period	16.6	—	—	ns
t_{DCLKL}	DCLK low period	16.6	—	—	ns
t_{VSMPSU}	CDSCLK2 setup time	6	—	—	ns
t_{VSMPH}	CDSCLK2 hold time	3	—	—	ns
t_{VSU}	Video level setup time	10	—	—	ns
t_{VH}	Video level hold time	3	—	—	ns
t_{RSU}	Reset level setup time	10	—	—	ns
t_{RH}	Reset level setup time	3	—	—	ns

Note : 1. t_{VSU} and t_{RSU} denote the setup time require after the input video signal has settled.

2. Parameters are measured at 50% of the rising/falling edge.

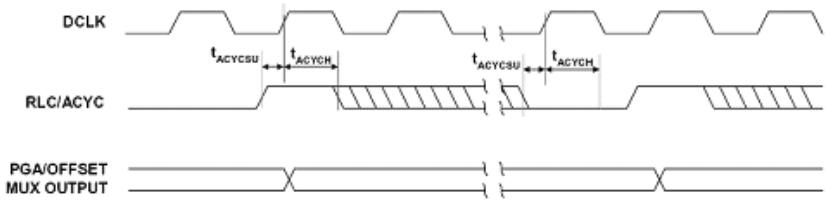
Output Data Timing



Output Data Timing

$AV_{DD}=DV_{DD1}=DV_{DD2}=3.3V$, AGND=DGND=0V, Ta=25°C, DCLK=30MHz unless otherwise stated.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PD}	Output propagation delay	—	—	16	ns

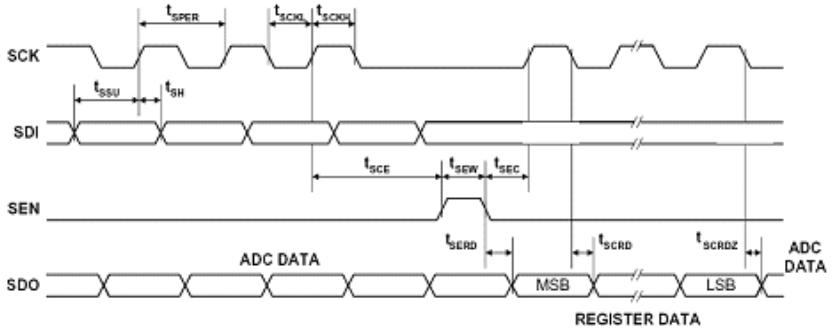


Auto Cycle Timing

$AV_{DD}=DV_{DD1}=DV_{DD2}=3.3V$, AGND=DGND=0V, Ta=25°C, DCLK=30MHz unless otherwise stated.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CYCSU}	Auto cycle setup time	6	—	—	ns
t_{ACYCH}	Auto cycle hold time	3	—	—	ns

Serial Interface



Serial Interface Timing

$AV_{DD}=DV_{DD1}=DV_{DD2}=3.3V$, AGND=DGND=0V, Ta=25°C, DCLK=30MHz unless otherwise stated.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SPER}	SCK period	37.6	—	—	ns
t_{SCKH}	SCK high	18.8	—	—	ns
t_{SCKLz}	SCK low	18.8	—	—	ns
t_{SSU}	SDI setup time	6	—	—	ns
t_{SH}	SDI hold time	6	—	—	ns
t_{SCE}	SCK to SEN setup time	12	—	—	ns
t_{SEC}	SEN to SCK setup time	12	—	—	ns
t_{SEW}	SEN pulse width	25	—	—	ns
t_{SERD}	SEN low to SDO = Register data	—	—	30	ns
t_{SCRD}	SCK low to SDO = Register data	—	—	30	ns
t_{SCRDZ}	SCK low to SDO = ADC data	—	—	30	ns

Note: Parameters are measured at 50% of the rising/falling edge.

System Architecture

Introduction

A device block diagram showing the signal paths present is provided. The HT82V42 samples a single channel input V_{IN}. The device then processes the sampled video signal with respect to the video reset level or an internally/externally generated reference level for signal processing. The processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and an 8-bit Programmable Gain Amplifier (PGA). The ADC then converts this analogue signal to a 16-bit digital word. The digital output from the ADC is presented on a 4-bit wide bus. On-chip control registers determine the configuration of the device, including the offsets and gains applied to R/G/B signal. These registers are programmable via a serial interface.

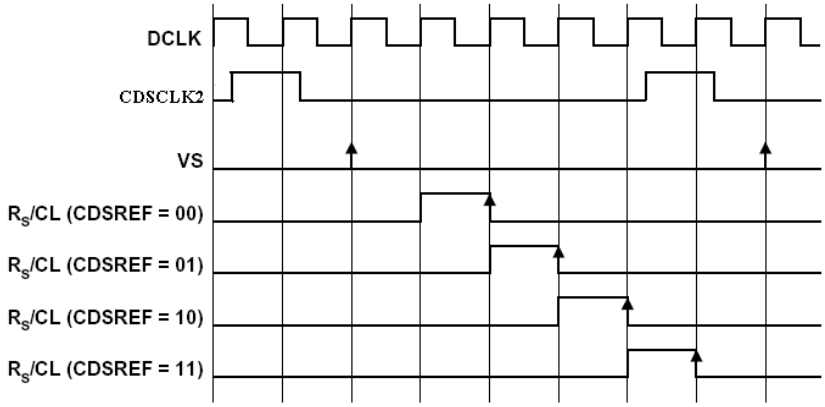
Input Sampling

The HT82V42 can sample and process the input analogue signals as follows:

- Monochrome
  A single chosen input VIN is sampled, processed by the corresponding channel, and converted by the ADC. The choice of input can be changed via the control interface, e.g. on a line-by-line basis if required.
- Colour Line-by-Line
  A single chosen input (Red, Green and Blue) is sampled and multiplexed into the analogue channel for processing before being converted by the ADC. The input selected can be switched in turn (Red → Green → Blue → Red …) together with the PGA and Offset DAC control registers by pulsing the RLC/ACYC pin. This is known as auto-cycling. Alternatively, other sampling sequences can be generated via the control registers. Refer to the Line-by-Line Operation section for more details.

Clamp Voltage

The device contains an integrated single 4-bit DAC which is controlled by register setting for the clamp voltage. The internal clamp is sampled on the positive edge of DCLK that occurs during each CDSCLK2 pulse. The sampled level, high (or low) controls the presence (or absence) of the internal CL pulse on the next reset level. The position of CL can be adjusted by using control bits CDSREF[1:0].



Reset Sample and Clamp Timing

CDS/CIS Processing

For CCD type input signals, the time at which the reset level is sampled, is adjustable by setting control bits CDSREF[1:0] as shown in the previous figure.

For CIS type input signals, non-CDS processing is used. During this case, the video level is processed with the voltage level on VRLC/VBIAS, the pin VRLC/VBIAS is generated internally or externally. The VRLC/VBIAS is sampled by Rs at the same time as Vs samples the video level in this mode.

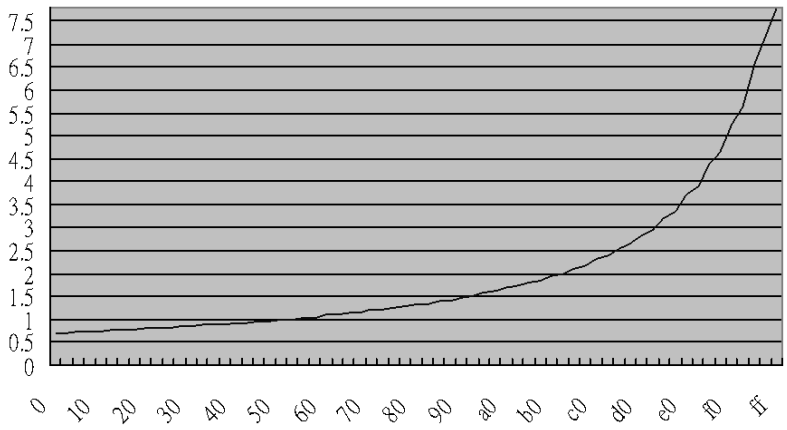
PGA Gain Registers

There are three PGA registers which are used to individually program the gain. Bits D7 through D0 control the gain range in 256 increments. See the figure for a graph of the PGA gain versus PGA register code. The coding for the PGA registers is a straight binary number, with all zero words corresponding to the minimum gain setting (0.68x) and all one words corresponding to the maximum gain setting (8x).

The PGA has a gain range from 0.68x (-3.3dB) to 8x (18dB), adjustable in 256 steps. The Figure shows the PGA gain as a function of the PGA register code. Although the gain curve is approximately linear in dB, the gain in V/V varies in nonlinear proportion with the register code, according to the following the equation:

Gain (V/V) = 186 / (278-PGA[7:0])

Gain (dB) = $20LOG_{10}$ (186/(278-PGA[7:0]))



PGA Gain Register Settings

D7	D6	D5	D4	D3	D2	D1	D0	Gain(V/V)	Gain (dB)
MSB							LSB		
0	0	0	0	0	0	0	0	0.68	-3.3
0	1	0	1	0	1	0	0	1	0*
1	1	0	0	0	0	0	0	2.23	7
1	1	1	0	0	0	0	0	3.50	10.8
1	1	1	1	1	1	1	1	8	18

Note: * Power-on default value

Offset Registers

There are three offset registers used to individually program the offset. Bits D7 through D0 control the offset range from -315mV to 315mV in 256 increments.

The Table shows the offset range as a function of the bits D7 through D0.

D7	D6	D5	D4	D3	D2	D1	D0	Offset (mV)
MSB							LSB	
0	0	0	0	0	0	0	0	-315
				:				:
1	0	0	0	0	0	0	0*	0
				:				:
1	1	1	1	1	1	1	1	+315

Note :*Power-on default value

Offset Register Settings

ADC Input Black Level Adjust

The output from the PGA should be offset to match the full-scale range of the ADC (VFS=2.0V). For negative-going input video signals, a black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS[1:0]=10. For positive going input signal the black level should be offset to the bottom of the ADC range by setting PGAFS[1:0]=11. Bipolar input video is accommodated by setting PGAFS[1:0]=00 or PGAFS[1:0]=01 (zero differential input voltage gives mid-range ADC output).

Overall Signal Flow Summary

The input sampling block produces an effective input voltage V1. For CDS, this is the difference between the input video level VIN and the input reset level VRESET. For non-CDS this is the difference between the input video level VIN and the voltage on the VRLC/VBIAS pin, VVRLC, optionally set via the RLC DAC.

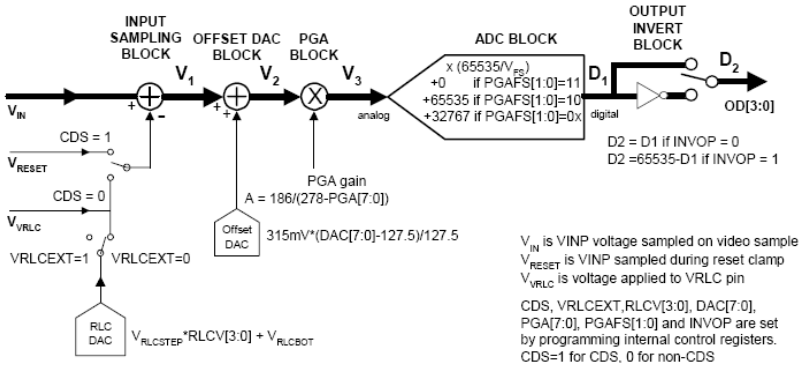
The offset DAC block then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing V2.

The PGA block then amplifies the white level of the input signal to maximise the ADC range, outputting voltage V3.

The ADC block then converts the analogue signal, V3, to a 16-bit unsigned digital output, D1. The digital output is then inverted, if required, through the output invert block to produce D2.

Calculating Output for any Given Input

The following equations describe the processing of the video and reset level signals through the HT82V42. The values of V1, V2 and V3 are often calculated in reverse order during device setup. The PGA value is written first to set the input Voltage range, the Offset DAC is then adjusted to compensate for any Black/Reset level offsets and finally the RLC DAC value is set to position the reset level correctly during operation.



Overall Signal Flow

Input Sampling Block: Input Sampling and Referencing

If CDS = 1, (i.e. CDS operation) the previously sampled reset level, VRESET, is subtracted from the input video.

V1 = VIN - VRESET.....Eqn. 1

If CDS = 0, (non-CDS operation) the simultaneously sampled voltage on pin VRLC is subtracted instead.

V1 = VIN - VVRLC.....Eqn. 2

If VRLCEXT = 1, VVRLC is an externally applied voltage on pin VRLC/VBIAS.

If VRLCEXT = 0, VVRLC is the output from the internal RLC DAC.

VVRLC = (VRLCSTEP × RLCV[3:0]) + VRLCBOT.....Eqn. 3

VRLCSTEP is the step size of the RLC DAC and VRLCBOT is the minimum output of the RLC DAC.

OFFSET DAC Block: OFFSET (BLACK - LEVEL) Adjust

The resultant signal V1 is added to the Offset DAC output.

V2 = V1 + { 315mV × (DAC[7:0] - 127.5) } / 127.5.....Eqn. 4

PGA NODE: GAIN Adjust

The signal is then multiplied by the PGA gain,

V3 = V2 × [186 / (278 - PGA[7:0])].....Eqn. 5

ADC Block: Analogue-Digital Conversion

The analogue signal is then converted to a 16-bit unsigned number, with input range configured by PGAFS[1:0].

D1[15:0] = INT{ (V3 /VFS) × 65535} + 32767 PGAFS[1:0] = 00 or 01.....Eqn. 6

D1[15:0] = INT{ (V3 /VFS) × 65535} PGAFS[1:0] = 11.....Eqn. 7

D1[15:0] = INT{ (V3 /VFS) × 65535} + 65535 PGAFS[1:0] = 10.....Eqn. 8

where the ADC full-scale range, VFS = 2.0V

if D1[15:0] < 0 D1[15:0] = 0

if D1[15:0] > 65535 D1[15:0] = 65535

Output Invert Block: Polarity Adjust

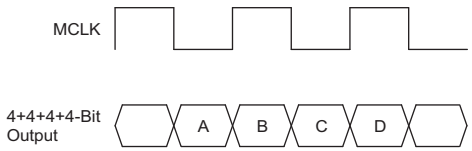
The polarity of the digital output may be inverted by control bit INVOP.

D2[15:0] = D1[15:0] (INVOP = 0).....Eqn. 9

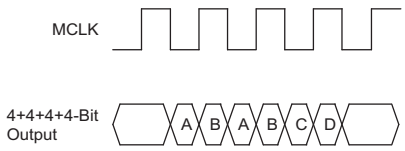
 D2[15:0] = 65535 - D1[15:0] (INVOP = 1).....Eqn. 10

Output Formats

Latency of valid output data with respect to CDSCLK2 is programmable by writing to control bits DEL[1:0]. The latency for each mode is shown in the Operating Mode Timing Diagrams section. Figure shows the output data formats for Modes 1, 3 and 4. Figure shows the output data formats for Mode 2. Table summarizes the output data obtained for each format.



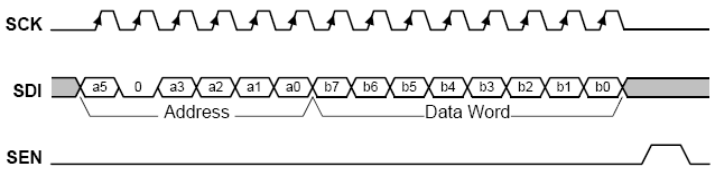
Output Data Formats (Mode 1, 3, 4)



Output Data Formats (Mode 2)

Output Format	Output Pins	Output
4+4+4+4-Bit (Nibble)	OD3~OD0	A= d15~d12 B= d11~d8 C= d7~d4 D= d3~d0

Details of Output Data



Serial Interface Register Write

Control Interface

The internal control registers are programmed via the serial digital control interface. The register contents can be read back via the serial interface on pin OD3/SDO. It is recommended that a software reset is carried out after the power-up sequence, before writing to any other register. This ensures that all registers are set to their default values

Serial Interface – Register Write

Figure shows the register writing in serial mode. Three pins, SCK, SDI and SEN are used. A six-bit address (a5, a4, a3, a2, a1, a0) is clocked in through SDI, MSB first, followed by an eight-bit data word (b7, b6, b5, b4, b3, b2, b1, b0), also MSB first. Each bit is latched on the rising edge of SCK. When the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register. Note all valid registers have address bit a4 equal to 0 in the write mode.

A software reset is carried out by writing to Address "000100" with any value of data, i.e. Data Word = XXXXXXXX.

Serial Interface – Register Read-back

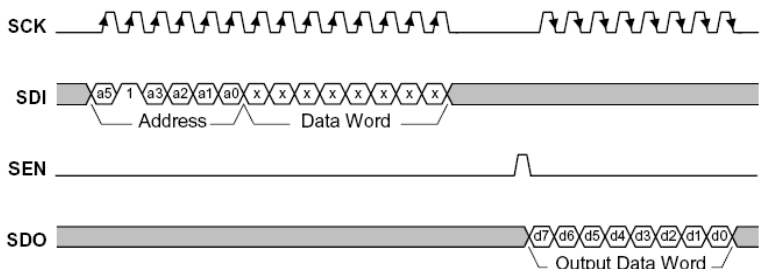
Figure shows register read-back in serial mode. Read-back is initiated by writing to the serial bus as described above but with address bit a4 set to 1, followed by an 8-bit dummy data word. Writing address (a5, 1, a3, a2, a1, a0) will cause the contents (d7, d6, d5, d4, d3, d2, d1, d0) of the corresponding register (a5, 0, a3, a2, a1, a0) to be output MSB first on pin SDO (on the falling edge of SCK). Note that pin SDO is shared with an output pin, OD3, therefore OEB should always be held low when register read-back data is expected on this pin. The next word may be read in to SDI while the previous word is still being output on SDO.

Timing Requirement

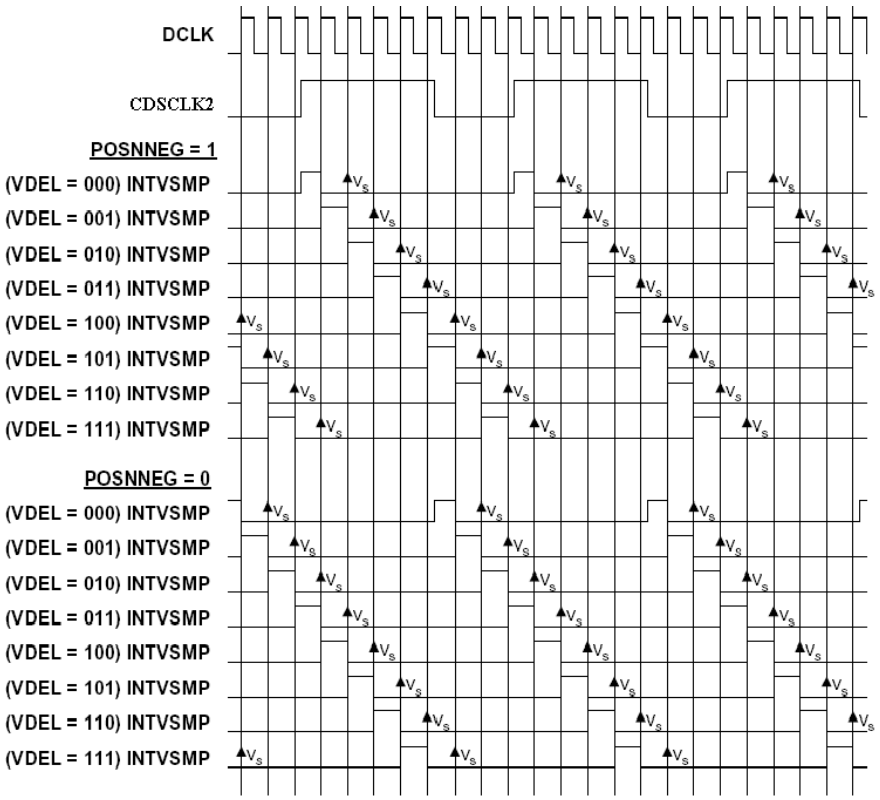
To use this device a master clock (DCLK) of up to 30MHz and a per-pixel synchronisation clock (CDSCLK2) of up to 15MHz are required. These clocks drive a timing control block, which produces internal signals to control the sampling of the video signal. The DCLK to CDSCLK2 ratios and maximum sample rates for the various modes are shown in Table.

Programmable CDSCLK2 Detect Circuit

The CDSCLK2 input is used to determine the sampling point and frequency of the HT82V42. Under normal operation a pulse of 1 DCLK period should be applied to CDSCLK2 at the desired sampling frequency (as shown in the Operating Mode Timing Diagrams) and the input sample will be taken on the first rising DCLK edge after CSDCLK2 has gone low. However, in certain applications such a signal may not be readily available. The programmable CDSCLK2 detect circuit in the HT82V42 allows the sampling point to be derived from any signal of the correct frequency, such as a CCD shift register clock, when applied to the CDSCLK2 pin. When enabled, by setting the VSMPDET control bit, the circuit detects either a rising or falling edge (determined by the POSNNEG control bit) on the CDSCLK2 input pin and generates an internal VSMP pulse. This pulse can optionally be delayed by a number of DCLK periods, specified by the VDEL[2:0] bits. Figure shows the internal VSMP pulses that can be generated by this circuit for a typical clock input signal. The internal VSMP pulse is then applied to the timing control block in place of the normal CDSCLK2 pulse provided from the input pin. The sampling point then occurs on the first rising DCLK edge after this internal VSMP pulse, as shown in the Operating Mode Timing Diagrams.



Serial Interface Register Read-back



Internal VSMP Pulse Generated by Programmable Internal Sample Detect Circuit

References

The ADC reference voltages are derived from an internal bandgap reference, and buffered to pins VRT and VRB, where they must be decoupled to ground. Pin VRX is driven by a similar buffer, and also requires decoupling. The output buffer from the RLCDAC also requires decoupling at pin VRLC/VBIAS.

Power Supply

The HT82V42 can run from a single 3.3V single supply.

Power Management

Power management for the device is performed via the Control Interface. The device can be powered on or off completely by clearing the EN bit low.

All the internal registers maintain their previously programmed value in the power down mode while the Serial Interface inputs remain active.

Line-by-Line Operation

Certain linear sensors (e.g. Contact Image Sensors) give a colour output on a line-by-line basis. i.e. a full line of red pixels followed by a line of green pixels followed by a line of blue pixels.

In this mode the input multiplexer and (optionally) the PGA/Offset register multiplexers can be auto-cycled by the application of pulses to the RLC/ACYC input pin by setting the ACYCNRLC register bit. See Figure for detailed timing information. The multiplexers change on the first DCLK rising edge after RLC/ACYC is taken high. A write to the auto-cycle reset register causes these multiplexers to be reset, selecting the colour R and the RED offset/gain registers. Alternatively, all three multiplexers can be controlled via the serial interface by writing to register bits INTM[1:0] to select the desired colour. It is also possible for the input multiplexer to be controlled separately from the PGA and Offset multiplexers. Table describes all the multiplexer selection modes that are possible.

ACYCNRLC	Name	Description
0	Internal no force mux	Input mux, offset and gain registers determined by internal register bits INTM1, INTM0.
1	Auto-cycling, no force mux	Input mux, offset and gain registers auto-cycled, RINP → GINP → BINP → RINP … on RLC/ACYC pulse.

Colour Selection Description in Line-by-Line Mode

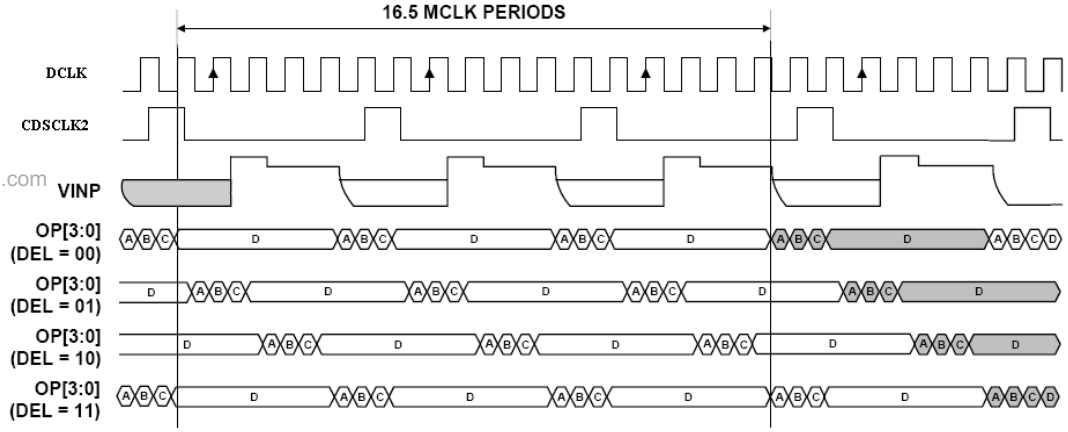
Operating Modes

Mode	Description	CDS	Max. Sample Rate	Sensor Interface Description	Timing Requirement	Register Contents With CDS	Register Contents Without CDS
1	Monochrome/Colour Line-by-Line	Yes	5 MSPS	Only one input channel at a time is continuously sampled.	DCLK = 30MHz DCLK: CDSCLK2 ratio is 6:1	SetReg1 : 3F(h)	SetReg1: 2D(h)
2	Fast Monochrome/ Colour Line-by-Line	Yes	10 MSPS	Identical to mode 1	DCLK = 30MHz DCLK: CDSCLK2 ratio is 3:1	Identical to mode 1 plus SetReg3: bits 5:4 must be set to 0 (h)	Identical to mode 1
3	Maximum speed Monochrome/Colour Line-by-Line	No	15 MSPS	Identical to mode 1	DCLK = 30MHz DCLK: CDSCLK2 ratio is 2:1	CDS not possible	SetReg1: 6D(h)
4	Slow Monochrome/ Colour Line-by-Line	Yes	3.75 MSPS	Identical to mode 1	DCLK = 30MHz DCLK: CDSCLK2 ratio is 2n:1, n>=4	Identical to mode 1	Identical to mode 1

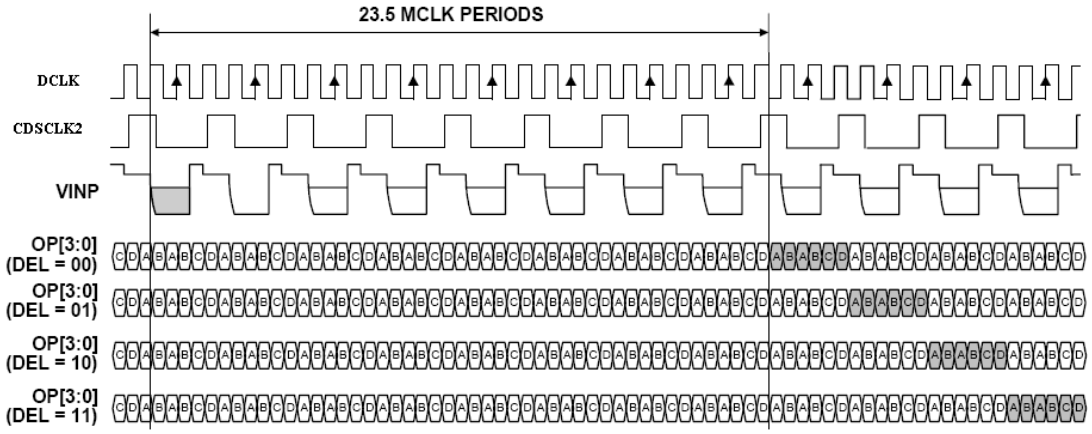
HT82V42 Operating Modes

Operating Mode Timing Diagrams

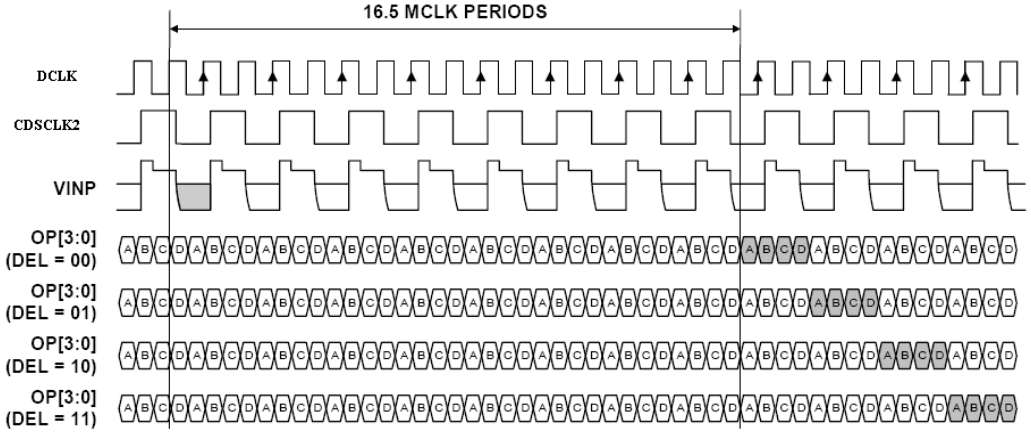
The following diagrams show 4-bit multiplexed output data and DCLK, CDSCLK2 and input video requirements for most common operations as shown in Table.



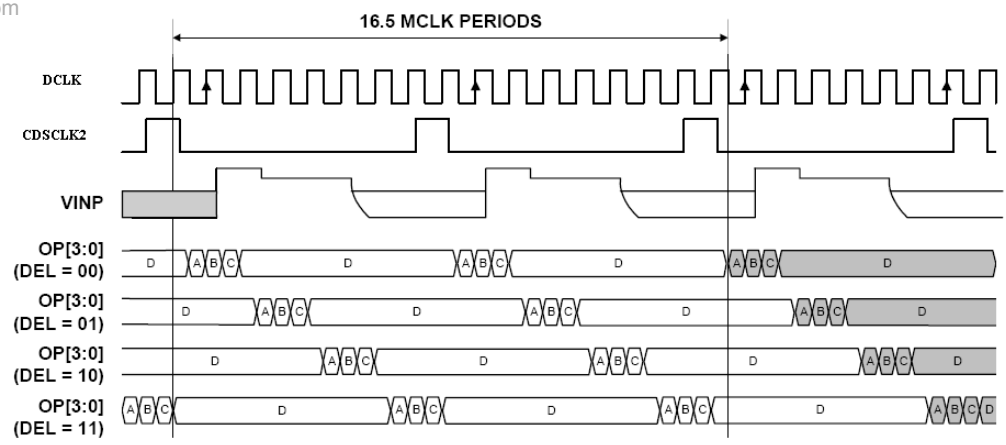
Mode 1 Operation



Mode 2 Operation



Mode 3 Operation



Mode 4 Operation

Device Configuration

- Register Map

  The following table describes the location of each control bit used to determine the device operation. The register map is programmed by writing the required codes to the appropriate address via the serial interface.

Address	Description	DEF (h)	R/W	Bit							
				7	6	5	4	3	2	1	0
000001	Setup Reg 1	0F	R/W	0	Mode3	PGAFS[1]	PGAFS[0]	1	1	CDS	EN
000010	Setup Reg 2	23	R/W	DEL[1]	DEL[0]	RLCDACRNG	0	VRLCEXT	INVOP	1	1
000011	Setup Reg 3	1F	R/W	0	0	CDSREF[1]	CDSREF[0]	RLVC[3]	RLVC[2]	RLVC[1]	RLVC[0]
000100	Software Reset	00	—	—	—	—	—	—	—	—	—
000101	Auto-cycle Reset	00	—	—	—	—	—	—	—	—	—
000110	Setup Reg 4	05	R/W	0	0	INTM[1]	INTM[0]	RLCINT	1	ACYCNRLC	LINEBYLINE
000111	Revision Number	41	R	—	—	—	—	—	—	—	—
001000	Setup Reg 5	00	R/W	0	0	0	PSENNEG	VDEL[2]	VDEL[1]	VDEL[0]	VSMPDET
001001	Setup Reg 6	00	R/W	ClkMotr	0	0	0	0	0	0	0
001010	Reserved	01	R	0	0	0	0	0	0	0	0
001011	Reserved	01	R	0	0	0	0	0	0	0	0
001100	Reserved	01	R	0	0	0	0	0	0	0	0
100000	Red Offset Value	80	R/W	RO[7]	RO[6]	RO[5]	RO[4]	RO[3]	RO[2]	RO[1]	RO[0]
100001	Green Offset Value	80	R/W	GO[7]	GO[6]	GO[5]	GO[4]	GO[3]	GO[2]	GO[1]	GO[0]
100010	Blue Offset Value	80	R/W	BO[7]	BO[6]	BO[5]	BO[4]	BO[3]	BO[2]	BO[1]	BO[0]
100011	RGB Offset Value	80	R/W	RGBO[7]	RGBO[6]	RGBO[5]	RGBO[4]	RGBO[3]	RGBO[2]	RGBO[1]	RGBO[0]
101000	Red PGA Gain	00	R/W	RPGA[7]	RPGA[6]	RPGA[5]	RPGA[4]	RPGA[3]	RPGA[2]	RPGA[1]	RPGA[0]
101001	Green PGA Gain	00	R/W	GPGA[7]	GPGA[6]	GPGA[5]	GPGA[4]	GPGA[3]	GPGA[2]	GPGA[1]	GPGA[0]
101010	Blue PGA Gain	00	R/W	BPGA[7]	BPGA[6]	BPGA[5]	BPGA[4]	BPGA[3]	BPGA[2]	BPGA[1]	BPGA[0]
101011	RGB PGA Gain	00	W	RGBPGA[7]	RGBPGA[6]	RGBPGA[5]	RGBPGA[4]	RGBPGA[3]	RGBPGA[2]	RGBPGA[1]	RGBPGA[0]

• Register Map Description

Register	Bit No.	Bit Name	POR	Description
Setup Register 1	0	EN	1	0: Complete power down 1: fully active
	1	CDS	1	Select correlated double sampling mode. 0: non-CDS mode 1: CDS mode
	2	Reserved	1	Default 1
	3	Reserved	1	Default 1
	5~4	PGAFS[1:0]	0	Adjust PGA output to optimize the ADC range for different polarity sensor output signals. Zero differential PGA input signal gives. 00: Zero output (use for bipolar video) 01: Zero output 10: Full-scale positive output (use for negative going video) 11: Full-scale negative output (use for positive going video)
	6	Mode3	0	Mode3 setting 1: Mode3 enable
Setup Register 2	2	INVOP	0	Digitally inverts the polarity of output data 0: negative going video gives negative going output 1: negative going video gives positive going output
	3	VRLCEXT	0	Setting this bit high, changes VRLC/VBIAS to Hi-Z, allowing VRLC/VBIAS to be driven from an external power source.
	5	RLCDACRNG	1	Sets the output range of the RLCDAC. 0: RLCDAC ranges from 0 to AVDD. 1: RLCDAC ranges from 0 to VRT
	7~6	DEL[1:0]	00	Sets the output latency for the ADC clock periods. 1 ADC clock=2 DCLK periods. Under mode3, 1 ADC clock=3 DCLK periods. 00: Minimum latency 01: Delay by 1 ADC clock 10: Delay by 2 ADC clock 11: Delay by 3 ADC clock
Setup Register 3	3~0	RLVC[3:0]	1111	Controls RLCDAC driving The VRLC pin defines the single ended signal reference voltage or Reset Level Clamp Voltage. Refer to the Electrical Characteristic section for details.
	5~	CDSREF[1:0]	01	Adjust reset timing under CDS mode 00: Advance 1 DCLK period 01: Normal 10: Retard 1 DCLK 11: Retard 2 DCLK
	7~6	Reserved	00	Reserved
Software Reset				Any write to this register will cause all functions to be reset. It is recommended to execute a software reset after each power on reset and before any other register writes. When this register is written, the reset function will be initiated immediately by an internal reset signal. If the DCLK exists, the internal reset signal will keep active for about 2 DCLK cycles. Otherwise, the device will keep in reset state all the time.

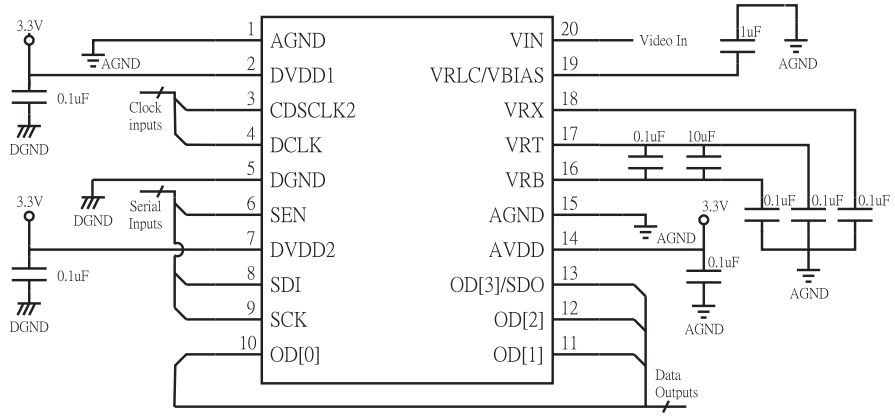
Register	Bit No.	Bit Name	POR	Description
Auto-cycle Reset				Writing to this register will cause the auto-cycle counter to be reset to colour R. This function is only required when LINEBYLINE=1. When this register is written, the reset function will be initiated immediately by an internal reset signal. If the DCLK exists, the internal reset signal will keep active for about 2 DCLK cycles. Otherwise, the device will keep in reset state all the time.
Setup Register 4	0	LINEBYLINE	1	Select line by line mode 0: normal operation 1: line by line operation
	1	ACYCNRLC	0	When LINEBYLINE=0, this bit has no effect When LINEBYLINE=1, this bit controls the function of the RLC/ACYC input signal and will control the multiplexer of the offset/gain register. 0: RLC/ACYC pin enabled for Reset Level Clamp, internal selection of input and offset/gain multiplexers. 1: Auto cycling enabled by pulsing the RLC/ACYC input pin.
	3	RLCINT	0	This bit is used to determine whether the Reset Level Clamping is used. 0: RLC disable 1: RLC enable
	5~4	INTM[1:0]	00	Colour selection bits used for internal modes. 00: Red 01: Green 10: Blue 11: Reserved
Setup Register 5	0	VSMPDET	0	0: Normal operation, signal on the CDSCLK2 input pin is applied directly to the Timing Control Block 1: Programmable CDSCLK2 detect circuit is enabled. An internal synchronization pulse is generated from the signal applied to the CDSCLK2 input pin and is applied to the Timing Control Block.
	3~1	VDEL[2:0]	000	When VSMPDEL=0, these bits have no effect. When VSMPDEL=1, these bits set the programmable delay from the detected edge of the signal on CDSCLK2. The internal generated pulse is delayed by VDEL DCLK periods from the detected edge.
	4	POSNNEG	0	When VSMPDEL=0, this bit has no effect When VSMPDEL=1, this bit controls whether positive or negative edges are detected. 0: Negative edge on the CDSCLK2 pin is detected and used to generate an internal timing pulse 1: Positive edge on the CDSCLK2 pin is detected and used to generate an internal timing pulse
Setup Register 6	7	ClkMotr	0	Internal clock monitor. 0: normal active, OD[3:0] output ADC data. 1: internal clock test mode.

Pin	ClkMotr=0	ClkMotr=1
OD3	OD3	INTVSMP
OD2	OD2	Video sample clock
OD1	OD1	ADC clock
OD0	OD0	Reset sample clock

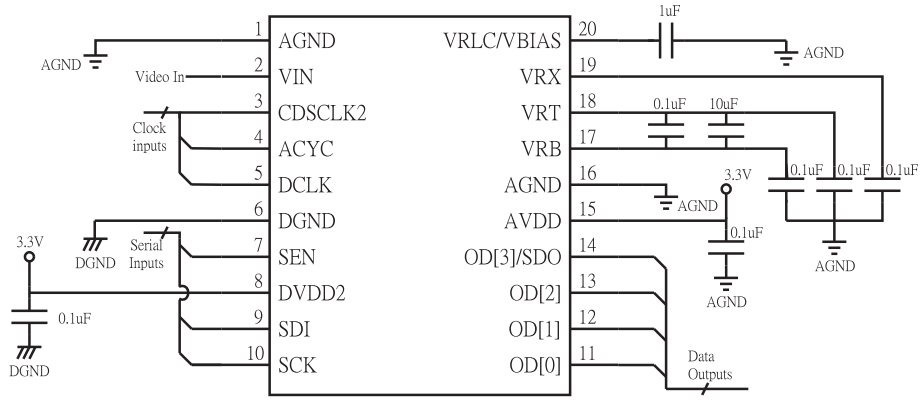
Register	Bit No.	Bit Name	POR	Description
Red Offset Value	7~0	RO	80	Red offset value
Green Offset Value	7~0	GO	80	Green offset value
Blue Offset Value	7~0	BO	80	Blue offset value
RGB Offset Value	7~0	RGBO	80	Writing to this register will overwrite the new value to the R/G/B Offset value
Red PGA gain	5~0	RPGA	0	Red PGA value
Green PGA gain	5~0	GPGA	0	Green PGA value
Blue PGA gain	5~0	BPGA	0	Blue PGA value
RGB PGA gain	5~0	RGBPGA	0	Writing to this register will overwrite the new value to the R/G/B PGA gain value

Application Circuits

Recommended External Components



HT82V42 SSOP-20



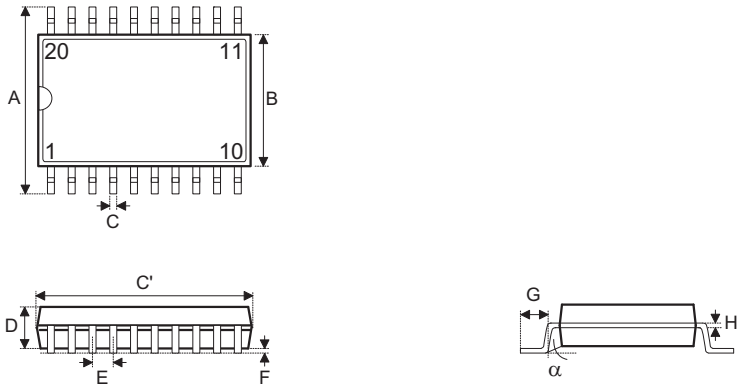
HT82V42 TSSOP-20

Note: 1. All capacitors should be located as close to the HT82V42 as possible.

2. AGND and DGND should be connected as close to the HT82V42 as possible.

Package Information

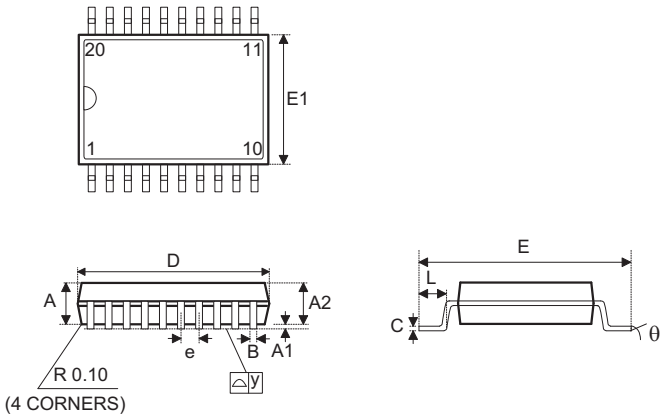
20-pin SSOP (209mil) Outline Dimensions



• MO-150

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	7.40	—	8.20
B	5.00	—	5.60
C	0.22	—	0.33
C′	6.90	—	7.50
D	—		2.00
E	—	0.65	—
F	0.05	—	—
G	0.55	—	0.95
H	0.09	—	0.21
α	0°	—	8°

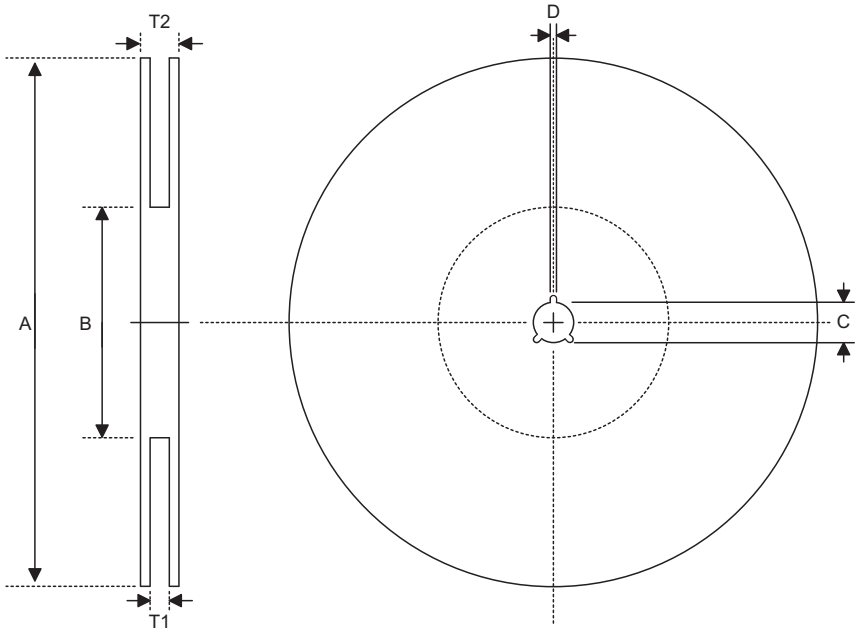
20-pin TSSOP Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	1.05	—	1.2
A1	0.05	—	0.15
A2	0.95	—	1.05
B	—	0.22	—
C	0.13	—	0.17
D	6.4	—	6.6
E	6.3	—	6.5
E1	4.3	—	4.5
e	—	0.65	—
L	0.45	—	0.75
y	—	—	0.1
θ	0°	—	8°

Product Tape and Reel Specifications

Reel Dimensions



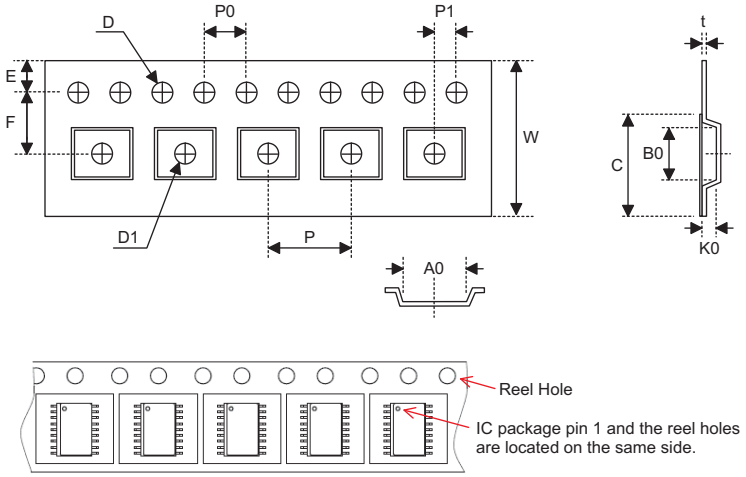
SSOP 20N (209mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	16.8 $^{+0.3/-0.2}$
T2	Reel Thickness	22.2±0.2

TSSOP 20L

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	16.4 $^{+0.3/-0.2}$
T2	Reel Thickness	19.1 max.

Carrier Tape Dimensions



SSOP 20N (209mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0 +0.3/-0.1
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	1.5 +0.1/-0.0
D1	Cavity Hole Diameter	1.50 +0.25/-0.00
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	7.1±0.1
B0	Cavity Width	7.2±0.1
K0	Cavity Depth	2.0±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	13.3±0.1

TSSOP 20L

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0±0.3
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	1.5 +0.1/-0.0
D1	Cavity Hole Diameter	1.5 +0.1/-0.0
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.8±0.1
B0	Cavity Width	6.9±0.1
K0	Cavity Depth	1.6±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	13.3±0.1

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