Features

- 3.3V operating voltage
- Up to 240MSPS for two 6-channel inputs
- Programmable CIS module timing generator
- Image sensor shading correction
  - 0 ~ -255 8-bit dark shading (offset) correction
  - 0.00x~8.00x 10-bit white shading (gain) correction
  - Embedded memory for up to 6 component coefficients of 1584 sensor elements
- Flexible frame start/stop control mechanism
- Provide Image line information
  - line index
  - Left and right boundary of a line
  - max/min/summation/histogram information of a line
- 8/16-bit image data output in VPFE or EMIF interface
- 3-wire/4-wire SPI interface
- 2-wire I^{2}C interface
- Built in voltage comparator for roller input signal
- 100-pin LQFP package

Applications

- Double-sided scanner currency detectors

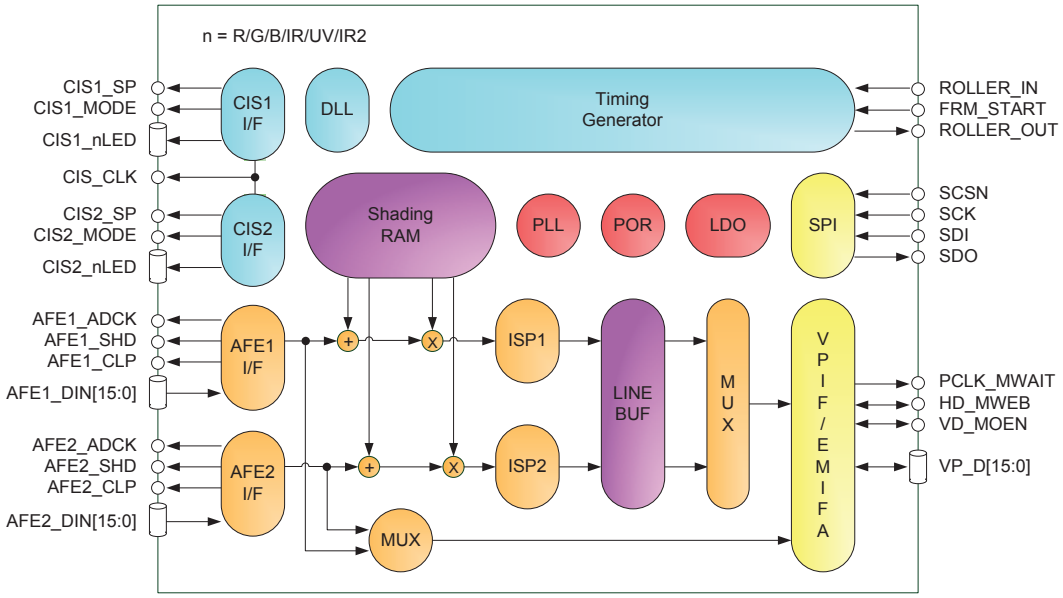
General Description

The HT82V70 is a fully integrated device for CIS imaging application. It features programmable timing generator and image sensor shading correction to sample and condition the outputs of CIS (Contact Image Sensor) arrays for high-speed double-sided scanner applications.

With up to two AFE HT82V48 ICs, it can support two 3~6-channel inputs up to 240MSPS. Intelligent image sensor shading correction is then employed on each sensor element. The sensor data can be not only corrected but also averaged per line for black level calculations. The Video Processing Front End (VPFE) Interface multiplexed shaded ADC's outputs two high-bytes for each ADC's output or one 16-bit wide output for each ADC. A pixel clock PCLK transports the 16-bit wide data to the output port.

The internal registers are programmed through a 2-wire I^{2}C or 3-wire/4-wire SPI interface, for timing control, gain, offset and operating mode adjustments.

Block Diagram



System Application Diagram

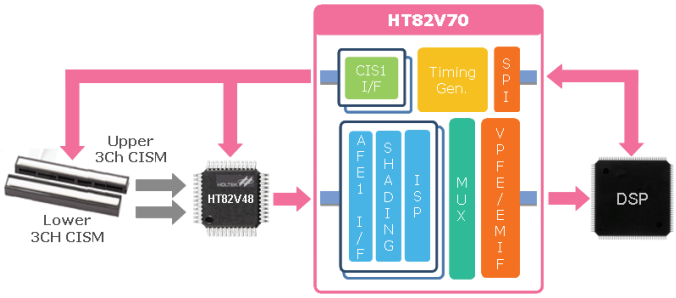


Figure 1. Two 3-ch CISMs System Diagram

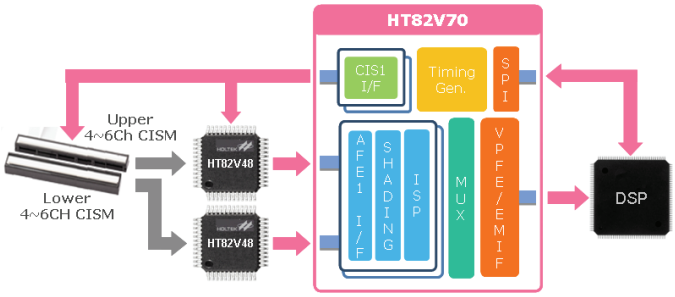
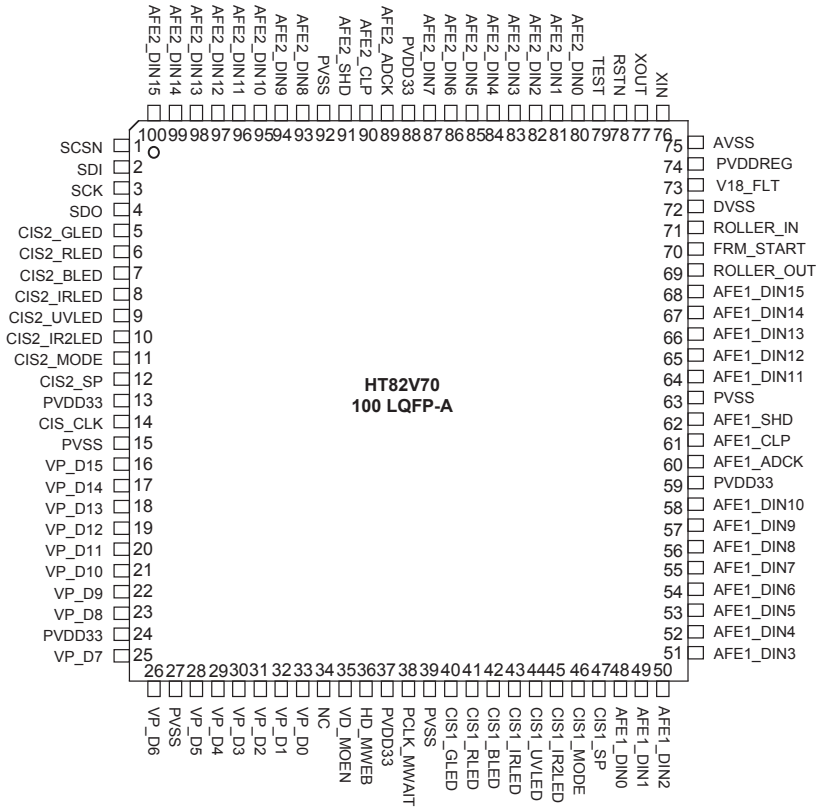


Figure 2. Two 6-ch CISMs System Diagram

Pin Assignment



Pin Description

Pin				100 pin	Description
Name	DIR	TYP	DRV		
SCSN	DI	U	—	1	SPI Chip Select, Active Low
SDI	DIO	U	8	2	3-wire SPI Serial Data I/O or 4-wire SPI Serial Data input
SCK	DI	U	—	3	SPI Serial Clock
SDO	DO	C	8	4	4-wire SPI Serial Data Output
CIS2_GLED	DO	T	8	5	2nd CIS Module Green LED Active Slot Control
CIS2_RLED	DO	T	8	6	2nd CIS Module Red LED Active Slot Control
CIS2_BLED	DO	T	8	7	2nd CIS Module Blue LED Active Slot Control
CIS2_IRLED	DO	T	8	8	2nd CIS Module IR LED Active Slot Control
CIS2_UVLED	DO	T	8	9	2nd CIS Module UV LED Active Slot Control
CIS2_IR2LED	DO	T	8	10	2nd CIS Module IR2 LED Active Slot Control
CIS2_MODE	DO	T	4	11	2nd CIS Mode Select
CIS2_SP	DO	T	8	12	2nd CIS Module Start Pulse
PVDD	P	—	—	13	Pad Power Pin
CIS_CLK	DO	C	8	14	CIS Module Pixel Clock
PVSS	P	—	—	15	Pad Ground Pin
VP_D15	DIO	U	4	16	VPFE Pixel Data Output 15, or EMIFA Data 15 In/Out
VP_D14	DIO	U	4	17	VPFE Pixel Data Output 14, or EMIFA Data 14 In/Out
VP_D13	DIO	U	4	18	VPFE Pixel Data Output 13, or EMIFA Data 13 In/Out
VP_D12	DIO	U	4	19	VPFE Pixel Data Output 12, or EMIFA Data 12 In/Out
VP_D11	DIO	U	4	20	VPFE Pixel Data Output 11, or EMIFA Data 11 In/Out
VP_D10	DIO	U	4	21	VPFE Pixel Data Output 10, or EMIFA Data 10 In/Out
VP_D9	DIO	U	4	22	VPFE Pixel Data Output 9, or EMIFA Data 9 In/Out
VP_D8	DIO	U	4	23	VPFE Pixel Data Output 8, or EMIFA Data 8 In/Out
PVDD	P	—	—	24	Pad Power Pin
VP_D7	DIO	U	4	25	VPFE Pixel Data Output 7, or EMIFA Data 7 In/Out
VP_D6	DIO	U	4	26	VPFE Pixel Data Output 6, or EMIFA Data 6 In/Out
PVSS	P	—	—	27	Pad Ground Pin
VP_D5	DIO	U	4	28	VPFE Pixel Data Output 5, or EMIFA Data 5 In/Out
VP_D4	DIO	U	4	29	VPFE Pixel Data Output 4, or EMIFA Data 4 In/Out
VP_D3	DIO	U	4	30	VPFE Pixel Data Output 3, or EMIFA Data 3 In/Out
VP_D2	DIO	U	4	31	VPFE Pixel Data Output 2, or EMIFA Data 2 In/Out
VP_D1	DIO	U	4	32	VPFE Pixel Data Output 1, or EMIFA Data 1 In/Out
VP_D0	DIO	U	4	33	VPFE Pixel Data Output 0, or EMIFA Data 0 In/Out
NC	—	—	—	34	Not connected
VD_MOEN	DIO	U	4	35	VPFE VD output , Active High or EMIFA OE# input, Active Low
HD_MWEN	DIO	U	4	36	VPFE HD output , Active High or EMIFA WE# input, Active Low
PVDD	P	—	—	37	Pad Power Pin
PCLK_MWAIT	DO	C	12	38	VPFE Pixel Clock output or EMIFA WAIT output, Active High
PVSS	P	—	—	39	Pad Ground Pin
CIS1_GLED	DIO	T,D	8	40	CIS Module Green LED Active Slot Control
CIS1_RLED	DIO	T,D	8	41	CIS Module Red LED Active Slot Control
CIS1_BLED	DIO	T,D	8	42	CIS Module Blue LED Active Slot Control
CIS1_IRLED	DO	T	8	43	CIS Module IR LED Active Slot Control

Pin				100 pin	Description
Name	DIR	TYP	DRV		
CIS1_UVLED	DO	T	8	44	CIS Module UV LED Active Slot Control
CIS1_IR2LED	DO	T	8	45	CIS Module IR2 LED Active Slot Control
CIS1_MODE	DO	C	4	46	CIS Mode Select
CIS1_SP	DO	C	8	47	CIS Module Start Pulse
AFE1_DIN0	DI	U	—	48	AFE_DIN0 from external 1ST AFE
AFE1_DIN1	DI	U	—	49	AFE_DIN1 from external 1ST AFE
AFE1_DIN2	DI	U	—	50	AFE_DIN2 from external 1ST AFE
AFE1_DIN3	DI	U	—	51	AFE_DIN3 from external 1ST AFE
AFE1_DIN4	DI	U	—	52	AFE_DIN4 from external 1ST AFE
AFE1_DIN5	DI	U	—	53	AFE_DIN5 from external 1ST AFE
AFE1_DIN6	DI	U	—	54	AFE_DIN6 from external 1ST AFE
AFE1_DIN7	DI	U	—	55	AFE_DIN7 from external 1ST AFE
AFE1_DIN8	DI	U	—	56	AFE_DIN8 from external 1ST AFE
AFE1_DIN9	DI	U	—	57	AFE_DIN9 from external 1ST AFE
AFE1_DIN10	DI	U	—	58	AFE_DIN10 from external 1ST AFE
PVDD	P	—	—	59	Pad Power Pin
AFE1_ADCK	DO	C	8	60	AFE ADCK Output to 1ST AFE
AFE1_CLP	DO	C	8	61	AFE Clamp Output to 1ST AFE
AFE1_SHD	DO	C	8	62	AFE SHD Output to 1ST AFE
PVSS	P	—	—	63	Pad Ground Pin
AFE1_DIN11	DI	U	—	64	AFE_DIN11 from external 1ST AFE
AFE1_DIN12	DI	U	—	65	AFE_DIN12 from external 1ST AFE
AFE1_DIN13	DI	U	—	66	AFE_DIN13 from external 1ST AFE
AFE1_DIN14	DI	U	—	67	AFE_DIN14 from external 1ST AFE
AFE1_DIN15	DI	U	—	68	AFE_DIN15 from external 1ST AFE
ROLLER_OUT	DO	T	8	69	Roller Square Wave Output
FRM_START	DI	U	—	70	Frame Start Input
ROLLER_IN	DI	U	—	71	Roller Input, Sine wave
DVSS	P	—	—	72	Digital Ground Pin
V18_FLT	P	—	—	73	1.8V LDO Filter
PVDDREG	P	—	—	74	Regulator Power 3.3V Pin
AVSS	P	—	—	75	Regulator Ground Pin
XIN	AI	—	—	76	Crystal Oscillator Input
XOUT	AO	—	—	77	Crystal Oscillator Output
RSTN	DI	S,U	—	78	System Reset, Active Low
TEST	DI	D	—	79	TEST mode pin
AFE2_DIN0	DI	U	—	80	AFE_DIN0 from external 2nd AFE
AFE2_DIN1	DI	U	—	81	AFE_DIN1 from external 2nd AFE
AFE2_DIN2	DI	U	—	82	AFE_DIN2 from external 2nd AFE
AFE2_DIN3	DI	U	—	83	AFE_DIN3 from external 2nd AFE
AFE2_DIN4	DI	U	—	84	AFE_DIN4 from external 2nd AFE
AFE2_DIN5	DI	U	—	85	AFE_DIN5 from external 2nd AFE
AFE2_DIN6	DI	U	—	86	AFE_DIN6 from external 2nd AFE
AFE2_DIN7	DI	U	—	87	AFE_DIN7 from external 2nd AFE
PVDD	P	—	—	88	Pad Power Pin
AFE2_ADCK	DO	T	8	89	AFE ADCK Output to 2nd AFE
AFE2_CLP	DO	T	8	90	AFE Clamp Output to 2nd AFE
AFE2_SHD	DO	T	8	91	AFE SHD Output to 2nd AFE

Pin				100 pin	Description
Name	DIR	TYP	DRV		
PVSS	P	—	—	92	Pad Ground Pin
AFE2_DIN8	DI	U	—	93	AFE_DIN8 from external 2nd AFE
AFE2_DIN9	DI	U	—	94	AFE_DIN9 from external 2nd AFE
AFE2_DIN10	DI	U	—	95	AFE_DIN10 from external 2nd AFE
AFE2_DIN11	DI	U	—	96	AFE_DIN11 from external 2nd AFE
AFE2_DIN12	DI	U	—	97	AFE_DIN12 from external 2nd AFE
AFE2_DIN13	DI	U	—	98	AFE_DIN13 from external 2nd AFE
AFE2_DIN14	DI	U	—	99	AFE_DIN14 from external 2nd AFE
AFE2_DIN15	DI	U	—	100	AFE_DIN15 from external 2nd AFE

DIR: AI=Analog input; AO=Analog output; AIO=Analog in/out; DI=Digital input; DO=Digital output; DIO=Digital in/out; P=Power

TYP: T=Tri-state; OD=Open-Drain; S=Schmitt trigger; C: Common; U=Pull-up 75kΩ resistance; D=Pull-down 75kΩ resistance

DRV: Pin driving current, unit: mA.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+4.3V
Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V
Analogue Supply Power .....3.0V~3.6V
Storage Temperature ..... -55°C to 125°C
Operating Temperature .....0°C to 70°C
Digital supply power ..... 3.0V~3.6V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply						
DV_{DD}	Digital Supply Power	—	3.0	3.3	3.6	V
Digital Inputs						
V_{IH}	High level input voltage	—	2.0	—	—	V
V_{IL}	Low level input voltage	—	—	—	0.8	V
V_{SIH}	Schmitt Trigger high level input voltage	—	—	1.6	2.0	V
V_{SIL}	Schmitt Trigger low level input voltage	—	0.8	1.1	—	V
R_I	Input pull-up/pull-down resistance	V_{IL} = 0V or V_{IH} = V_{DD}	—	75	—	KΩ
Digital Outputs						
V_{OH}	High level output voltage	—	2.4	—	—	V
V_{OL}	Low level output voltage	—	—	—	0.4	V

A.C. Characteristics

DV_{DD} = 3.3V, DV_{SS} = 0V, Ta = 25°C, Crystal = 12MHz unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Low-dropout Regulator						
V_{IN}	Input voltage	—	—	3.3	—	V
V_{OUT}	Output voltage	—	—	1.8	—	V
Supply Currents						
I_{OUT}	Total supply current	—	—	150	—	mA

Timing Specification

DV_{DD} = 3.3V, DV_{SS} = 0V, Ta = 25°C, Crystal = 12MHz unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Clock Parameter						
f_{XTAL}	Crystal input	—	—	12	—	MHz
$XTAL_{ACC}$	Crystal accuracy	—	—	500	—	ppm
f_{ISP_CLK}	ISP clock frequency	—	—	144	—	MHz
Reset						
t_{RST}	Reset active time	—	—	1	—	ms
Serial Control Interface						
f_{SCK}	Serial input clock frequency	—	—	1M	2M	MHz
t_{CSU}	SCSN falling to SCK rising edge	—	200	—	—	ns
t_{CHO}	SCK falling to SCSN rising edge	—	200	—	—	ns
t_{IS}	Input setup time	—	200	—	—	ns
t_{IH}	Input hold time	—	200	—	—	ns
t_{DL}	SCK falling edge to SDO transition	—	—	—	300	ns
EMIF Output Interface						
t_{VD_MOEN}	VD_MOEN low time	—	50	—	—	ns
TG Output Interface						
f_{AFE1_ADCK}	AFE1_ ADC pixel clock	—	—	48	—	MHz
f_{AFE2_ADCK}	AFE2_ ADC pixel clock	—	—	48	—	MHz
f_{CIS_CLK}	CIS Module pixel clock	—	—	16	—	MHz
t_{CIS_SP}	CIS_SP pulse width	—	1	—	—	t_{CIS_CLK}
VPFE Data Output						
f_{PCLK}	VPFE pixel clock output	—	—	—	144	MHz

Notes: 1. Parameters are measured at the 50% point of the rising/falling edge.

2. $t_{CIS\_CLK} = 1/f_{CIS\_CLK}$

Function Description

Introduction

The HT82V70 is a fully integrated chip for CIS imaging application. It features a programmable timing generator and image sensor shading correction to sample and condition the CIS – Contact Image Sensor - array for high-speed double-sided scanner applications.

With up to two AFE HT82V48 ICs, it can support two 3~6-channel inputs up to 240MSPS. An intelligent image sensor shading correction is employed to unitise each sensor element. The sensor data can be not only corrected but also averaged per line for black level calculation. A Video Processing Front End – VPFE - Interface multiplexed shaded ADCs outputs in two high-bytes for each ADC's output or one 16-bit wide output for each ADC. A pixel clock PCLK transports the 16-bit wide data to the output port.

The internal registers are programmed through 2-wire I^2C 3-wire/4-wire SPI interface for timing control, gain, offset and operating mode adjustments.

Power-On-Reset – POR

The POR circuit is powered by DV_{DD} and used to reset the digital logic into a default state after power-up. The POR is active from $0.6V_{Typ.}$ of DV_{DD} and released at $1.2V_{Typ.}$ of DV_{DD}. When DV_{DD} returns back to $0.6V_{Typ.}$ the POR will be actived again. To ensure the contents of the control registers are at their default values before carrying out any other register writes it is recommended to execute a software reset each time the power is cycled.

Power Management

When the device default is fully enabled, the register bit PDNB allows the device to be fully powered down when set low. Individual blocks can be powered down using the bits in the System Setup Register 1.

Serial Interface for Register Configuration

3-wire SPI

A serial interface is used to write and read the configuration registers. The interface is a three wire interface using SCK, SCSN, SDIO, where SDIO is bi-directional.

To write to registers, the conditions in the timing diagram shown in Figure 3 must be met. First SCSN is toggled low. At the rising edge of the first clock period, the master should assume control of the SDIO pin and begin issuing the new command. Data is clocked into the HT82V70 on the rising edge of SCK through the SDIO pin. The complete 16 bits are composed of a "write" command bit (a zero), a five bit register address, two zero bits and the eight bit register value to be written. When SCSN toggles high, the register is written to, and the device now functions with this new data.

To read registers, the conditions in the timing diagram shown in Figure 3 must be met. First SCSN is toggled low. At the rising edge of the first clock period, the master should assume control of the SDIO pin and begin issuing the new command. Data is clocked into the HT82V70 on the rising edge of SCK through the SDIO pin. The complete 8 bits are composed of the "read" command bit (a one), a five bit register address and two zero bits. The eight bits of data are clocked out of the device on the falling edge of the ninth clock period SCK to the sixteenth through the SDIO pin.

4-wire SPI

The difference between the 4-wire SPI and 3-wire SPI is due to separate data pins. The 4-wire SPI has separate pins for input and output data, making it full-duplex.

The default setting is for the 3-wire SPI interface. Set register P0_19[5] can change the SPI from 3-wire to 4-wire. For the 4-wire SPI mode, the input data pin is the SDIO pin and the output data pin is the ROLLER_OUT pin.

To write to the registers, the conditions in the timing diagram shown in Figure 5 must be met. First SCSN is toggled low. At the rising edge of the first clock period, the master should assume control of the SDIO pin and begin issuing the new command. SDIO is clocked into the HT82V70 on the rising edge of SCK. The complete 16 bits are composed of the "write" command bit (a zero), a five bit register address, two zero bits and the eight bit register value to be written. When SCSN toggles high, the register is written to, and the HT82V70 now functions with this new data.

To read the registers, the conditions in the timing diagram shown in Figure 5 must be met. First SCSN is toggled low. On the rising edge of the first clock period, the master should assume control of the SDI pin and begin issuing the new command. SDIO is clocked into the HT82V70 at the rising edge of SCK. The complete 8 bits are composed of the "read" command bit (a one), a five bit register address and the two zero bits to be written. The eight bits of data are clocked out on the ROLLER_OUT pin on the falling edge of the ninth clock period SCK to the sixteenth.

I^2C

The device also supports register programming through the I^2C interface. The clock pin is SCK and the data pin is SDIO.

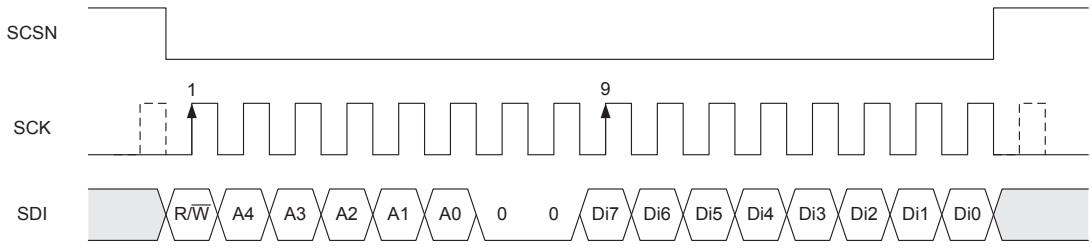


Figure 1. 3-wire serial write

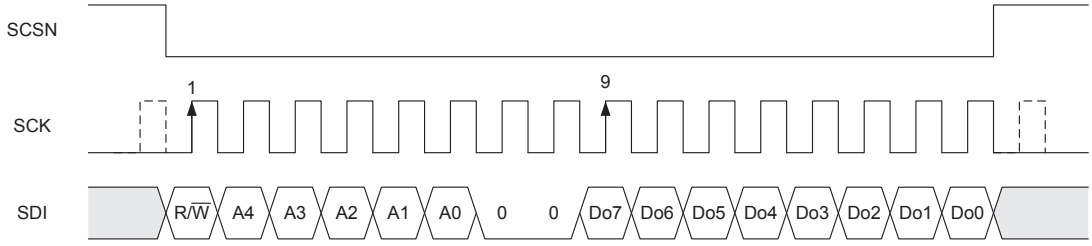


Figure 2. 3-wire serial read

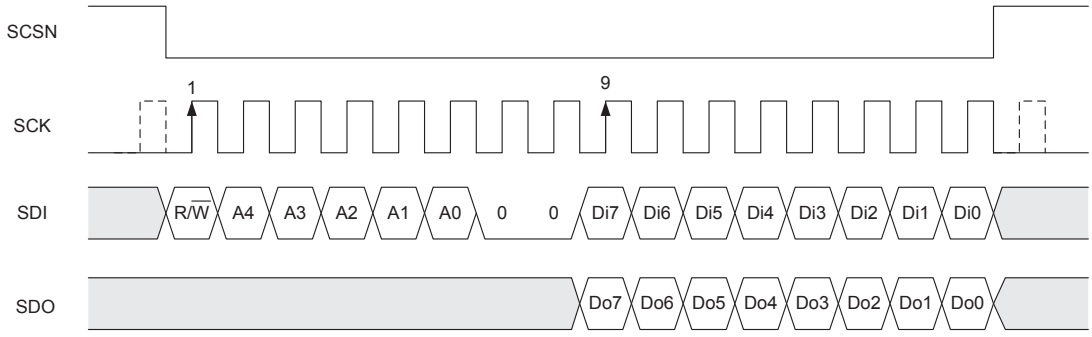


Figure 3. 4-wire serial write/read

Timing Generator

This is a programmable 96-step precision timing generator, embedded with a DLL to execute timing fine tuning and generate signals for internal AFE sampling. The timing generator can also provide the CIS sensor related control timing. The device supports up to 5 lamps,

CIS1_RLED, CIS1_GLED, CIS1_BLED, CIS1_IRLED, and CIS1_UVLED. The on and off points are individually programmed for each LED output. The LEDs can be on simultaneously if desired and permitted by the CIS and system design.

Auto Dark & White Correction

The device provides hardware shading correction. The shading correction includes dark and white correction and up to 1584 elements with 6 independent coefficients for different colour LED lights. There is an embedded memory for coefficient storage which is pre-loaded by the SPI or EMIF interfaces. The shading correction formula is as follows, New Element (n) = (Element (n) + Offset (n)) × Gain (n), where Offset is 8-bit from 0 to -255, Gain is 10-bits from 0.00x ~ 8.00x and n is the number of sensor elements.

Video Output Interface

The device supports two kind of video output Interfaces. One is the Asynchronous External Memory Interface (EMIF) and the other is Video Processing Front End (VPFE). Both of them are the most commonly used interfaces for the Texas Instruments CPU, such as the TMS320DM64xx series. Users can easily connect the HT82V70 to the back-end CPU for further signal processing through one of the two interfaces.

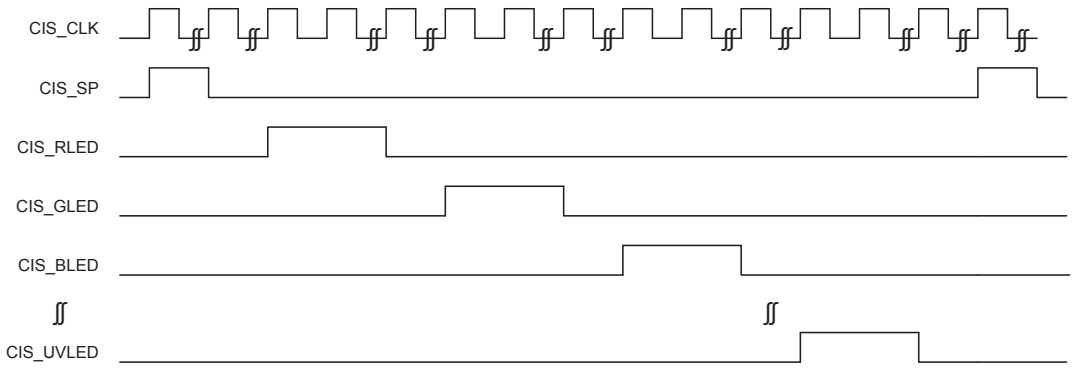


Figure 4. CIS output

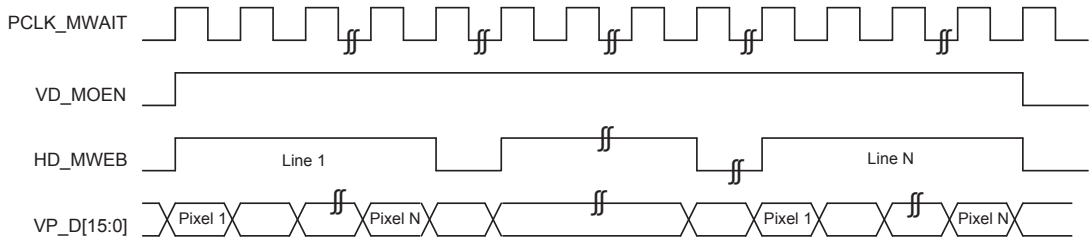


Figure 5. VPFE Output Sync Valid Mode

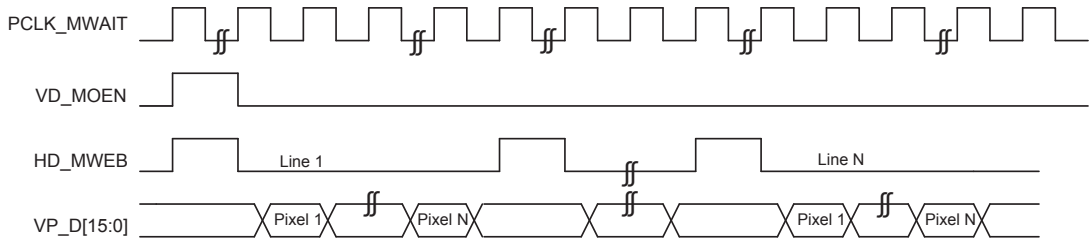


Figure 6. VPFE Output Sync Mode

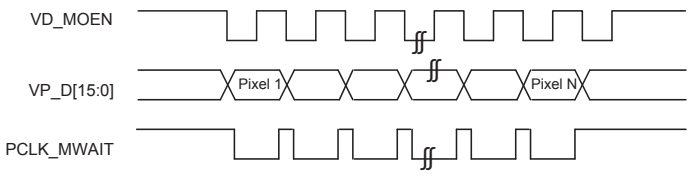


Figure 7. EMIF Output

Line Information

The device provides 80 bytes of line information for further signal processing. This includes maximum, minimum, summation, and line Histogram. It also includes line index and roller information which is often used in computing the roller speed. A left and right boundary is provided which is necessity information when implementing image slant correction.

Voltage Comparator

A voltage comparator is included in the HT82V70. The comparator deals with an analog roller signal and converts it into a digital signal for internal use or outputs it onto the ROLLER_OUT pin for external usage. The reference voltage to be compared is programmed using a 5 bit register.

Frame Start mechanism

A mechanism to control the image scan procedure is provided in the device. Users can choose a suitable control mechanism between frames (Images) either from the FRM_START pin or by setting the register to start a frame based on the system requirements.

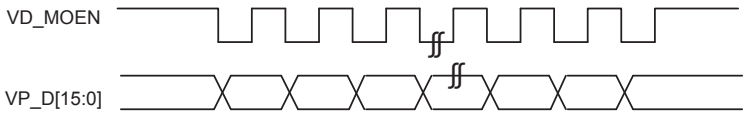


Figure 8. EMIF Read

Control Registers

Register Mapping

Address	Mode	Description	Default
Page 0	**System Setup Registers: Page Register 1Fh = 00h**		
01h	R/W	Software Reset Register	00h
02h	R/W	Mode Setting Register	00h
03h	R/W	Pixel Clock Configuration Register 0	00h
04h	R/W	Pixel Clock Configuration Register 1	00h
05h	R/W	ADC Clock Configuration Register 0	00h
06h	R/W	ADC Clock Configuration Register 1	00h
07h	R/W	VPFE Clock Configuration Register 0	00h
08h	R/W	VPFE Clock Configuration Register 1	00h
09h	R/W	ISP Clock Configuration Register 0	00h
0Ah	R/W	ISP Clock Configuration Register 1	00h
0Bh	R/W	ARM Clock Configuration Register 0	50h
0Ch	R/W	ARM Clock Configuration Register 1	01h
	—		
0Eh	R/W	PLL1 M/N value Register	80h
0Fh	R/W	PLL Control Register	C3h
10h	R/W	Data Path Control Register 0	98h
11h	R/W	Data Path Control Register 1	70h
12h	R/W	Data Path Control Register 2	01h
13h	R/W	Frame Wait Counter MSB Register	00h
14h	R/W	Frame Wait Counter LSB Register	00h
15h	R/W	AFE Output Ctrl Signals Strength Register	55h
16h	R/W	VPFE/EMIF Output Ctrl Signals Strength Register	02h
17h	R/W	Video Port PAD Delay Control Register	00h
18h	R/W	Misc Control Register 0	04h
19h	R/W	Misc Control Register 1	8Fh
1Ah	R/W	Wheel Comparator Control Register	6Fh
1Bh	RO	Pin and Pwr-On-Strapped Status Register	—
1Ch	R/W	Debug Control Register 0	00h
1Dh	R/W	Debug Control Register 1	00h
1Eh	RO	Data Bus Debug Error Status Register	—
1Fh	R/W	Page Register	00h
Page 1	**AFE Control Registers: Page Register 1Fh = 01h**		
		Reserved	
Page 2	**TG Control Registers: Page Register 1Fh = 02h**		
00h	R/W	TG Main Configuration Register 0	11h
01h	R/W	TG Main Configuration Register 1	22h
02h	R/W	TG Control Register 0	01h
03h	R/W	TG Control Register 1	00h
04h	R/W	TG Control Register 2	10h
05h	R/W	TG CIS_CLK/AFE_CLK Control Register	45h
06h	R/W	TG CIS_CLK Start Register	00h
07h	R/W	TG CIS_CLK End Register	40h
08h	R/W	TG AFE1_SHD Start Register	40h

Address	Mode	Description	Default
09h	R/W	TG AFE1_SHD End Register	60h
0Ah	R/W	TG AFE2_SHD Start Register	40h
0Bh	R/W	TG AFE2_SHD End Register	60h
0Ch	R/W	TG CIS_CLK/SH On Guardband Register	00h
0Dh	R/W	TG CIS_CLK/SH Off Guardband Register	00h
0Eh	R/W	TG Wheel Step MSB Register	00h
0Fh	R/W	TG Wheel Step LSB Register	80h
10h	R/W	TG Wheel Control Register	01h
11h	R/W	CIS1/CIS2 Dummy LAMP Selection Register	00h
12h	R/W	CIS1/CIS2 Dummy LAMP On MSB Register	00h
13h	R/W	CIS1/CIS2 Dummy LAMP On LSB Register	00h
14h	R/W	CIS1/CIS2 Dummy LAMP Off MSB Register	00h
15h	R/W	CIS1/CIS2 Dummy LAMP Off LSB Register	00h
16h	R/W	CIS1 LAMP Component Selection Register	00h
17h	R/W	CIS2 LAMP Component Selection Register	00h
18h	R/W	CIS Black Level Clamp Control Register	00h
19h	R/W	CIS1/2 Black Level Clamp Position Register	00h
1Ah	R/W	CIS To ASIC Data Mapping Register	00h
1Bh	R/W	AFE Data Output To ASIC Data Input Order Register	00h
1Ch	R/W	CIS Bypass Selection Register	00h
1Dh	R/W	CIS1 Output Ctrl Signals Strength Register	51h
1Eh	R/W	CIS2 Output Ctrl Signals Strength Register	11h
1Fh	R/W	Page Register	00h
Page 3	**TG Timing 1 Registers: Page Register 1Fh = 03h**		
00h	R/W	TG CIS_1 CH_1/4 Start of Valid Pixels MSB Register	00h/00h
01h	R/W	TG CIS_1 CH_1/4 Start of Valid Pixels LSB Register	01h/01h
02h	R/W	TG CIS_1 CH_1/4 End of Valid Pixels MSB Register	01h/01h
03h	R/W	TG CIS_1 CH_1/4 End of Valid Pixels LSB Register	B0h/B0h
04h	R/W	TG CIS_1 CH_2/5 Start of Valid Pixels MSB Register	00h/00h
05h	R/W	TG CIS_1 CH_2/5 Start of Valid Pixels LSB Register	01h/01h
06h	R/W	TG CIS_1 CH_2/5 End of Valid Pixels MSB Register	01h/01h
07h	R/W	TG CIS_1 CH_2/5 End of Valid Pixels LSB Register	B0h/B0h
08h	R/W	TG CIS_1 CH_3/6 Start of Valid Pixels MSB Register	00h/00h
09h	R/W	TG CIS_1 CH_3/6 Start of Valid Pixels LSB Register	01h/01h
0Ah	R/W	TG CIS_1 CH_3/6 End of Valid Pixels MSB Register	02h/02h
0Bh	R/W	TG CIS_1 CH_3/6 End of Valid Pixels LSB Register	40h/40h
0Ch	R/W	TG CIS_1 Line Valid Start and End MSB Register	00h
0Dh	R/W	TG CIS_1 Line Valid Start LSB Register	00h
0Eh	R/W	TG CIS_1 Line Valid End LSB Register	00h
0Fh	R/W	TG CIS_2 CH_1/4 Start of Valid Pixels MSB Register	00h/00h
10h	R/W	TG CIS_2 CH_1/4 Start of Valid Pixels LSB Register	01h/01h
11h	R/W	TG CIS_2 CH_1/4 End of Valid Pixels MSB Register	01h/01h
12h	R/W	TG CIS_2 CH_1/4 End of Valid Pixels LSB Register	B0h/B0h
13h	R/W	TG CIS_2 CH_2/5 Start of Valid Pixels MSB Register	00h/00h
14h	R/W	TG CIS_2 CH_2/5 Start of Valid Pixels LSB Register	01h/01h
15h	R/W	TG CIS_2 CH_2/5 End of Valid Pixels MSB Register	01h/01h
16h	R/W	TG CIS_2 CH_2/5 End of Valid Pixels LSB Register	B0h/B0h
17h	R/W	TG CIS_2 CH_3/6 Start of Valid Pixels MSB Register	00h/00h
18h	R/W	TG CIS_2 CH_3/6 Start of Valid Pixels LSB Register	01h/01h

Address	Mode	Description	Default
19h	R/W	TG CIS_2 CH_3/6 End of Valid Pixels MSB Register	02h/02h
1Ah	R/W	TG CIS_2 CH_3/6 End of Valid Pixels LSB Register	40h/40h
1Bh	R/W	TG CIS_2 Line Valid Start and End MSB Register	00h
1Ch	R/W	TG CIS_2 Line Valid Start LSB Register	00h
1Dh	R/W	TG CIS_2 Line Valid End LSB Register	00h
1Eh	R/W	CIS Channel Switching Selection Register	00h
1Fh	R/W	Page Register	00h
Page 4	**TG Timing 2 Registers: Page Register 1Fh = 04h**		
00h	R/W	TG MODE Output Selection Register	00h
01h	R/W	TG CIS1/2 MODE On MSB Register	00h/00h
02h	R/W	TG CIS1/2 MODE On LSB Register	00h/00h
03h	R/W	TG CIS1/2 MODE Off MSB Register	00h/00h
04h	R/W	TG CIS1/2 MODE Off LSB Register	00h/00h
05h	R/W	TG SI Mode Selection Register	0ch
06h	R/W	TG SI Width Register	04h
07h	R/W	TG_1 Line End MSB Register	00h
08h	R/W	TG_1 Line End LSB Register	20h
09h	R/W	TG_2 Line End MSB Register	00h
0Ah	R/W	TG_2 Line End LSB Register	20h
0Bh	R/W	Frame Start/End Selection Register	00h
0Ch	R/W	Pixel Threshold for Auto Detection of Frame Start Register	00h
0Dh	R/W	Number of Pixel Per Line for Auto Detection of Frame Start MSB Register	00h
0Eh	R/W	Number of Pixel Per Line for Auto Detection of Frame Start LSB Register	00h
0Fh	R/W	Number of Lines for Auto Detection of Frame Start MSB Register	30h
10h	R/W	Number of Lines for Auto Detection of Frame Start LSB Register	00h
11h	R/W	Pixel Threshold For Auto Detection of Frame End Register	00h
12h	R/W	Number of Pixel Per Line for Auto Detection of Frame End MSB Register	00h
13h	R/W	Number of Pixel Per Line for Auto Detection of Frame End LSB Register	00h
14h	R/W	Number of Lines for Auto Detection of Frame End MSB Register	00h
15h	R/W	Number of Lines for Auto Detection of Frame End LSB Register	00h
16h	R/W	Delay Lines for Starting Detection of Frame End MSB Register	00h
17h	R/W	Delay Lines for Starting Detection of Frame End LSB Register	00h
18h	R/W	Number of Lines for Fix Length of Frame End MSB Register	00h
19h	R/W	Number of Lines for Fix Length of Frame End LSB Register	00h
1Ah	R/W	Frame Jam Counter Register 0	00h
1Bh	R/W	Frame Jam Counter Register 1	00h
1Ch	R/W	Frame Jam Counter Register 2	00h
1Dh	R/W	Frame Jam Counter Register 3	00h
1Fh	R/W	Page Register	00h
Page 5	**CIS1 LAMP Control Registers: Page Register 1Fh = 05h**		
00h	R/W	CIS1 LAMP Mode Register	00h/00h
01h	R/W	CIS1 Component 1/Component 7 LAMP Selection Register	20h/00h
02h	R/W	CIS1 Component 2/Component 8 LAMP Selection Register	10h/00h
03h	R/W	CIS1 Component 3/Component 9 LAMP Selection Register	08h/00h
04h	R/W	CIS1 Component 4/Component 10 LAMP Selection Register	04h/00h
05h	R/W	CIS1 Component 5/Component 11 LAMP Selection Register	02h/00h
06h	R/W	CIS1 Component 6/Component 12 LAMP Selection Register	01h/00h
07h	R/W	CIS1 Red LAMP On MSB Register	00h

Address	Mode	Description	Default
08h	R/W	CIS1 Red LAMP On LSB Register	2Eh
09h	R/W	CIS1 Red LAMP Off MSB Register	01h
0Ah	R/W	CIS1 Red LAMP Off LSB Register	06h
0Bh	R/W	CIS1 Green LAMP On MSB Register	00h
0Ch	R/W	CIS1 Green LAMP On LSB Register	2Eh
0Dh	R/W	CIS1 Green LAMP Off MSB Register	01h
0Eh	R/W	CIS1 Green LAMP Off LSB Register	06h
0Fh	R/W	CIS1 Blue LAMP On MSB Register	00h
10h	R/W	CIS1 Blue LAMP On LSB Register	2Eh
11h	R/W	CIS1 Blue LAMP Off MSB Register	01h
12h	R/W	CIS1 Blue LAMP Off LSB Register	06h
13h	R/W	CIS1 IR1 LAMP On MSB Register	00h
14h	R/W	CIS1 IR1 LAMP On LSB Register	2Eh
15h	R/W	CIS1 IR1 LAMP Off MSB Register	01h
16h	R/W	CIS1 IR1 LAMP Off LSB Register	06h
17h	R/W	CIS1 IR2 LAMP On MSB Register	00h
18h	R/W	CIS1 IR2 LAMP On LSB Register	2Eh
19h	R/W	CIS1 IR2 LAMP Off MSB Register	01h
1Ah	R/W	CIS1 IR2 LAMP Off LSB Register	06h
1Bh	R/W	CIS1 UV LAMP On MSB Register	00h
1Ch	R/W	CIS1 UV LAMP On LSB Register	2Eh
1Dh	R/W	CIS1 UV LAMP Off MSB Register	01h
1Eh	R/W	CIS1 UV LAMP Off LSB Register	06h
1Fh	R/W	Page Register	00h
Page 6	**CIS2 LAMP Control Registers: Page Register 1Fh = 06h**		
00h	R/W	CIS2 LAMP Mode Register	00h
01h	R/W	CIS2 Component 1/Component 7 LAMP Selection Register	20h/00h
02h	R/W	CIS2 Component 2/Component 8 LAMP Selection Register	10h/00h
03h	R/W	CIS2 Component 3/Component 9 LAMP Selection Register	08h/00h
04h	R/W	CIS2 Component 4/Component 10 LAMP Selection Register	04h/00h
05h	R/W	CIS2 Component 5/Component 11 LAMP Selection Register	02h/00h
06h	R/W	CIS2 Component 6/Component 12 LAMP Selection Register	01h/00h
07h	R/W	CIS2 Red LAMP On MSB Register	00h
08h	R/W	CIS2 Red LAMP On LSB Register	2Eh
09h	R/W	CIS2 Red LAMP Off MSB Register	01h
0Ah	R/W	CIS2 Red LAMP Off LSB Register	06h
0Bh	R/W	CIS2 Green LAMP On MSB Register	00h
0Ch	R/W	CIS2 Green LAMP On LSB Register	2Eh
0Dh	R/W	CIS2 Green LAMP Off MSB Register	01h
0Eh	R/W	CIS2 Green LAMP Off LSB Register	06h
0Fh	R/W	CIS2 Blue LAMP On MSB Register	00h
10h	R/W	CIS2 Blue LAMP On LSB Register	2Eh
11h	R/W	CIS2 Blue LAMP Off MSB Register	01h
12h	R/W	CIS2 Blue LAMP Off LSB Register	06h
13h	R/W	CIS2 IR1 LAMP On MSB Register	00h
14h	R/W	CIS2 IR1 LAMP On LSB Register	2Eh
15h	R/W	CIS2 IR1 LAMP Off MSB Register	01h
16h	R/W	CIS2 IR1 LAMP Off LSB Register	06h
17h	R/W	CIS2 IR2 LAMP On MSB Register	00h

Address	Mode	Description	Default
18h	R/W	CIS2 IR2 LAMP On LSB Register	2Eh
19h	R/W	CIS2 IR2 LAMP Off MSB Register	01h
1Ah	R/W	CIS2 IR2 LAMP Off LSB Register	06h
1Bh	R/W	CIS2 UV LAMP On MSB Register	00h
1Ch	R/W	CIS2 UV LAMP On LSB Register	2Eh
1Dh	R/W	CIS2 UV LAMP Off MSB Register	01h
1Eh	R/W	CIS2 UV LAMP Off LSB Register	06h
1Fh	R/W	Page Register	00h
Page 7	**CIS1 Shading Control Registers: Page Register 1Fh = 07h**		
00h	R/W	Shading Control Register	00h
02h	R/W	Shading RAM/DSP Combination Select Register	00h
03h	R/W	Shading RAM /DSP Start Address MSB Register	00h
04h	R/W	Shading RAM /DSP Start Address LSB Register	00h
05h	R/W	Shading RAM /DSP Transfer Count MSB Register	00h
06h	R/W	Shading RAM /DSP Transfer Count LSB Register	00h
07h	R/W	CIS1 Global Shading Gain Coefficient Register	00h
08h	R/W	CIS2 Global Shading Gain Coefficient Register	00h
0Ah	R/W	CIS 1 Dark Shading Offset Virtual Address MSB Register	00h
0Bh	R/W	CIS 1 Dark Shading Offset Virtual Address LSB Register	00h
0Ch	R/W	CIS 1 Dark Shading Offset Coefficient Register	00h
0Dh	R/W	CIS 1 Combination 1 Shading Gain Virtual Address MSB Register	00h
0Eh	R/W	CIS 1 Combination 1 Shading Gain Virtual Address LSB Register	00h
0Fh	R/W	CIS 1 Combination 1 Shading Gain Coefficient Register	00h
10h	R/W	CIS 1 Combination 2 Shading Gain Virtual Address MSB Register	00h
11h	R/W	CIS 1 Combination 2 Shading Gain Virtual Address LSB Register	00h
12h	R/W	CIS 1 Combination 2 Shading Gain Coefficient Register	00h
13h	R/W	CIS 1 Combination 3 Shading Gain Virtual Address MSB Register	00h
14h	R/W	CIS 1 Combination 3 Shading Gain Virtual Address LSB Register	00h
15h	R/W	CIS 1 Combination 3 Shading Gain Coefficient Register	00h
16h	R/W	CIS 1 Combination 4 Shading Gain Virtual Address MSB Register	00h
17h	R/W	CIS 1 Combination 4 Shading Gain Virtual Address LSB Register	00h
18h	R/W	CIS 1 Combination 4 Shading Gain Coefficient Register	00h
19h	R/W	CIS 1 Combination 5 Shading Gain Virtual Address MSB Register	00h
1Ah	R/W	CIS 1 Combination 5 Shading Gain Virtual Address LSB Register	00h
1Bh	R/W	CIS 1 Combination 5 Shading Gain Coefficient Register	00h
1Ch	R/W	CIS 1 Combination 6 Shading Gain Virtual Address MSB Register	00h
1Dh	R/W	CIS 1 Combination 6 Shading Gain Virtual Address LSB Register	00h
1Eh	R/W	CIS 1 Combination 6 Shading Gain Coefficient Register	00h
1Fh	R/W	Page Register	00h
Page 8	**CIS2 Shading Control Registers: Page Register 1Fh = 08h**		
00h	R/W	CIS 2 Dark Shading Offset Virtual Address MSB Register	00h
01h	R/W	CIS 2 Dark Shading Offset Virtual Address LSB Register	00h
02h	R/W	CIS 2 Dark Shading Offset Coefficient Register	00h
03h	R/W	CIS 2 Combination 1 Shading Gain Virtual Address MSB Register	00h
04h	R/W	CIS 2 Combination 1 Shading Gain Virtual Address LSB Register	00h
05h	R/W	CIS 2 Combination 1 Shading Gain Coefficient Register	00h
06h	R/W	CIS 2 Combination 2 Shading Gain Virtual Address MSB Register	00h

Address	Mode	Description	Default
07h	R/W	CIS 2 Combination 2 Shading Gain Virtual Address LSB Register	00h
08h	R/W	CIS 2 Combination 2 Shading Gain Coefficient Register	00h
09h	R/W	CIS 2 Combination 3 Shading Gain Virtual Address MSB Register	00h
0Ah	R/W	CIS 2 Combination 3 Shading Gain Virtual Address LSB Register	00h
0Bh	R/W	CIS 2 Combination 3 Shading Gain Coefficient Register	00h
0Ch	R/W	CIS 2 Combination 4 Shading Gain Virtual Address MSB Register	00h
0Dh	R/W	CIS 2 Combination 4 Shading Gain Virtual Address LSB Register	00h
0Eh	R/W	CIS 2 Combination 4 Shading Gain Coefficient Register	00h
0Fh	R/W	CIS 2 Combination 5 Shading Gain Virtual Address MSB Register	00h
10h	R/W	CIS 2 Combination 5 Shading Gain Virtual Address LSB Register	00h
11h	R/W	CIS 2 Combination 5 Shading Gain Coefficient Register	00h
12h	R/W	CIS 2 Combination 6 Shading Gain Virtual Address LSB Register	00h
13h	R/W	CIS 2 Combination 6 Shading Gain Virtual Address MSB Register	00h
14h	R/W	CIS 2 Combination 6 Shading Gain Coefficient Register	00h
	—		
1Fh	R/W	Page Register	00h
Page 9	**ISP Control Registers: Page Register 1Fh = 09h**		
00h	R/W	ISP Control Register 0	00h
01h	R/W	ISP Control Register 1	00h
02h	R/W	ISP Control Register 2	00h
03h	R/W	ISP Control Register 3	00h
04h	R/W	ISP Control Register 4	00h
05h	R/W	Line Border Control Register 0	30h
06h	R/W	Line Border Control Register 1	AAh
	—		
0Ah	R/W	ISP1 Sharpness Gain 1 Register	40h
0Bh	R/W	ISP1 Sharpness Gain 2 Register	40h
0Ch	R/W	ISP2 Sharpness Gain 1 Register	40h
0Dh	R/W	ISP2 Sharpness Gain 2 Register	40h
0Eh	R/W	ISP1 Line Border Static Threshold Register	20h
0Fh	R/W	ISP2 Line Border Static Threshold Register	20h
10h	R/W	ISP1 Line Border Big Window Threshold Register	20h
11h	R/W	ISP1 Line Border Small Window Threshold Register	08h
12h	R/W	ISP2 Line Border Big Window Threshold Register	20h
13h	R/W	ISP2 Line Border Small Window Threshold Register	08h
	—		
16h	R/W	ISP1 Valid Range Start/End Address MSB Register	07h
17h	R/W	ISP1 Valid Range Start Address LSB Register	00h
18h	R/W	ISP1 Valid Range End Address LSB Register	FFh
19h	R/W	ISP2 Valid Range Start/End Address MSB Register	07h
1Ah	R/W	ISP2 Valid Range Start Address LSB Register	00h
1Bh	R/W	ISP2 Valid Range End Address LSB Register	FFh
	—		
1Fh	R/W	Page Register	1Fh

Register Description

Page 0 Register – System Setup

- **Address P0_01h: Software Reset Register**

Bit	Mode	Description	Default
7-2	—	Reserved	—
1	R/W	ISP Engine Software reset (Self clear) 1: Reset	0
0	R/W	TG Controller Software reset (Self clear) 1: Reset	0

- **Address P0_02h: Mode Setting Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R/W	Register Mode Setting Enable 0: Disable 1: Enable	0
3-0	R/W	Register Mode Selection 4'h0: Normal mode 4'h1: Reserved 4'h2: DFT Test Mode 4'h3: Tie-High Test Mode 4'h4: Tie-Low Test Mode 4'h5: Nand-tree Test Mode 4'h6: Pull-Up-Down Test Mode 4'h7: Iptest Test Mode 4'h8: Debug1 Mode 4'h9: Debug2 Mode 4'ha: Debug3 Mode	0h

- **Address P0_03h: Pixel Clock Configuration Register 0**

Bit	Mode	Description	Default
7	—	Pixel Clock Enable 0: Disable 1: Enable	—
6-5	R/W	Input Clock selection, used with b7 00: OSC – 12Mhz 01: OSC – 12Mhz 10: PLL1 (96Mhz) 11: PLL2 (144Mhz)	0h
4	R/W	Clock Division Enable 0: Not Divided 1: Divided	0
3-0	—	Reserved	—

- **Address P0_04h: Pixel Clock Configuration Register 1**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Clock Division Factor (DIV_FACT) [5:0] Output clock = input_clock/ (DIV_FACT+2)	00h

Note: set P0_04 first and then set P0_03h latter.

- **Address P0_05h: ADC Clock Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	ADC Clock Enable 0: Disable 1: Enable	0
6-5	R/W	Input Clock selection 00: OSC – 12Mhz 01: OSC – 12Mhz 10: PLL1 (96Mhz) 11: PLL2 (144Mhz)	0h
4	R/W	Clock Division Enable 0: Not Divided 1: Divided	0
3-0	—	Reserved	—

- **Address P0_06h: ADC Clock Configuration Register 1**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Clock Division Factor (DIV_FACT) [5:0] Output clock = input_clock/ (DIV_FACT+2)	00h

Note: set P0_06 first and then set P0_05h latter.

- **Address P0_07h: VPFE Clock Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	VPFE Clock Enable 0: Disable 1: Enable	0
6-5	R/W	Input Clock selection 00: OSC – 12Mhz 01: OSC – 12Mhz 10: PLL1 (96Mhz) 11: PLL2 (144Mhz)	0h
4	R/W	Clock Division Enable 0: Not Divided 1: Divided	0
3-0	—	Reserved	—

- **Address P0_08h: VPFE Clock Configuration Register 1**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Clock Division Factor (DIV_FACT) [5:0] Output clock = input_clock/ (DIV_FACT+2)	00h

Note: set P0_08 first and then set P0_07h latter.

- **Address P0_09h: ISP Clock Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	ISP Clock Enable 0: Disable 1: Enable	0
6-5	R/W	Input Clock selection 00: OSC – 12Mhz 01: OSC – 12Mhz 10: PLL1 (96Mhz) 11: PLL2 (144Mhz)	0h

Bit	Mode	Description	Default
4	R/W	Clock Division Enable 0: Not Divided 1: Divided	0
3-0	—	Reserved	—

- **Address P0_0Ah: ISP Clock Configuration Register 1**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Clock Division Factor (DIV_FACT) [5:0] Output clock = input_clock/ (DIV_FACT+2)	00h

- **Address P0_0Bh: ARM Clock Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	ARM Clock Enable 0: Disable 1: Enable	0
6-5	R/W	Input Clock selection 00: OSC – 12Mhz 01: OSC – 12Mhz 10: PLL1 (96Mhz) 11: PLL2 (144Mhz)	10
4	R/W	Clock Division Enable 0: Not Divided 1: Divided	1
3-0	—	Reserved	—

- **Address P0_0Ch: ARM Clock Configuration Register 1**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Clock Division Factor (DIV_FACT) [5:0] Output clock = input_clock/ (DIV_FACT+2)	01h

- **Address P0_0Eh: PLL1 M/N value Register**

Bit	Mode	Description	Default
7-4	R/W	PLL1 M value [3:0] 4'b0001: 12Mhz 4'b0010: 24Mhz 4'b0011: 36Mhz 4'b0100: 48Mhz 4'b0101: 60Mhz 4'b0110: 72Mhz 4'b0111: 84Mhz 4'b1000: 96Mhz Others: Reserved	8h
3-2	—	Reserved	—
1-0	—	PLL1 N value [2:0] 2'b00: divided by 1 2'b01: Divided by 2 2'b10: divided by 4 2'b11: Divided by 8	0h

- **Address P0_0Fh: PLL Control Register**

Bit	Mode	Description	Default
7-4	R/W	PLL2 M value [3:0] 4'b0001: 12Mhz 4'b0010: 24Mhz 4'b0011: 36Mhz 4'b0100: 48Mhz 4'b0101: 60Mhz 4'b0110: 72Mhz 4'b0111: 84Mhz 4'b1000: 96Mhz 4'b1001: 108Mhz 4'b1010: 120Mhz 4'b1011: 132Mhz 4'b1100: 144Mhz Others: Reserved	Ch
3-2	—	Reserved	—
1	R/W	PLL2 Enable 0: Disable 1: Enable	1
0	R/W	PLL1 Enable 0: Disable 1: Enable	1

- **Address P0_10h: Data Path Control Register 0**

Bit	Mode	Description	Default
7	R/W	CIS1 Data Capture Enable 0: Disable 1: Enable Note:CIS1 Sensor data passes to Video Port When this bit is enable	1
6	R/W	Output Data Format 0: Pixel by pixel 1: Line by line	0
5	R/W	Video Port Interface Selection 0: EMIF 1: VPFE	1
4	R/W	CIS2 Data Capture Enable 0: Disable 1: Enable Note: CIS2 Sensor data passes to the Video Port when this bit is enabled	1
3-2	R/W	Data Path Selection (source ↔ destination) 00: SPI ↔ Shading Ram (SPI can be from DSP or PC) 01: EMIF ↔ Shading Ram 10: Video Port ↔ line Buffer (selected by bit5) Others: Reserved	2h
1	R/W	Data Transfer Selection 0: Write, source → destination 1: Read, source ← destination	0
0	R/W	Shading/DSP Transfer Start Writing 1 to this register starts a transfer between the Shading Ram and DSP. After the transfer is complete this bit will auto clear. Note: only for Shading Ram ↔ DSP	0

- **Address P0_11h: Data Path Control Register 1**

Bit	Mode	Description	Default
7-6	R/W	Video Port VD signal selection 00: V sync 01: V valid 10: H sync 11: H valid	01
5-4	R/W	Video Port HD signal selection 00: V sync 01: V valid 10: H sync 11: H valid	11
3-2	—	Reserved	—
1	R/W	Video Port clock out polarity selection 0: Positive edge 1: Negative edge	0
0	RO	Shading/DSP Transfer Done Note: only for Shading Ram ↔ DSP	—

- **Address P0_12h: Data Path Control Register 2**

Bit	Mode	Description	Default
7-3	—	Reserved	
2	R/W	CIS Data Output Order on Video Port 0: Big endian 1: Little endian Note: 1. If P0_10[6] is pixel-by-pixel and big endian is chosen, then the data output format is {CIS1[7:0], CIS2[7:0]} and vice versa. 2. If P0_10[6] is line-by-line and big endian is chosen, the data output format is {CIS1_0[7:0], CIS1_1[7:0]}, {CIS1_2[7:0], CIS1_3[7:0]}, …{CIS2_0[7:0], CIS2_1[7:0]}, {CIS2_2[7:0], CIS2_3[7:0]}	0
1	R/W	Line wait enable 0: Disable 1: Enable Note: If Line wait enable and Output Data Format is "Line-by-Line" as set in register P0_10[6], after the CIS1 data of a line has been transferred, the CIS2 data will not be transferred until the counter reaches the value set by registers P0_13h and P0_14h	0
0	R/W	CIS2 Lamp Control Selection 0: Depend on tg1,CIS1 Lamp, mode relative register 1: Depends on tg2,CIS2 Lamp, mode relative registers Note: When CIS2 Lamp Control Selection is not set; CIS2 light signals only depend on TG1 and CIS1 lamp control, mode relative registers and TG2 and CIS2 registers are ignored.	1

- **Address P0_13h: Line Wait Counter MSB Register**

Bit	Mode	Description	Default
7-0	R/W	Line Wait Counter MSB Note: Counter is based on the VPFE clock	00h

- **Address P0_14h: Line Wait Counter LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Line Wait Counter LSB Note: Counter is based on the VPFE clock	00h

- **Address P0_15h: AFE Output Ctrl Signal Strength Register**

Bit	Mode	Description	Default
7-6	R/W	AFE2 CLP, SHD Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01
5-4	R/W	AFE1 CLP, SHD Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01
3-2	R/W	AFE2 ADCK Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01
1-0	R/W	AFE1 ADCK Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01

- **Address P0_16h: VPFE/EMIF Ctrl Signal Strength Register**

Bit	Mode	Description	Default
7-6	R/W	HD_MWEN Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	00
5-4	R/W	VD_MOEN Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	00
3-2	—	Reserved	—
1-0	R/W	PCLK_MWAIT Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	10

- **Address P0_17h: Video Port Delay Control Register**

Bit	Mode	Description	Default
7-2	—	Reserved	—
1-0	R/W	Video_Port_DATA[15:0] Delay Mode [1:0] b15, b14, b13, b12, b11, b10, b9, b8, b7, b6, b5, b4, b3, b2, b1, b0 00: No delay 01: 1D,2D,1D,2D,1D,2D,1D,2D,1D,2D,1D,2D,1D,2D,1D,2D 10: 1D,2D,3D,4D,1D,2D,3D,4D,1D,2D,3D,4D,1D,2D,3D,4D 11: Reserved	00

- **Address P0_18h: Misc Control Register 0**

Bit	Mode	Description	Default
7	—	Reserved	—
6	R/W	AFE2 ADCCLK Output Pin Tri-State Control 0: Tri-State 1: Output	0
5	R/W	AFE2 CLP Output Pin Tri-State Control 0: Tri-State 1: Output	0
4	R/W	AFE2 SHD Output Pin Tri-State Control 0: Tri-State 1: Output	0
3	R/W	Led UV pin and oscillator output selection 0: for LED UV used 1: for Oscillator output	0
2	R/W	CIS2 Lamp output pin Tri-State Control 0: Tri-State 1: Output	1
1	R/W	CIS2 Mode and SP output pin Tri-State Control 0: Tri-State 1: Output	0
0	R/W	Roller Output pin Tri-Sate Control 0: Tri-State 1: Output	0

- **Address P0_19h: Misc Control Register 1**

Bit	Mode	Description	Default
7	R/W	AFE2_ADCK pin enable 0: Disable 1: Enable	1
6	—	Reserved	—
5	R/W	SPI Interface number selection 0: 3-wire SPI interface 1: 4-wire SPI interface Note: If the 3-wire is selected PADSDIO is bidirectional. If the 4-wire is selected then PADSDIO is input only and PADROLLER_OUT is an SPI SDO output.	0
4	R/W	LVR disable control 0: Enable 1: Disable	0
3	R/W	PAD "SCK" Schmitt trigger enable 0: Disable 1: Enable	1
2	R/W	PAD "PADHD_MWEN "," PADVD_MOEN" Schmitt trigger enable 0: Disable 1: Enable	1
1	R/W	CIS1 R, G, B lamp output pin pull down enable 0: Disable 1: Enable	1
0	R/W	CIS1 lamp output pin Tri state control 0: Tri state 1: output	1

- **Address P0_1Ah: Wheel Comparator Control Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6	R/W	comparator operation ON/ OFF control 0: Comparator power down 1: Comparator normal operation	1
5	R/W	Comparator hysteresis ON / OFF control 0: Hysteresis is OFF 1: Hysteresis is ON	1
4-0	R/W	Comparator voltage register 5'd0: 0V 5'd1: VREF = (3.3/32)×1V 5'd2: VREF = (3.3/32)×2V 5'd3: VREF = (3.3/32)×3V . . . 5'd31: VREF = (3.3/32)×31V	5'h0f

- **Address P0_1Bh: Pin and Pwr-On-Strapped Status Register**

Bit	Mode	Description	Default
7-5	RO	Pwr-On-Strapped Status Selection 3'h0: Normal Mode 3'h1: DFT 3'h2: Tie-High 3'h3: Tie-Low 3'h4: Nand-tree 3'h5: Pull-Up-Down 3'h6: Iptest 3'h7: Reserved	—
4	RO	Pwr-On-Strapped Status Enable	—
3-1	RO	Pin Mode Status Selection 3'h0: Reserved 3'h1: DFT 3'h2: Tie-High 3'h3: Tie-low 3'h4: Nand-tree 3'h5: Pull-Up-Down 3'h6: Iptest Others: Reserved	—
0	RO	Pin Mode Status Enable	—

- **Address P0_1Ch: Debug Control Register 0**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R/W	TG debug bus selection[4]	0
3	R/W	Function pattern enable	0
2	R/W	Data path debug enable	0
1	R/W	DSP debug enable	0
0	R/W	TG debug enable	0

- **Address P0_1Dh: Debug Control Register 1**

Bit	Mode	Description	Default
7-4	R/W	DSP debug bus selection[3:0]	0h
3-0	R/W	TG debug bus selection[3:0]	0h

- **Address P0_1Eh: Data Bus Debug Error Status Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R	Data Path Error after Line-Buffer Controller	—
3	R	Data Path Error after Asyn-FIFO	—
2	R	Data Path Error after ISP	—
1	R	Data Path Error after Shading	—
0	R	Data Path Error after TG Controller	—

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Reserved 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 2 Register – TG Control

- **Address P2_00h: TG Main Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	TG2 Color Order. Configures the pixel processing sequence 0: Forward 1: Reverse	0
6-4	R/W	TG2 Color Sequence Length. Used in Mode 1a to determine the number of colors sequenced during a scan. 111: Not valid 110: Six color (component) sequence 101: Five color (component) sequence 100: Four color (component) sequence 011: Three color (component) sequence 010: Two color (component) sequence 001: One color (component) sequence (Default) 000: Not valid	001
3	R/W	TG1 Color Order. Configures the sequence of the pixel processing. 0: Forward 1: Reverse	0
2-0	R/W	TG1 Color Sequence Length. Used in Mode 1a to determine the number of colors sequenced during a scan. 111: Not valid 110: Six color (component) sequence 101: Five color (component) sequence 100: Four color (component) sequence 011: Three color (component) sequence 010: Two color (component) sequence 001: One color (component) sequence (Default) 000: Not valid	001

- **Address P2_01h: TG Main Configuration Register 1**

Bit	Mode	Description	Default
7	—	Reserved	—
6	R/W	TG Test Pattern Enable 0: Disable 1: Enable	0
5	R/W	TG2 Function Active_n (active low) 0: TG2 Function Active 1: TG2 Function Inactive Notes: 1. When Frame Start Selection is "SPI" at P4_0B and TG2 Function is Active, setting TG2 Start Scan (BOS) will start capturing data and lighting signals to sensor 2. When Frame End Selection is "SPI" at P4_0B and TG2 Function is Inactive or resetting TG2 Start Scan (BOS) will stop capturing data and lighting signals to sensor	1
4	R/W	TG2 Start Scan (BOS) 0: Ready 1: Start Scan	0
3	—	Reserved	—
2	R/W	Software Reset. Performs a reset for TG1, TG2 Controller and TG1, TG2 Register when set to a 1. Self clear.	0
1	R/W	TG1 Function Active_n (active low) 0: TG1 Function Active 1: TG1 Function InActive	1
0	R/W	TG1 Start Scan (BOS) 0: Ready 1: Start Scan Notes: 1. When Frame Start Selection is "SPI" at P4_0B and TG1 Function is Active, setting TG1 Start Scan (BOS) will start capturing data and lighting signals to sensor 2. When Frame End Selection is "SPI" at P4_0B and TG1 Function is Inactive or resetting TG1 Start Scan (BOS) will stop capturing data and lighting signals to sensor	0

- **Address P2_02h: TG Control Register 0**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	RO	DLL Test output status when bit4 =1 0: DLL OK 1: DLL Fail	—
4	R/W	DLL Test mode Enable 0: No detection 1: Detection	0
3-2	R/W	DLL control selection	00
1	R/W	CIS_CLK output level when CIS_CLK BLK is Low 1: High level 0: Low level	0
0	R/W	DLL Enable Should generate an Active_Low pulse after power_on reset.	1

- **Address P2_03h: TG Control Register 1**

Bit	Mode	Description	Default
7	R/W	Vertical DPI Selection 0: 100dpi 1: 200dpi	0
6	—	Reserved	—

Bit	Mode	Description	Default
5	RO	TG2 Activity On/Off 0: TG2 is not active 1: TG2 is active Note: Checking TG2 status when setting P2_01[5] and P4_0B[1:0] relative selection	0
4	RO	TG1 Activity On/Off 0: TG1 is not active 1: TG1 is active Note: Checking TG1 status when setting P2_01[1] and P4_0B[1:0] relative selection	0
3	R/W	TG2 Color Sequence Length Minus One 0: Disable 1: Enable Note: When register is set to 1, TG2 total color sequence length will reduce	0
2	R/W	TG1 Color Sequence Length Minus One 0: Disable 1: Enable Note: When register is set to 1, TG1 total color sequence length will reduce	0
1	R/W	TG2 Color Sequence Length Multiply by 2 0: Diable 1: Enable Note: When register is set to 1, TG2 color sequence length on register "P2_00 bit[6-4]" will multiply by 2	0
0	R/W	TG1 Color Sequence Length Multiply by 2 0: Diable 1: Enable Note: When register is set to 1, TG2 color sequence length on register "P2_00 bit[2-0]" will multiply by 2	0

- **Address P2_04h: TG Control Register 2**

Bit	Mode	Description	Default
7	R/W	AFE Data Sampling Edge Selection 0: Negative Edge Sampled 1: Positive Edge Sampled V72 sampling AFE Data on positive edge or negative edge of adcclk	0
6	R/W	Line Pixel Number Adjustment Enable 0: Disable 1: Enable Line Pixel numbers are adjusted on the positive edge of ROLLER_IN when enabled	0
5-4	R/W	Latency of adcclk with respect to pixel clock where current AFE Data appears 00: No adcclk latency with respect to pixel clock 01: One adcclk latency with respect to pixel clock 10: Two adcclk latency with respect to pixel clock 11: Reserved	01
3-2	R/W	CIS2 Sensor Channel Number Selection 00: Three Channel Numbers 01: Four Channel Numbers 10: Five Channel Numbers 11: Six Channel Numbers	00
1-0	R/W	CIS1 Sensor Channel Number Selection 00: Three Channel Numbers 01: Four Channel Numbers 10: Five Channel Numbers 11: Six Channel Numbers	00

- **Address P2_05h: TG CIS_CLK/AFE_CLK Control Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6	R/W	AFE_CLK Polarity. 0: Normal – Low when off. 1: Inverted – High when off.	1
5-3	—	Reserved	—
2	R/W	CIS_CLK Polarity. 0: Normal – Low when off. 1: Inverted – High when off.	1
1	—	Reserved	—
0	R/W	CIS_CLK Activity During SH. 0: Inactive 1: Active	1

- **Address P2_06h: TG CIS_CLK Start Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	CIS_CLK on point. Defines when the CIS_CLK signal turns on within the pixel period. Can be set to any available edge within the pixel period.	00h

- **Address P2_07h: TG CIS_CLK End Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	CIS_CLK off point. Defines when the CIS_CLK signal turns off within the pixel period. Can be set to any available edge within the pixel period.	40h

- **Address P2_08h: TG AFE1_SHD Start Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	AFE1_SHD on point. Defines when the AFE1_SHD signal turns on within the pixel period. Can be set to any available edge within the pixel period.	40h

- **Address P2_09h: TG AFE1_SHD End Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	AFE1_SHD off point. Defines when the AFE1_SHD signal turns off within the pixel period. Can be set to any available edge within the pixel period.	60h

- **Address P2_0Ah: TG AFE2_SHD Start Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	AFE2_SHD on point. Defines when the AFE2_SHD signal turns on within the pixel period. Can be set to any available edge within the pixel period.	40h

- **Address P2_0Bh: TG AFE2_SHD End Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	AFE2_SHD off point. Defines when the AFE2_SHD signal turns off within the pixel period. Can be set to any available edge within the pixel period.	60h

- **Address P2_0Ch: TG CIS_CLK/SH On Guardband Register**

Bit	Mode	Description	Default
7-0	R/W	CIS_CLK on guardband. Number of pixel periods from end of the SH pulse to start of CIS_CLK.	00h

- **Address P2_0Dh: TG CIS_CLK/SH Off Guardband Register**

Bit	Mode	Description	Default
7-0	R/W	CIS_CLK off guardband. Number of pixel periods before start of the SH pulse that CIS_CLK stops.	00h

- **Address P2_0Eh: TG Wheel Step MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	TG wheel Step Most Significant 3 Bits Wheel Step is from 1.0~8.0 mm/step and wheel step should multiply 128 to set the whole register Ex: @100DPI, 1 mm/step = 4 lines/step 2 mm/step = 8 lines/step	0h

- **Address P2_0Fh: TG Wheel Step LSB Register**

Bit	Mode	Description	Default
7-0	R/W	TG wheel Step Least Significant Byte Wheel Step is from 1.0~8.0 mm/step and wheel step should multiply 128 to set the whole register	80h

- **Address P2_10h: TG Wheel Control Register**

Bit	Mode	Description	Default
7	R/W	TG Wheel input selection 0: Internal wheel after shaping signal from pad "PADROLLER_IN" 1: From pad "PADROLLER_IN"	0
6	R/W	TG Wheel signal inversion enable 0: Inversion disable 1: Inversion enable	0
5-4	R/W	TG Wheel Fast Ignoring Line Enable 00: No dropping Lines when next wheel in 01: Dropping some Lines when next wheel in 1x: Dropping all Lines when next wheel in Note: Choosing "00" may obtain more smooth pictures	0h
3	R/W	TG Wheel Activation Selection 0: After Current Line End 1: After Lights End and AFE sampling End Note: Choosing "1" will prevent dropping lines well	0
2-1	R/W	TG Wheel Filtering Selection 00: 3-tap filtering 01: 5-tap filtering 10: 8-tap filtering 11: 12-tap filtering	0h
0	R/W	TG Wheel Filtering Enable 0: Disable 1: Enable	1

- **Address P2_11h: CIS1/CIS2 Dummy LAMP Selection Register**

Bit	Mode	Description	Default
7-6	R/W	Dummy LAMP mode selection 00: Dummy LAMP following register by bit[5:0] 01: Dummy LAMP following previous light signal 10: Dummy LAMP following post light signal 11: Reserved	00
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	0

- **Address P2_12h: CIS1/CIS2 Dummy LAMP On MSB Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R/W	Dummy LAMP Enable 0: Dummy LAMP Disabled 1: Dummy LAMP Enable Note: If Dummy LAMP is disabled, all LAMP off in dummy LAMP region	0
3-0	R/W	CIS1/CIS2 Dummy LAMP On Time Most Significant Byte This selects the pixel count at which the Dummy LAMP output goes active.	0h

- **Address P2_13h: CIS1/CIS2 Dummy LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	CIS1/CIS2 Dummy LAMP On Time Least Significant Bits. This selects the pixel count at which the DUMMY LAMPR output goes active. Note: Real CIS1/CIS2 Dummy on position = Dummy Lamp on register × 4.	00h

- **Address P2_14h: CIS1/CIS2 Dummy LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	CIS1/CIS2 Dummy LAMP Off Time Most Significant Byte This selects the pixel count at which the Dummy LAMP output goes inactive.	0h

- **Address P2_15h: CIS1/CIS2 Dummy LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	CIS1/CIS2 Dummy LAMP Off Time Least Significant Bits. This selects the pixel count at which the Dummy LAMP output goes inactive. Note: Real CIS1/CIS2 Lamp off position = Lamp off register × 4.	00h

- **Address P2_16h: CIS1 LAMP Component Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	CIS1 Component 6 LAMP or CIS1 Component 12 LAMP Selection 0: CIS1 Component 6 LAMP 1: CIS1 Component 12 LAMP Note: When setting this bit to "0", register P5_06[5:0] belongs to Component 6 LAMP and vice versa.	0
4	R/W	CIS1 Component 5 LAMP or CIS1 Component 11 LAMP Selection 0: CIS1Component 5 LAMP 1: CIS1Component 11 LAMP Note: When setting this bit to "0", register P5_05[5:0] belongs to Component 5 LAMP and vice versa.	0
3	R/W	CIS1 Component 4 LAMP or CIS1 Component 10 LAMP Selection 0: CIS1 Component 4 LAMP 1: CIS1 Component 10 LAMP Note: When setting this bit to "0", register P5_04[5:0] belongs to Component 4 LAMP and vice versa.	0
2	R/W	CIS1 Component 3 LAMP or CIS1 Component 9 LAMP Selection 0: CIS1 Component 3 LAMP 1: CIS1 Component 9 LAMP Note: When setting this bit to "0", register P5_03[5:0] belongs to Component 3 LAMP and vice versa.	0
1	R/W	CIS1 Component 2 LAMP or CIS1 Component 8 LAMP Selection 0: CIS1 Component 2 LAMP 1: CIS1 Component 8 LAMP Note: When setting this bit to "0", register P5_02[5:0] belongs to Component 2 LAMP and vice versa.	0
0	R/W	CIS1 Component 1 LAMP or CIS1 Component 7 LAMP Selection 0: CIS1 Component 1 LAMP 1: CIS1 Component 7 LAMP Note: When setting this bit to "0", register P5_01[5:0] belongs to Component 1 LAMP and vice versa.	0

- **Address P2_17h: CIS2 LAMP Component Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	CIS2 Component 6 LAMP or CIS2 Component 12 LAMP Selection 0: CIS2 Component 6 LAMP 1: CIS2 Component 12 LAMP Note: When setting this bit to "0", register P6_06[5:0] belongs to Component 6 LAMP and vice versa.	0
4	R/W	CIS2 Component 5 LAMP or CIS2 Component 11 LAMP Selection 0: CIS2 Component 5 LAMP 1: CIS2 Component 11 LAMP Note: When setting this bit to "0", register P6_05[5:0] belongs to Component 5 LAMP and vice versa.	0
3	R/W	CIS2 Component 4 LAMP or CIS2 Component 10 LAMP Selection 0: CIS2 Component 4 LAMP 1: CIS2 Component 10 LAMP Note: When setting this bit to "0", register P6_04[5:0] belongs to Component 4 LAMP and vice versa.	0
2	R/W	CIS2 Component 3 LAMP or CIS2 Component 9 LAMP Selection 0: CIS2 Component 3 LAMP 1: CIS2 Component 9 LAMP Note: When setting this bit to "0", register P6_03[5:0] belongs to Component 3 LAMP and vice versa.	0

Bit	Mode	Description	Default
1	R/W	CIS2 Component 2 LAMP or CIS2 Component 8 LAMP Selection 0: CIS2 Component 2 LAMP 1: CIS2 Component 8 LAMP Note: When setting this bit to "0", register P6_02[5:0] belongs to Component 2 LAMP and vice versa.	0
0	R/W	CIS2 Component 1 LAMP or CIS2 Component 7 LAMP Selection 0: CIS2 Component 1 LAMP 1: CIS2 Component 7 LAMP Note: When setting this bit to "0", register P6_01[5:0] belongs to Component 1 LAMP and vice versa.	0

- **Address P2_18h: CIS Black Level Clamp Control Register**

Bit	Mode	Description	Default
7	R/W	CIS Black Level Clamp Position Selection 0: CIS1 Black Level Clamp Position Selection 1: CIS2 Black Level Clamp Position Selection Note: CIS1/CIS2 Black Level Clamp Position Register at P2_19 is selected by this bit register.	0
6	—	Reserved	—
5	R/W	CIS2 Black Level Enable 0: Disable 1: Enable	0
4	R/W	CIS1 Black Level Enable 0: Disable 1: Enable	0
3-2	R/W	CIS2 Black Level Clamp Width 00: 4 pixels 01: 8 pixels 10: 16 pixels 11: 32 pixels	00
1-0	R/W	CIS1 Black Level Clamp Width 00: 4 pixels 01: 8 pixels 10: 16 pixels 11: 32 pixels	00

- **Address P2_19h: CIS1/2 Black Level Clamp Position Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	Black Level Clamp Position. Number of pixels in which Auto Black pulse is delayed, relative to falling edge of the SH pulse	0

- **Address P2_1Ah: CIS To ASIC Data Mapping Register**

Bit	Mode	Description	Default
7	R/W	CIS2 4~6 Output Sequence Reverse 0: Normal (4 5 6 4 5 6 4 5 6) 1: Reverse (6 5 4 6 5 4 6 5 4)	0
6	R/W	CIS2 1~3 Output Sequence Reverse 0: Normal 1: Reverse	0
5	R/W	CIS1 4~6 Output Sequence Reverse 0: Normal 1: Reverse	0
4	R/W	CIS1 1~3 Output Sequence Reverse 0: Normal 1: Reverse	0
3	—	Reserved	0

Bit	Mode	Description	Default
2-0	R/W	CIS to ASIC Data Mapping Selection 000: 1-2-3-4 ASIC AFE_DIN[7:0] AFE_DIN[15:8] AFE2_DIN[7:0] AFE2_DIN[15:8] ↔ CIS (123) CIS (456) CIS2 (123) CIS2 (456) 001: 1-3-2-4 ASIC AFE_DIN[7:0] AFE_DIN[15:8] AFE2_DIN[7:0] AFE2_DIN[15:8] ↔ CIS (123) CIS2 (123) CIS (456) CIS2 (456) 010: 1-4-3-2 ASIC AFE_DIN[7:0] AFE_DIN[15:8] AFE2_DIN[7:0] AFE2_DIN[15:8] ↔ CIS (123) CIS2 (456) CIS2 (123) CIS (456) 011: 3-2-1-4 ASIC AFE_DIN[7:0] AFE_DIN[15:8] AFE2_DIN[7:0] AFE2_DIN[15:8] ↔ CIS2 (123) CIS (456) CIS (123) CIS2 (456) 100: 4-2-3-1 ASIC AFE_DIN[7:0] AFE_DIN[15:8] AFE2_DIN[7:0] AFE2_DIN[15:8] ↔ CIS2 (456) CIS (456) CIS2 (123) CIS (123) 101: 3-4-1-2 ASIC AFE_DIN[7:0] AFE_DIN[15:8] AFE2_DIN[7:0] AFE2_DIN[15:8] ↔ CIS2 (123) CIS2 (456) CIS (123) CIS (456) Others:Reserved	000

- **Address P2_1Bh: AFE Data Output To ASIC Data Input Order Register**

Bit	Mode	Description	Default
7	R/W	ASIC AFE2_DIN[15:8] Bit Reverse 0: Normal 1: Reverse	0
6	R/W	ASIC AFE2_DIN[7:0] Bit Reverse 0: Normal 1: Reverse	0
5	R/W	ASIC AFE_DIN[15:8] Bit Reverse 0: Normal 1: Reverse	0
4	R/W	ASIC AFE_DIN[7:0] Bit Reverse 0: Normal 1: Reverse Note: When bit reverse AFE_DIN[7:0] → AFE_DIN[0:7]	0
3-2	—	Reserved	—
1	R/W	ASIC AFE2_DIN Byte Exchange 0: Normal 1: Exchange Note: When byte exchange AFE2_DIN[15:0] → {AFE2_DIN[7:0], AFE2_DIN[15:8]}.	0
0	R/W	ASIC AFE_DIN Byte Exchange 0: Normal 1: Exchange Note: When byte exchange AFE_DIN[15:0] → {AFE_DIN[7:0], AFE_DIN[15:8]}.	0

- **Address P2_1Ch: CIS Bypass Selection Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2	R/W	Bypass Channel Number Selection 0: 1,2,3 channel 1: 4,5,6 channel	0
1	R/W	Bypass Original 16-bit CIS Data Selection 0: CIS1 1: CIS2 Note: When bit 0 is enabled, P7_00 should be 8'h00, P9_00 should be 8'h00, P9_01 should be 8'h00, P9_02 should be 8'h00.	0

Bit	Mode	Description	Default
0	R/W	Bypass Original 16-bit CIS Data to Video Port enable 0: Disable 1: Enable Note: When the number of channels is greater than 3, the bypass data should be captured two times. One is to capture the channels 1, 2 and 3 16-bit CIS data, the other is to capture channels 4, 5 and 6.	0

- **Address P2_1Dh: CIS1 Output Ctrl Signal Strength Register**

Bit	Mode	Description	Default
7-6	R/W	CIS_CLK Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01
5-4	R/W	CIS2_LAMP Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01
3-2	R/W	CIS1_MODE Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	00
1-0	R/W	CIS1_SP Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01

- **Address P2_1Eh: CIS2 Output Ctrl Signals Strength Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-4	R/W	CIS2_LAMP Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01
3-2	R/W	CIS2_MODE Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	00
1-0	R/W	CIS2_SP Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01

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- **Address P3_00h: TG CIS_1 CH_1/4 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h/00h

- **Address P3_01h: TG CIS_1 CH_1/4 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Note: Start valid pixels means distance from falling edge of SH to beginning of valid pixel. If channel_1/4 start valid pixel and end valid pixel register are all zero, there is no data captured in this channel.	01h/01h

- **Address P3_02h: TG CIS_1 CH_1/4 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	01h/01h

- **Address P3_03h: TG CIS_1 CH_1/4 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Note: End valid pixels means the distance from the falling edge of SH to the end of valid pixel. If the channel_1/4 start valid pixel and the end valid pixel registers are all zero, there is no data captured in this channel.	B0h/B0h

- **Address P3_04h: TG CIS_1 CH_2/5 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h/00h

- **Address P3_05h: TG CIS_1 CH_2/5 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Note: Start valid pixels means the distance from falling edge of SH to the beginning of valid pixel. If the channel_2/5 start valid pixel and the end valid pixel registers are all zero, there is no data captured in this channel.	01h/01h

- **Address P3_06h: TG CIS_1 CH_2/5 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	01h/01h

- **Address P3_07h: TG CIS_1 CH_2/5 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Note: End valid pixels means the distance from the falling edge of SH to the end of valid pixel. If the channel_2/5 start valid pixel and the end valid pixel registers are all zero, there is no data captured in this channel.	B0h/B0h

- **Address P3_08h: TG CIS_1 CH_3/6 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h/00h

- **Address P3_09h: TG CIS_1 CH_3/6 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Note: Start valid pixels means the distance from the falling edge of SH to the beginning of valid pixel. If the channel_3/6 start valid pixel and the end valid pixel register are all zero, there is no data captured in this channel.	01h/01h

- **Address P3_0Ah: TG CIS_1 CH_3/6 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	02h/02h

- **Address P3_0Bh: TG CIS_1 CH_3/6 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Note: End valid pixels mean the distance from the falling edge of SH to the end of valid pixel. If the channel_3/6 start valid pixel and the end valid pixel register are all zero, there is no data captured in this channel.	40h/40h

- **Address P3_0Ch: TG CIS_1 Valid Line Start and End MSB Register**

Bit	Mode	Description	Default
7-4	R/W	AFE1 Line Valid Start Value – Most Significant 4 Bits Selects the Line count where the valid line is started after BOS	0h
3-0	R/W	AFE1 Line Valid End Value – Most Significant 4 Bits Selects the Line count where the valid line is ended after BOS	0h

- **Address P3_0Dh: TG CIS_1 Valid Line Start LSB Register**

Bit	Mode	Description	Default
7-0	R/W	AFE1 Line Valid Start Value – Least Significant Byte Selects the Line count where the valid line is ended after BOS	00h

- **Address P3_0Eh: TG CIS_1 Valid Line End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	AFE1 Line Valid End Value – Least Significant Byte Selects the Line count where the valid line is ended after BOS Note: When line valid Start equal to zero and End equal to zero, line is always valid after BOS.	00h

- **Address P3_0Fh: TG CIS_2 CH_1/4 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h/00h

- **Address P3_10h: TG CIS_2 CH_1/4 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Notes: 1. Start valid pixels means distance from falling edge of SH to beginning of valid pixel. 2. If the channel_1/4 start valid pixel and the end valid pixel register are equal, there is no data captured in this channel. 3. "End valid pixel – Start valid pixel + 1 " should be even.	01h/01h

- **Address P3_11h: TG CIS_2 CH_1/4 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	01h/01h

- **Address P3_12h: TG CIS_2 CH_1/4 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Notes: 1. End valid pixels mean distance from falling edge of SH to end of valid pixel. 2. If the channel_1/4 start valid pixel and the end valid pixel register are equal, there is no data captured in this channel. 3. "End valid pixel – Start valid pixel + 1 " should be even.	B0h/B0h

- **Address P3_13h: TG CIS_2 CH_2/5 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h/00h

- **Address P3_14h: TG CIS_2 CH_2/5 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Notes: 1. Start valid pixels means distance from falling edge of SH to beginning of valid pixel. 2. If the channel_2/5 start valid pixel and the end valid pixel register are equal, there is no data captured in this channel. 3. "End valid pixel – Start valid pixel + 1 " should be even.	01h/01h

- **Address P3_15h: TG CIS_2 CH_2/5 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	01h/01h

- **Address P3_16h: TG CIS_2 CH_2/5 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Notes: 1. End valid pixels mean distance from falling edge of SH to end of valid pixel. 2. If the channel_2/5 start valid pixel and the end valid pixel register are equal, there is no data captured in this channel. 3. "End valid pixel – Start valid pixel + 1 " should be even.	B0h/B0h

- **Address P3_17h: TG CIS_2 CH_3/6 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h/00h

- **Address P3_18h: TG CIS_2 CH_3/6 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Notes: 1. Start valid pixels means distance from falling edge of SH to beginning of valid pixel. 2. If the channel_3/6 start valid pixel and the end valid pixel register are equal ,there is no data captured in this channel. 3. "End valid pixel – Start valid pixel + 1 " should be even.	01h/01h

- **Address P3_19h: TG CIS_2 CH_3/6 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	02h/02h

- **Address P3_1Ah: TG CIS_2 CH_3/6 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Notes: 1. End valid pixels mean distance from falling edge of SH to end of valid pixel. 2. If the channel_3/6 start valid pixel and the end valid pixel register are equal, there is no data captured in this channel. 3. "End valid pixel – Start valid pixel + 1 " should be even.	40h/40h

- **Address P3_1Bh: TG CIS_2 Line Valid Start and End MSB Register**

Bit	Mode	Description	Default
7-4	R/W	AFE2 Line Valid Start Value – Most Significant 4 Bits Selects the Line count where the valid line is started after BOS	0h
3-0	R/W	AFE2 Line Valid End Value – Most Significant 4 Bits Selects the Line count where the valid line is ends after BOS	0h

- **Address P3_1Ch: TG CIS_2 Line Valid Start LSB Register**

Bit	Mode	Description	Default
7-0	R/W	AFE2 Line Valid Start Value – Least Significant Byte Selects the Line count where the valid line is ends after BOS	00h

- **Address P3_1Dh: TG CIS_2 Line Valid End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	AFE2 Line Valid End Value – Least Significant Byte Selects the Line count where the valid line ends after BOS Note: When line valid Start and End are equal to zero, the line is always valid after BOS.	00h

- **Address P3_1Eh: CIS Channel Switching Selection Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6	R/W	CIS2_CH_3/6 Setting Selection Register 0: CIS2_CH_3 Register Setting 1: CIS2_CH_6 Register Setting Note: CIS2_CH_3/CIS2_CH_6 Setting on register P3_17~P3_1A is set by this bit.	0
5	R/W	CIS2_CH_2/5 Setting Selection Register 0: CIS2_CH_2 Register Setting 1: CIS2_CH_5 Register Setting Note: CIS2_CH_2/CIS2_CH_5 Setting on register P3_13~P3_16 is set by this bit.	0
4	R/W	CIS2_CH_1/4 Setting Selection Register 0: CIS2_CH_1 Register Setting 1: CIS2_CH_4 Register Setting Note: CIS2_CH_1/CIS2_CH_4 Setting on register P3_0F~P3_12 is set by this bit.	0
3	—	Reserved	—
2	R/W	CIS1_CH_3/6 Setting Selection Register 0:CIS1_CH_3 Register Setting 1:CIS1_CH_6 Register Setting Note: CIS1_CH_3/CIS1_CH_6 Setting on register P3_08~P3_0B is set by this bit.	0
1	R/W	CIS1_CH_2/5 Setting Selection Register 0: CIS1_CH_2 Register Setting 1: CIS1_CH_5 Register Setting Note: CIS1_CH_2/CIS1_CH_5 Setting on register P3_04~P3_07 is set by this bit.	0

Bit	Mode	Description	Default
0	R/W	CIS1_CH_1/4 Setting Selection Register 0: CIS1_CH_1 Register Setting 1: CIS1_CH_4 Register Setting Note: CIS1_CH_1/CIS1_CH_4 Setting on register P3_00~P3_03 is set by this bit.	0

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- **Address P4_00h: TG MODE Output Selection Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R/W	TG CIS1/2 Mode On/Off Selection 0: CIS1 1: CIS2 Note: P4_01~P4_04 Mode On/Off for individual CIS1/CIS2 is set by this register.	0
3-2	R/W	TG CIS2 Mode Selection 2'h0: TG_MODE 2'h1: ~TG_MODE 2'h2: TG_MODE = 0 2'h3: TG_MODE = 1	0h
1-0	R/W	TG CIS1 Mode Selection 2'h0: TG_MODE 2'h1: ~TG_MODE 2'h2: TG_MODE = 0 2'h3: TG_MODE = 1	0h

- **Address P4_01h: TG CIS1/CIS2 MODE On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Mode On Time Most Significant Bits This selects the pixel count at which the Mode output goes high	0h/0h

- **Address P4_02h: TG CIS1/CIS2 MODE On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Mode On Time Least Significant Byte This selects the pixel count at which the Mode output goes high	00h/00h

- **Address P4_03h: TG CIS1/CIS2 MODE Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Mode Off Time Most Significant Bits This selects the pixel count at which the Mode output goes low	0h/0h

- **Address P4_04h: TG CIS1/CIS2 MODE Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Mode Off Time Least Significant Byte This selects the pixel count at which the Mode output goes low	00h/00h

- **Address P4_05h: SI MODE Selection Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-2	R/W	SI Master/Slave/Continuous Selection 00: SP and LAMP generated by external wheel.TG runs in Slave mode, with SI and LAMP triggered by an external pulse on the ROLLER_IN pin 01: Auto generated SI and LAMP.TG runs in Master mode, with SI and LAMP generated internally with a programmable period and width 11: SI automatic generated and LAMP generated by external wheel 10: Reserved	11
1-0	R/W	SI Output Mode 00: SI Output = SI 01: SI Output = ~SI 10: SI Output = 0 11: SI Output = 1	00h

- **Address P4_06h: SI Width Register**

Bit	Mode	Description	Default
7-0	R/W	SI Pulse Width SI Pulse Width = (2×[7:0]) + 1	04h

- **Address P4_07h: TG_1 Line End MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	
5-0	R/W	TG1 Line End Value – Most Significant 6 Bits Selects the pixel count where the current line has ended and the next one begins. Controls the integration time of one line and period between the SP pulses.	00h

- **Address P4_08h: TG_1 Line End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	TG1 Line End Value – Least Significant Byte Selects the pixel count where the current line has ended and next one begins. Controls the integration time of one line and the period between the SP pulses, which is (0 – 16383) pixels.	20h

- **Address P4_09h: TG_2 Line End MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	
5-0	R/W	TG_2 Line End Value – Most Significant 6 Bits Selects the pixel count where the current line is ended and next one begins. Controls the integration time of one line and the period between the SP pulses.	00

- **Address P4_0Ah: TG_2 Line End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	TG_2 Line End Value – Least Significant Byte Selects the pixel count where the current line is ended and next one begins. Controls the integration time of one line and the period between the SP pulses, which is (0 – 16383) pixels. Note: This is the 2nd set of TG, and only the 80pin package is required to program it. TG1, TG2 Line start and Line end must be equal.	20h

- **Address P4_0Bh: Frame Start/End Selection Register**

Bit	Mode	Description	Default
7	R0	Frame Jam status 0: Normal 1: Frame jam	-
6	R/W	Sensor Domination Selection for Frame End by Fix Length and auto detection 0: CIS1 1: CIS2	0
5-4	R/W	Frame End Selection 00: By SPI 01: Auto detection 10: Frame Fixed length 11: By Pad "FRAME_START" low level Notes: 1. When P2_01 Bit1 or Bit5 is active, Frame End will take effect and vice versa. 2. Frame End selection is by Pad "FRAME_START" low level, Frame Start selection is by Pad "FRAME_START" high level.	00
3	R/W	Frame Jam Function Enable 0: Disable 1: Enable Note: When this bit is enabled, register "P4_1A~P4_1D" should be set.	0
2	R/W	Senor Domination Selection for Frame Start by auto detection 0: CIS1 1: CIS2	0
1-0	R/W	Frame Start Selection 00: By SPI 01: Auto detection 10: By Pad "FRAME_START" pulse 11: By Pad "FRAME_START" high level Notes: 1. When P2_01 Bit1 or Bit5 is active, Frame Start will take effect and vice versa. 2. When Frame Start selection is via a Pad "FRAME_START" high level, the Frame End selection must be by a Pad "FRAME_END" low level.	00

- **Address P4_0Ch: Pixel Threshold for Auto Detection of Frame Start Register**

Bit	Mode	Description	Default
7-0	R/W	Pixel Threshold For Auto Detection Of Frame Start EX. If the background is black on register P9_01 Bit2/Bit6 and the input data is larger than or equal to pixel threshold, the input data is probably valid data. If the background is white and the input data is smaller than the pixel threshold the Input data is probably valid data	00h

- **Address P4_0Dh: Number of Pixel Per Line for Auto Detection of Frame Start MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Number Of Pixel Per Line For Auto Detection Of Frame Start	0h

- **Address P4_0Eh: Number of Pixel Per Line for Auto Detection of Frame Start LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Number Of Pixel Per Line For Auto Detection Of Frame Start Notes: 1. Checking how many pixels should meet register P4_0C. 2. Pixel comparison region are referenced by register P9_08~P9_0F and P4_0B bit[2].	00h

- **Address P4_0Fh: Number of Lines for Auto Detection of Frame Start MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Line order restart enable after auto detection of frame start 0: Disable 1: Enable Note: If the line order is R, G, B, IR, UV then when this bit is enabled, the line sequence order restarts after detection of a frame start.	1
4	R/W	Continuous Line meets line threshold enable for auto detection of frame start 0: Disable 1: Enable	1
3-0	R/W	Number Of Lines For Auto Detection Of Frame Start	0h

- **Address P4_10h: Number of Lines for Auto Detection of Frame Start LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Number Of Lines For Auto Detection Of Frame Start Checking how many lines should meet register P4_0D, P4_0E	00h

- **Address P4_11h: Pixel Threshold for Auto Detection of Frame End Register**

Bit	Mode	Description	Default
7-0	R/W	Pixel Threshold For Auto Detection Of Frame End Ex: If background is black on register P9_01 Bit2/Bit6 and input data is smaller than the pixel threshold, the input data is probably invalid data. If the background is white and the input data is larger than the pixel threshold, the input data is probably invalid data	00h

- **Address P4_12h: Number of Pixel Per Line for Auto Detection of Frame End MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Number Of Pixels Per Line For Auto Detection Of Frame End Checking how many pixels should meet register P4_11	00h

- **Address P4_13h: Number of Pixel Per Line for Auto Detection of Frame End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Number Of Pixels Per Line For Auto Detection Of Frame End 2. Pixel comparison regions are referenced by register P9_08~P9_0F and P4_0B bit[6]	00h

- **Address P4_14h: Number of Lines for Auto Detection of Frame End MSB Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R/W	Continuous Line meets the line threshold enable for auto detection of frame end 0: Disable 1: Enable	0
3-0	R/W	Number Of Lines For Auto Detection Of Frame End	0h

- **Address P4_15h: Number of Lines for Auto Detection of Frame End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Number of Lines for Auto Detection of Frame End Checking how many lines should meet register P4_12,P4_13	00h

- **Address P4_16h: Delay Lines for Starting Detection of Frame End MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Delay Lines for Starting Detection of Frame End Most Significant Byte	00h

- **Address P4_17h: Delay Lines for Starting Detection of Frame End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Delay Lines for Starting Detection Of Frame End Least Significant Byte Note: This register is only effective for Frame Start By Pad FRAME_START or spi on and Frame end by auto detection.	00h

- **Address P4_18h: Number of Lines for Fix Length of Frame End MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Delay Lines for Fixed Length of Frame End Most Significant Byte	0h

- **Address P4_19h: Number of Lines for Fix Length of Frame End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Delay Lines for Fixed Length of Frame End Least Significant Byte Note: This register is only effective by choosing frame end with fix length on register P4_0B[5:4].	00h

- **Address P4_1Ah: Frame Jam Counter Register 0**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Frame Jam Counter[27:24] due to wheel stock by pixel clock Note: If wheel is not detected after a frame jam counter meet, the TG controller will not be activated.	0h

- **Address P4_1Bh: Frame Jam Counter Register 1**

Bit	Mode	Description	Default
7-0	R/W	Frame Jam Counter[23:16] due to wheel stock by pixel clock Note: If wheel is not detected after a frame jam counter meet, the TG controller will not be activated.	00h

- **Address P4_1Ch: Frame Jam Counter Register 2**

Bit	Mode	Description	Default
7-0	R/W	Frame Jam Counter[15:8] due to wheel stock by pixel clock Note: If wheel is not detected after a frame jam counter meet, the TG controller will not be activated.	00h

- **Address P4_1Dh: Frame Jam Counter Register 3**

Bit	Mode	Description	Default
7-0	R/W	Frame Jam Counter[7:0] due to wheel stock by pixel clock Note: If wheel is not detected after a frame jam counter meet, the TG controller will not be activated.	00h

Page 5 Register – CIS 1 LAMP Control

- **Address P5_00h: CIS1 LAMP Mode Register**

Bit	Mode	Description	Default
7	R/W	$LAMP_R$ Normal State 0: Low 1: High	0
6	R/W	$LAMP_G$ Normal State 0: Low 1: High	0

Bit	Mode	Description	Default
5	R/W	$LAMP_B$ Normal State 0: Low 1: High	0
4	R/W	$LAMP_{IR1}$ Normal State 0: Low 1: High	0
3	R/W	$LAMP_{IR2}$ Normal State 0: Low 1: High	0
2	R/W	$LAMP_{UV}$ Normal State 0: Low 1: High	0
1-0	—	Reserved	—

- **Address P5_01h: CIS1 Component 1/Component 7 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	1/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled Note: If CIS 1 sequence W W W IR W W W UV Setting sequence length register on P2_00 bit[3:0] → 4'h04 Setting multiplication register on P2_03 bit[0] → 1'h1 Setting component selection register on P2_16 bit[5-0] → 6'h0 and component 1 LAMP at P5_01h bit[5-0] → 6'h38 d. Component 2 LAMP at P5_02h bit[5-0] → 6'h38 e. Component 3 LAMP at P5_03h bit[5-0] → 6'h38 f. Component 4 LAMP at P5_04h bit[5-0] → 6'h04 g. Component 5 LAMP at P5_05h bit[5-0] → 6'h38 h. Component 6 LAMP at P5_06h bit[5-0] → 6'h38 Setting component selection register on P2_16 bit[1-0] → 3'h3 and component 7 LAMP at P5_01h bit[5-0] → 6'h38 Component 8 LAMP at P5_02h bit[5-0] → 6'h01	0/0

- **Address P5_02h: CIS1 Component 2/Component 8 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	1/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	0/0

- **Address P5_03h: CIS1 Component 3/ Component 9 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	1/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	0/0

- **Address P5_04h: CIS1 Component 4/ Component 10 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0

Bit	Mode	Description	Default
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	1/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	0/0

- **Address P5_05h: CIS1 Component 5/ Component 11 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	1/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	0/0

- **Address P5_06h: CIS1 Component 6/Component 12 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	1/0

- **Address P5_07h: CIS1 Red LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_R$ On Time Most Significant Byte This selects the pixel count at which the LAMPR output goes high.	0h

- **Address P5_08h: CIS1 Red LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_R$ On Time Least Significant Bits. This selects the pixel count at which the LAMPR output goes high. Note: Real CIS1 Lampr on position = Lampr on register × 4.	2Eh

- **Address P5_09h: CIS1 Red LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_R$ Off Time Most Significant Byte This selects the pixel count at which the LAMPR output goes low.	1h

- **Address P5_0Ah: CIS1 Red LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_R$ Off Time Least Significant Bits This selects the pixel count at which the LAMPR output goes low. Note: Real CIS1 Lampr off position = Lampr off register × 4.	06h

- **Address P5_0Bh: CIS1 Green LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_G$ On Time Most Significant Byte This selects the pixel count at which the LAMPG output goes high.	0h

- **Address P5_0Ch: CIS1 Green LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_G$ On Time Least Significant Bits This selects the pixel count at which the LAMPG output goes high. Note: Real CIS1 Lampg on position = Lampg on register × 4.	2Eh

- **Address P5_0Dh: CIS1 Green LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_G$ Off Time Most Significant Byte This selects the pixel count at which the LAMPG output goes low.	1h

- **Address P5_0Eh: CIS1 Green LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_G$ Off Time Least Significant Bits This selects the pixel count at which the LAMPG output goes low. Note: Real CIS1 Lampg off position = Lampg off register × 4.	06h

- **Address P5_0Fh: CIS1 Blue LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_B$ On Time Most Significant Byte This selects the pixel count at which the LAMPB output goes high.	0h

- **Address P5_10h: CIS1 Blue LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_B$ On Time Least Significant Bits This selects the pixel count at which the LAMPB output goes high. Note: Real CIS1 Lampb on position = Lampb on register × 4.	2Eh

- **Address P5_11h: CIS1 Blue LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_B$ Off Time Most Significant Byte This selects the pixel count at which the LAMPB output goes low.	1h

- **Address P5_12h: CIS1 Blue LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_B$ Off Time Least Significant Bits This selects the pixel count at which the LAMPB output goes low. Note: Real CIS1 Lampb off position = Lampb off register × 4..	06h

- **Address P5_13h: CIS1 IR1 LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR1}$ On Time Most Significant Byte This selects the pixel count at which the LAMPIR output goes high.	0h

- **Address P5_14h: CIS1 IR1 LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR1}$ On Time Least Significant Bits This selects the pixel count at which the LAMPIR output goes high. Note: Real CIS1 Lampir1 on position = Lampir1 on register × 4.	2Eh

- **Address P5_15h: CIS1 IR1 LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR1}$ Off Time Most Significant Byte This selects the pixel count at which the LAMPIR output goes low.	1h

- **Address P5_16h: CIS1 IR1 LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR1}$ Off Time Least Significant Bits This selects the pixel count at which the LAMPIR output goes low. Note: Real CIS1 Lampir1 off position = Lampir1 off register × 4.	06h

- **Address P5_17h: CIS1 IR2 LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR2}$ On Time Most Significant Byte This selects the pixel count at which the LAMPIR output goes high.	0h

- **Address P5_18h: CIS1 IR2 LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR2}$ On Time Least Significant Bits This selects the pixel count at which the LAMPIR output goes high. Note: Real CIS1 Lampir2 on position = Lampir2 on register × 4.	2Eh

- **Address P5_19h: CIS1 IR2 LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR2}$ Off Time Most Significant Byte This selects the pixel count at which the LAMPIR output goes low.	1h

- **Address P5_1Ah: CIS1 IR2 LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR2}$ Off Time Least Significant Bits This selects the pixel count at which the LAMPIR output goes low. Note: Real CIS1 Lampir2 off position = Lampir2 off register × 4.	06h

- **Address P5_1Bh: CIS1 UV LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{UV}$ On Time Most Significant Byte This selects the pixel count at which the LAMPUV output goes high.	0h

- **Address P5_1Ch: CIS1 UV LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{UV}$ On Time Least Significant Bits This selects the pixel count at which the LAMPUV output goes high. Note: Real CIS1 Lampuv on position = Lampuv on register × 4.	2Eh

- **Address P5_1Dh: CIS1 UV LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{UV}$ Off Time Most Significant Byte This selects the pixel count at which the LAMPUV output goes low.	1h

- **Address P5_1Eh: CIS1 UV LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{UV}$ Off Time Least Significant Bits This selects the pixel count at which the LAMPUV output goes low. Note: Real CIS1 Lampuv off position = Lampuv off register × 4.	06h

Page 6 Register – CIS 2 LAMP Control

- **Address P6_00h: CIS2 LAMP Mode Register**

Bit	Mode	Description	Default
7	R/W	$LAMP_{R}$ Normal State 0: Low 1: High	0
6	R/W	$LAMP_{G}$ Normal State 0: Low 1: High	0
5	R/W	$LAMP_{B}$ Normal State 0: Low 1: High	0
4	R/W	$LAMP_{IR1}$ Normal State 0: Low 1: High	0
3	R/W	$LAMP_{IR2}$ Normal State 0: Low 1: High	0
2	R/W	$LAMP_{UV}$ Normal State 0: Low 1: High	0

Bit	Mode	Description	Default
1-0	—	Reserved	—

- **Address P6_01h: CIS2 Component 1 / Component 7 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	1/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled Note: If CIS 2 sequence W W W IR W W W UV Setting sequence length register on P2_00 bit[7:4] → 4'h04 Setting multiplication register on P2_03 bit[1] → 1'h1 Setting component selection register on P2_12 bit[5-0] → 6'h0 and Component 1 LAMP at P6_01h bit[5-0] → 6'h38 Component 2 LAMP at P6_02h bit[5-0] → 6'h38 Component 3 LAMP at P6_03h bit[5-0] → 6'h38 Component 4 LAMP at P6_04h bit[5-0] → 6'h04 Component 5 LAMP at P6_05h bit[5-0] → 6'h38 Component 6 LAMP at P6_06h bit[5-0] → 6'h38 Setting component selection register on P2_17 bit[1-0] → 3'h1 and Component 7 LAMP at P6_01h bit[5-0] → 6'h38 Component 8 LAMP at P6_02h bit[5-0] → 6'h01	0/0

- **Address P6_02h: CIS2 Component 2 / Component 8 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	1/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	0/0

- **Address P6_03h: CIS2 Component 3 / Component 9 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	1/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	0/0

- **Address P6_04h: CIS2 Component 4 / Component 10 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	1/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	0/0

- **Address P6_05h: CIS2 Component 5 / Component 11 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0

Bit	Mode	Description	Default
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	1/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	0/0

- **Address P6_06h: CIS2 Component 6 / Component 12 Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable 0: Red Disabled 1: Red Enabled	0/0
4	R/W	Green LAMP Enable 0: Green Disabled 1: Green Enabled	0/0
3	R/W	Blue LAMP Enable 0: Blue Disabled 1: Blue Enabled	0/0
2	R/W	IR1 LAMP Enable 0: IR1 Disabled 1: IR1 Enabled	0/0
1	R/W	IR2 LAMP Enable 0: IR2 Disabled 1: IR2 Enabled	0/0
0	R/W	UV LAMP Enable 0: UV Disabled 1: UV Enabled	1/0

- **Address P6_07h: CIS2 Red LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_R$ On Time Most Significant Byte This selects the pixel count at which the LAMPR output goes high.	0h

- **Address P6_08h: CIS2 Red LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_R$ On Time Least Significant Bits. This selects the pixel count at which the LAMPR output goes high. Note: Real CIS2 Lampr on position = Lampr on register × 4.	2Eh

- **Address P6_09h: CIS2 Red LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_R$ Off Time Most Significant Byte This selects the pixel count at which the LAMPR output goes low.	1h

- **Address P6_0Ah: CIS2 Red LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_R$ Off Time Least Significant Bits This selects the pixel count at which the LAMPR output goes low. Note: Real CIS2 Lampr off position = Lampr off register × 4.	06h

- **Address P6_0Bh: CIS2 Green LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_G$ On Time Most Significant Byte This selects the pixel count at which the LAMPG output goes high.	0h

- **Address P6_0Ch: CIS2 Green LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_G$ On Time Least Significant Bits This selects the pixel count at which the LAMPG output goes high. Note: Real CIS2 Lampg on position = Lampg on register × 4.	2Eh

- **Address P6_0Dh: CIS2 Green LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_G$ Off Time Most Significant Byte This selects the pixel count at which the LAMPG output goes low.	1h

- **Address P6_0Eh: CIS2 Green LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_G$ Off Time Least Significant Bits This selects the pixel count at which the LAMPG output goes low. Note: Real CIS2 Lampg off position = Lampg off register × 4.	06h

- **Address P6_0Fh: CIS2 Blue LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_B$ On Time Most Significant Byte This selects the pixel count at which the LAMPB output goes high.	0h

- **Address P6_10h: CIS2 Blue LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_B$ On Time Least Significant Bits This selects the pixel count at which the LAMPB output goes high. Note: Real CIS2 Lampb on position = Lampb on register × 4.	2Eh

- **Address P6_11h: CIS2 Blue LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_B$ Off Time Most Significant Byte This selects the pixel count at which the LAMPB output goes low.	1h

- **Address P6_12h: CIS2 Blue LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_B$ Off Time Least Significant Bits This selects the pixel count at which the LAMPB output goes low. Note: Real CIS2 Lampb off position = Lampb off register × 4.	06h

- **Address P6_13h: CIS2 IR1 LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR1}$ On Time Most Significant Byte This selects the pixel count at which the LAMPIR output goes high.	0h

- **Address P6_14h: CIS2 IR1 LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR1}$ On Time Least Significant Bits This selects the pixel count at which the LAMPIR output goes high. Note: Real CIS2 Lampir1 on position = Lampir1 on register × 4.	2Eh

- **Address P6_15h: CIS2 IR1 LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR1}$ Off Time Most Significant Byte This selects the pixel count at which the LAMPIR output goes low.	1h

- **Address P6_16h: CIS2 IR1 LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR1}$ Off Time Least Significant Bits This selects the pixel count at which the LAMPIR output goes low. Note: Real CIS2 Lampir1 off position = Lampir1 off register × 4.	06h

- **Address P6_17h: CIS2 IR2 LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR2}$ On Time Most Significant Byte This selects the pixel count at which the LAMPIR output goes high.	0h

- **Address P6_18h: CIS2 IR2 LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR2}$ On Time Least Significant Bits This selects the pixel count at which the LAMPIR output goes high. Note: Real CIS2 Lampir2 on position = Lampir2 on register × 4.	2Eh

- **Address P6_19h: CIS2 IR2 LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR2}$ Off Time Most Significant Byte This selects the pixel count at which the LAMPIR output goes low.	1h

- **Address P6_1Ah: CIS2 IR2 LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR2}$ Off Time Least Significant Bits This selects the pixel count at which the LAMPIR output goes low. Note: Real CIS2 Lampir2 off position = Lampir2 off register × 4.	06h

- **Address P6_1Bh: CIS2 UV LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{UV}$ On Time Most Significant Byte This selects the pixel count at which the LAMPUV output goes high.	0h

- **Address P6_1Ch: CIS2 UV LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{UV}$ On Time Least Significant Bits This selects the pixel count at which the LAMPUV output goes high. Note: Real CIS2 Lampuv on position = Lampuv on register × 4.	2Eh

- **Address P6_1Dh: CIS2 UV LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{UV}$ Off Time Most Significant Byte This selects the pixel count at which the LAMPUV output goes low.	1h

- **Address P6_1Eh: CIS2 UV LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{UV}$ Off Time Least Significant Bits This selects the pixel count at which the LAMPUV output goes low. Note: Real CIS2 Lampuv off position = Lampuv off register × 4.	06h

Page 7 Register – CIS 1 Shading Control

- **Address P7_00h: Shading Control Register**

Bit	Mode	Description	Default
7	R/W	Data width selection 0: 8bit 1: 10bit	0
6	R/W	CIS1 Global Shading gain enable 0: Disable 1: Enable	0
5	R/W	CIS2 Global Shading gain enable 0: Disable 1: Enable	0
4-2	R/W	Component Shading gain format (fixpoint) selection 000: 2.4 001: 2.6 010: 2.8 011: Reserved 100: 3.3 101: 3.5 110: 3.7 111: Reserved	000
1	R/W	Component Shading gain enable 0: Disable 1: Enable	0
0	R/W	Dark Shading offset enable 0: Disable 1: Enable Note: Disable shading while writing shading values to the Shading RAM.	0

- **Address P7_02h: Shading RAM/EMIF Combination Select Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Shading RAM/EMIF Component Select 0000: CIS1 Shading Offset 0001: CIS1 Combination1 Shading Gain 0010: CIS1 Combination2 Shading Gain 0011: CIS1 Combination3 Shading Gain 0100: CIS1 Combination4 Shading Gain 0101: CIS1 Combination5 Shading Gain 0110: CIS1 Combination6 Shading Gain 0111: Reserved 1000: CIS2 Shading Offset 1001: CIS2 Combination1 Shading Gain 1010: CIS2 Combination2 Shading Gain 1011: CIS2 Combination3 Shading Gain 1100: CIS2 Combination4 Shading Gain 1101: CIS2 Combination5 Shading Gain 1110: CIS2 Combination6 Shading Gain 1111: Reserved Notes: 1. If Light sequence is "R G B IR1 IR2" CIS Component 1 → R and CIS Combination 1 → R CIS Component 2 → G and CIS Combination 2 → G CIS Component 3 → B and CIS Combination 3 → B CIS Component 4 → IR1 and CIS Combination 4 → IR1 CIS Component 5 → IR2 and CIS Combination 5 → IR2 2. If Light sequence is "W W W IR1 W W W IR2" CIS Component 1 → W (R+G+B) and CIS Combination 1 → W CIS Component 2 → W (R+G+B) and CIS Combination 2 → IR1 CIS Component 3 → W (R+G+B) and CIS Combination 3 → IR2 CIS Component 4 → IR1 CIS Component 5 → W (R+G+B) CIS Component 6 → W (R+G+B) CIS Component 7 → W (R+G+B) CIS Component 8 → IR2	0h

- **Address P7_03h: Shading RAM/DSP Start Address MSB Register**

Bit	Mode	Description	Default
7-3	R/W	Reserved	—
2-0	R/W	Shading RAM/DSP Start Address Most Significant Byte	0h

- **Address P7_04h: Shading RAM/DSP Start Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Shading RAM /DSP Start Address Least Significant Byte	00h

- **Address P7_05h: Shading RAM/DSP Transfer Count MSB Register**

Bit	Mode	Description	Default
7-3	R/W	Reserved	—
2-0	R/W	Shading RAM/DSP Transfer Count Most Significant Byte	0h

- **Address P7_06h: Shading RAM/DSP Transfer Count LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Shading RAM/DSP Transfer Count Least Significant Byte	00h

- **Address P7_07h: CIS1 Global Shading gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	CIS1 Global Shading gain Coefficient	00h

- **Address P7_08h: CIS2 Global Shading gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	CIS2 Global Shading gain Coefficient	00h

- **Address P7_0Ah: CIS 1 Dark Shading Offset Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Dark Shading Offset Value Virtual Address Most Significant Byte. Points the write pointer to the dark shading RAM Auto increases when writing to register address 0Ch on page 7.	0h

- **Address P7_0Bh: CIS 1 Dark Shading Offset Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Dark Shading Offset Value Virtual Address Least Significant Byte. Points the write pointer to the dark shading RAM Auto increases when writing to register address 0Ch on page 7.	00h

- **Address P7_0Ch: CIS 1 Dark Shading Offset Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Dark Shading Offset Coefficient for CIS 1 Writing value to this register will store the value to Points shading RAM, and the address is specified by register address 0Ah & 0Bh on page 7.	00h

- **Address P7_0Dh: CIS 1 Combination 1 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 1 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 0Fh on page 7.	00h

- **Address P7_0Eh: CIS 1 Combination 1 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 1 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 0Fh on page 7.	00h

- **Address P7_0Fh: CIS 1 Combination 1 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 1 Shading Gain Coefficient for CIS 1 Writing value to this register will store the value to the shading RAM, and the address is specified by register address 0Dh & 0Eh on page 7 Notes: 1. If Light sequence is "R G B IR1 IR2" CIS Component 1 → R and CIS Combination 1 → R CIS Component 2 → G and CIS Combination 2 → G CIS Component 3 → B and CIS Combination 3 → B CIS Component 4 → IR1 and CIS Combination 4 → IR1 CIS Component 5 → IR2 and CIS Combination 5 → IR2 2. If Light sequence is "W W W IR1 W W W IR2" CIS Component 1 → W (R+G+B) and CIS Combination 1 → W CIS Component 2 → W (R+G+B) and CIS Combination 2 → IR1 CIS Component 3 → W (R+G+B) and CIS Combination 3 → IR2 CIS Component 4 → IR1 CIS Component 5 → W (R+G+B) CIS Component 6 → W (R+G+B) CIS Component 7 → W (R+G+B) CIS Component 8 → IR2 3. Read / write sequence Gain coefficient MSB XXXXXX0000000000 LSB first r/w second r/w Must read/write twice for one pixel gain coefficient.	00h

- **Address P7_10h: CIS 1 Combination 2 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 2 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 12h on page 7.	0h

- **Address P7_11h: CIS 1 Combination 2 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 2 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 12h on page 7.	00h

- **Address P7_12h: CIS 1 Combination 2 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 2 Shading Gain Coefficient for CIS 1 Writing to this register will store the value to Points shading RAM, and the address is specified by register address 10h & 11h on page 7.	00h

- **Address P7_13h: CIS 1 Combination 3 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 3 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 15h on page 7.	0h

- **Address P7_14h: CIS 1 Combination 3 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 3 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 15h on page 7.	00h

- **Address P7_15h: CIS 1 Combination 3 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 3 Shading Gain Coefficient for CIS 1 Writing to this register will store the value to the shading RAM, and the address is specified by register address 13h & 14h on page 7.	00h

- **Address P7_16h: CIS 1 Combination 4 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 4 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 18h on page 7.	0h

- **Address P7_17h: CIS 1 Combination 4 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 4 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 18h on page 7.	00h

- **Address P7_18h: CIS 1 Combination 4 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 4 Shading Gain Coefficient for CIS 1 Writing to this register will store the value to the shading RAM, and the address is specified by register address 16h & 17h on page 7.	00h

- **Address P7_19h: CIS 1 Combination 5 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 5 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 1Bh on page 7.	0h

- **Address P7_1Ah: CIS 1 Combination 5 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 1Bh on page 7.	00h

- **Address P7_1Bh: CIS 1 Combination 5 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Coefficient for CIS 1 Writing value to this register will store the value to the shading RAM, and the address is specified by register address 19h & 1Ah on page 7	00h

- **Address P7_1Ch: CIS 1 Combination 6 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 6 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 1Eh on page 7.	0h

- **Address P7_1Dh: CIS 1 Combination 6 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 1Eh on page 7.	00h

- **Address P7_1Eh: CIS 1 Combination 6 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Coefficient for CIS 1 Writing value to this register will store the value to the shading RAM, and the address is specified by register address 1Ch & 1Dh on page 7	00h

Page 8 Register – CIS 2 Shading Control

- **Address P8_00h: CIS 2 Dark Shading Offset Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Shading Offset Value Virtual Address Most Significant Byte. Points the write pointer to the dark shading RAM Auto increases when writing to register address 02h on page 8.	0h

- **Address P8_01h: CIS 2 Dark Shading Offset Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Dark Shading Offset Value Virtual Address Least Significant Byte. Points the write pointer to the dark shading RAM Auto increases when writing to register address 02h on page 8.	00h

- **Address P8_02h: CIS 2 Dark Shading Offset Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Dark Shading Offset Coefficient for CIS 2 Writing value to this register will store the value to the shading RAM, and the address is specified by register address 00h & 01h on page 8	00h

- **Address P8_03h: CIS 2 Combination 1 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 1 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 05h on page 8.	0h

- **Address P8_04h: CIS 2 Combination 1 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 1 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 05h on page 8.	00h

- **Address P8_05h: CIS 2 Combination 1 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 1 Shading Gain Coefficient for CIS 2 Writing to this register will store the value to the shading RAM, and the address is specified by register address 03h & 04h on page 8.	00h

- **Address P8_06h: CIS 2 Combination 2 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 2 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 08h on page 8.	0h

- **Address P8_07h: CIS 2 Combination 2 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 2 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 08h on page 8.	00h

- **Address P8_08h: CIS 2 Combination 2 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 2 Shading Gain Coefficient for CIS 2 Writing to this register will store the value to the shading RAM, and the address is specified by register address 06h & 07h on page 8.	00h

- **Address P8_09h: CIS 2 Combination 3 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 3 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 0Bh on page 8.	0h

- **Address P8_0Ah: CIS 2 Combination 3 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 3 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 0Bh on page 8.	00h

- **Address P8_0Bh: CIS 2 Combination 3 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 3 Shading Gain Coefficient for CIS 2 Writing value to this register will store the value to the shading RAM, and the address is specified by register address 09h & 0Ah on page 8.	00h

- **Address P8_0Ch: CIS 2 Combination 4 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 4 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 0Eh on page 8.	0h

- **Address P8_0Dh: CIS 2 Combination 4 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 4 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 0Eh on page 8.	00h

- **Address P8_0Eh: CIS 2 Combination 4 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 4 Shading Gain Coefficient for CIS 2 Writing value to this register will store the value to the shading RAM, and the address is specified by register address 0Ch & 0Dh on page 8.	00h

- **Address P8_0Fh: CIS 2 Combination 5 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 5 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 11h on page 8.	0h

- **Address P8_10h: CIS 2 Combination 5 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 11h on page 8.	00h

- **Address P8_11h: CIS 2 Combination 5 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Coefficient for CIS 2 Writing value to this register will store the value to the shading RAM, and the address is specified by register address 0Fh & 10h on page 8	00h

- **Address P8_12h: CIS 2 Combination 6 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 6 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 11h on page 8.	0h

- **Address P8_13h: CIS 2 Combination 6 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 6 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increases when writing to register address 11h on page 8.	00h

- **Address P8_14h: CIS 2 Combination 6 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 6 Shading Gain Coefficient for CIS 2 Writing value to this register will store the value to shading RAM, and the address is specified by register address 0Fh & 10h on page 8.	00h

Page 9 Register – ISP Control Registers

- **Address P9_00h: ISP Control 0 Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3	R/W	ISP1 (positive page) Background Color Selection 0: Black 1: White	0
2	R/W	ISP2 (negative page) Background Color Selection 0: Black 1: White	0
1	R/W	Line Information Position 0: End of data 1: Front of data	0
0	R/W	Line Information Enable 0: Disable 1: Enable	0

- **Address P9_01h: ISP Control 1 Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3	R/W	ISP1 (positive page) Image Sharpness Enable	0
2	R/W	ISP1 (positive page) Image Mirror Enable	0
1	R/W	ISP1 (positive page) Line Border De-noise Enable	0
0	R/W	ISP1 (positive page) Data De-noise Enable	0

- **Address P9_02h: ISP Control 2 Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3	R/W	ISP2 (negative page) Image Sharpness Enable	0
2	R/W	ISP2 (negative page) Image Mirror Enable	0
1	R/W	ISP2 (negative page) Line Border De-noise Enable	0
0	R/W	ISP2 (negative page) Data De-noise Enable	0

- **Address P9_03h: Line Information Control 0 Register**

Bit	Mode	Description	Default
7	R/W	ISP1 (positive page) Line Number Calculation Enable 0: Disable 1: Enable	0
6	R/W	ISP1 (positive page) Line Color Calculation Enable 0: Disable 1: Enable	0
5	R/W	ISP1 (positive page) Line Max/MIN/SUM Calculation Enable 0: Disable 1: Enable	0
4	R/W	ISP1 (positive page) Line Border Calculation Enable 0: Disable 1: Enable	0
3	R/W	ISP1 (positive page) Line Histogram Calculation Enable 0: Disable 1: Enable	0
2	R/W	ISP1 (positive page) Wheel Counter Calculation Enable 0: Disable 1: Enable	0

Bit	Mode	Description	Default
1-0	R/W	ISP1 (positive page) Wheel Information Calculation Enable 00: Disable 01: The SI number of current line 10: The sum of SI in previous wheel step 11: Reserved	00

- **Address P9_04h: Line Information Control 1 Register**

Bit	Mode	Description	Default
7	R/W	ISP2 (negative page) Line Number Calculation Enable 0: Disable 1:Enable	0
6	R/W	ISP2 (negative page) Line Color Calculation Enable 0: Disable 1: Enable	0
5	R/W	ISP2 (negative page) Line Max/MIN/SUM Calculation Enable 0: Disable 1: Enable	0
4	R/W	ISP2 (negative page) Line Border Calculation Enable 0: Disable 1: Enable	0
3	R/W	ISP2 (negative page) Line Histogram Calculation Enable 0: Disable 1: Enable	0
2	R/W	ISP2 (negative page) Wheel Counter Calculation Enable 0: Disable 1: Enable	0
1-0	R/W	ISP2 (negative page) Wheel Information Calculation Enable 00: Disable 01: The SI number of the current line 10: The sum of SI in previous wheel step 11: Reserved	00

- **Address P9_05h: Line Border Control 0 Register**

Bit	Mode	Description	Default
7	R/W	Line Border Algorithm Selection 0: Two windows differential comparison 1: Continuous pixel detection with static threshold	0
6-4	R/W	Continuous Pixel Selection 000: 1 pixel 001: 2 pixels 010: 3 pixels 011: 4 pixels 100: 5 pixel 101: 6 pixels 110: 7 pixels 111: 8 pixels How many continuous pixels fit the static threshold	011
3-2	—	Reserved	—
1	R/W	Big Window Width Selection 0: 6 pixels 1: 8 pixels	0
0	R/W	Small Window Width Selection 0: 3 pixels 1: 4 pixels	0

- **Address P9_06h: Line Border Control 1 Register**

Bit	Mode	Description	Default
7-6	R/W	ISP1 Left Border Detection Range Selection 00: 144 pixels 01: 288 pixels 10: 432 pixels 11: 576 pixels ISP hardware will detect image left border from ISP1 valid range start address (set in P9_16[6:4] and P9_17) to 144/288/432/576 pixels by selection.	10
5-4	R/W	ISP1 Right Border Detection Range Selection 00: 144 pixels 01: 288 pixels 10: 432 pixels 11: 576 pixels ISP hardware will detect image right border before ISP1 valid range end address (set in P9_16[2:0] and P9_18) with 144/288/432/576 pixels by selection.	10
3-2	R/W	ISP2 Left Border Detection Range Selection 00: 144 pixels 01: 288 pixels 10: 432 pixels 11: 576 pixels ISP hardware will detect image left border from ISP2 valid range start address (set in P9_19[6:4] and P9_1A) to 144/288/432/576 pixels by selection.	10
1-0	R/W	ISP2 Right Border Detection Range Selection 00: 144 pixels 01: 288 pixels 10: 432 pixels 11: 576 pixels ISP hardware will detect image right border before ISP2 valid range end address (set in P9_19[2:0] and P9_1B) with 144/288/432/576 pixels by selection.	10

- **Address P9_0Ah: ISP1 Sharpness Gain 1 Register**

Bit	Mode	Description	Default
7-0	R/W	ISP1 Sharpness Gain 1 Real gain value = reg/128	40h

- **Address P9_0Bh: ISP1 Sharpness Gain 2 Register**

Bit	Mode	Description	Default
7-0	R/W	ISP1 Sharpness Gain 2 Real gain value = reg/128	40h

- **Address P9_0Ch: ISP2 Sharpness Gain 1 Register**

Bit	Mode	Description	Default
7-0	R/W	ISP2 Sharpness Gain 1 Real gain value = reg/128	40h

- **Address P9_0Dh: ISP2 Sharpness Gain 2 Register**

Bit	Mode	Description	Default
7-0	R/W	ISP2 Sharpness Gain 2 Real gain value = reg/128	40h

- **Address P9_0Eh: ISP1 Line Border Static Threshold**

Bit	Mode	Description	Default
7-0	R/W	ISP1 (positive page) Line Border Static Threshold	20h

- **Address P9_0Fh: ISP2 Line Border Static Threshold**

Bit	Mode	Description	Default
7-0	R/W	ISP2 (negative page) Line Border Static Threshold	20h

- **Address P9_10h: ISP1 Line Border Big Window Threshold**

Bit	Mode	Description	Default
7-0	R/W	ISP1 (positive page) Line Border Big Window Threshold	20h

- **Address P9_11h: ISP1 Line Border Small Window Threshold**

Bit	Mode	Description	Default
7-0	R/W	ISP1 (positive page) Line Border Small Window Threshold	8h

- **Address P9_12h: ISP2 Line Border Big Window Threshold**

Bit	Mode	Description	Default
7-0	R/W	ISP2 (positive page) Line Border Big Window Threshold	20h

- **Address P9_13h: ISP2 Line Border Small Window Threshold**

Bit	Mode	Description	Default
7-0	R/W	ISP2 (positive page) Line Border Small Window Threshold	08h

- **Address P9_16h: ISP1 Valid Range Start/End Address MSB**

Bit	Mode	Description	Default
7	—	Reserved	—
6-4	R/W	ISP1 valid range start address MSB	0h
3	—	Reserved	—
2-0	R/W	ISP1 valid range end address MSB	7h

- **Address P9_17h: ISP1 Valid Range Start Address LSB**

Bit	Mode	Description	Default
7-0	R/W	ISP1 valid range start address LSB	00h

- **Address P9_18h: ISP1 Valid Range End Address LSB**

Bit	Mode	Description	Default
7-0	R/W	ISP1 valid range end address LSB	FFh

- **Address P9_19h: ISP2 Valid Range Start/End Address MSB**

Bit	Mode	Description	Default
7	—	Reserved	—
6-4	R/W	ISP2 valid range start address MSB	0h
3	—	Reserved	—
2-0	R/W	ISP2 valid range end address MSB	7h

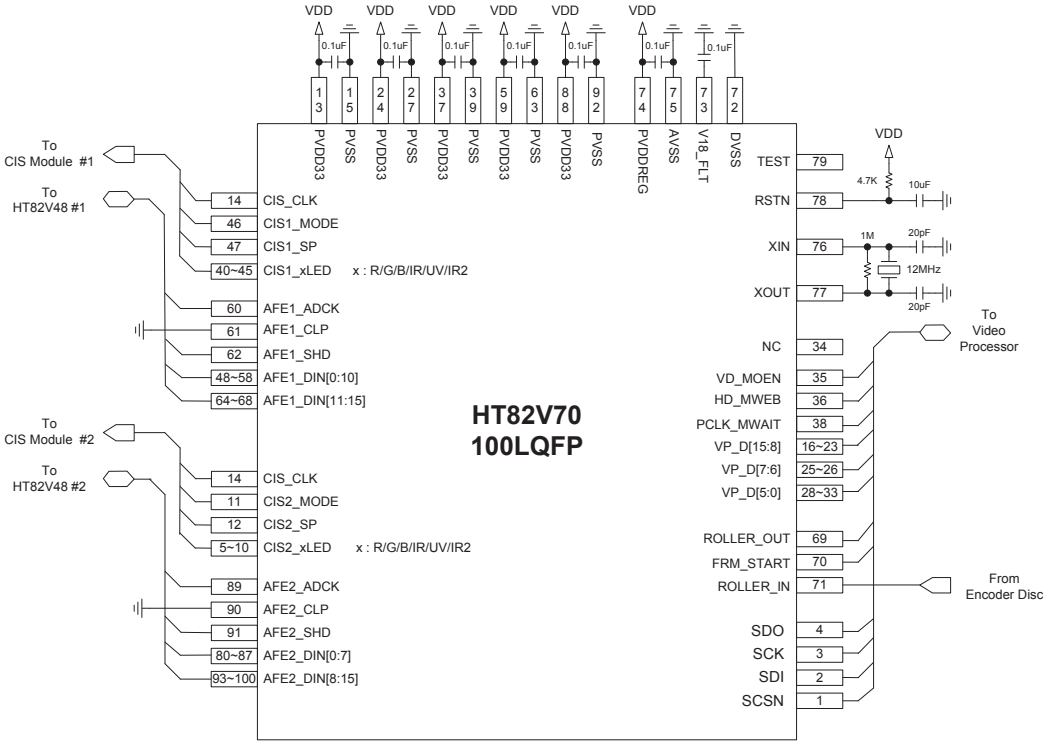
- **Address P9_1Ah: ISP2 Valid Range Start Address LSB**

Bit	Mode	Description	Default
7-0	R/W	ISP2 valid range start address LSB	00h

- **Address P9_1Bh: ISP2 Valid Range End Address LSB**

Bit	Mode	Description	Default
7-0	R/W	ISP2 valid range end address LSB	FFh

Application Circuits



Note: All de-coupling capacitors should be located as close as possible to the device DFE.

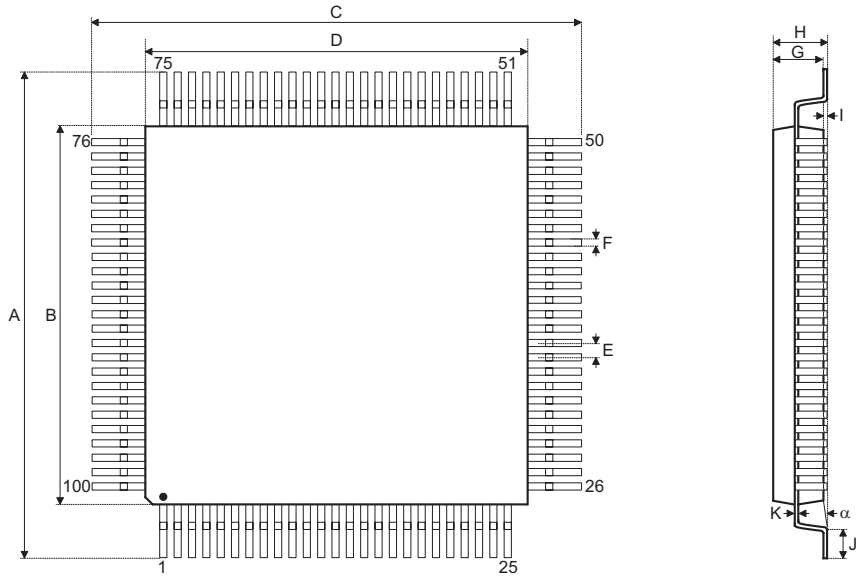
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

100-pin LQFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.630 BSC	—
B	—	0.551 BSC	—
C	—	0.630 BSC	—
D	—	0.551 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	16.00 BSC	—
B	—	14.00 BSC	—
C	—	16.00 BSC	—
D	—	14.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°