Features

- 3.3V operating voltage
- Up to 120MSPS for two 3-channel inputs
- Programmable CIS module timing generator
- 9-bit programmable gain amplifier
- 8-bit programmable offset
- 4-bit programmable line-clamping bias
- Internal voltage reference
- Image sensor shading correction
  - 0 ~ -255 8-bit dark shading (offset) correction
  - 0.00x~8.00x 10-bit white shading (gain) correction
  - Embedded memory for up to 6 component coefficients of 1584 sensor elements
- Flexible frame start/stop control mechanism
- Provide Image line information
  - line index
  - Left and right boundary of a line
  - max/min/summation/histogram information of a line
- 8/16-bit image data output in VPFE or EMIF interface
- 3-wire/4-wire SPI interface
- 2-wire I^{2}C interface
- Built in voltage comparator for roller input signal
- 64-pin TQFP-EP package

General Description

The HT82V72 is a fully integrated device for CIS imaging application. It features two high performance 16-bit 3-channel 60MSPS analog signal processors, programmable timing generator and image sensor shading correction to sample and condition the outputs of CIS (Contact Image Sensor) array for high-speed double-sided scanner applications.

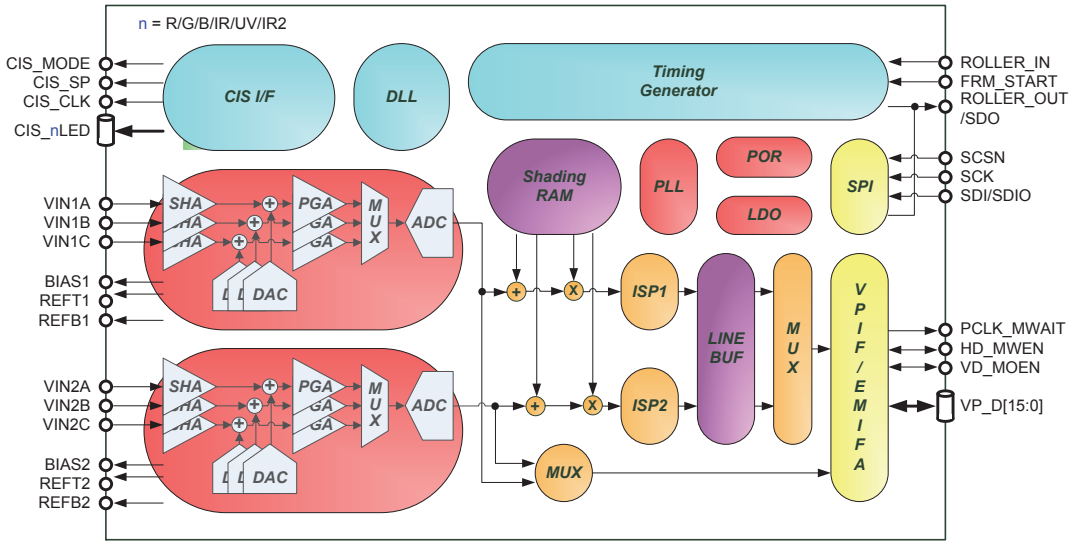
Each channel consists of a Sample and Hold Amplifier, SHA, a 9-bit Programmable Gain Amplifier, PGA, and an 8-bit offset correction Digital to Analog Converter, DAC. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for the two 3-channel analog inputs. Each the 3-channel signals are routed to a 60MHz high performance Analog to Digital converter, ADC. Then an intelligent image sensor shading correction is employed to unitize each sensor elements. The sensor data can be not only corrected but also averaged per line for black level calculation. The Video Processing Front End, VPFE, Interface multiplexes shaded ADC's outputs in a two high-bytes of each ADC's output or one 16-bit wide output of each ADC. A pixel clock PCLK transports the 16-bit wide data to the output port.

The internal registers are programmed through a 2-wire I^{2}C or 3-wire/4-wire SPI interface, for timing control, gain, offset and operating mode adjustments.

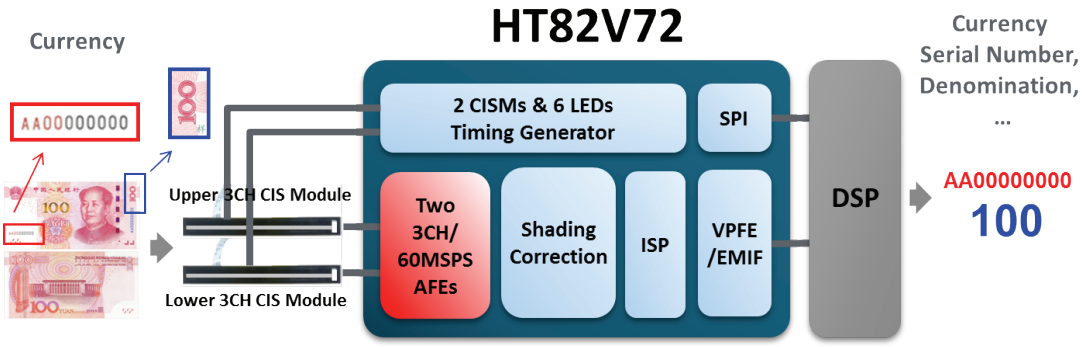
Applications

- Double-sided scanner currency detectors

Block Diagram

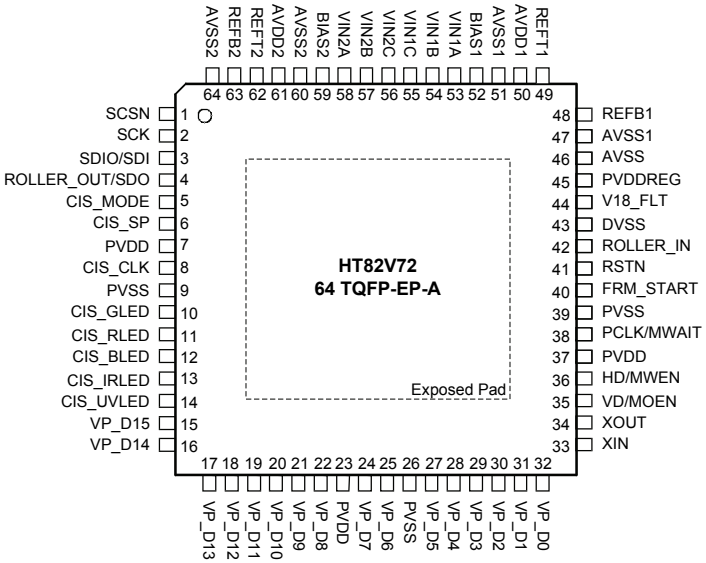


System Application Diagram



Two 3-ch CISMs System Diagram

Pin Assignment



Pin Description

Pin					Description
Name	DIR	TYP	DRV	No.	
SCSN	DI	U	—	1	SPI Chip Select, active low.
SCK	DI	U	—	2	SPI Serial Clock
SDIO/SDI	DIO	U	8	3	3-wire SPI Serial Data I/O or 4-wire SPI Serial Data input
ROLLER_OUT/SDO	DO	C	8	4	Roller Square Wave Output or 4-wire SPI Serial Data Output
CIS_MODE	DO	C	4	5	CIS Mode Select
CIS_SP	DO	C	8	6	CIS Module Start Pulse
PVDD	P	—	—	7	Pad Power Pin
CIS_CLK	DO	C	8	8	CIS Module Pixel Clock
PVSS	P	—	—	9	Pad Ground Pin
CIS_GLED	DIO	T	8	10	CIS Module Green LED Active Slot Control
CIS_RLED	DIO	T	8	11	CIS Module Red LED Active Slot Control
CIS_BLED	DIO	T	8	12	CIS Module Blue LED Active Slot Control
CIS_IRLED	DO	T	8	13	CIS Module IR LED Active Slot Control
CIS_UVLED	DO	T	8	14	CIS Module UV LED Active Slot Control
VP_D15	DIO	U	4	15	VPFE Pixel Data Output 15 or EMIFA Data 15 In/Out
VP_D14	DIO	U	4	16	VPFE Pixel Data Output 14 or EMIFA Data 14 In/Out
VP_D13	DIO	U	4	17	VPFE Pixel Data Output 13 or EMIFA Data 13 In/Out
VP_D12	DIO	U	4	18	VPFE Pixel Data Output 12 or EMIFA Data 12 In/Out
VP_D11	DIO	U	4	19	VPFE Pixel Data Output 11 or EMIFA Data 11 In/Out
VP_D10	DIO	U	4	20	VPFE Pixel Data Output 10 or EMIFA Data 10 In/Out
VP_D9	DIO	U	4	21	VPFE Pixel Data Output 9 or EMIFA Data 9 In/Out
VP_D8	DIO	U	4	22	VPFE Pixel Data Output 8 or EMIFA Data 8 In/Out
PVDD	P	—	—	23	Pad Power Pin
VP_D7	DIO	U	4	24	VPFE Pixel Data Output 7 or EMIFA Data 7 In/Out
VP_D6	DIO	U	4	25	VPFE Pixel Data Output 6 or EMIFA Data 6 In/Out
PVSS	P	—	—	26	Pad Ground Pin
VP_D5	DIO	U	4	27	VPFE Pixel Data Output 5 or EMIFA Data 5 In/Out
VP_D4	DIO	U	4	28	VPFE Pixel Data Output 4 or EMIFA Data 4 In/Out
VP_D3	DIO	U	4	29	VPFE Pixel Data Output 3 or EMIFA Data 3 In/Out
VP_D2	DIO	U	4	30	VPFE Pixel Data Output 2 or EMIFA Data 2 In/Out
VP_D1	DIO	U	4	31	VPFE Pixel Data Output 1 or EMIFA Data 1 In/Out
VP_D0	DIO	U	4	32	VPFE Pixel Data Output 0 or EMIFA Data 0 In/Out
XIN	AI	—	—	33	Crystal Oscillator Input
XOUT	AO	—	—	34	Crystal Oscillator Output
VD/MOEN	DIO	U	4	35	VPFE VD output, active high or EMIFA OE# input, active low.
HD/MWEN	DIO	U	4	36	VPFE HD output, active high or EMIFA WE# input, active low.
PVDD	P	—	—	37	Pad Power Pin
PCLK/MWAIT	DO	C	12	38	VPFE Pixel Clock output or EMIFA WAIT output, active high.
PVSS	P	—	—	39	Pad Ground Pin
FRM_START	DI	U	—	40	Frame Start Input
RSTN	DI	S,U	—	41	System Reset, active low.
ROLLER_IN	DI	U	—	42	Roller Sine wave Input
DVSS	P	—	—	43	Digital Ground Pin
V18_FLT	P	—	—	44	1.8V LDO Filter
PVDDREG	P	—	—	45	Regulator Power 3.3V Pin
AVSS	P	—	—	46	Regulator Ground Pin

Pin					Description
Name	DIR	TYP	DRV	No.	
AVSS1	P	—	—	47	1st AFE Analog Ground Pin
REFB1	AO	—	—	48	1st AFE ADC Bottom Reference Voltage Decoupling
REFT1	AO	—	—	49	1st AFE ADC Top Reference Voltage Decoupling
AVDD1	P	—	—	50	1st AFE Analog Power Pin
AVSS1	P	—	—	51	1st AFE Analog Ground Pin
BIAS1	AIO	—	—	52	1st AFE Single-ended Offset/Bias Reference
VIN1A	AI	—	—	53	1st AFE Analog Input Channel A
VIN1B	AI	—	—	54	1st AFE Analog Input Channel B
VIN1C	AI	—	—	55	1st AFE Analog Input Channel C
VIN2C	AI	—	—	56	2nd AFE Analog Input Channel C
VIN2B	AI	—	—	57	2nd AFE Analog Input Channel B
VIN2A	AI	—	—	58	2nd AFE Analog Input Channel A
BIAS2	AIO	—	—	59	2nd AFE Single-ended Offset/Bias Reference
AVSS2	P	—	—	60	2nd AFE Analog Ground Pin
AVDD2	P	—	—	61	2nd AFE Analog Power Pin
REFT2	AO	—	—	62	2nd AFE ADC Top Reference Voltage Decoupling
REFB2	AO	—	—	63	2nd AFE ADC Bottom Reference Voltage Decoupling
AVSS2	P	—	—	64	2nd AFE Analog Ground Pin

DIR: AI=Analog input; AO=Analog output; AIO=Analog in/out, DI=Digital input; DO=Digital output; DIO=Digital in/out; P=Power

TYP: T=Tri-state; OD=Open-Drain; S=Schmitt trigger; C=Common; U=Pull-up 75kΩ resistance; D=Pull-down 75kΩ resistance

DRV: Pin driving current, unit: mA

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+4.3V
Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V
Storage Temperature ..... -50°C to 125°C
Operating Temperature .....0°C to 70°C
Analogue Supply Power .....3.0V~3.6V
Digital supply power .....3.0V~3.6V

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply						
PV_{DD}	Digital Supply Power	—	3.0	3.3	3.6	V
Digital Inputs						
V_{IH}	High level input voltage	—	2.0	—	—	V
V_{IL}	Low level input voltage	—	—	—	0.8	V
V_{SIH}	Schmitt Trigger high level input voltage	—	—	1.6	2.0	V
V_{SIL}	Schmitt Trigger low level input voltage	—	0.8	1.1	—	V
R_I	Input pull-up/pull-down resistance	V_{IL} = 0V or V_{IH} = V_{DD}	—	75	—	kΩ
Digital Outputs						
V_{OH}	High level output voltage	—	2.4	—	—	V
V_{OL}	Low level output voltage	—	—	—	0.4	V

PV_{DD} = 3.3V, DV_{SS} = 0V, Ta = 25°C, Crystal = 12MHz, unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Low-dropout Regulator						
V_{IN}	Input voltage	—	—	3.3	—	V
V_{OUT}	Output voltage	—	—	1.8	—	V
Supply Currents						
I_{AVDD}	Analogue supply current	—	—	220	—	mA
I_{PVDD}	Digital supply current	—	—	74	—	mA
Power Down Current						
I_{STB_AVDD}	Analogue power down current	—	—	8	—	μA
I_{STB_PVDD}	Digital power down current	—	—	145	—	μA

ADC Characteristics

AV_{DD} = PV_{DD} = 3.3V, AV_{SS} = DV_{SS} = 0V, Ta = 25°C, ADCK = 60MHz, unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Overall system specification (including 16-bit ADC, PGA, Offset and SHA functions)						
	Maximum Conversion rate	—	—	60	—	MSPS
	Full-scale input voltage range	LOR=0; Max Gain	—	0.25	—	V_{P-P}
		LOR=0; Min Gain	—	3.03	—	
		LOR=1; Max Gain	—	0.15	—	
		LOR=1; Min Gain	—	1.82	—	
V_{IN}	Input signal limits	—	AV_{SS}-0.3	—	AV_{DD}+0.3	V
	Full-scale transition error	Gain = 0dB	—	30	—	mV
	Zero-scale transition error	Gain = 0dB	—	30	—	mV
DNL	Differential non-linearity	—	—	2	—	LSB
INL	Integral non-linearity	—	—	50	—	LSB
	Channel to channel gain matching	—	—	1.5	—	%
	Total output noise	Min Gain	—	30	—	LSB_{rms}
		Max Gain	—	300	—	
References						
V_{RT}	Upper reference voltage	LOR=0	1.95	2.05	2.25	V
		LOR=1	—	1.85	—	
V_{RB}	Lower reference voltage	LOR=0	0.95	1.05	1.25	V
		LOR=1	—	1.25	—	
CML	Input return bias voltage	—	—	1.5	—	V
V_{RTB}	Differential reference voltage	LOR=0	0.90	1.0	1.10	V
		LOR=1	—	0.6	—	
Clamping (CLP) DAC						
	Resolution	—	—	4	—	bits
V_{CSTEP}	step size	CRNG=0	—	0.173	—	V/step
		CRNG=1	—	0.11	—	
V_{CBOT}	output voltage at code 0h	—	—	0.4	—	V
V_{CTOP}	output voltage at code Fh	CRNG=0	—	3.0	—	V
		CRNG=1	—	2.05	—	
DNL	Differential non-linearity	—	-0.5	—	+0.5	LSB
INL	Integral non-linearity	—	—	+/-1	—	LSB
Offset DAC						
	Resolution	—	—	8	—	bits
	Step size	—	—	2.04	—	mV/ step
	Output voltage	Code 0x00	—	-260	—	mV
		Code 0xFF	—	+260	—	mV
Programmable Gain Amplifier						
	Resolution	—	—	9	—	bits
	Gain equation	—	0.67+PGA[8:0]×5.35/511			V/V
G_{MAX}	Max gain, each channel	—	—	7.5	—	V/V
G_{MIN}	Min gain, each channel	—	—	0.65	—	V/V
	Channel Matching	—	—	1	5	%
A/D Converter						
	Resolution	—	—	16	—	bits
	Speed	—	—	60	—	MSPS
	Full-scale input range	LOR=0	—	2	—	V
		LOR=1	—	1.2	—	

Timing Specification

PV_{DD} = 3.3V, DV_{SS} = 0V, TA = 25°C, Crystal = 12MHz, unless otherwise stated.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Clock Parameter						
f_{XTAL}	Crystal input	—	—	12	—	MHz
$XTAL_{ACC}$	Crystal accuracy	—	—	500	—	ppm
f_{ISP_CLK}	ISP clock frequency	—	—	144	—	MHz
Rest						
t_{RST}	Reset active time	—	—	1	—	ms
Serial Control Interface						
f_{SCK}	Serial input clock frequency	—	—	1	2	MHz
t_{CSU}	SCSN falling to SCK rising edge	—	200	—	—	ns
t_{CHO}	SCK falling to SCSN rising edge	—	200	—	—	ns
t_{IS}	Input setup time	—	200	—	—	ns
t_{IH}	Input hold time	—	200	—	—	ns
t_{DL}	SCK falling edge to SDO transition	—	—	—	300	ns
EMIF Output Interface						
t_{VD_MOEN}	VD_MOEN low time	—	50	—	—	ns
TG Output Interface						
f_{AFE1_ADCK}	1st AFE ADC pixel clock	—	—	48	—	MHz
f_{AFE2_ADCK}	2nd AFE ADC pixel clock	—	—	48	—	MHz
f_{CIS_CLK}	CIS Module pixel clock	—	—	16	—	MHz
t_{CIS_SP}	CIS_SP pulse width	—	1	—	—	t_{CIS_CLK}
VPFE Data Output						
f_{PCLK}	VPFE pixel clock output	—	—	—	144	MHz

Notes: 1. Parameters are measured at the 50% point of the rising/falling edge.

2. $t_{CIS\_CLK} = 1/f_{CIS\_CLK}$

Function Description

Introduction

The device is a fully integrated chip for CIS imaging application. It features a programmable timing generator and image sensor shading correction to sample and condition the CIS – Contact Image Sensor - array for high-speed double-sided scanner applications.

An intelligent image sensor shading correction is employed to unitize each sensor element. The sensor data can be not only corrected but also averaged per line for black level calculation. A Video Processing Front End – VPFE – Interface multiplexed shaded ADCs outputs in two high-bytes for each ADC's output or one 16-bit wide output for each ADC. A pixel clock PCLK transports the 16-bit wide data to the output port.

The internal registers are programmed through 2-wire I^2C 3-wire/4-wire SPI interface for timing control, gain, offset and operating mode adjustments.

Power-On-Reset – POR

The POR circuit is powered by PV_{DD} and used to reset the digital logic into a default state after power-up. The POR is active from $0.6V_{Typ.}$ of PV_{DD} and released at $1.2V_{Typ.}$ of PV_{DD}. When PV_{DD} returns back to $0.6V_{Typ.}$, the POR will be active again. To ensure the contents of the control registers are at their default values before carrying out any other register writes it is recommended to execute a software reset each time the power is cycled.

Power Management

When the device default is fully enabled, the register bit PDNB allows the device to be fully powered down when set low. Individual blocks can be powered down using the bits in the System Setup Register 1.

Serial Interface for Register Configuration

3-wire SPI Interface

A serial interface is used to write and read the configuration registers. The interface is a three wire interface using SCK, SCSN, SDIO, where SDIO is bi-directional.

To write to registers, the conditions in the timing diagram shown in Figure 3 must be met. First SCSN is toggled low. At the rising edge of the first clock period, the master should assume control of the SDIO pin and begin issuing the new command. Data is clocked into the device on the rising edge of SCK through the SDIO pin. The complete 16 bits are composed of a "write" command bit (a zero), a five bit register address, two zero bits and the eight bit register value to be written. When SCSN toggles high, the register is written to, and the device now functions with this new data.

To read registers, the conditions in the timing diagram shown in Figure 3 must be met. First SCSN is toggled low. At the rising edge of the first clock period, the master should assume control of the SDIO pin and begin issuing the new command. Data is clocked into the device on the rising edge of SCK through the SDIO pin. The complete 8 bits are composed of the "read" command bit (a one), a five bit register address and two zero bits. The eight bits of data are clocked out of the device on the falling edge of the ninth clock period SCK to the sixteenth through the SDIO pin.

4-wire SPI Interface

The difference between the 4-wire SPI and 3-wire SPI is due to separate data pins. The 4-wire SPI has separate pins for input and output data, making it full-duplex.

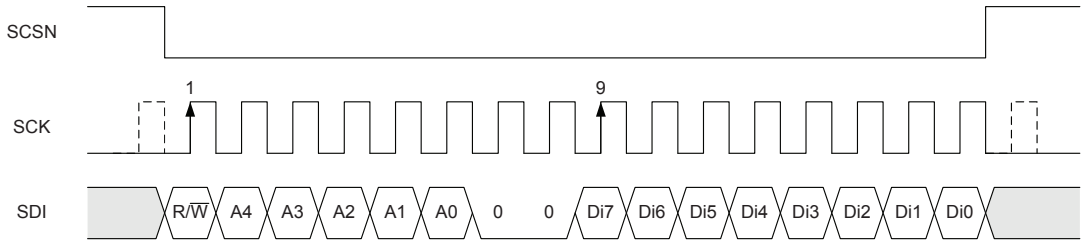
The default setting is for the 3-wire SPI interface. Set register P0_19[5] can change the SPI from 3-wire to 4-wire. For the 4-wire SPI mode, the input data pin is the SDIO pin and the output data pin is the ROLLER_OUT pin.

To write to the registers, the conditions in the timing diagram shown in Figure 5 must be met. First SCSN is toggled low. At the rising edge of the first clock period, the master should assume control of the SDIO pin and begin issuing the new command. SDIO is clocked into the device on the rising edge of SCK. The complete 16 bits are composed of the "write" command bit (a zero), a five bit register address, two zero bits and the eight bit register value to be written. When SCSN toggles high, the register is written to, and the device now functions with this new data.

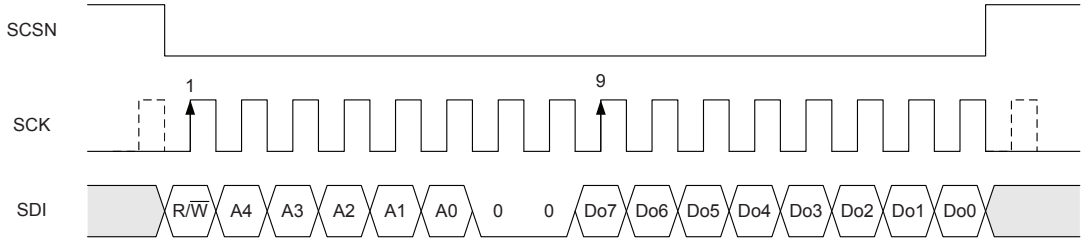
To read the registers, the conditions in the timing diagram shown in Figure 5 must be met. First SCSN is toggled low. On the rising edge of the first clock period, the master should assume control of the SDI pin and begin issuing the new command. SDIO is clocked into the device at the rising edge of SCK. The complete 8 bits are composed of the "read" command bit (a one), a five bit register address and the two zero bits to be written. The eight bits of data are clocked out on the ROLLER_OUT pin on the falling edge of the ninth clock period SCK to the sixteenth.

I^2C Interface

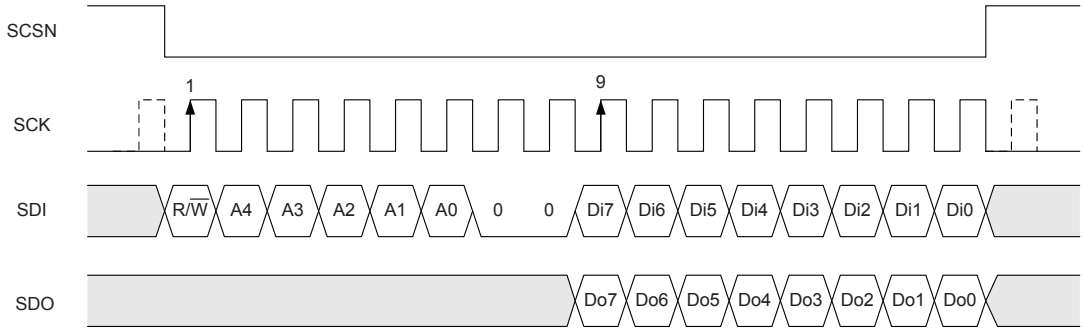
The device also supports register programming through the I^2C interface. The clock pin is SCK and the data pin is SDIO.



3-wire serial write



3-wire serial read



4-wire serial write/read

Timing Generator

This is a programmable 96-step precision timing generator, embedded with a DLL to execute timing fine tuning and generate signals for internal AFE sampling. The timing generator can also provide the CIS sensor related control timing. The device supports up to 5 lamps, CIS1_RLED, CIS1_GLED, CIS1_BLED, CIS1_IRLED and CIS1_UVLED. The on and off points are individually programmed for each LED output. The LEDs can be on simultaneously if desired and permitted by the CIS and system design.

Auto Dark & White Correction

The device provides hardware shading correction. The shading correction includes dark and white correction and up to 1584 elements with 6 independent coefficients for different colour LED lights. There is an embedded memory for coefficient storage which is pre-loaded by the SPI or EMIF interfaces. The shading correction formula is as follows, New Element(n) = (Element(n) + Offset(n)) × Gain(n), where Offset is 8-bit from 0 to -255, Gain is 10-bits from 0.00x ~ 8.00x and n is the number of sensor elements.

Video Output Interface

The device supports two kinds of video output Interfaces. One is the Asynchronous External Memory Interface, EMIF, and the other is Video Processing Front End, VPFE. Both of them are the most commonly used interfaces for the Texas Instruments CPU, such as the TMS-320DM64xx series. Users can easily connect this device to the back-end CPU for further signal processing through one of the two interfaces.

Line Information

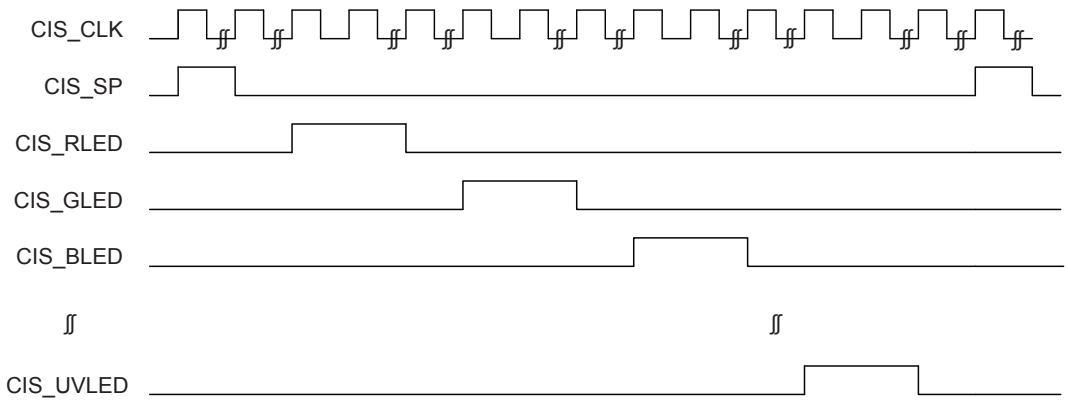
The device provides 80 bytes of line information for further signal processing. This includes maximum, minimum, summation and line Histogram. It also includes line index and roller information which is often used in computing the roller speed. A left and right boundary is provided which is necessity information when implementing image slant correction.

Voltage Comparator

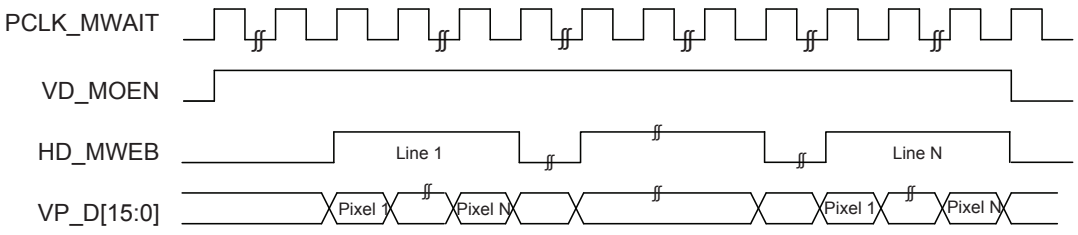
A voltage comparator is included in the device. The comparator deals with an analog roller signal and converts it into a digital signal for internal use or outputs it onto the ROLLER_OUT pin for external usage. The reference voltage to be compared is programmed using a 5-bit register.

Frame Start mechanism

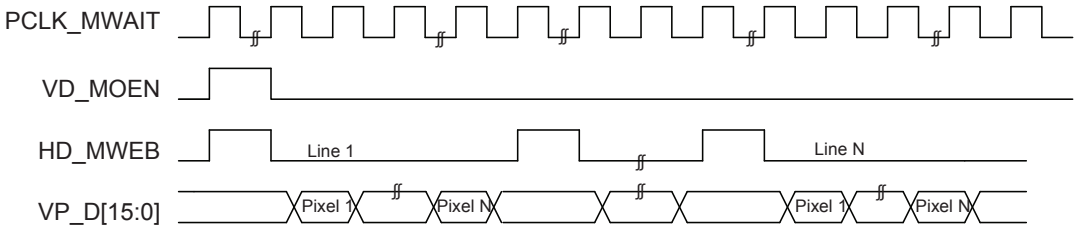
A mechanism to control the image scan procedure is provided in the device. Users can choose a suitable control mechanism between frames (Images) either from the FRM_START pin or by setting the register to start a frame based on the system requirements.



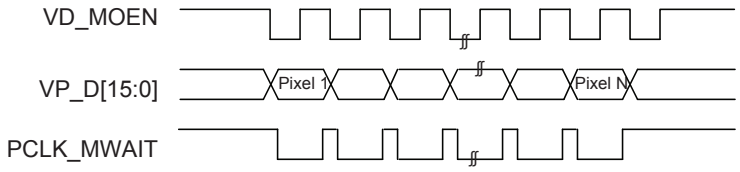
CIS Output



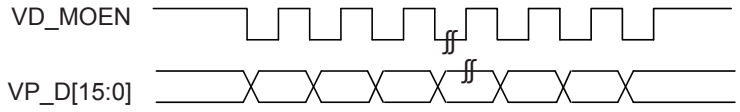
VPFE Output Sync Valid Mode



VPFE Output Sync Mode



EMIF Output



EMIF Read

Control Registers

Register Mapping

Address	Mode	Description	Default
Page 0	**System Setup Registers: Page Register 1Fh = 00h**		
01h	R/W	Software Reset Register	00h
02h	R/W	Mode Setting Register	00h
03h	R/W	Pixel Clock Configuration Register 0	00h
04h	R/W	Pixel Clock Configuration Register 1	00h
05h	R/W	ADC Clock Configuration Register 0	00h
06h	R/W	ADC Clock Configuration Register 1	00h
07h	R/W	VPFE Clock Configuration Register 0	00h
08h	R/W	VPFE Clock Configuration Register 1	00h
09h	R/W	ARM Clock Configuration Register 0	50h
0Ah	R/W	ARM Clock Configuration Register 1	01h
:	—	—	—
0Eh	R/W	PLL1 M/N value Register	80h
0Fh	R/W	PLL Control Register	C3h
10h	R/W	Data Path Control Register 0	98h
11h	R/W	Data Path Control Register 1	2Ch
12h	R/W	Data Path Control Register 2	31h
13h	R/W	Line Wait Counter MSB Register	00h
14h	R/W	Line Wait Counter LSB Register	00h
16h	R/W	VPFE/EMIF Output Ctrl Signals Strength Register	02h
17h	R/W	Video Port Delay Control Register	00h
18h	R/W	Miscellaneous Control Register 0	04h
19h	R/W	Miscellaneous Control Register 1	8Fh
1Ah	R/W	Wheel Comparator Control Register	EFh
1Bh	RO	Pin and Power-On-Strapped Status Register	—
1Ch	R/W	Debug Control Register 0	00h
1Dh	R/W	Debug Control Register 1	00h
1Eh	RO	Data Bus Debug Error Status Register	—
1Fh	R/W	Page Register	00h
Page 1	**AFE Control Registers: Page Register 1Fh = 01h**		
00h	R/W	AFE Setup Register 0	07h
01h	R/W	AFE Setup Register 1	00h
02h	R/W	1st AFE CH_A PGA Gain LSB Register	00h
03h	R/W	1st AFE CH_A PGA Gain MSB Register	00h
04h	R/W	1st AFE CH_B PGA Gain LSB Register	00h
05h	R/W	1st AFE CH_B PGA Gain MSB Register	00h
06h	R/W	1st AFE CH_C PGA Gain LSB Register	00h
07h	R/W	1st AFE CH_C PGA Gain MSB Register	00h
08h	R/W	2nd AFE CH_A PGA Gain LSB Register	00h
09h	R/W	2nd AFE CH_A PGA Gain MSB Register	00h
0Ah	R/W	2nd AFE CH_B PGA Gain LSB Register	00h
0Bh	R/W	2nd AFE CH_B PGA Gain MSB Register	00h
0Ch	R/W	2nd AFE CH_C PGA Gain LSB Register	00h
0Dh	R/W	2nd AFE CH_C PGA Gain MSB Register	00h

Address	Mode	Description	Default
0Eh	R/W	1st AFE CH_A Offset Register	00h
0Fh	R/W	1st AFE CH_B Offset Register	00h
10h	R/W	1st AFE CH_C Offset Register	00h
11h	R/W	2nd AFE CH_A Offset Register	00h
12h	R/W	2nd AFE CH_B Offset Register	00h
13h	R/W	2nd AFE CH_C Offset Register	00h
14h	R/W	AFE Current Setup Register	50h
15h	R/W	AFE 60MHz Current Setup Register	00h
:	—	—	—
1Fh	R/W	Page Register	00h
Page 2	**TG Control Registers: Page Register 1Fh = 02h**		
00h	R/W	TG Main Configuration Register 0	11h
01h	R/W	TG Main Configuration Register 1	22h
02h	R/W	TG Control Register 0	01h
03h	R/W	TG Control Register 1	00h
04h	R/W	TG Control Register 2	1Fh
05h	R/W	TG CIS_CLK/AFE_CLK Control Register	45h
06h	R/W	TG CIS_CLK Start Register	00h
07h	R/W	TG CIS_CLK End Register	40h
:	—	—	—
0Ah	R/W	TG AFE_SHD Start Register	40h
0Bh	R/W	TG AFE_SHD End Register	60h
0Ch	R/W	TG CIS_CLK/SH On Guardband Register	00h
0Dh	R/W	TG CIS_CLK/SH Off Guardband Register	00h
0Eh	R/W	TG Wheel Step MSB Register	00h
0Fh	R/W	TG Wheel Step LSB Register	80h
10h	R/W	TG Wheel Control Register	01h
11h	R/W	CIS1/CIS2 Dummy LAMP Selection Register	00h
12h	R/W	CIS1/CIS2 Dummy LAMP On MSB Register	00h
13h	R/W	CIS1/CIS2 Dummy LAMP On LSB Register	00h
14h	R/W	CIS1/CIS2 Dummy LAMP Off MSB Register	00h
15h	R/W	CIS1/CIS2 Dummy LAMP Off LSB Register	00h
16h	R/W	CIS1 LAMP Component Selection Register	00h
17h	R/W	CIS2 LAMP Component Selection Register	00h
18h	R/W	CIS Black Level Clamp Control Register	00h
19h	R/W	CIS Black Level Clamp Position Register	00h
1Ah	R/W	CIS to AFE Sequence Mapping Register	00h
:	—	—	—
1Dh	R/W	CIS1 Output Control Signals Strength Register	51h
1Eh	R/W	CIS2 Output Control Signals Strength Register	01h
1Fh	R/W	Page Register	00h
Page 3	**TG Timing1 Registers: Page Register 1Fh = 03h**		
00h	R/W	TG CIS_1 CH_1 Start of Valid Pixels MSB Register	00h
01h	R/W	TG CIS_1 CH_1 Start of Valid Pixels LSB Register	01h
02h	R/W	TG CIS_1 CH_1 End of Valid Pixels MSB Register	01h
03h	R/W	TG CIS_1 CH_1 End of Valid Pixels LSB Register	B0h
04h	R/W	TG CIS_1 CH_2 Start of Valid Pixels MSB Register	00h
05h	R/W	TG CIS_1 CH_2 Start of Valid Pixels LSB Register	01h
06h	R/W	TG CIS_1 CH_2 End of Valid Pixels MSB Register	01h

Address	Mode	Description	Default
07h	R/W	TG CIS_1 CH_2 End of Valid Pixels LSB Register	B0h
08h	R/W	TG CIS_1 CH_3 Start of Valid Pixels MSB Register	00h
09h	R/W	TG CIS_1 CH_3 Start of Valid Pixels LSB Register	01h
0Ah	R/W	TG CIS_1 CH_3 End of Valid Pixels MSB Register	02h
0Bh	R/W	TG CIS_1 CH_3 End of Valid Pixels LSB Register	40h
0Ch	R/W	TG CIS_1 Line Valid Start and End MSB Register	00h
0Dh	R/W	TG CIS_1 Line Valid Start LSB Register	00h
0Eh	R/W	TG CIS_1 Line Valid End LSB Register	00h
0Fh	R/W	TG CIS_2 CH_1 Start of Valid Pixels MSB Register	00h
10h	R/W	TG CIS_2 CH_1 Start of Valid Pixels LSB Register	01h
11h	R/W	TG CIS_2 CH_1 End of Valid Pixels MSB Register	01h
12h	R/W	TG CIS_2 CH_1 End of Valid Pixels LSB Register	B0h
13h	R/W	TG CIS_2 CH_2 Start of Valid Pixels MSB Register	00h
14h	R/W	TG CIS_2 CH_2 Start of Valid Pixels LSB Register	01h
15h	R/W	TG CIS_2 CH_2 End of Valid Pixels MSB Register	01h
16h	R/W	TG CIS_2 CH_2 End of Valid Pixels LSB Register	B0h
17h	R/W	TG CIS_2 CH_3 Start of Valid Pixels MSB Register	00h
18h	R/W	TG CIS_2 CH_3 Start of Valid Pixels LSB Register	01h
19h	R/W	TG CIS_2 CH_3 End of Valid Pixels MSB Register	02h
1Ah	R/W	TG CIS_2 CH_3 End of Valid Pixels LSB Register	40h
1Bh	R/W	TG CIS_2 Line Valid Start and End MSB Register	00h
1Ch	R/W	TG CIS_2 Line Valid Start LSB Register	00h
1Dh	R/W	TG CIS_2 Line Valid End LSB Register	00h
1Fh	R/W	Page Register	00h
Page 4	**TG Timing 2 Registers: Page Register 1Fh = 04h**		
00h	R/W	TG MODE Output Selection Register	00h
01h	R/W	TG MODE On MSB Register	00h
02h	R/W	TG MODE On LSB Register	00h
03h	R/W	TG MODE Off MSB Register	00h
04h	R/W	TG MODE Off LSB Register	00h
05h	R/W	TG SI Mode Selection Register	0Ch
06h	R/W	TG SI Width Register	04h
07h	R/W	TG_1 Line End MSB Register	00h
08h	R/W	TG_1 Line End LSB Register	20h
:	—	—	—
0Bh	R/W	Frame Start/End Selection Register	00h
0Ch	R/W	Pixel Threshold for Frame Start Auto Detection Register	00h
0Dh	R/W	Number of Pixel per Line for Frame Start Auto Detection MSB Register	00h
0Eh	R/W	Number of Pixel per Line for Frame Start Auto Detection LSB Register	00h
0Fh	R/W	Number of Lines for Frame Start Auto Detection MSB Register	30h
10h	R/W	Number of Lines for Frame Start Auto Detection LSB Register	00h
11h	R/W	Pixel Threshold for Frame End Auto Detection Register	00h
12h	R/W	Number of Pixel per Line for Frame End Auto Detection MSB Register	00h
13h	R/W	Number of Pixel per Line for Frame End Auto Detection LSB Register	00h
14h	R/W	Number of Lines for Frame End Auto Detection MSB Register	00h
15h	R/W	Number of Lines for Frame End Auto Detection LSB Register	00h
16h	R/W	Delay Lines for Frame End Starting Detection MSB Register	00h
17h	R/W	Delay Lines for Frame End Starting Detection LSB Register	00h

Address	Mode	Description	Default
18h	R/W	Number of Lines for Frame End Fix Length MSB Register	00h
19h	R/W	Number of Lines for Frame End Fix Length LSB Register	00h
1Ah	R/W	Frame Jam Counter Register 0	00h
1Bh	R/W	Frame Jam Counter Register 1	00h
1Ch	R/W	Frame Jam Counter Register 2	00h
1Dh	R/W	Frame Jam Counter Register 3	00h
1Fh	R/W	Page Register	00h
Page 5	**CIS1 LAMP Control Registers: Page Register 1Fh = 05h**		
00h	R/W	CIS1 LAMP Mode Register	00h
01h	R/W	CIS1 Component 1/Component 7 LAMP Selection Register	20h
02h	R/W	CIS1 Component 2/Component 8 LAMP Selection Register	10h
03h	R/W	CIS1 Component 3/Component 9 LAMP Selection Register	08h
04h	R/W	CIS1 Component 4/Component 10 LAMP Selection Register	04h
05h	R/W	CIS1 Component 5/Component 11 LAMP Selection Register	02h
06h	R/W	CIS1 Component 6/Component 12 LAMP Selection Register	01h
07h	R/W	CIS1 Red LAMP On MSB Register	00h
08h	R/W	CIS1 Red LAMP On LSB Register	2Eh
09h	R/W	CIS1 Red LAMP Off MSB Register	01h
0Ah	R/W	CIS1 Red LAMP Off LSB Register	06h
0Bh	R/W	CIS1 Green LAMP On MSB Register	00h
0Ch	R/W	CIS1 Green LAMP On LSB Register	2Eh
0Dh	R/W	CIS1 Green LAMP Off MSB Register	01h
0Eh	R/W	CIS1 Green LAMP Off LSB Register	06h
0Fh	R/W	CIS1 Blue LAMP On MSB Register	00h
10h	R/W	CIS1 Blue LAMP On LSB Register	2Eh
11h	R/W	CIS1 Blue LAMP Off MSB Register	01h
12h	R/W	CIS1 Blue LAMP Off LSB Register	06h
13h	R/W	CIS1 IR1 LAMP On MSB Register	00h
14h	R/W	CIS1 IR1 LAMP On LSB Register	2Eh
15h	R/W	CIS1 IR1 LAMP Off MSB Register	01h
16h	R/W	CIS1 IR1 LAMP Off LSB Register	06h
17h	R/W	CIS1 IR2 LAMP On MSB Register	00h
18h	R/W	CIS1 IR2 LAMP On LSB Register	2Eh
19h	R/W	CIS1 IR2 LAMP Off MSB Register	01h
1Ah	R/W	CIS1 IR2 LAMP Off LSB Register	06h
1Bh	R/W	CIS1 UV LAMP On MSB Register	00h
1Ch	R/W	CIS1 UV LAMP On LSB Register	2Eh
1Dh	R/W	CIS1 UV LAMP Off MSB Register	01h
1Eh	R/W	CIS1 UV LAMP Off LSB Register	06h
1Fh	R/W	Page Register	00h
Page 6	**CIS2 LAMP Control Registers: Page Register 1Fh = 06h**		
00h	R/W	CIS2 LAMP Mode Register	00h
01h	R/W	CIS2 Component 1/Component 7 LAMP Selection Register	20h
02h	R/W	CIS2 Component 2/Component 8 LAMP Selection Register	10h
03h	R/W	CIS2 Component 3/Component 9 LAMP Selection Register	08h
04h	R/W	CIS2 Component 4/Component 10 LAMP Selection Register	04h
05h	R/W	CIS2 Component 5/Component 11 LAMP Selection Register	02h
06h	R/W	CIS2 Component 6/Component 12 LAMP Selection Register	01h

Address	Mode	Description	Default
07h	R/W	CIS2 Red LAMP On MSB Register	00h
08h	R/W	CIS2 Red LAMP On LSB Register	2Eh
09h	R/W	CIS2 Red LAMP Off MSB Register	01h
0Ah	R/W	CIS2 Red LAMP Off LSB Register	06h
0Bh	R/W	CIS2 Green LAMP On MSB Register	00h
0Ch	R/W	CIS2 Green LAMP On LSB Register	2Eh
0Dh	R/W	CIS2 Green LAMP Off MSB Register	01h
0Eh	R/W	CIS2 Green LAMP Off LSB Register	06h
0Fh	R/W	CIS2 Blue LAMP On MSB Register	00h
10h	R/W	CIS2 Blue LAMP On LSB Register	2Eh
11h	R/W	CIS2 Blue LAMP Off MSB Register	01h
12h	R/W	CIS2 Blue LAMP Off LSB Register	06h
13h	R/W	CIS2 IR1 LAMP On MSB Register	00h
14h	R/W	CIS2 IR1 LAMP On LSB Register	2Eh
15h	R/W	CIS2 IR1 LAMP Off MSB Register	01h
16h	R/W	CIS2 IR1 LAMP Off LSB Register	06h
17h	R/W	CIS2 IR2 LAMP On MSB Register	00h
18h	R/W	CIS2 IR2 LAMP On LSB Register	2Eh
19h	R/W	CIS2 IR2 LAMP Off MSB Register	01h
1Ah	R/W	CIS2 IR2 LAMP Off LSB Register	06h
1Bh	R/W	CIS2 UV LAMP On MSB Register	00h
1Ch	R/W	CIS2 UV LAMP On LSB Register	2Eh
1Dh	R/W	CIS2 UV LAMP Off MSB Register	01h
1Eh	R/W	CIS2 UV LAMP Off LSB Register	06h
1Fh	R/W	Page Register	00h
Page 7	**CIS1 Shading Control Registers: Page Register 1Fh = 07h**		
00h	R/W	Shading Control Register	00h
02h	R/W	Shading RAM/DSP Combination Select Register	00h
03h	R/W	Shading RAM/DSP Start Address MSB Register	00h
04h	R/W	Shading RAM/DSP Start Address LSB Register	00h
05h	R/W	Shading RAM/DSP Transfer Count MSB Register	00h
06h	R/W	Shading RAM/DSP Transfer Count LSB Register	00h
07h	R/W	CIS1 Global Shading Gain Coefficient Register	00h
08h	R/W	CIS2 Global Shading Gain Coefficient Register	00h
0Ah	R/W	CIS 1 Dark Shading Offset Virtual Address MSB Register	00h
0Bh	R/W	CIS 1 Dark Shading Offset Virtual Address LSB Register	00h
0Ch	R/W	CIS 1 Dark Shading Offset Coefficient Register	00h
0Dh	R/W	CIS 1 Combination 1 Shading Gain Virtual Address MSB Register	00h
0Eh	R/W	CIS 1 Combination 1 Shading Gain Virtual Address LSB Register	00h
0Fh	R/W	CIS 1 Combination 1 Shading Gain Coefficient Register	00h
10h	R/W	CIS 1 Combination 2 Shading Gain Virtual Address MSB Register	00h
11h	R/W	CIS 1 Combination 2 Shading Gain Virtual Address LSB Register	00h
12h	R/W	CIS 1 Combination 2 Shading Gain Coefficient Register	00h
13h	R/W	CIS 1 Combination 3 Shading Gain Virtual Address MSB Register	00h
14h	R/W	CIS 1 Combination 3 Shading Gain Virtual Address LSB Register	00h
15h	R/W	CIS 1 Combination 3 Shading Gain Coefficient Register	00h
16h	R/W	CIS 1 Combination 4 Shading Gain Virtual Address MSB Register	00h

Address	Mode	Description	Default
17h	R/W	CIS 1 Combination 4 Shading Gain Virtual Address LSB Register	00h
18h	R/W	CIS 1 Combination 4 Shading Gain Coefficient Register	00h
19h	R/W	CIS 1 Combination 5 Shading Gain Virtual Address MSB Register	00h
1Ah	R/W	CIS 1 Combination 5 Shading Gain Virtual Address LSB Register	00h
1Bh	R/W	CIS 1 Combination 5 Shading Gain Coefficient Register	00h
1Ch	R/W	CIS 1 Combination 6 Shading Gain Virtual Address MSB Register	00h
1Dh	R/W	CIS 1 Combination 6 Shading Gain Virtual Address LSB Register	00h
1Eh	R/W	CIS 1 Combination 6 Shading Gain Coefficient Register	00h
1Fh	R/W	Page Register	00h
Page 8	**CIS2 Shading Control Registers: Page Register 1Fh = 08h**		
00h	R/W	CIS 2 Dark Shading Offset Virtual Address MSB Register	00h
01h	R/W	CIS 2 Dark Shading Offset Virtual Address LSB Register	00h
02h	R/W	CIS 2 Dark Shading Offset Coefficient Register	00h
03h	R/W	CIS 2 Combination 1 Shading Gain Virtual Address MSB Register	00h
04h	R/W	CIS 2 Combination 1 Shading Gain Virtual Address LSB Register	00h
05h	R/W	CIS 2 Combination 1 Shading Gain Coefficient Register	00h
06h	R/W	CIS 2 Combination 2 Shading Gain Virtual Address MSB Register	00h
07h	R/W	CIS 2 Combination 2 Shading Gain Virtual Address LSB Register	00h
08h	R/W	CIS 2 Combination 2 Shading Gain Coefficient Register	00h
09h	R/W	CIS 2 Combination 3 Shading Gain Virtual Address MSB Register	00h
0Ah	R/W	CIS 2 Combination 3 Shading Gain Virtual Address LSB Register	00h
0Bh	R/W	CIS 2 Combination 3 Shading Gain Coefficient Register	00h
0Ch	R/W	CIS 2 Combination 4 Shading Gain Virtual Address MSB Register	00h
0Dh	R/W	CIS 2 Combination 4 Shading Gain Virtual Address LSB Register	00h
0Eh	R/W	CIS 2 Combination 4 Shading Gain Coefficient Register	00h
0Fh	R/W	CIS 2 Combination 5 Shading Gain Virtual Address MSB Register	00h
10h	R/W	CIS 2 Combination 5 Shading Gain Virtual Address LSB Register	00h
11h	R/W	CIS 2 Combination 5 Shading Gain Coefficient Register	00h
12h	R/W	CIS 2 Combination 6 Shading Gain Virtual Address LSB Register	00h
13h	R/W	CIS 2 Combination 6 Shading Gain Virtual Address MSB Register	00h
14h	R/W	CIS 2 Combination 6 Shading Gain Coefficient Register	00h
:	—	—	—
1Fh	R/W	Page Register	00h
Page 9	**ISP Control Registers: Page Register 1Fh = 09h**		
00h	R/W	ISP Control Register 0	00h
01h	R/W	ISP Control Register 1	00h
02h	R/W	ISP Control Register 2	00h
03h	R/W	Line Information Control Register 0	00h
04h	R/W	Line Information Control Register 1	00h
05h	R/W	Line Border Control Register 0	30h
06h	R/W	Line Border Control Register 1	AAh
:	—	—	—
0Ah	R/W	ISP1 Sharpness Gain 1 Register	40h
0Bh	R/W	ISP1 Sharpness Gain 2 Register	40h
0Ch	R/W	ISP2 Sharpness Gain 1 Register	40h
0Dh	R/W	ISP2 Sharpness Gain 2 Register	40h
0Eh	R/W	ISP1 Line Border Static Threshold Register	20h
0Fh	R/W	ISP2 Line Border Static Threshold Register	20h
10h	R/W	ISP1 Line Border Big Window Threshold Register	20h

Address	Mode	Description	Default
11h	R/W	ISP1 Line Border Small Window Threshold Register	08h
12h	R/W	ISP2 Line Border Big Window Threshold Register	20h
13h	R/W	ISP2 Line Border Small Window Threshold Register	08h
:	—	—	—
16h	R/W	ISP1 Valid Range Start/End Address MSB Register	07h
17h	R/W	ISP1 Valid Range Start Address LSB Register	00h
18h	R/W	ISP1 Valid Range End Address LSB Register	FFh
19h	R/W	ISP2 Valid Range Start/End Address MSB Register	07h
1Ah	R/W	ISP2 Valid Range Start Address LSB Register	00h
1Bh	R/W	ISP2 Valid Range End Address LSB Register	FFh
:	—	—	—
1Fh	R/W	Page Register	00h

Register Description

Page 0 Registers – System Setup Registers

- **Address P0_01h: Software Reset Register**

Bit	Mode	Description	Default
7-2	—	Reserved	—
1	R/W	ISP Engine Software reset (Self clear) 1: Reset	0
0	R/W	TG Controller Software reset (Self clear) 1: Reset	0

- **Address P0_02h: Mode Setting Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R/W	Register Mode Setting Enable 0: Disable 1: Enable	0
3-0	R/W	Register Mode Selection 4'h0: Normal mode 4'h1: AFE Only Mode 4'h2: DFT Test Mode 4'h3: Tie-High Test Mode 4'h4: Tie-Low Test Mode 4'h5: Nand-tree Test Mode 4'h6: Pull-Up-Down Test Mode 4'h7: IPtest Test Mode 4'h8: Debug1 Mode 4'h9: Debug2 Mode 4'ha: Debug3 Mode	0

- **Address P0_03h: Pixel Clock Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	Pixel Clock Enable 0: Disable 1: Enable	—
6-5	R/W	Input Clock selection, used with bit7 00: OSC – 12MHz 01: OSC – 12MHz 10: PLL1 – 96MHz 11: PLL2 – 144MHz	00
4	R/W	Clock Division Enable 0: Not Divided 1: Divided	0
3-0	—	Reserved	-

- **Address P0_04h: Pixel Clock Configuration Register 1**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Clock Division Factor – DIV_FACT[5:0] Output clock = Input_clock/(DIV_FACT+2)	00h

Note: Set P0_04h first and then set P0_03h latter.

- **Address P0_05h: ADC Clock Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	ADC Clock Enable 0: Disable 1: Enable	0
6-5	R/W	Input Clock selection 00: OSC – 12MHz 01: OSC – 12MHz 10: PLL1 – 96MHz 11: PLL2 – 144MHz	00
4	R/W	Clock Division Enable 0: Not Divided 1: Divided	0
3-0	—	Reserved	—

- **Address P0_06h: ADC Clock Configuration Register 1**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Clock Division Factor – DIV_FACT[5:0] Output clock = Input_clock/(DIV_FACT+2)	00h

Note: Set P0_06h first and then set P0_05h latter.

- **Address P0_07h: VPFE Clock Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	VPFE Clock Enable 0: Disable 1: Enable	0
6-5	R/W	Input Clock selection 00: OSC – 12MHz 01: OSC – 12MHz 10: PLL1 – 96MHz 11: PLL2 – 144MHz	00
4	R/W	Clock Division Enable 0: Not Divided 1: Divided	0
3-0	—	Reserved	—

- **Address P0_08h: VPFE Clock Configuration Register 1**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Clock Division Factor – DIV_FACT[5:0] Output clock = Input_clock/(DIV_FACT+2)	00h

Note: Set P0_08h first and then set P0_07h latter.

- **Address P0_09h: ARM Clock Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	ARM Clock Enable 0: Disable 1: Enable	0
6-5	R/W	Input Clock selection 00: OSC – 12MHz 01: OSC – 12MHz 10: PLL1 – 96MHz 11: PLL2 – 144MHz	10
4	R/W	Clock Division Enable 0: Not Divided 1: Divided	1
3-0	—	Reserved	—

- **Address P0_0Ah: ARM Clock Configuration Register 1**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Clock Division Factor – DIV_FACT[5:0] Output clock = Input_clock/(DIV_FACT+2)	01h

- **Address P0_0Eh: PLL1 M/N value Register**

Bit	Mode	Description	Default
7-4	R/W	PLL1 M value [3:0] 4'b0001: 12MHz 4'b0010: 24MHz 4'b0011: 36MHz 4'b0100: 48MHz 4'b0101: 60MHz 4'b0110: 72MHz 4'b0111: 84MHz 4'b1000: 96MHz Others: Reserved	8h
3-2	—	Reserved	—
1-0	—	PLL1 N value [2:0] 2'b00: Divided by 1 2'b01: Divided by 2 2'b10: Divided by 4 2'b11: Divided by 8	00

- **Address P0_0Fh: PLL Control Register**

Bit	Mode	Description	Default
7-4	R/W	PLL2 M value [3:0] 4'b0001: 12MHz 4'b0010: 24MHz 4'b0011: 36MHz 4'b0100: 48MHz 4'b0101: 60MHz 4'b0110: 72MHz 4'b0111: 84MHz 4'b1000: 96MHz 4'b1001: 108MHz 4'b1010: 120MHz 4'b1011: 132MHz 4'b1100: 144MHz Others: Reserved	Ch
3-2	—	Reserved	—
1	R/W	PLL2 Enable 0: Disable 1: Enable	1
0	R/W	PLL1 Enable 0: Disable 1: Enable	1

- **Address P0_10h: Data Path Control Register 0**

Bit	Mode	Description	Default
7	R/W	CIS1 Data Capture Enable 0: Disable 1: Enable Note: The CIS1 Sensor data passes to Video Port When this bit is set high to enable the CIS1 Data Capture function.	1
6	R/W	Output Data Format 0: Pixel by pixel 1: Line by line	0
5	R/W	Video Port Interface Selection 0: EMIF 1: VPFE	0
4	R/W	CIS2 Data Capture Enable 0: Disable 1: Enable Note: The CIS2 Sensor data passes to Video Port When this bit is set high to enable the CIS2 Data Capture function.	1
3-2	R/W	Data Path Selection (source ↔ destination) 00: SPI ↔ Shading Ram (SPI can be from DSP or PC) 01: EMIF ↔ Shading Ram 10: Video Port ↔ Line Buffer (selected by bit5) Others: Reserved	10
1	R/W	Data Transfer Selection 0: Write, source → destination 1: Read, source ← destination	0
0	R/W	Shading/DSP Transfer Start Writing 1 to this register start transfer between Shading Ram and DSP, and after transfer done, this bit will be self-cleared. Note: Only for Shading Ram ↔ DSP	0

- **Address P0_11h: Data Path Control Register 1**

Bit	Mode	Description	Default
7-5	R/W	Video Port VD signal selection 000 : V sync 001 : V valid 010 : H sync 011 : H valid 1xx : H sync interval	001
4-2	R/W	Video Port HD signal selection 000 : V sync 001 : V valid 010 : H sync 011 : H valid 1xx : H sync interval	011
1	R/W	Video Port clock out polarity selection 0 : Positive edge 1 : Negative edge	0
0	RO	Shading/DSP Transfer Done Note: Only for Shading Ram ↔ DSP	—

- **Address P0_12h: Data Path Control Register 2**

Bit	Mode	Description	Default
7	R/W	H sync interval/CIS2 IR2LED2_DIN4 selection 0: Normal CIS1 $LAMP_{IR2}$ to Pad IR2LED2_DIN4 1: H sync interval to Pad IR2LED2_DIN4	0
6-4	R/W	H sync interval counter [2:0] Note: H sync interval counter is based on H sync	011
3	R/W	H sync interval/CIS1 $LAMP_{IR2}$ selection 0: Normal CIS1 $LAMP_{IR2}$ to Pad CIS_IR2LED 1: H sync interval to Pad CIS_IR2LED	0
2	R/W	CIS Data Output Order on Video Port 0: Big endian 1: Little endian Notes: 1. If the P0_10h[6] bit is set to pixel-by-pixel format and the big endian is chosen, then data output format is {CIS1[7:0], CIS2[7:0]} and vice versa. 2. If the P0_10h[6] bit is set to line-by-line format and the big endian is chosen, the data output format is {CIS1_0[7:0], CIS1_1[7:0]}, {CIS1_2[7:0], CIS1_3[7:0]}, …, {CIS2_0[7:0], CIS2_1[7:0]}, {CIS2_2[7:0], CIS2_3[7:0]}	0
1	R/W	Line wait control 0: Disable 1: Enable Note: If the Line wait function is enabled and the Output Data Format is selected as “Line-by-Line” format set by the P0_10h[6] bit, after the CIS1 data of a line has been transferred, the CIS2 data will not be transferred until the counter reaches the value set by the registers P0_13h and P0_14h.	0
0	R/W	Package Select 0: 64-pin (must) 1: Reserved	1

- **Address P0_13h: Line Wait Counter MSB Register**

Bit	Mode	Description	Default
7-0	R/W	Line Wait Counter MSB Note: The Line Wait Counter is driven by the VPFE clock	00h

- **Address P0_14h: Line Wait Counter LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Line Wait Counter LSB Note: The Line Wait Counter is driven by the VPFE clock	00h

- **Address P0_16h: VPFE/EMIF Ctrl Signals Strength Register**

Bit	Mode	Description	Default
7-6	R/W	HD_MWEN Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	00
5-4	R/W	VD_MOEN Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	00
3-2	—	Reserved	00
1-0	R/W	PCLK_MWAIT Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	10

- **Address P0_17h: Video Port Delay Control Register**

Bit	Mode	Description	Default
7-2	—	Reserved	—
1-0	R/W	Video_Port_DATA[15:0] Delay Mode [1:0] b15, b14, b13, b12, b11, b10, b9, b8, b7, b6, b5, b4, b3, b2, b1, b0 00: No delay 01: 1D,2D,1D,2D,1D,2D,1D,2D,1D,2D,1D,2D,1D,2D,1D,2D 10: 1D,2D,3D,4D,1D,2D,3D,4D,1D,2D,3D,4D,1D,2D,3D,4D 11: Reserved The notation "D" means the unit delay time between each data bit with an approximate value from 0.1ns to 0.15ns.	00

- **Address P0_18h: Miscellaneous Control Register 0**

Bit	Mode	Description	Default
7-6	—	Reserved	00
5	R/W	Internal 1st AFE and 2nd AFE output control 0: Output enable 1: Output disable	0
4	R/W	Second data output group enable control in the AFE only mode 0: Output disable 1: Output enable	0
3	—	Reserved	0
2	—	Reserved	1
1-0	R/W	External AFE data input format selection 00: Din[9:0] = {AFE2[15:11], AFE1[15:11]} 01: Din[9:0] = AFE1[15:6] 10: Din[9:0] = AFE2[15:6] Others: Reserved	00

- **Address P0_19h: Miscellaneous Control Register 1**

Bit	Mode	Description	Default
7	R/W	AFE ADCK Output 0: Gated to "0" 1: Normal	1
6	R/W	AFE Control Signals (SHD, ADCK, CLAMP) Output Enable 0: Disable with a tri-state 1: Enable output function (must)	0
5	R/W	SPI Interface selection 0: 3-wire SPI interface 1: 4-wire SPI interface Note: If the 3-wire SPI interface is selected, the SDI/SDIO pin will function as the SDIO bidirectional pin. If the 4-wire SPI interface is selected, the SDI/SDIO pin will function as the SDI input pin only and the ROLLER_OUT/SDO pin will function as the SDO output pin.	0
4	R/W	LVR disable control 0: Enable 1: Disable	0
3	R/W-	SCK pin Schmitt trigger enable control 0: Disable 1: Enable	1
2	R/W	HD_MWEN and VD_MOEN pins Schmitt trigger enable control 0: Disable 1: Enable	1
1	R/W	CIS1 R/G/B lamp output pin pull down function enable control 0: Disable 1: Enable	1
0	R/W	CIS1 lamp pin output enable control 0: Disable with a tri-state 1: Enable output function	1

- **Address P0_1Ah: Wheel Comparator Control Register**

Bit	Mode	Description	Default
7	R/W	ROLLER_OUT pin output enable Control 0: Disable with a tri-state 1: Enable output function	1
6	R/W	Comparator operation ON/ OFF control 0: Comparator power down 1: Comparator normal operation	1
5	R/W	Comparator hysteresis ON / OFF control 0: Hysteresis is OFF 1: Hysteresis is ON.	1
4-0	R/W	Comparator reference voltage selection 5'd0: V_{REF} = 0V 5'd1: V_{REF} = (3.3/32)×1V 5'd2: V_{REF} = (3.3/32)×2V 5'd3: V_{REF} = (3.3/32)×3V : : 5'd31: V_{REF} = (3.3/32)×31V	0Fh

- **Address P0_1Bh: Pin and Power-On-Strapped Status Register**

Bit	Mode	Description	Default
7-5	RO	Power-On-Strapped Status Selection 3'h0: Normal Mode 3'h1: DFT 3'h2: Tie-High 3'h3: Tie-Low 3'h4: Nand-tree 3'h5: Pull-Up-Down 3'h6: Iptest 3'h7: AFE-Only	—
4	RO	Power-On-Strapped Status Enable	—
3-1	RO	Pin Mode Status Selection 3'h0: AFE-Only 3'h1: DFT 3'h2: Tie-High 3'h3: Tie-low 3'h4: Nand-tree 3'h5: Pull-Up-Down 3'h6: Iptest Others: Reserved	—
0	RO	Pin Mode Status Enable	—

- **Address P0_1Ch: Debug Control Register 0**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	SPI register setting debug enable	0
4	R/W	I^2C register setting debug enable	0
3	R/W	Function Pattern enable	0
2	R/W	Data path debug enable	0
1	R/W	DSP debug enable	0
0	R/W	TG debug enable	0

- **Address P0_1Dh: Debug Control Register 1**

Bit	Mode	Description	Default
7-4	R/W	DSP debug bus selection[3:0]	0h
3-0	R/W	TG debug bus selection[3:0]	0h

- **Address P0_1Eh: Data Bus Debug Error Status Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	RO	Data Path Error after Line-Buffer Controller	—
3	RO	Data Path Error after Asyn-FIFO	—
2	RO	Data Path Error after ISP	—
1	RO	Data Path Error after Shading	—
0	RO	Data Path Error after TG Controller	—

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 1 Registers – AFE Control Registers

- **Address P1_00h: AFE Setup Register 0**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2	R/W	AFE2B: 2nd AFE power down control 0: 2nd AFE is powered down 1: 2nd AFE is active This bit is only available when the PDNB bit is set to 1. If the PDNB bit is cleared to 0, the 2nd AFE will be powered down.	1
1	R/W	AFE1B: 1st AFE power down control 0: 1st AFE is powered down 1: 1st AFE is active This bit is only available when the PDNB bit is set to 1. If the PDNB bit is cleared to 0, the 1st AFE will be powered down.	1
0	R/W	PDNB: Global AFE power down control 0: 1st and 2nd AFEs are all powered down 1: 1st and 2nd AFEs are not powered down When this bit is cleared to 0, both 1st and 2nd AFEs are all powered down regardless of the AFE1B or AFE2B bit value. When this bit is set to 1, the 1st or 2nd AFE can be controlled by the AFE1B or AFE2B bit respectively.	1

- **Address P1_01h: AFE Setup Register 1**

<table>
<tr><th>Bit</th><th>Mode</th><th>Description</th><th>Default</th></tr>
<tr><td>7-4</td><td>R/W</td><td>CLPV: Clamping voltage selection on BIAS1 and BIAS2 pins
These bits are used to select the clamping voltage which appears on BIAS1 and BIAS2 pins. Note that the following table shows an approximate clamping voltage value derived from sampling tested results.
<table>
<tr><th>CLPV</th><th>CRNG=1</th><th>CRNG=0</th></tr>
<tr><td>0</td><td>0.437</td><td>0.438</td></tr>
<tr><td>1</td><td>0.512</td><td>0.582</td></tr>
<tr><td>2</td><td>0.625</td><td>0.755</td></tr>
<tr><td>3</td><td>0.734</td><td>0.928</td></tr>
<tr><td>4</td><td>0.843</td><td>1.098</td></tr>
<tr><td>5</td><td>0.952</td><td>1.271</td></tr>
<tr><td>6</td><td>1.06</td><td>1.442</td></tr>
<tr><td>7</td><td>1.167</td><td>1.613</td></tr>
<tr><td>8</td><td>1.274</td><td>1.782</td></tr>
<tr><td>9</td><td>1.382</td><td>1.953</td></tr>
<tr><td>10</td><td>1.49</td><td>2.124</td></tr>
<tr><td>11</td><td>1.598</td><td>2.295</td></tr>
<tr><td>12</td><td>1.705</td><td>2.466</td></tr>
<tr><td>13</td><td>1.813</td><td>2.637</td></tr>
<tr><td>14</td><td>1.921</td><td>2.806</td></tr>
<tr><td>15</td><td>2.031</td><td>2.976</td></tr>
</table></td><td>0h</td></tr>
<tr><td>3</td><td>—</td><td>Reserved</td><td>0</td></tr>
<tr><td>2</td><td>R/W</td><td>CRNG: Clamping DAC output range selection
This bit is used to select the clamping DAC output range
0: Clamping DAC output ranges from 0 to AV_{DD}
1: Clamping DAC output ranges from 0 to V_{RT}.</td><td>0</td></tr>
<tr><td>1</td><td>R/W</td><td>CDACB: Clamping DAC enable control
0: Clamping DAC power down
1: Clamping DAC active</td><td>0</td></tr>
<tr><td>0</td><td>R/W</td><td>Reduces the ADC reference range $2\times(V_{RT} - V_{RB})$, thus changing the max/min input voltages.
0: ADC reference range = 2V
1: ADC reference range = 1.2V</td><td>0</td></tr>
</table>

- **Address P1_02h: 1st AFE CH_A PGA Gain LSB Register**

Bit	Mode	Description	Default
7-0	R/W	PGA1A[7:0] This register bits forms the 8 LSBs of the 1st AFE CH_A channel PGA gain code. The PGA gain is determined by combining this register bit and the MSB contained in register P1_03h.	00h

- **Address P1_03h: 1st AFE CH_A PGA Gain MSB Register**

Bit	Mode	Description	Default
7-1	—	Reserved	—
0	R/W	PGA1A[8] 1st AFE CH_A PGA gain setting register. 0.67+PGA1A[8:0]×5.35/511	0

- **Address P1_04h: 1st AFE CH_B PGA Gain LSB Register**

Bit	Mode	Description	Default
7-0	R/W	PGA1B[7:0] This register bits forms the 8 LSBs of the 1st AFE CH_B channel PGA gain code. The PGA gain is determined by combining this register bit and the MSB contained in register P1_05h.	00h

- **Address P1_05h: 1st AFE CH_B PGA Gain MSB Register**

Bit	Mode	Description	Default
7-1	——	Reserved	—
0	R/W	PGA1B[8] 1st AFE CH_B PGA gain setting register. 0.67+PGA1B[8:0]×5.35/511	0

- **Address P1_06h: 1st AFE CH_C PGA Gain LSB Register**

Bit	Mode	Description	Default
7-0	R/W	PGA1C[7:0] This register bits forms the 8 LSBs of the 1st AFE CH_C channel PGA gain code. The PGA gain is determined by combining this register bit and the MSB contained in register P1_07h.	00h

- **Address P1_07h: 1st AFE CH_C PGA Gain MSB Register**

Bit	Mode	Description	Default
7-1	—	Reserved	—
0	R/W	PGA1C[8] 1st AFE CH_C PGA gain setting register. 0.67+PGA1C[8:0]×5.35/511	0

- **Address P1_08h: 2nd AFE CH_A PGA Gain LSB Register**

Bit	Mode	Description	Default
7-0	R/W	PGA2A[7:0] This register bits forms the 8 LSBs of the 2nd AFE CH_A channel PGA gain code. The PGA gain is determined by combining this register bit and the MSB contained in register P1_09h.	00h

- **Address P1_09h: 2nd AFE CH_A PGA Gain MSB Register**

Bit	Mode	Description	Default
7-1	—	Reserved	—
0	R/W	PGA2A[8] 2nd AFE CH_A PGA gain setting register. 0.67+PGA2A[8:0]×5.35/511	0

- **Address P1_0Ah: 2nd AFE CH_B PGA Gain LSB Register**

Bit	Mode	Description	Default
7-0	R/W	PGA2B[7:0] This register bits forms the 8 LSBs of the 2nd AFE CH_B channel PGA gain code. The PGA gain is determined by combining this register bit and the MSB contained in register P1_0Bh.	00h

- **Address P1_0Bh: 2nd AFE CH_B PGA Gain MSB Register**

Bit	Mode	Description	Default
7-1	—	Reserved	—
0	R/W	PGA2B[8] 2nd AFE CH_B PGA gain setting register. 0.67+PGA2B[8:0]×5.35/511	0

- **Address P1_0Ch: 2nd AFE CH_C PGA Gain LSB Register**

Bit	Mode	Description	Default
7-0	R/W	PGA2C[7:0] This register bits forms the 8 LSBs of the 2nd AFE CH_C channel PGA gain code. The PGA gain is determined by combining this register bit and the MSB contained in register P1_0Dh.	00h

- **Address P1_0Dh: 2nd AFE CH_C PGA Gain MSB Register**

Bit	Mode	Description	Default
7-1	—	Reserved	—
0	R/W	PGA2C[8] 2nd AFE CH_C PGA gain setting register. 0.67+PGA2C[8:0]×5.35/511	0

- **Address P1_0Eh: 1st AFE CH_A Offset Register**

Bit	Mode	Description	Default
7-0	R/W	DAC1A[7:0] 1st AFE channel A 8-bit offset DAC value	00h

- **Address P1_0Fh: 1st AFE CH_B Offset Register**

Bit	Mode	Description	Default
7-0	R/W	DAC1B[7:0] 1st AFE channel B 8-bit offset DAC value	00h

- **Address P1_10h: 1st AFE CH_C Offset Register**

Bit	Mode	Description	Default
7-0	R/W	DAC1C[7:0] 1st AFE channel C 8-bit offset DAC value	00h

- **Address P1_11h: 2nd AFE CH_A Offset Register**

Bit	Mode	Description	Default
7-0	R/W	DAC2A[7:0] 2nd AFE channel A 8-bit offset DAC value	00h

- **Address P1_12h: 2nd AFE CH_B Offset Register**

Bit	Mode	Description	Default
7-0	R/W	DAC2B[7:0] 2nd AFE channel B 8-bit offset DAC value	00h

- **Address P1_13h: 2nd AFE CH_C Offset Register**

Bit	Mode	Description	Default
7-0	R/W	DAC2C[7:0] 2nd AFE channel C 8-bit offset DAC value	00h

- **Address P1_14h: AFE Current Setup Register**

Bit	Mode	Description	Default
7-6	R/W	IPGA[1:0]: AFE PGA driving current level selection 00: 191.24μA 01: 210.39μA 10: 229.3μA 11: 172μA These bits are used to select different PGA driving current levels. Note that the current listed above is an approximate tested result and only used to explain the different current level.	01
5-4	R/W	IADC[1:0]: AFE ADC driving current level selection 00: 100μA 01: 110μA 10: 120μA 11: 80μA These bits are used to select different ADC driving current levels. Note that the current listed above is an approximate tested result and only used to explain the different current level.	01
3-2	R/W	Test mode 1	00
1-0	R/W	Test mode 0	00

- **Address P1_15h: AFE 60MHz Current Setup Register**

Bit	Mode	Description	Default
—	—	Reserved	—
0	R/W	ADC driving current enhance function enable control 0: Disable 1: Enable	0

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 2 Registers – TG Control Registers

- **Address P2_00h: TG Main Configuration Register 0**

Bit	Mode	Description	Default
7	R/W	TG2 pixel processing color order 0: Forward 1: Reverse	0
6-4	R/W	TG2 Color Sequence Length. Used in Mode 1a to determine the number of colors sequenced during a scan. 111: Not valid 110: Six color (component) sequence 101: Five color (component) sequence 100: Four color (component) sequence 011: Three color (component) sequence 010: Two color (component) sequence 001: One color (component) sequence (Default) 000: Not Valid	001
3	R/W	TG1 pixel processing color order 0: Forward 1: Reverse	0
2-0	R/W	TG1 Color Sequence Length. Used in Mode 1a to determine the number of colors sequenced during a scan. 111: Not valid 110: Six color (component) sequence 101: Five color (component) sequence 100: Four color (component) sequence 011: Three color (component) sequence 010: Two color (component) sequence 001: One color (component) sequence (Default) 000: Not Valid	001

- **Address P2_01h: TG Main Configuration Register 1**

Bit	Mode	Description	Default
7	R/W	Bypass Original 16-bit AFE Data to Video Port enable control 0: Disable 1: Enable	0
6	R/W	TG Test Pattern Enable control 0: Disable 1: Enable	0
5	R/W	TG2 Function Active_n (active low) 0: TG2 Function Active 1: TG2 Function Inactive Notes: 1. When the Frame Start source is selected from the “SPI” by configuring the P4_0Bh and the TG2 Function is Active, setting the TG2 Start Scan (BOS) trigger bit will start capturing data and lighting signals to sensor. 2. When the Frame End source is selected from the “SPI” by configuring the P4_0Bh and the TG2 Function is Inactive or resetting the TG2 Start Scan (BOS) trigger bit will stop capturing data and lighting signals to sensor.	1
4	R/W	TG2 Start Scan (BOS) trigger bit 0: Ready 1: Start Scan	0
3	R/W	Bypass Original 16-bit AFE Data Selection 0: AFE1 1: AFE2 Note: When the bit 7 is set high to enable the bypass AFE data function, the P7_00h content should be 8’h00, the P9_00h content should be 8’h00, the P9_01h content should be 8’h00 and the P9_02h content should be 8’h00.	0

Bit	Mode	Description	Default
2	R/W	Software Reset bit Performs a reset for TG1, TG2 Controller and TG1, TG2 Register when setting this bit to 1. This bit will be cleared automatically after setting high.	0
1	R/W	TG1 Function Active_n (active low) 0: TG1 Function Active 1: TG1 Function Inactive	1
0	R/W	TG1 Start Scan (BOS) trigger bit 0: Ready 1: Start Scan Notes: 1. When the Frame Start source is selected from the “SPI” by configuring the P4_0Bh and the TG1 Function is Active, setting the TG1 Start Scan (BOS) trigger bit will start capturing data and lighting signals to sensor. 2. When the Frame End source is selected from the “SPI” by configuring the P4_0Bh and the TG1 Function is Inactive or resetting TG1 Start Scan (BOS) trigger bit will stop capturing data and lighting signals to sensor.	0

- **Address P2_02h: TG Control Register 0**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	RO	DLL Test output status when bit4=1 0: DLL OK 1: DLL Fail	—
4	R/W	DLL Test mode Enable control 0: Disable – No detection 1: Enable – Detection	0
3-2	R/W	DLL control selection 00: Input frequency < 12MHz 01: 12MHz < Input frequency < 16MHz 10: Input frequency > 16MHz 11: Reserved	00
1	R/W	CIS_CLK output level when CIS_CLK is inactive 1: High level 0: Low level	0
0	R/W	DLL Enable control 0: Disable 1: Enable The DLL circuit will generate an Active_Low pulse after a power_on reset.	1

- **Address P2_03h: TG Control Register 1**

Bit	Mode	Description	Default
7	R/W	Vertical DPI Selection 0: 100dpi 1: 200dpi	0
6	—	Reserved	—
5	RO	TG2 Activation On/Off status 0: TG2 is not activated 1: TG2 is activated Note: Checking the TG2 Activation On/Off status when setting the relative selection in the P2_01h [5] and P4_0Bh [1:0] fields.	0
4	RO	TG1 Activation On/Off status 0: TG1 is not activated 1: TG1 is activated Note: Checking the TG1 Activation On/Off status when setting the relative selection in the P2_01h [1] and P4_0Bh [1:0] fields.	0
3	R/W	TG2 Color Sequence Length Minus One function enable control 0: Disable 1: Enable Note: When this bit is set to 1, the TG2 total color sequence length will be decreased by one.	0
2	R/W	TG1 Color Sequence Length Minus One function enable control 0: Disable 1: Enable Note: When this bit is set to 1, the TG1 total color sequence length will be decreased by one.	0
1	R/W	TG2 Color Sequence Length Multiply by 2 function enable control 0: Disable 1: Enable Note: When this bit is set to 1, the TG2 color sequence length defined in the register P2_00h bit6~bit4 will be multiplied by 2.	0
0	R/W	TG1 Color Sequence Length Multiply by 2 function enable control 0: Disable 1: Enable Note: When this bit is set to 1, the TG2 color sequence length defined in the register P2_00h bit2~bit0 will be multiplied by 2.	0

- **Address P2_04h: TG Control Register 2**

Bit	Mode	Description	Default
7	R/W	AFE Data Sampling Edge Selection 0: Negative Edge Sampled 1: Positive Edge Sampled This bit is used to select that the device samples the AFE Data on the ADC clock positive edge or negative edge.	0
6	R/W	Line Pixel Number Adjustment Enable control 0: Disable 1: Enable The Line Pixel numbers are adjusted by positive edge of the ROLLER_IN input when the adjustment function is enabled. Note: 1. For TG SI Slave mode, adjust line end. 2. For TG SI Continuous mode, adjust Active LEDs averagely.	0
5-4	R/W	ADC Clock Latency Number with respect to pixel clock 00: No ADC clock latency with respect to pixel clock 01: One ADC clock latency with respect to pixel clock 10: Two ADC clock latency with respect to pixel clock 11: Reserved These bits are used to select the ADC clock latency number with respect to the pixel clock when the current AFE Data appears.	01
3-2	R/W	CIS2 Sensor Channel Number Selection 00: Reserved 01: One Channel Number 10: Two Channel Numbers 11: Three Channel Numbers	11
1-0	R/W	CIS1 Sensor Channel Number Selection 00: Reserved 01: One Channel Number 10: Two Channel Numbers 11: Three Channel Numbers	11

- **Address P2_05h: TG CIS_CLK/AFE_CLK Control Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6	R/W	AFE_CLK Polarity 0: Normal – Low when inactive 1: Inverted – High when inactive	1
5-3	—	Reserved	—
2	R/W	CIS_CLK Polarity 0: Normal – Low when inactive 1: Inverted – High when inactive	1
1	—	Reserved	—
0	R/W	CIS_CLK Activity During SH 0: Inactive 1: Active	1

- **Address P2_06h: TG CIS_CLK Start Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	CIS_CLK on point This field is used to define when the CIS_CLK signal turns on during the pixel period. It can be set to any available edge during the pixel period.	00h

- **Address P2_07h: TG CIS_CLK End Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	CIS_CLK off point This field is used to define when the CIS_CLK signal turns off during the pixel period. It can be set to any available edge during the pixel period.	40h

- **Address P2_0Ah: TG AFE_SHD Start Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	AFE_SHD on point This field is used to define when the AFE_SHD signal turns on during the pixel period. It can be set to any available edge within the pixel period.	40h

- **Address P2_0Bh: TG AFE_SHD End Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-0	R/W	AFE_SHD off point This field is used to define when the AFE_SHD signal turns off during the pixel period. It can be set to any available edge during the pixel period.	60h

- **Address P2_0Ch: TG CIS_CLK/SH On Guardband Register**

Bit	Mode	Description	Default
7-0	R/W	CIS_CLK on guardband This field is used to define the number of pixel periods from the end of the SH pulse to the start of the CIS_CLK signal.	00h

- **Address P2_0Dh: TG CIS_CLK/SH Off Guardband Register**

Bit	Mode	Description	Default
7-0	R/W	CIS_CLK off guardband This field is used to define the number of pixel periods before the start of the SH pulse as the CIS_CLK stops.	00h

- **Address P2_0Eh: TG Wheel Step MSB Register**

Bit	Mode	Description	Default
7-3	-	Reserved	-
2-0	R/W	TG wheel Step Most Significant 3 Bits Wheel Step is from 1.0~8.0 mm/step and wheel step should multiply 128 to set whole register Ex: 1 mm/step: 100DPI → 4 lines/step 2 mm/step: 100DPI → 8 lines/step	00h

- **Address P2_0Fh: TG Wheel Step LSB Register**

Bit	Mode	Description	Default
7-0	R/W	TG wheel Step Least Significant Byte Wheel Step is from 1.0~8.0 mm/step and wheel step should multiply 128 to set whole register	80h

- **Address P2_10h: TG Wheel Control Register**

Bit	Mode	Description	Default
7	R/W	TG Wheel input selection 0: Internal wheel after shaping signal from pad “PADROLLER_IN” 1: From pad “PADROLLER_IN”	0
6	R/W	TG Wheel signal inversion enable control 0: Inversion disable 1: Inversion enable	0
5-3	R/W	Reserved	—
2-1	R/W	TG Wheel Filtering Selection 00: 3-tap filtering 01: 5-tap filtering 10: 8-tap filtering 11: 12-tap filtering	00
0	R/W	TG Wheel Filtering enable control 0: Disable 1: Enable	1

- **Address P2_11h: CIS1/CIS2 Dummy LAMP Selection Register**

Bit	Mode	Description	Default
7-6	R/W	Dummy LAMP mode selection 00: Dummy LAMP following register by bit[5:0] 01: Dummy LAMP following previous light signal 10: Dummy LAMP following post light signal 11: Reserved	00
5	R/W	Red LAMP Enable control 0: Red Disabled 1: Red Enabled	0
4	R/W	Green LAMP Enable control 0: Green Disabled 1: Green Enabled	0
3	R/W	Blue LAMP Enable control 0: Blue Disabled 1: Blue Enabled	0
2	R/W	IR1 LAMP Enable control 0: IR1 Disabled 1: IR1 Enabled	0
1	R/W	IR2 LAMP Enable control 0: IR2 Disabled 1: IR2 Enabled	0
0	R/W	UV LAMP Enable control 0: UV Disabled 1: UV Enabled	0

- **Address P2_12h: CIS1/CIS2 Dummy LAMP On MSB Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R/W	Dummy LAMP Enable control 0: Dummy LAMP Disabled 1: Dummy LAMP Enable Note: If Dummy LAMP is disabled, all LAMP will be off in the dummy LAMP region	0
3-0	R/W	CIS1/CIS2 Dummy LAMP On Time Most Significant Byte This selects the pixel count at which the Dummy LAMP output goes active.	0h

- **Address P2_13h: CIS1/CIS2 Dummy LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	CIS1/CIS2 Dummy LAMP On Time Least Significant Bits. This selects the pixel count at which the DUMMY LAMPR output goes active. Note: Real CIS1/CIS2 Dummy on position = Dummy Lamp on register × 4	00h

- **Address P2_14h: CIS1/CIS2 Dummy LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	CIS1/CIS2 Dummy LAMP Off Time Most Significant Byte This selects the pixel count at which the Dummy LAMP output goes inactive.	0h

- **Address P2_15h: CIS1/CIS2 Dummy LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	CIS1/CIS2 Dummy LAMP Off Time Least Significant Bits. This selects the pixel count at which the Dummy LAMP output goes inactive. Note: Real CIS1/CIS2 Lamp off position = Lamp off register × 4	00h

- **Address P2_16h: CIS1 LAMP Component Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	
5	R/W	CIS1 Component 6 LAMP or CIS1 Component 12 LAMP Selection 0: CIS1 Component 6 LAMP 1: CIS1 Component 12 LAMP Note: When setting this bit to "0", register P5_06h [5:0] belongs to component 6 LAMP and vice versa.	0
4	R/W	CIS1 Component 5 LAMP or CIS1 Component 11 LAMP Selection 0: CIS1Component 5 LAMP 1: CIS1Component 11 LAMP Note: When setting this bit to "0", register P5_05h [5:0] belongs to component 5 LAMP and vice versa.	0
3	R/W	CIS1 Component 4 LAMP or CIS1 Component 10 LAMP Selection 0: CIS1 Component 4 LAMP 1: CIS1 Component 10 LAMP Note: When setting this bit to "0", register P5_04h [5:0] belongs to component 4 LAMP and vice versa.	0
2	R/W	CIS1 Component 3 LAMP or CIS1 Component 9 LAMP Selection 0: CIS1 Component 3 LAMP 1: CIS1 Component 9 LAMP Note: When setting this bit to "0", register P5_03h [5:0] belongs to Component 3 LAMP and vice versa.	0
1	R/W	CIS1 Component 2 LAMP or CIS1 Component 8 LAMP Selection 0: CIS1 Component 2 LAMP 1: CIS1 Component 8 LAMP Note: When setting this bit to "0", register P5_02h [5:0] belongs to Component 2 LAMP and vice versa.	0
0	R/W	CIS1 Component 1 LAMP or CIS1 Component 7 LAMP Selection 0: CIS1 Component 1 LAMP 1: CIS1 Component 7 LAMP Note: When setting this bit to "0", register P5_01h [5:0] belongs to Component 1 LAMP and vice versa.	0

- **Address P2_17h: CIS2 LAMP Component Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	
5	R/W	CIS2 Component 6 LAMP or CIS2 Component 12 LAMP Selection 0: CIS2 Component 6 LAMP 1: CIS2 Component 12 LAMP Note: When setting this bit to "0", register P6_06h [5:0] belongs to Component 6 LAMP and vice versa.	0
4	R/W	CIS2 Component 5 LAMP or CIS2 Component 11 LAMP Selection 0: CIS2 Component 5 LAMP 1: CIS2 Component 11 LAMP Note: When setting this bit to "0", register P6_05h [5:0] belongs to Component 5 LAMP and vice versa.	0
3	R/W	CIS2 Component 4 LAMP or CIS2 Component 10 LAMP Selection 0: CIS2 Component 4 LAMP 1: CIS2 Component 10 LAMP Note: When setting this bit to "0", register P6_04h [5:0] belongs to Component 4 LAMP and vice versa.	0
2	R/W	CIS2 Component 3 LAMP or CIS2 Component 9 LAMP Selection 0: CIS2 Component 3 LAMP 1: CIS2 Component 9 LAMP Note: When setting this bit to "0", register P6_03h [5:0] belongs to Component 3 LAMP and vice versa.	0
1	R/W	CIS2 Component 2 LAMP or CIS2 Component 8 LAMP Selection 0: CIS2 Component 2 LAMP 1: CIS2 Component 8 LAMP Note: When setting this bit to "0", register P6_02h [5:0] belongs to Component 2 LAMP and vice versa.	0
0	R/W	CIS2 Component 1 LAMP or CIS2 Component 7 LAMP Selection 0: CIS2 Component 1 LAMP 1: CIS2 Component 7 LAMP Note: When setting this bit to "0", register P6_01h [5:0] belongs to Component 1 LAMP and vice versa.	0

- **Address P2_18h: CIS Black Level Clamp Control Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R/W	CIS Black Level Enable control 0: Disable 1: Enable	0
3-2	—	Reserved	—
1-0	R/W	CIS Black Level Clamp Width selection 00: 4 pixels 01: 8 pixels 10: 16 pixels 11: 32 pixels	00

- **Address P2_19h: CIS Black Level Clamp Position Register**

Bit	Mode	Description	Default
7	—	Reserved	
6-0	R/W	Black Level Clamp Position Number of pixels in which the Auto Black pulse is delayed relative to falling edge of SH pulse.	00h

- **Address P2_1Ah: CIS to AFE Sequence Mapping Register**

Bit	Mode	Description	Default
7	—	Reserved	—
6-4	R/W	CIS2 to AFE Sequence Mapping Selection 000: 1-2-3, CIS Analog input 1 2 3 ↔ ASIC AFE R1 G1 B1 001: 3-2-1, CIS Analog input 1 2 3 ↔ ASIC AFE B1 G1 R1 010: 2-1-3, CIS Analog input 1 2 3 ↔ ASIC AFE G1 R1 B1 011: 3-1-2, CIS Analog input 1 2 3 ↔ ASIC AFE B1 R1 G1 100: 1-3-2, CIS Analog input 1 2 3 ↔ ASIC AFE R1 B1 G1 101: 2-3-1, CIS Analog input 1 2 3 ↔ ASIC AFE G1 B1 R1 Others: Reserved	000
3	—	Reserved	—
2-0	R/W	CIS1 to AFE Sequence Mapping Selection 000: 1-2-3, CIS Analog input 1 2 3 ↔ ASIC AFE R1 G1 B1 001: 3-2-1, CIS Analog input 1 2 3 ↔ ASIC AFE B1 G1 R1 010: 2-1-3, CIS Analog input 1 2 3 ↔ ASIC AFE G1 R1 B1 011: 3-1-2, CIS Analog input 1 2 3 ↔ ASIC AFE B1 R1 G1 100: 1-3-2, CIS Analog input 1 2 3 ↔ ASIC AFE R1 B1 G1 101: 2-3-1, CIS Analog input 1 2 3 ↔ ASIC AFE G1 B1 R1 Others: Reserved	000

- **Address P2_1Dh: CIS1 Output Control Signals Strength Register**

Bit	Mode	Description	Default
7-6	R/W	CIS_CLK Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01
5-4	R/W	CIS1_LAMP Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01
3-2	R/W	CIS1_MODE Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	00
1-0	R/W	CIS1_SP Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01

- **Address P2_1Eh: CIS2 Output Control Signals Strength Register**

Bit	Mode	Description	Default
7-2	—	Reserved	—
1-0	R/W	CIS2_LAMP Strength Selection 2'b00: 4mA 2'b01: 8mA 2'b10: 12mA 2'b11: 16mA	01

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 3 Registers – TG Timing 1 Registers

- **Address P3_00h: TG CIS_1 CH_1 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h

- **Address P3_01h: TG CIS_1 CH_1 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Note: Start valid pixels mean the distance from the falling edge of the SH to the beginning of the valid pixel. If CH_A start valid pixel and end valid pixel register are all zero, there will be no data captured in this channel.	01h

- **Address P3_02h: TG CIS_1 CH_1 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	01h

- **Address P3_03h: TG CIS_1 CH_1 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Note: End valid pixels mean the distance from the falling edge of the SH to the end of the valid pixel. If CH_A start valid pixel and end valid pixel register are all zero, there will be no data captured in this channel.	B0h

- **Address P3_04h: TG CIS_1 CH_2 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h

- **Address P3_05h: TG CIS_1 CH_2 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Note: Start valid pixels mean the distance from the falling edge of the SH to the beginning of the valid pixel. If CH_B start valid pixel and end valid pixel register are all zero, there will be no data captured in this channel.	01h

- **Address P3_06h: TG CIS_1 CH_2 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	01h

- **Address P3_07h: TG CIS_1 CH_2 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Note: End valid pixels mean the distance from the falling edge of the SH to the end of the valid pixel. If CH_B start valid pixel and end valid pixel register are all zero, there will be no data captured in this channel	B0h

- **Address P3_08h: TG CIS_1 CH_3 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h

- **Address P3_09h: TG CIS_1 CH_3 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Note: Start valid pixels mean the distance from the falling edge of the SH to the beginning of the valid pixel. If CH_C start valid pixel and end valid pixel register are all zero, there will be no data captured in this channel.	01h

- **Address P3_0Ah: TG CIS_1 CH_3 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	02h

- **Address P3_0Bh: TG CIS_1 CH_3 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Note: End valid pixels mean the distance from the falling edge of the SH to the end of the valid pixel. If CH_C start valid pixel and end valid pixel register are all zero, there will be no data captured in this channel	40h

- **Address P3_0Ch: TG CIS_1 Line Valid Start and End MSB Register**

Bit	Mode	Description	Default
7-4	R/W	AFE1 Line Valid Start Value – Most Significant 4 Bits Selects the Line count where the valid line is started after BOS	0h
3-0	R/W	AFE1 Line Valid End Value – Most Significant 4 Bits Selects the Line count where the valid line is ended after BOS	0h

- **Address P3_0Dh: TG CIS_1 Line Valid Start LSB Register**

Bit	Mode	Description	Default
7-0	R/W	AFE1 Line Valid Start Value – Least Significant Byte Selects the Line count where the valid line is ended after BOS	00h

- **Address P3_0Eh: TG CIS_1 Line Valid End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	AFE1 Line Valid End Value – Least Significant Byte Selects the Line count where the valid line is ended after BOS Note: When line valid Start value is equal to zero and the valid End value is equal to zero, the line is always valid after BOS.	00h

- **Address P3_0Fh: TG CIS_2 CH_1 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h

- **Address P3_10h: TG CIS_2 CH_1 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Note: Start valid pixels mean the distance from the falling edge of the SH to the beginning of the valid pixel. If CH_A start valid pixel and end valid pixel register are equal, there will be no data captured in this channel. Note that the (End valid pixel-Start valid pixel+1) value should be even.	01h

- **Address P3_11h: TG CIS_2 CH_1 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	01h

- **Address P3_12h: TG CIS_2 CH_1 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Note: End valid pixels mean the distance from the falling edge of the SH to the end of the valid pixel. If CH_A start valid pixel and end valid pixel register are equal, there will be no data captured in this channel. Note that the (End valid pixel-Start valid pixel+1) value should be even.	B0h

- **Address P3_13h: TG CIS_2 CH_2 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h

- **Address P3_14h: TG CIS_2 CH_2 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Note: Start valid pixels mean the distance from the falling edge of the SH to the beginning of the valid pixel. If CH_B start valid pixel and end valid pixel register are equal, there will be no data captured in this channel. Note that the (End valid pixel-Start valid pixel+1) value should be even.	01h

- **Address P3_15h: TG CIS_2 CH_2 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	01h

- **Address P3_16h: TG CIS_2 CH_2 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Note: End valid pixels mean the distance from the falling edge of the SH to the end of the valid pixel. If CH_B start valid pixel and end valid pixel register are equal, there will be no data captured in this channel. Note that the (End valid pixel-Start valid pixel+1) value should be even.	B0h

- **Address P3_17h: TG CIS_2 CH_3 Start of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	Start of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits begin to indicate valid pixels.	00h

- **Address P3_18h: TG CIS_2 CH_3 Start of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Start of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits begin to indicate valid pixels. Note: Start valid pixels mean the distance from the falling edge of the SH to the beginning of the valid pixel. If CH_C start valid pixel and end valid pixel register are equal, there will be no data captured in this channel. Note that the (End valid pixel-Start valid pixel+1) value should be even.	01h

- **Address P3_19h: TG CIS_2 CH_3 End of Valid Pixels MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5-0	R/W	End of Valid Pixels – Most Significant 6 Bits. Selects the pixel count where the data status bits stop indicating valid pixels.	02h

- **Address P3_1Ah: TG CIS_2 CH_3 End of Valid Pixels LSB Register**

Bit	Mode	Description	Default
7-0	R/W	End of Valid Pixels – Least Significant Byte. Selects the pixel count where the data status bits stop indicating valid pixels. Note: End valid pixels mean the distance from the falling edge of the SH to the end of the valid pixel. If CH_C start valid pixel and end valid pixel register are equal, there will be no data captured in this channel. Note that the (End valid pixel-Start valid pixel+1) value should be even.	40h

- **Address P3_1Bh: TG CIS_2 Line Valid Start and End MSB Register**

Bit	Mode	Description	Default
7-4	R/W	AFE2 Line Valid Start Value – Most Significant 4 Bits Selects the Line count where the valid line is started after BOS	0h
3-0	R/W	AFE2 Line Valid End Value – Most Significant 4 Bits Selects the Line count where the valid line is ended after BOS	0h

- **Address P3_1Ch: TG CIS_2 Line Valid Start LSB Register**

Bit	Mode	Description	Default
7-0	R/W	AFE2 Line Valid Start Value – Least Significant Byte Selects the Line count where the valid line is started after BOS	00h

- **Address P3_1Dh: TG CIS_2 Line Valid End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	AFE2 Line Valid End Value – Least Significant Byte Selects the Line count where the valid line is ended after BOS Note: When the line valid Start and End values are equal to zero , the line value is always valid after BOS	00h

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 4 Registers – TG Timing 2 Registers

- **Address P4_00h: TG MODE Output Selection Register**

Bit	Mode	Description	Default
7-2	—	Reserved	—
1-0	R/W	TG mode selection 2'h0: TG_MODE 2'h1: ~TG_MODE 2'h2: TG_MODE = 0 2'h3: TG_MODE = 1	00

- **Address P4_01h: TG MODE On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Mode On Time Most Significant Bits This selects the pixel count at which the Mode output goes high.	0h

- **Address P4_02h: TG MODE On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Mode On Time Least Significant Byte This selects the pixel count at which the Mode output goes high.	00h

- **Address P4_03h: TG MODE Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Mode Off Time Most Significant Bits This selects the pixel count at which the Mode output goes low.	00h

- **Address P4_04h: TG MODE Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Mode Off Time Least Significant Byte This selects the pixel count at which the Mode output goes low.	00h

- **Address P4_05h: TG SI MODE Selection Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-2	R/W	SI Master/Slave/Continuous Selection 00: SP and LAMP generated by external wheel. The TG runs in Slave mode with SI and LAMP triggered by an external pulse on the ROLLER_IN pin. 01: Auto generated SI and LAMP. The TG runs in Master mode with SI and LAMP generated internally with a programmable period and width. 11: SI automatic generated and LAMP generated by external wheel. 10: Reserved	11
1-0	R/W	SI Output Mode 00: SI Output = SI 01: SI Output = ~SI 10: SI Output = 0 11: SI Output = 1	00

- **Address P4_06h: TG SI Width Register**

Bit	Mode	Description	Default
7-0	R/W	SI Pulse Width SI Pulse Width = (2×[7:0]) + 1	04h

- **Address P4_07h: TG_1 Line End MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	
5-0	R/W	TG1 Line End Value – Most Significant 6 Bits Selects the pixel count where the current line is ended and next one begins. Control the integration time of one line and period between SP pulses.	00h

- **Address P4_08h: TG_1 Line End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	TG1 Line End Value – Least Significant Byte Selects the pixel count where the current line is ended and next one begins. Control the integration time of one line and period between SP pulses, which is (0 ~ 16383) pixels.	20h

- **Address P4_0Bh: Frame Start/End Selection Register**

Bit	Mode	Description	Default
7	RO	Frame Jam status 0: Normal 1: Frame jam	—
6	R/W	Sensor Domination Selection for Frame End by Fix Length and auto detection 0: CIS1 1: CIS2	0
5-4	R/W	Frame End control Selection 00: By SPI 01: Auto detection 10: Frame Fixed length 11: By “FRM_START” pin low level Notes: 1. When the P2_01h Bit1 or Bit5 is set to be active, the Frame End will take effect and vice versa. 2. If the field is set to “11”, the Frame End will take place by the “FRM_START” pin going low while the Frame Start will take place by the “FRM_START” pin going high.	00
3	R/W	Frame Jam Function Enable 0: Disable 1: Enable Note: When this bit is set high to enable the Frame Jan function, the registers from P4_1Ah to P4_1Dh should be properly configured.	0
2	R/W	Senor Domination Selection for Frame Start by auto detection 0: CIS1 1: CIS2	0
1-0	R/W	Frame Start Selection 00: By SPI 01: Auto detection 10: By Pad “FRM_START” pulse 11: By Pad “FRM_START” high level Notes: 1. When the P2_01h Bit1 or Bit5 is set to be active, the Frame Start will take effect and vice versa. 2. When the field is set to “11”, the Frame Start will take place by the “FRM_START” pin going high while the Frame End will take place by the “FRAME_END” pin going low.	00

- **Address P4_0Ch: Pixel Threshold for Auto Detection of Frame Start Register**

Bit	Mode	Description	Default
7-0	R/W	Pixel Threshold For Frame Start Auto Detection EX. If the background is black on register P9_01h Bit2/Bit6 and the input data is larger than or equal to the pixel threshold, the input data will be probably a valid data. If the background is white and the input data is smaller than the pixel threshold, the Input data will probably be a valid data.	00h

- **Address P4_0Dh: Number of Pixel per Line for Frame Start Auto Detection MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Number of Pixel per Line for Frame Start Auto Detection	000

- **Address P4_0Eh: Number of Pixel per Line for Frame Start Auto Detection LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Number of Pixel per Line for Frame Start Auto Detection Notes: 1. Checking how many pixels should meet the register P4_0Ch. 2. Pixel comparison region are referenced by registers P9_16h ~ P9_1Bh and P4_0Bh bit [2].	00h

- **Address P4_0Fh: Number of Lines for Frame Start Auto Detection MSB Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Line order restart enable control after frame start auto detection 0: Disable 1: Enable Note: For the line order of R, G, B, IR and UV when this bit is set high to enable the restart function, the line sequence order will restart after the frame start auto detection.	1
4	R/W	Continuous Line meet line threshold function enable control for frame start auto detection 0: Disable 1: Enable	1
3-0	R/W	Number of Lines for Frame Start Auto Detection	0h

- **Address P4_10h: Number of Lines for Auto Detection of Frame Start LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Number of Lines for Frame Start Auto Detection Checking how many lines should meet registersP4_0Dh and P4_0Eh.	00h

- **Address P4_11h: Pixel Threshold for Auto Detection of Frame End Register**

Bit	Mode	Description	Default
7-0	R/W	Pixel Threshold for Frame End Auto Detection Ex: If the background is black on register P9_01h Bit2/Bit6 and the input data is smaller than the pixel threshold, the input data will be probably invalid data. If the background is white and the input data is larger than the pixel threshold, the input data will be probably an invalid data.	00h

- **Address P4_12h: Number of Pixel per Line for Frame End Auto Detection MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Number of Pixel per Line for Frame End Auto Detection Checking how many pixels should meet the register P4_11h.	000

- **Address P4_13h: Number of Pixel per Line for Frame End Auto Detection LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Number of Pixel per Line for Frame End Auto Detection 1. Checking how many pixels should meet the register P4_11h. 2. Pixel comparison region are referenced by registers P9_16h ~ P9_1Bh and P4_0Bh bit [6].	00h

- **Address P4_14h: Number of Lines for Frame End Auto Detection MSB Register**

Bit	Mode	Description	Default
7-5	—	Reserved	—
4	R/W	Continuous Line meet line threshold function enable control for frame end auto detection 0: Disable 1: Enable	0
3-0	R/W	Number of Lines for Frame End Auto Detection	0h

- **Address P4_15h: Number of Lines for Auto Detection of Frame End LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Number of Lines for Frame End Auto Detection Checking how many lines should meet registers P4_12h and P4_13h.	00h

- **Address P4_16h: Delay Lines for Frame End Starting Detection MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Delay Lines for Frame End Starting Detection Most Significant Byte	0h

- **Address P4_17h: Delay Lines for Frame End Starting Detection LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Delay Lines for Frame End Starting Detection Least Significant Byte Note: This register is only available for Frame Start By the pin FRM_START or the SPI on and Frame end by auto detection.	00h

- **Address P4_18h: Number of Lines for Frame End Fix Length MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Delay Lines for Frame End Fix Length Most Significant Byte	0h

- **Address P4_19h: Number of Lines for Frame End Fix Length LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Delay Lines for Frame End Fix Length Least Significant Byte Note: This register is only available by choosing frame end with the fix length via the register P4_0Bh [5:4].	00h

- **Address P4_1Ah: Frame Jam Counter Register 0**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Frame Jam Counter [27:24] due to wheel stock by pixel clock Note: If the wheel is not detected after meeting the frame jam counter, the TG controller will not be activated.	0h

- **Address P4_1Bh: Frame Jam Counter Register 1**

Bit	Mode	Description	Default
7-0	R/W	Frame Jam Counter [23:16] due to wheel stock by pixel clock Note: If the wheel is not detected after meeting the frame jam counter, the TG controller will not be activated.	00h

- **Address P4_1Ch: Frame Jam Counter Register 2**

Bit	Mode	Description	Default
7-0	R/W	Frame Jam Counter [15:8] due to wheel stock by pixel clock Note: If the wheel is not detected after meeting the frame jam counter, the TG controller will not be activated.	00h

- **Address P4_1Dh: Frame Jam Counter Register 3**

Bit	Mode	Description	Default
7-0	R/W	Frame Jam Counter [7:0] due to wheel stock by pixel clock Note: If the wheel is not detected after meeting the frame jam counter, the TG controller will not be activated.	00h

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 5 Registers – CIS 1 LAMP Control Registers

- **Address P5_00h: CIS1 LAMP Mode Register**

Bit	Mode	Description	Default
7	R/W	$LAMP_R$ Normal State 0: Low 1: High	0
6	R/W	$LAMP_G$ Normal State 0: Low 1: High	0
5	R/W	$LAMP_B$ Normal State 0: Low 1: High	0
4	R/W	$LAMP_{IR1}$ Normal State 0: Low 1: High	0
3	R/W	$LAMP_{IR2}$ Normal State 0: Low 1: High	0
2	R/W	$LAMP_{UV}$ Normal State 0: Low 1: High	0
1-0	—	Reserved	—

- **Address P5_01h: CIS1 Component 1/Component 7 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	1
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled Note: If the CIS 1 sequence is W, W, W, IR, W, W, W and UV, 1. Setting sequence length register on P2_00h bit [3:0] → 4'h04 2. Setting multiplication register on P2_03h bit [0] → 1'h1 3. Setting component selection register on P2_16h bit [5-0] → 6'h0 and component 1 LAMP at P5_01h bit [5:0] → 6'h38 4. Component 2 LAMP at P5_02h bit [5:0] → 6'h38 5. Component 3 LAMP at P5_03h bit [5:0] → 6'h38 6. Component 4 LAMP at P5_04h bit [5:0] → 6'h04 7. Component 5 LAMP at P5_05h bit [5:0] → 6'h38 8. Component 6 LAMP at P5_06h bit [5:0] → 6'h38 9. Setting component selection register on P2_16h bit [1:0] → 3'h3 and component 7 LAMP at P5_01h bit [5:0] → 6'h38 10. Component 8 LAMP at P5_02h bit [5:0] → 6'h01	0

- **Address P5_02h: CIS1 Component 2/Component 8 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	1
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	0

- **Address P5_03h: CIS1 Component 3/Component 9 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	1
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	0

- **Address P5_04h: CIS1 Component 4/Component 10 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	1
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	0

- **Address P5_05h: CIS1 Component 5/Component 11 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	1
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	0

- **Address P5_06h: CIS1 Component 6/Component 12 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable 0: Disabled control 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	1

- **Address P5_07h: CIS1 Red LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_R$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_R$ output goes high.	0h

- **Address P5_08h: CIS1 Red LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_R$ On Time Least Significant Bits. This field selects the pixel count at which the $LAMP_R$ output goes high. Note: Real CIS1 $LAMP_R$ on position = $LAMP_R$ on register × 4	2Eh

- **Address P5_09h: CIS1 Red LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_R$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_R$ output goes low.	1h

- **Address P5_0Ah: CIS1 Red LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_R$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_R$ output goes low. Note: Real CIS1 $LAMP_R$ off position = $LAMP_R$ off register × 4	06h

- **Address P5_0Bh: CIS1 Green LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_G$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_G$ output goes high.	0h

- **Address P5_0Ch: CIS1 Green LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_G$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_G$ output goes high. Note: Real CIS1 $LAMP_G$ on position = $LAMP_G$ on register × 4	2Eh

- **Address P5_0Dh: CIS1 Green LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_G$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_G$ output goes low.	1h

- **Address P5_0Eh: CIS1 Green LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_G$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_G$ output goes low. Note: Real CIS1 $LAMP_G$ off position = $LAMP_G$ off register × 4	06h

- **Address P5_0Fh: CIS1 Blue LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_B$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_B$ output goes high.	0h

- **Address P5_10h: CIS1 Blue LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_B$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_B$ output goes high. Note: Real CIS1 $LAMP_B$ on position = $LAMP_B$ on register × 4	2Eh

- **Address P5_11h: CIS1 Blue LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_B$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_B$ output goes low.	1h

- **Address P5_12h: CIS1 Blue LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_B$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_B$ output goes low. Note: Real CIS1 $LAMP_B$ off position = $LAMP_B$ off register × 4	06h

- **Address P5_13h: CIS1 IR1 LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR1}$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_{IR1}$ output goes high.	0h

- **Address P5_14h: CIS1 IR1 LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR1}$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_{IR1}$ output goes high. Note: Real CIS1 $LAMP_{IR1}$ on position = $LAMP_{IR1}$ on register × 4	2Eh

- **Address P5_15h: CIS1 IR1 LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR1}$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_{IR1}$ output goes low.	1h

- **Address P5_16h: CIS1 IR1 LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR1}$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_{IR1}$ output goes low. Note: Real CIS1 $LAMP_{IR1}$ off position = $LAMP_{IR1}$ off register × 4	06h

- **Address P5_17h: CIS1 IR2 LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR2}$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_{IR2}$ output goes high.	0h

- **Address P5_18h: CIS1 IR2 LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR2}$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_{IR2}$ output goes high. Note: Real CIS1 $LAMP_{IR2}$ on position = $LAMP_{IR2}$ on register × 4	2Eh

- **Address P5_19h: CIS1 IR2 LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR2}$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_{IR2}$ output goes low.	1h

- **Address P5_1Ah: CIS1 IR2 LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR2}$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_{IR2}$ output goes low. Note: Real CIS1 $LAMP_{IR2}$ off position = $LAMP_{IR2}$ off register × 4	06h

- **Address P5_1Bh: CIS1 UV LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{UV}$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_{UV}$ output goes high.	0h

- **Address P5_1Ch: CIS1 UV LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{UV}$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_{UV}$ output goes high. Note: Real CIS1 $LAMP_{UV}$ on position = $LAMP_{UV}$ on register × 4	2Eh

- **Address P5_1Dh: CIS1 UV LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{UV}$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_{UV}$ output goes low.	1h

- **Address P5_1Eh: CIS1 UV LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{UV}$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_{UV}$ output goes low. Note: Real CIS1 $LAMP_{UV}$ off position = $LAMP_{UV}$ off register × 4	06h

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—-
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 6 Registers – CIS 2 LAMP Control Registers

- **Address P6_00h: CIS2 LAMP Mode Register**

Bit	Mode	Description	Default
7	R/W	$LAMP_R$ Normal State 0: Low 1: High	0
6	R/W	$LAMP_G$ Normal State 0: Low 1: High	0
5	R/W	$LAMP_B$ Normal State 0: Low 1: High	0
4	R/W	$LAMP_{IR1}$ Normal State 0: Low 1: High	0
3	R/W	$LAMP_{IR2}$ Normal State 0: Low 1: High	0
2	R/W	$LAMP_{UV}$ Normal State 0: Low 1: High	0
1-0	—	Reserved	—

- **Address P6_01h: CIS2 Component 1/Component 7 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	-—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	1
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled Note: If the CIS 2 sequence is W, W, W, IR, W, W, W and UV, 1. Setting sequence length register on P2_00h bit [7:4] → 4'h04 2. Setting multiplication register on P2_03h bit [1] → 1'h1 3. Setting component selection register on P2_12h bit [5:0] → 6'h0 and component 1 LAMP at P6_01h bit [5:0] → 6'h38 4. Component 2 LAMP at P6_02h bit [5:0] → 6'h38 5. Component 3 LAMP at P6_03h bit [5:0] → 6'h38 6. Component 4 LAMP at P6_04h bit [5:0] → 6'h04 7. Component 5 LAMP at P6_05h bit [5:0] → 6'h38 8. Component 6 LAMP at P6_06h bit [5:0] → 6'h38 9. Setting component selection register on P2_17h bit [1:0] → 3'h1 and component 7 LAMP at P6_01h bit [5:0] → 6'h38 10. Component 8 LAMP at P6_02h bit [5:0] → 6'h01	0

- **Address P6_02h: CIS2 Component 2/Component 8 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	1
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	0

- **Address P6_03h: CIS2 Component 3/Component 9 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	1
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	0

- **Address P6_04h: CIS2 Component 4/Component 10 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	1
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	0

- **Address P6_05h: CIS2 Component 5/Component 11 LAMP Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	1
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	0

- **Address P6_06h: CIS2 Component 6/Component 12 Selection Register**

Bit	Mode	Description	Default
7-6	—	Reserved	—
5	R/W	Red LAMP Enable control 0: Disabled 1: Enabled	0
4	R/W	Green LAMP Enable control 0: Disabled 1: Enabled	0
3	R/W	Blue LAMP Enable control 0: Disabled 1: Enabled	0
2	R/W	IR1 LAMP Enable control 0: Disabled 1: Enabled	0
1	R/W	IR2 LAMP Enable control 0: Disabled 1: Enabled	0
0	R/W	UV LAMP Enable control 0: Disabled 1: Enabled	1

- **Address P6_07h: CIS2 Red LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_R$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_R$ output goes high.	0h

- **Address P6_08h: CIS2 Red LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_R$ On Time Least Significant Bits. This field selects the pixel count at which the $LAMP_R$ output goes high. Note: Real CIS2 $LAMP_R$ on position = $LAMP_R$ on register × 4	2Eh

- **Address P6_09h: CIS2 Red LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_R$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_R$ output goes low.	1h

- **Address P6_0Ah: CIS2 Red LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_R$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_R$ output goes low. Note: Real CIS2 $LAMP_R$ off position = $LAMP_R$ off register × 4	06h

- **Address P6_0Bh: CIS2 Green LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_G$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_G$ output goes high.	0h

- **Address P6_0Ch: CIS2 Green LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_G$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_G$ output goes high. Note: Real CIS2 $LAMP_G$ on position = $LAMP_G$ on register × 4	2Eh

- **Address P6_0Dh: CIS2 Green LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_G$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_G$ output goes low.	1h

- **Address P6_0Eh: CIS2 Green LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_G$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_G$ output goes low. Note: Real CIS2 $LAMP_G$ off position = $LAMP_G$ off register × 4	06h

- **Address P6_0Fh: CIS2 Blue LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_B$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_B$ output goes high.	0h

- **Address P6_10h: CIS2 Blue LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_B$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_B$ output goes high. Note: Real CIS2 $LAMP_B$ on position = $LAMP_B$ on register × 4	2Eh

- **Address P6_11h: CIS2 Blue LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_B$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_B$ output goes low.	1h

- **Address P6_12h: CIS2 Blue LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_B$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_B$ output goes low. Note: Real CIS2 $LAMP_B$ off position = $LAMP_B$ off register × 4	06h

- **Address P6_13h: CIS2 IR1 LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR1}$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_{IR1}$ output goes high.	0h

- **Address P6_14h: CIS2 IR1 LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR1}$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_{IR1}$ output goes high. Note: Real CIS2 $LAMP_{IR1}$ on position = $LAMP_{IR1}$ on register × 4	2Eh

- **Address P6_15h: CIS2 IR1 LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR1}$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_{IR1}$ output goes low.	1h

- **Address P6_16h: CIS2 IR1 LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR1}$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_{IR1}$ output goes low. Note: Real CIS2 $LAMP_{IR1}$ off position = $LAMP_{IR1}$ off register × 4	06h

- **Address P6_17h: CIS2 IR2 LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR2}$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_{IR2}$ output goes high.	0h

- **Address P6_18h: CIS2 IR2 LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR2}$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_{IR2}$ output goes high. Note: Real CIS2 $LAMP_{IR2}$ on position = $LAMP_{IR2}$ on register × 4	2Eh

- **Address P6_19h: CIS2 IR2 LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{IR2}$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_{IR2}$ output goes low.	1h

- **Address P6_1Ah: CIS2 IR2 LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{IR2}$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_{IR2}$ output goes low. Note: Real CIS2 $LAMP_{IR2}$ off position = $LAMP_{IR2}$ off register × 4	06h

- **Address P6_1Bh: CIS2 UV LAMP On MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{UV}$ On Time Most Significant Byte This field selects the pixel count at which the $LAMP_{UV}$ output goes high.	0h

- **Address P6_1Ch: CIS2 UV LAMP On LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{UV}$ On Time Least Significant Bits This field selects the pixel count at which the $LAMP_{UV}$ output goes high. Note: Real CIS2 $LAMP_{UV}$ on position = $LAMP_{UV}$ on register × 4	2Eh

- **Address P6_1Dh: CIS2 UV LAMP Off MSB Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	$LAMP_{UV}$ Off Time Most Significant Byte This field selects the pixel count at which the $LAMP_{UV}$ output goes low.	1h

- **Address P6_1Eh: CIS2 UV LAMP Off LSB Register**

Bit	Mode	Description	Default
7-0	R/W	$LAMP_{UV}$ Off Time Least Significant Bits This field selects the pixel count at which the $LAMP_{UV}$ output goes low. Note: Real CIS2 $LAMP_{UV}$ off position = $LAMP_{UV}$ off register × 4	06h

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 7 Registers – CIS 1 Shading Control Registers

- **Address P7_00h: Shading Control Register**

Bit	Mode	Description	Default
7	R/W	Data width selection 0: 8-bit 1: 10-bit	0
6	R/W	CIS1 Global Shading gain enable control 0: Disable 1: Enable	0
5	R/W	CIS2 Global Shading gain enable control 0: Disable 1: Enable	0
4-2	R/W	Component Shading gain format (fixpoint) selection 000: 2.4 001: 2.6 010: 2.8 011: Reserved 100: 3.3 101: 3.5 110: 3.7 111: Reserved	000
1	R/W	Component Shading gain enable control 0: Disable 1: Enable	0
0	R/W	Dark Shading offset enable control 0: Disable 1: Enable Note: Be sure to disable shading function when writing the shading values to the Shading RAM.	0

- **Address P7_02h: Shading RAM/DSP Combination Select Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Shading RAM/DSP Component Select 0000: CIS1 Shading Offset 0001: CIS1 Combination1 Shading Gain 0010: CIS1 Combination2 Shading Gain 0011: CIS1 Combination3 Shading Gain 0100: CIS1 Combination4 Shading Gain 0101: CIS1 Combination5 Shading Gain 0110: CIS1 Combination6 Shading Gain 0111: Reserved 1000: CIS2 Shading Offset 1001: CIS2 Combination1 Shading Gain 1010: CIS2 Combination2 Shading Gain 1011: CIS2 Combination3 Shading Gain 1100: CIS2 Combination4 Shading Gain 1101: CIS2 Combination5 Shading Gain 1110: CIS2 Combination6 Shading Gain 1111: Reserved Notes: 1. If the Light sequence is “R, G, B, IR1 and IR2”, CIS Component 1 → R and CIS Combination 1 → R CIS Component 2 → G and CIS Combination 2 → G CIS Component 3 → B and CIS Combination 3 → B CIS Component 4 → IR1 and CIS Combination 4 → IR1 CIS Component 5 → IR2 and CIS Combination 5 → IR2 2. If Light sequence is “W, W, W, IR1, W, W, W and IR2”, CIS Component 1 → W(R+G+B) and CIS Combination 1 → W CIS Component 2 → W(R+G+B) and CIS Combination 2 → IR1 CIS Component 3 → W(R+G+B) and CIS Combination 3 → IR2 CIS Component 4 → IR1 CIS Component 5 → W(R+G+B) CIS Component 6 → W(R+G+B) CIS Component 7 → W(R+G+B) CIS Component 8 → IR2	0h

- **Address P7_03h: Shading RAM/DSP Start Address MSB Register**

Bit	Mode	Description	Default
7-3	R/W	Reserved	—
2-0	R/W	Shading RAM/DSP Start Address Most Significant Byte	000

- **Address P7_04h: Shading RAM/DSP Start Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Shading RAM /DSP Start Address Least Significant Byte	00h

- **Address P7_05h: Shading RAM/DSP Transfer Count MSB Register**

Bit	Mode	Description	Default
7-3	R/W	Reserved	—
2-0	R/W	Shading RAM/DSP Transfer Count Most Significant Byte	000

- **Address P7_06h: Shading RAM/DSP Transfer Count LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Shading RAM/DSP Transfer Count Least Significant Byte	00h

- **Address P7_07h: CIS1 Global Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	CIS1 Global Shading Gain Coefficient	00h

- **Address P7_08h: CIS2 Global Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	CIS2 Global Shading Gain Coefficient	00h

- **Address P7_0Ah: CIS 1 Dark Shading Offset Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Dark Shading Offset Value Virtual Address Most Significant Byte. Points the write pointer to the dark shading RAM Auto increasing when writing data to the register P7_0Ch.	000

- **Address P7_0Bh: CIS 1 Dark Shading Offset Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Dark Shading Offset Value Virtual Address Least Significant Byte. Points the write pointer to the dark shading RAM Auto increasing when writing data to the register P7_0Ch.	00h

- **Address P7_0Ch: CIS 1 Dark Shading Offset Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Dark Shading Offset Coefficient for CIS 1 Writing value to this register will store the value to the shading RAM, and the address is specified by registers P7_0Ah & P7_0Bh.	00h

- **Address P7_0Dh: CIS 1 Combination 1 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 1 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_0Fh.	000

- **Address P7_0Eh: CIS 1 Combination 1 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 1 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_0Fh.	00h

- **Address P7_0Fh: CIS 1 Combination 1 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 1 Shading Gain Coefficient for CIS 1 Writing value to this register will store the value to shading RAM, and the address is specified by register address 0Dh & 0Eh on page 7 Notes: 1. If the Light sequence is "R G B IR1 IR2" CIS Component 1 → R and CIS Combination 1 → R CIS Component 2 → G and CIS Combination 2 → G CIS Component 3 → B and CIS Combination 3 → B CIS Component 4 → IR1 and CIS Combination 4 → IR1 CIS Component 5 → IR2 and CIS Combination 5 → IR2 2. If the Light sequence is "W, W, W, IR1, W, W, W and IR2", CIS Component 1 → W(R+G+B) and CIS Combination 1 → W CIS Component 2 → W(R+G+B) and CIS Combination 2 → IR1 CIS Component 3 → W(R+G+B) and CIS Combination 3 → IR2 CIS Component 4 → IR1 CIS Component 5 → W(R+G+B) CIS Component 6 → W(R+G+B) CIS Component 7 → W(R+G+B) CIS Component 8 → IR2 3. Read / write sequence Gain coefficient MSB XXXXXX0000000000 LSB first r/w second r/w Must read/write twice for one pixel gain coefficient.	00h

- **Address P7_10h: CIS 1 Combination 2 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 2 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_12h.	000

- **Address P7_11h: CIS 1 Combination 2 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 2 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_12h.	00h

- **Address P7_12h: CIS 1 Combination 2 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 2 Shading Gain Coefficient for CIS 1 Writing to this register will store the value to the shading RAM, and the address is specified by registers P7_10h & P7_11h.	00h

- **Address P7_13h: CIS 1 Combination 3 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 3 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_15h.	000

- **Address P7_14h: CIS 1 Combination 3 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 3 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_15h.	00h

- **Address P7_15h: CIS 1 Combination 3 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 3 Shading Gain Coefficient for CIS 1 Writing to this register will store the value to the shading RAM, and the address is specified by registers P7_13h & P7_14h.	00h

- **Address P7_16h: CIS 1 Combination 4 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 4 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_18h.	000

- **Address P7_17h: CIS 1 Combination 4 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 4 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_18h.	00h

- **Address P7_18h: CIS 1 Combination 4 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 4 Shading Gain Coefficient for CIS 1 Writing to this register will store the value to the shading RAM, and the address is specified by registers P7_16h & P7_17h.	00h

- **Address P7_19h: CIS 1 Combination 5 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 5 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_1Bh.	000

- **Address P7_1Ah: CIS 1 Combination 5 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_1Bh.	00h

- **Address P7_1Bh: CIS 1 Combination 5 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Coefficient for CIS 1 Writing value to this register will store the value to the shading RAM, and the address is specified by registers P7_19h & P7_1Ah.	00h

- **Address P7_1Ch: CIS 1 Combination 6 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 6 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_1Eh.	000

- **Address P7_1Dh: CIS 1 Combination 6 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 6 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P7_1Eh.	00h

- **Address P7_1Eh: CIS 1 Combination 6 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 6 Shading Gain Coefficient for CIS 1 Writing value to this register will store the value to the shading RAM, and the address is specified by registers P7_1Ch & P7_1Dh.	00h

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 8 Registers – CIS 2 Shading Control Registers

- **Address P8_00h: CIS 2 Dark Shading Offset Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Shading Offset Value Virtual Address Most Significant Byte. Points the write pointer to the dark shading RAM Auto increasing when writing data to the register P8_02h.	000

- **Address P8_01h: CIS 2 Dark Shading Offset Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Dark Shading Offset Value Virtual Address Least Significant Byte. Points the write pointer to the dark shading RAM Auto increasing when writing data to the register P8_02h.	00h

- **Address P8_02h: CIS 2 Dark Shading Offset Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Dark Shading Offset Coefficient for CIS 2 Writing value to this register will store the value to the shading RAM, and the address is specified by registers P8_00h & P8_01h.	00h

- **Address P8_03h: CIS 2 Combination 1 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 1 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_05h.	000

- **Address P8_04h: CIS 2 Combination 1 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 1 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_05h.	00h

- **Address P8_05h: CIS 2 Combination 1 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 1 Shading Gain Coefficient for CIS 2 Writing to this register will store the value to the shading RAM, and the address is specified by registers P8_03h & P8_04h.	00h

- **Address P8_06h: CIS 2 Combination 2 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 2 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_08h.	000

- **Address P8_07h: CIS 2 Combination 2 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 2 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_08h.	00h

- **Address P8_08h: CIS 2 Combination 2 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 2 Shading Gain Coefficient for CIS 2 Writing to this register will store the value to the shading RAM, and the address is specified by registers P8_06h & P8_07h.	00h

- **Address P8_09h: CIS 2 Combination 3 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 3 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_0Bh.	000

- **Address P8_0Ah: CIS 2 Combination 3 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 3 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_0Bh.	00h

- **Address P8_0Bh: CIS 2 Combination 3 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 3 Shading Gain Coefficient for CIS 2 Writing value to this register will store the value to the shading RAM, and the address is specified by registers P8_09h & P8_0Ah.	00h

- **Address P8_0Ch: CIS 2 Combination 4 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 4 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_0Eh.	000

- **Address P8_0Dh: CIS 2 Combination 4 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 4 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_0Eh.	00h

- **Address P8_0Eh: CIS 2 Combination 4 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 4 Shading Gain Coefficient for CIS 2 Writing value to this register will store the value to the shading RAM, and the address is specified by registers P8_0Ch & P8_0Dh.	00h

- **Address P8_0Fh: CIS 2 Combination 5 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 5 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_11h.	000

- **Address P8_10h: CIS 2 Combination 5 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_11h.	00h

- **Address P8_11h: CIS 2 Combination 5 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 5 Shading Gain Coefficient for CIS 2 Writing value to this register will store the value to the shading RAM, and the address is specified by registers P8_0Fh & P8_10h.	00h

- **Address P8_12h: CIS 2 Combination 6 Shading Gain Virtual Address MSB Register**

Bit	Mode	Description	Default
7-3	—	Reserved	—
2-0	R/W	Combination 6 Shading Gain Value Virtual Address Most Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_11h.	000

- **Address P8_13h: CIS 2 Combination 6 Shading Gain Virtual Address LSB Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 6 Shading Gain Value Virtual Address Least Significant Byte. Points the write pointer to the shading RAM Auto increasing when writing data to the register P8_11h.	00h

- **Address P8_14h: CIS 2 Combination 6 Shading Gain Coefficient Register**

Bit	Mode	Description	Default
7-0	R/W	Combination 6 Shading Gain Coefficient for CIS 2 Writing value to this register will store the value to the shading RAM, and the address is specified by registers P8_0Fh & P8_10h.	00h

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Page 9 Registers – ISP Control Registers

- **Address P9_00h: ISP Control Register 0**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3	R/W	ISP1 (positive page) Background Color Selection 0: Black 1: White	0
2	R/W	ISP2 (negative page) Background Color Selection 0: Black 1: White	0
1	R/W	Line Information Position 0: End of data 1: Front of data	0
0	R/W	Line Information Enable control 0: Disable 1: Enable	0

- **Address P9_01h: ISP Control Register 1**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3	R/W	ISP1 (positive page) Image Sharpness Enable control 0: Disable 1: Enable	0
2	R/W	ISP1 (positive page) Image Mirror Enable control 0: Disable 1: Enable	0
1	R/W	ISP1 (positive page) Line Border De-noise Enable control 0: Disable 1: Enable	0
0	R/W	ISP1 (positive page) Data De-noise Enable control 0: Disable 1: Enable	0

- **Address P9_02h: ISP Control Register 2**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3	R/W	ISP2 (negative page) Image Sharpness Enable control 0: Disable 1: Enable	0
2	R/W	ISP2 (negative page) Image Mirror Enable control 0: Disable 1: Enable	0
1	R/W	ISP2 (negative page) Line Border De-noise Enable control 0: Disable 1: Enable	0
0	R/W	ISP2 (negative page) Data De-noise Enable control 0: Disable 1: Enable	0

- **Address P9_03h: Line Information Control Register 0**

Bit	Mode	Description	Default
7	R/W	ISP1 (positive page) Line Number Calculation Enable control 0: Disable 1: Enable	0
6	R/W	ISP1 (positive page) Line Color Calculation Enable control 0: Disable 1: Enable	0
5	R/W	ISP1 (positive page) Line Max/MIN/SUM Calculation Enable control 0: Disable 1: Enable	0
4	R/W	ISP1 (positive page) Line Border Calculation Enable control 0: Disable 1: Enable	0
3	R/W	ISP1 (positive page) Line Histogram Calculation Enable control 0: Disable 1: Enable	0
2	R/W	ISP1 (positive page) Wheel Counter Calculation Enable control 0: Disable 1: Enable	0
1-0	R/W	ISP1 (positive page) Wheel Information Calculation Enable control 00: Disable 01: The SI number of current line 10: The sum of SI in previous wheel step 11: Reserved	00

- **Address P9_04h: Line Information Control Register 1**

Bit	Mode	Description	Default
7	R/W	ISP2 (negative page) Line Number Calculation Enable control 0: Disable 1: Enable	0
6	R/W	ISP2 (negative page) Line Color Calculation Enable control 0: Disable 1: Enable	0
5	R/W	ISP2 (negative page) Line Max/MIN/SUM Calculation Enable control 0: Disable 1: Enable	0
4	R/W	ISP2 (negative page) Line Border Calculation Enable control 0: Disable 1: Enable	0
3	R/W	ISP2 (negative page) Line Histogram Calculation Enable control 0: Disable 1: Enable	0
2	R/W	ISP2 (negative page) Wheel Counter Calculation Enable control 0: Disable 1: Enable	0
1-0	R/W	ISP2 (negative page) Wheel Information Calculation Enable control 00: Disable 01: The SI number of current line 10: The sum of SI in previous wheel step 11: Reserved	00

- **Address P9_05h: Line Border Control Register 0**

Bit	Mode	Description	Default
7	R/W	Line Border Algorithm Selection 0: Two windows differential comparison 1: Continuous pixel detection with static threshold	0
6-4	R/W	Continuous Pixel Selection 000: 1 pixel 001: 2 pixels 010: 3 pixels 011: 4 pixels 100: 5 pixels 101: 6 pixels 110: 7 pixels 111: 8 pixels This field is used to specify the continuous comparison pixel value which is regarded as the static threshold if the continuous compare match occurs.	011
3-2	—	Reserved	—
1	R/W	Big Window Width Selection 0: 6 pixels 1: 8 pixels	0
0	R/W	Small Window Width Selection 0: 3 pixels 1: 4 pixels	0

- **Address P9_06h: Line Border Control Register 1**

Bit	Mode	Description	Default
7-6	R/W	ISP1 Left Border Detection Range Selection 00: 144 pixels 01: 288 pixels 10: 432 pixels 11: 576 pixels The ISP hardware will detect the image left border from the ISP1 valid range start address specified in P9_16h [6:4] and P9_17h registers to the above selection of 144/288/432/576 pixels respectively.	10
5-4	R/W	ISP1 Right Border Detection Range Selection 00: 144 pixels 01: 288 pixels 10: 432 pixels 11: 576 pixels The ISP hardware will detect the image right border before the ISP1 valid range end address specified in P9_16h [2:0] and P9_18h registers with the above selection of 144/288/432/576 pixels.	10
3-2	R/W	ISP2 Left Border Detection Range Selection 00: 144 pixels 01: 288 pixels 10: 432 pixels 11: 576 pixels The ISP hardware will detect the image left border from the ISP2 valid range start address specified in P9_19h [6:4] and P9_1Ah registers to the above selection of 144/288/432/576 pixels respectively.	10
1-0	R/W	ISP2 Right Border Detection Range Selection 00: 144 pixels 01: 288 pixels 10: 432 pixels 11: 576 pixels The ISP hardware will detect the image right border before the ISP2 valid range end address specified in P9_19h [2:0] and P9_1Bh registers with the above selection of 144/288/432/576 pixels.	10

- **Address P9_0Ah: ISP1 Sharpness Gain 1 Register**

Bit	Mode	Description	Default
7-0	R/W	ISP1 Sharpness Gain 1 Real gain value = register content/128	40h

- **Address P9_0Bh: ISP1 Sharpness Gain 2 Register**

Bit	Mode	Description	Default
7-0	R/W	ISP1 Sharpness Gain 2 Real gain value = register content/128	40h

- **Address P9_0Ch: ISP2 Sharpness Gain 1 Register**

Bit	Mode	Description	Default
7-0	R/W	ISP2 Sharpness Gain 1 Real gain value = register content/128	40h

- **Address P9_0Dh: ISP2 Sharpness Gain 2 Register**

Bit	Mode	Description	Default
7-0	R/W	ISP2 Sharpness Gain 2 Real gain value = register content/128	40h

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- **Address P9_0Eh: ISP1 Line Border Static Threshold Register**

Bit	Mode	Description	Default
7-0	R/W	ISP1 (positive page) Line Border Static Threshold	20h

- **Address P9_0Fh: ISP2 Line Border Static Threshold Register**

Bit	Mode	Description	Default
7-0	R/W	ISP2 (negative page) Line Border Static Threshold	20h

- **Address P9_10h: ISP1 Line Border Big Window Threshold Register**

Bit	Mode	Description	Default
7-0	R/W	ISP1 (positive page) Line Border Big Window Threshold	20h

- **Address P9_11h: ISP1 Line Border Small Window Threshold Register**

Bit	Mode	Description	Default
7-0	R/W	ISP1 (positive page) Line Border Small Window Threshold	08h

- **Address P9_12h: ISP2 Line Border Big Window Threshold**

Bit	Mode	Description	Default
7-0	R/W	ISP2 (positive page) Line Border Big Window Threshold	20h

- **Address P9_13h: ISP2 Line Border Small Window Threshold**

Bit	Mode	Description	Default
7-0	R/W	ISP2 (positive page) Line Border Small Window Threshold	08h

- **Address P9_16h: ISP1 Valid Range Start/End Address MSB**

Bit	Mode	Description	Default
7	—	Reserved	—
6-4	R/W	ISP1 valid range start address MSB	000
3	—	Reserved	—
2-0	R/W	ISP1 valid range end address MSB	111

- **Address P9_17h: ISP1 Valid Range Start Address LSB**

Bit	Mode	Description	Default
7-0	R/W	ISP1 valid range start address LSB	00h

- **Address P9_18h: ISP1 Valid Range End Address LSB**

Bit	Mode	Description	Default
7-0	R/W	ISP1 valid range end address LSB	FFh

- **Address P9_19h: ISP2 Valid Range Start/End Address MSB**

Bit	Mode	Description	Default
7	—	Reserved	—
6-4	R/W	ISP2 valid range start address MSB	000
3	—	Reserved	—
2-0	R/W	ISP2 valid range end address MSB	111

- **Address P9_1Ah: ISP2 Valid Range Start Address LSB**

Bit	Mode	Description	Default
7-0	R/W	ISP2 valid range start address LSB	00h

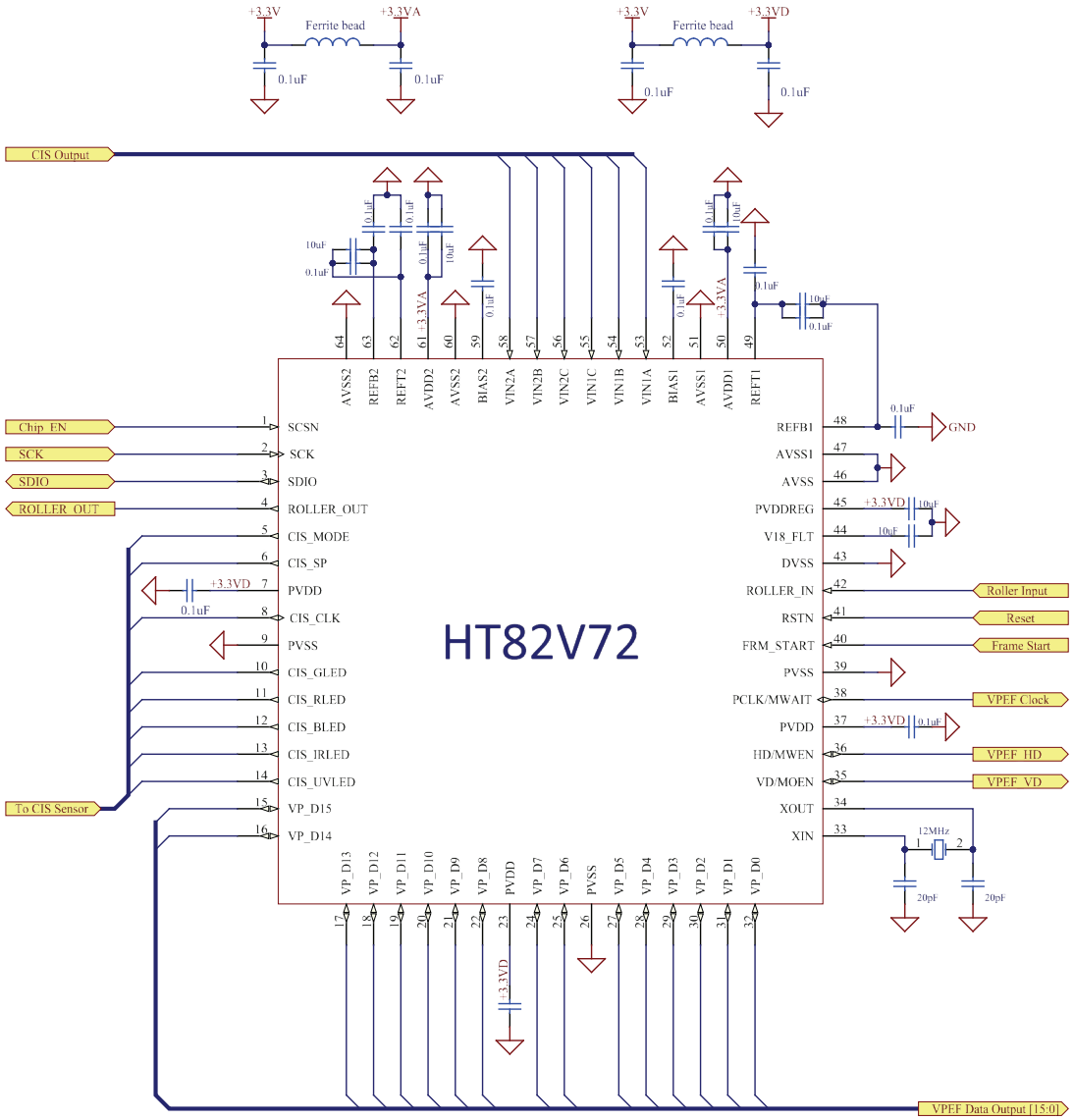
- **Address P9_1Bh: ISP2 Valid Range End Address LSB**

Bit	Mode	Description	Default
7-0	R/W	ISP2 valid range end address LSB	FFh

- **Address Px_1Fh: Page Register**

Bit	Mode	Description	Default
7-4	—	Reserved	—
3-0	R/W	Used to select desired page of registers being accessed. 0000: Page 0 0001: Page 1 0010: Page 2 0011: Page 3 0100: Page 4 0101: Page 5 0110: Page 6 0111: Page 7 1000: Page 8 1001: Page 9 Others: Reserved	0h

Application Circuits



Note: All de-coupling capacitors should be located as close as possible to the device DFE.

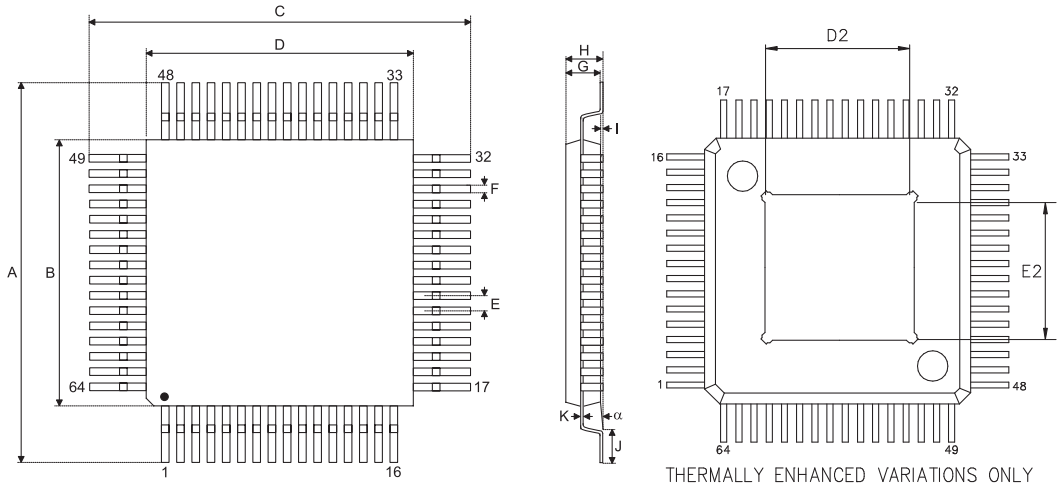
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

64-pin TQFP (7mm×7mm) Outline Dimensions (Exposed Pad)



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
D2	0.079	—	—
E2	0.079	—	—
F	0.005	0.007	0.009
G	0.037	0.039	0.041
H	—	—	0.047
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
D2	2.00	—	—
E2	2.00	—	—
F	0.13	0.18	0.23
G	0.95	1.00	1.05
H	—	—	1.20
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°