Features

- Operating voltage: 2.7V~6V
- Extremely low power consumption current
  - I_{CC}= 0μA (typ.) in battery-saving mode
  - I_{CC}= 8.5mA (typ.) in standby mode
  - I_{CC}= 13.5mA (typ.) for communication
- Built-in IF decoder, compander and PLL
- IF decoder
  - 1st/2nd Mixers, RX VCO
  - RSSI quadrature detector, IF AMP
  - Noise detector
- Compander
  - Expander, Compressor, Limiter
  - Receive AMP, MIC AMP, PRE AMP
- PLL
  - RX PLL, TX PLL
  - Local oscillator
  - Data latch control
  - Unlock detector
- Four threshold variable battery alarms

General Description

The HT9015 is an RF single chip for cordless phone systems. Internally these are three major parts, a PLL, an IF decoder and a compander.

The PLL provides radio channel selection for either the transmitter or receiver. Frequency locking status of the selected channel can be monitored by a control register.

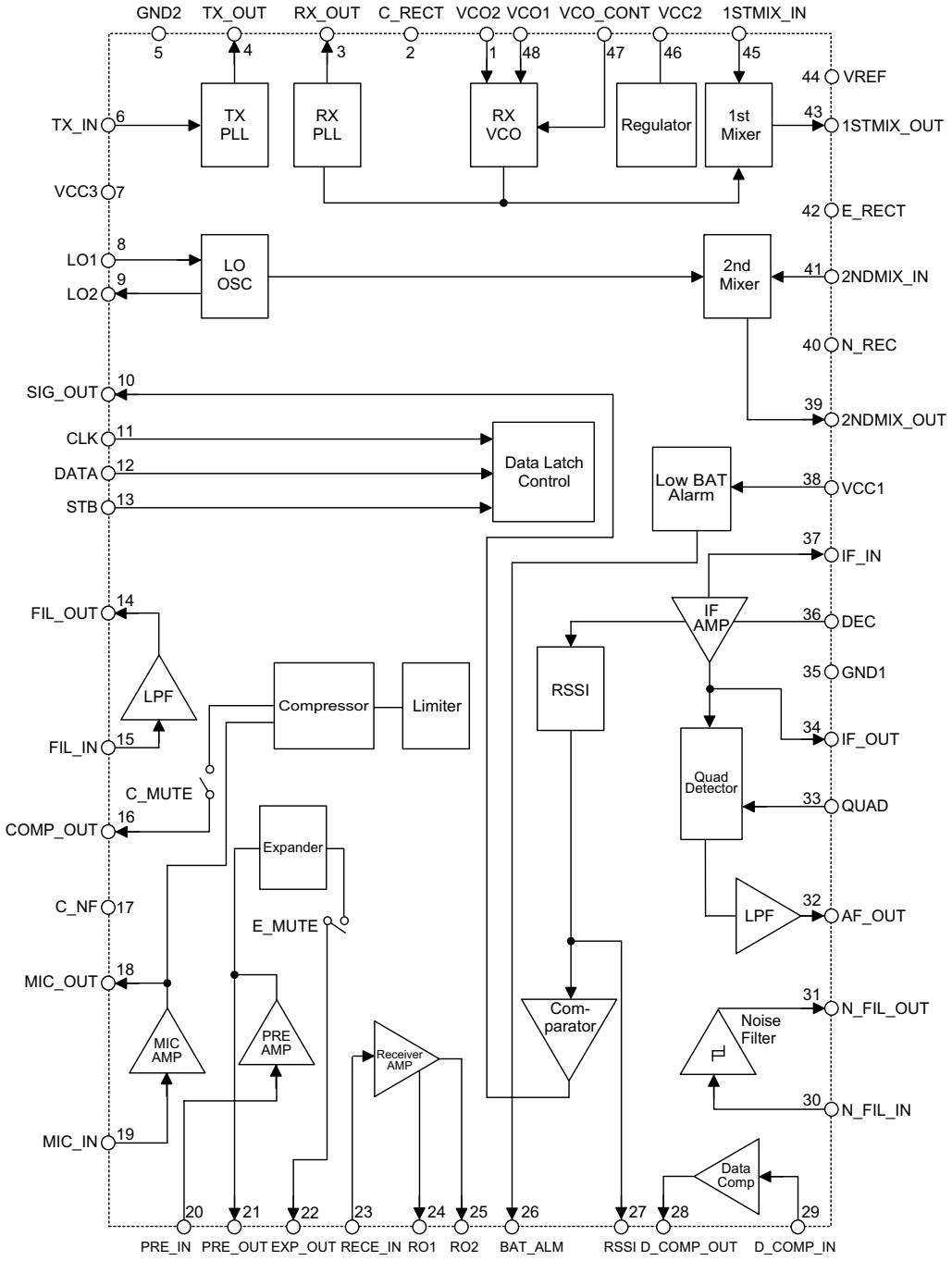
The IF decoder provides two frequency down converters that let high frequency signals pass through a mixer and local oscillator to be lowered for frequency even base band signals. It also provides an RSSI (receiver signal strength indicator) function to detect the IF output signal strength and built-in noise detector for S/N quality.

The compander provides better S/N ratio for audio signal processing.

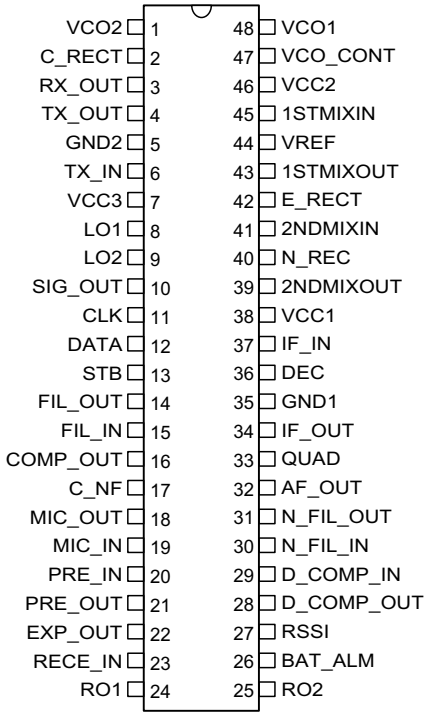
The HT9015 has a wide-range applications in FM/FSK, Transmitting/Receiving of VHF bandwidth including cordless phone, narrow band voice and data transceiver systems.

The most significant advantage of the HT9015 is in the reduction of many external components making it well suited for cordless phone baseset, handset radio section.

Block Diagram



Pin Assignment



HT9015
– 48 SSOP

Pin Description

Pin No.	Pin Name	I/O	Description
1	VCO2	I	Connects LC network with VCO1 pin to provide the tank circuit for the received voltage control oscillator
2	C_RECT	—	Normally connected to ground through a capacitor.
3	RX_OUT	O	Receiver phase detector output. The PDT of RX-PLL detects phase errors from the received PLL. The output is connected to external low pass filter.
4	TX_OUT	O	Transmitter phase detector output. The PDT of TX-PLL detects phase errors from the transmitted PLL. The output is connected to an external low pass filter.
5	GND2	—	Digital ground
6	TX_IN	I	14-bit programmable transmit counter input. The output signal from the external VCO circuit can be AC coupled to this pin.

Pin No.	Pin Name	I/O	Description
7	VCC3	—	Positive power supply for digital block circuits.
8	LO1	I	This pin connects to LO2 pin with external crystal and capacitor.
9	LO2	O	This output pin generates a reference frequency used for the PLL and the second mixer local oscillator when connected to LO1 pin with an external crystal and capacitor.
10	SIG_OUT	O	This pin outputs four-type states and is selected by an internal control register. There are RSSI state and noise state and RX/TX PLL lock states. Open drain output.
11	CLK	I	Clock input pin
12	DATA	I	Serial data input pin
13	STB	I	Data strobe control pin
14	FIL_OUT	O	Splatter filter output pin
15	FIL_IN	I	Splatter filter input pin
16	COMP_OUT	O	Compressor output pin
17	C_NF	—	Normally connected to ground through a capacitor.
18	MIC_OUT	O	Microphone amplifier output pin
19	MIC_IN	I	Microphone amplifier input pin
20	PRE_IN	I	Pre-amplifier input pin
21	PRE_OUT	O	Pre-amplifier output pin
22	EXP_OUT	O	Expander output pin
23	RECE_IN	I	Receiver amplifier input pin
24	RO1	O	Receiver amplifier output pin
25	RO2	O	Receiver amplifier output pin
26	BAT_ALM	O	Battery alarm output pin. When the battery voltage is lower than the internal setting threshold this pin is active. Open drain output.
27	RSSI	O	Receiver signal strength indicator output pin, the output signal depends on the IF amplifier output signal.
28	D_COMP_OUT	O	Data comparator output pin
29	D_COMP_IN	I	Data comparator input pin. Input to comparator to distinguish digital data from audio.
30	N_FIL_IN	I	Input to noise filter
31	N_FIL_OUT	O	Output from noise filter

Pin No.	Pin Name	I/O	Description
32	AF_OUT	O	FM demodulator output pin. Output signal frequency is within the audio band.
33	QUAD	I	Normally provides a 455kHz carry frequency for the FM quadrature detector.
34	IF_OUT	O	IF amplifier output pin. Signal will later pass through external 90°C phase shifter for quadrature detector.
35	GND1	—	Analog ground
36	DEC	—	Normally connected to VCC1 through a capacitor.
37	IF_IN	I	IF amplifier input pin it is necessary to use the IF filter network to get high quality IF signal.
38	VCC1	—	Analog power supply
39	2NDMIX_OUT	O	Second mixer IF signal output pin and down converter. IF frequency is 455kHz.
40	N_REC	—	Connect to ground through capacitor.
41	2NDMIX_IN	I	Second mixer RF signal input pin and down converter. Frequency is 455kHz.
42	E_RECT	—	Expander rectifier filter capacitor pin.
43	1STMIX_OUT	O	First mixer IF signal output pin and down converter. IF frequency is 10.7MHz.
44	VREF	O	Reference voltage input for compander.
45	1STMIX_IN	I	The first mixer RF signal input. Carrier frequency from 20~60MHz.
46	VCC2	—	Directly connects to the two voltage regulators inside.
47	VCO_CONT	I	Normally connected to ground through a capacitor.
48	VCO1	I	Connects LC network with VCO2 pin to provide the tank circuit for the received voltage control oscillator.

Absolute Maximum Ratings

Supply Voltage.....V_{SS}–0.3V to 6V

Input Voltage .....V_{SS}–0.3V to V_{CC}+0.3V

Storage Temperature.....–55°C to 150°C

Operating Temperature .....–20°C to 70°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{CC}	Operating Voltage	—	V_{CC1}=V_{CC3}	—	3.6	—	V
I_{CC1}	Current 1 Consumption	3.6V	All on	—	13.5	—	mA
I_{CC2}	Current 2 Consumption	3.6V	RX-RF ON	—	8.5	—	mA
I_{CC3}	Current 3 Consumption	3.6V	RX-AF ON	—	3.5	—	mA
I_{CC4}	Current 4 Consumption	3.6V	TX-RF ON	—	2.1	—	mA
I_{CC5}	Current 5 Consumption	3.6V	TX-AF ON	—	1.7	—	mA
$I_{CC(A)}$	Current Alarm Supply	3.6V	R_L= 100kΩ	—	100	—	μA
$I_{CC(BS)}$	Supply Current in Battery Saving Mode	3.6V	All off	—	0	—	μA
I_{REF}	V_{REF} Voltage	3.6V	—	—	1.5	—	V
V_{IH}	Data Input Threshold	3.6V	—	—	V_{CC3}	—	V
V_{IL}	Data Input Threshold	3.6V	—	—	0	—	V
I_{IH}	Data Input Current	3.6V	V_{IH}= V_{CC}	—	0	—	μA
I_{IL}	Data Input Current	3.6V	V_{IL}= GND	—	0	—	μA
f_{CK}	CK Input Frequency	3.6V	—	—	38	1000	kHz

Regulator

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{REG}	Output Voltage	3.6V	I_{OUT}= 1mA	1.7	2	2.3	V
$I_{OUT\ (MIN)}$	Minimum Load Current	3.6V	V_{OUT}= V_{REG} (Open)–0.05V	—	3	—	mA

Detector

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{BAT-L}	Detection Voltage 1	3.6V	—	—	3.3	—	V
V_{BAT-H}	Detection Voltage 1	3.6V	—	—	3.37	—	V
V_{BAT-L}	Detection Voltage 2	3.6V	—	—	3.15	—	V
V_{BAT-H}	Detection Voltage 2	3.6V	—	—	3.2	—	V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{BAT-L}	Detection Voltage 3	3.6V	—	—	3.05	—	V
V_{BAT-H}	Detection Voltage 3	3.6V	—	—	3.10	—	V
V_{BAT-L}	Detection Voltage 4	3.6V	—	—	2.78	—	V
V_{BAT-H}	Detection Voltage 4	3.6V	—	—	2.82	—	V
V_{OL}	Output Low Level Voltage	3.6V	I_{SINK}= 0.1mA	—	0.1	—	V
I_{LEAK}	Output Leak Current	3.6V	V_{ALM}= 3.6V	—	0	—	μA
V_{TH}	Minimum Detection Level	3.6V	f= 500Hz	—	—	—	mVrms
V_{OL}	Output Low Level Voltage	3.6V	I_{SINK}= 0.2mA	—	0.1	—	V
I_{LEAK}	Output Leak Current	3.6V	V_{DATA}= 3.6V	—	0	—	μA
V_{TH-H}	Noise Detection Level	3.6V	—	—	0.57	—	V
V_{TH-L}	Noise Detection Level	3.6V	—	—	0.47	—	V
V_{OL}	Noise Detection Level Voltage	3.6V	I_{SINK}= 0.2mA	—	0.1	—	V
I_{LEAK}	Output Leak Current	3.6V	VSIG= 3.6V	—	0	—	$_{\mu}$A
V_{TH-L}	RSSI Comparator Detection Voltage	3.6V	Comparator Output L → H	—	0.72	—	V
V_{TH-H}	RSSI Comparator Detection Voltage	3.6V	Comparator Output H → L	—	0.8	—	V
V_{HYS}	RSSI Comparator Hysteresis	3.6V	—	—	0.08	—	V

PLL Detection dBμV=dBμV EMF (Open), Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
f_{IN}	Operating Frequency	3.6V	—	—	46.61	—	MHz
V_{IN}	TX-PLL Input Sensitivity	3.6V	—	—	103	—	dBμV
V_{LO}	Local Oscillator Input Sensitivity	3.6V	f_{LO}= 10.240MHz	—	110	—	dBμV
I_{CP1}	Charge Pump Output Current	3.6V	V_{CP}= 1.8V	—	200	—	μA
I_{CP2}	Charge Pump Output Current	3.6V	V_{CP}= 1.8V	—	400	—	μA
I_{LEAK}	Charge Pump Leak Current	3.6V	—	—	0	—	μA
f_{LO}	Local Oscillator Operating Frequency	3.6V	V_{LO}= 112dBμV	—	10.24	—	MHz

RX-VCO IF + MIX section

f_{IN} (MIX 1)=46.61MHz, f_{IN} (IF)=455kHz, Δf=3kHz f_m= 1kHz, dBμV=dBμV EMF (Open), Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
K_V	Conversion Gain	3.6V	—	—	1	—	MHz/V
V_{VCO}	RX VCO Oscillation Level	3.6V	f_{VCO}= 25~55MHz	—	110	—	dBμV

1st and 2nd Mixer, IF AMP

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
12dB SINAD	12dB SINAD Sensitivity	3.6V	Input 50Ω	—	20	—	dBμV
f_{MIX1}	Mixer Operating Frequency	3.6V	1STMIXER	—	46.61	—	MHz
f_{MIX2}	Mixer Operating Frequency	3.6V	2NDMIXER	—	10.7	—	MHz
G_{VC}	Conversion Gain	3.6V	Excluding Filter Loss	—	26	—	dB
G_{IF}	IF AMP Gain	3.6V	—	—	75	—	dB
V_{OD}	Demodulated Output	3.6V	V_{IN} (MIX 1)= 70dBμV	—	220	—	mVrms
S/N	S/N Ratio	3.6V	V_{IN} (MIX 1)= 70dBμV	—	55	—	dB
AMR	AM Rejection Ratio	3.6V	V_{IN} (MIX 1)= 70dBμV	—	40	—	dB
R_{IN1}	Input Impedance	3.6V	1st MIX IN	—	2.1	—	kΩ
C_{IN1}	Input Impedance	3.6V	1st MIX IN	—	3.5	—	pF
R_{IN2}	Input Impedance	3.6V	2nd MIX IN	—	5.8	—	kΩ
C_{IN12}	Input Impedance	3.6V	2nd MIX IN	—	2.5	—	pF
R_{IN}	Input Resistance	3.6V	IF IN	—	1.5	—	kΩ
R_{O1}	Output Resistance	3.6V	1st MIX OUT	—	330	—	Ω
R_{O2}	Output Resistance	3.6V	2nd MIX OUT	—	1.5	—	kΩ
V_{RSSI1}	RSSI Output Voltage	3.6V	V_{IN} (MIX 1)= 20dBμV	—	1	—	V
V_{RSSI2}	RSSI Output Voltage	3.6V	V_{IN} (MIX 1)= 60dBμV	—	2.4	—	V

Compressor + MIC AMP

f_{IN}=1kHz, Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{refc}	Input Reference Level	3.6V	V_{OM}=–10dBV		–10.5		dBV
V_{OC}	Output Deviation	3.6V	V_{OM}=–30dBV		–0.2		dB
V_4	MIC AMP Voltage Gain	3.6V		—	20	—	dB
t_{HDC}	Total Harmonic Distortion	3.6V	V_{OM}=–10dBV	—	0.3		%
V_{NOC}	Output Noise Level	3.6V	Input-GND Short	—	–61		dBV
V_{lim1}	Limiting Level	3.6V	COMP Out, V_{IM}= 0dBV	—	1.3	—	V_{P-P}
V_{lim2}	Limiting Level	3.6V	MIC Out, V_{IM}= 0dBV	—	2.6	—	V_{P-P}
V_{MUTE}	Mute Output Level	3.6V		—	–96	—	dBV

Expander + PRE AMP + Receiver AMP

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{refE}	Input Reference Level	3.6V	V_{OP}=–10dBV	—	–10	—	dBV
V_{OE}	Output Deviation	3.6V	V_{OP}=–35dBV	—	0.5	—	dB
G_{P3}	PRE AMP Voltage Gain	3.6V	—	—	0	—	dB
THD1	Total Harmonic Distortion	3.6V	R_L= 150Ω V_{RI}=–15dBV	—	0.5	—	%
V_{MUTE}	Mute Output Level	3.6V	—	—	–76	—	dBV
G_{RNG2}	PRE AMP Voltage Gain Setting Range	3.6V	—	—	0	—	dB
G_{RNG1}	Receiver AMP Voltage Gain Setting Range	3.6V	—	—	6	—	dB
CT_{CE}	Crosstalk CE	3.6V	V_{IM}=–20dBV	—	–95	—	dB
G_S	Voltage Gain	3.6V		—	0	—	dB
DR_S	Maximum Output Level	3.6V	THD= 3%	—	3	—	V_{P-P}

Functional Description

The HT9015 is a signal chip RF IC for cordless phone applications. It has applications for 46/49MHz cordless phones as well as CT0 cordless phones that have frequency bands between 20MHz and 60MHz. This chip enables external components in the base set and hand set radio section application circuits to be reduced.

The HT9015 is manufactured or a special process called BiCMOS, or bipolar process and CMOS process. Because the RF and IF parts need high frequency actions such as mixer, VCO, IF amplifier and demodulator, those parts are implemented in high performance bipolar circuits. The other digital functions are designed using CMOS circuits. Sometimes this chip is known as "COMBO", the meaning of COMBO is one chip combined with RF, IF and PLL parts.

The HT9015 provides data latch interface controlled by a microcontroller. There are four internal registers inside the HT9015; TX (transmitter) divider, RX (receiver) Divider, REF (reference) divider and Control Register. All registers can be set through the data latch control interface. The data latch control interface contains DATA, CLK and STB control signals.

Input timing for serial data

Data is read on the timing of the rising edge of CLK. When STB receives a high signal, DATA in the shift register is sent into the latch to control the block, see the input timing for serial data as shown below.

Serial data format of four registers

According to previous input timing Specs, the HT9015 can be easily set up using four registers. The TX divider determines the TX PLL locked frequency; the RX divider determines the RX PLL locked frequency; the REF divider determines the TX and RX PLL frequency reference which is also called channel space. The control register is an important unit which controls the radio link, voice control and power saving during base set and hand set communication.

All data format contains 20 bits, but some registers need only 16 bits, They have a common field of 20 bits data format called "code" which determine what data belongs to whom. See the table below.

Code		Register
1	1	REF register
1	0	TX register
0	1	RX register
0	0	Control register

Four register selection

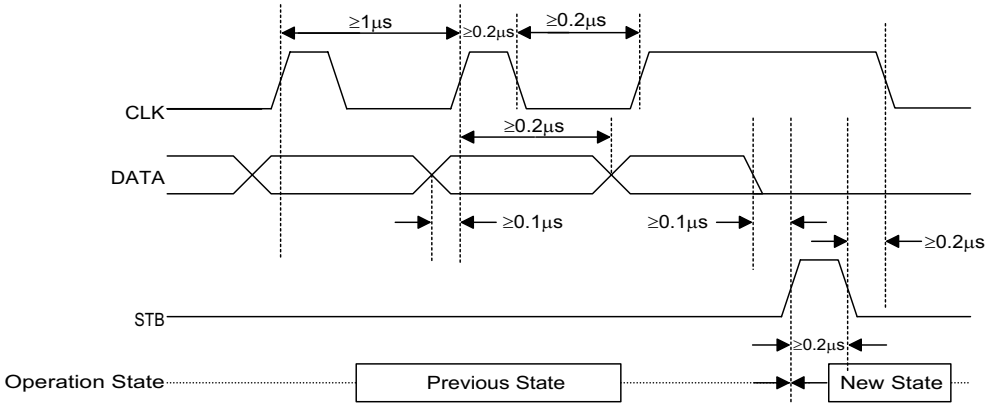
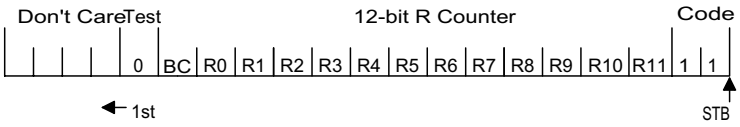


Figure 1 Input timing for serial data

- REF register

  Divide number range is from 5 to 4095.

  This register includes TEST bits which must be set to 0.



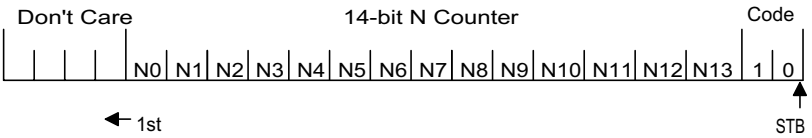
  Divide number:

  $R = R0 + R1 \times 2 + R2 \times 2^2 + R3 \times 2^3 + \ldots + R11 \times 2^{11}$

  BC bit is BATTERY ALARM detection setting.

- TX register

  Divide number range is from 5 to 16383.

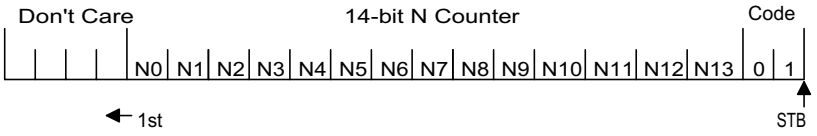


  Divide number:

  $N = N0 + N1 \times 2 + N2 \times 2^2 + N3 \times 2^3 + \ldots + N12 \times 2^{12} + N13 \times 2^{13}$

- RX register

  Divide number range is from 5 to 16383.

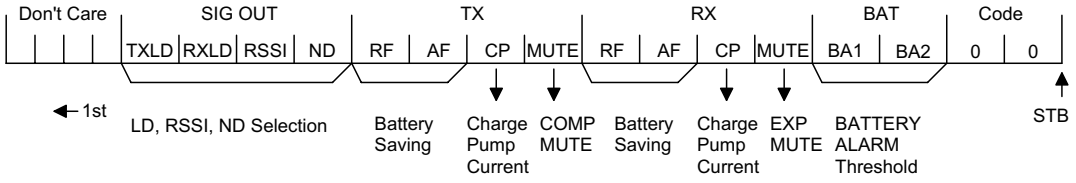


  Divide number:

  $N = N0 + N1 \times 2 + N2 \times 2^2 + N3 \times 2^3 + \ldots + N12 \times 2^{12} + N13 \times 2^{13}$

- Control register

  This register includes battery saving control for the TX/RX circuits or MUTE controls for the commander block or changing threshold level for the battery alarm.



♦ Battery saving control

0 ……Operation 1 ……Battery saving

Bit	Control Block	
TX-RF	TX-PLL	TX-RF= 1 and RX-RF= 1 LOCAL OSC= OFF
TX-AF	MIC AMP, Compressor, Splatter	
RX-RF	RX-VCO, RX-PLL, 1st MIX, 2nd MIX IF AMP, NOISE DET, DATA COMP, RSSI	
RX-AF	Pre AMP, Expander, Receiver AMP	

♦ MUTE control

0 ……normal 1 ……MUTE

MUTE for Compressor output.

These bits prevent the compander block going into a battery saving mode. Current consumption therefore does not decrease.

♦ Charge pump current control

PLL loop performance such as lock-up time can be changed by these control bits.

Bit	Control Output	0	1
TX CP	TX-PLL Charge Pump Output Current	200μA	400μA
RX CP	RX-PLL Charge Pump Output Current	200μA	400μA

♦ BATTERY ALARM detection setting

There are has four threshold levels for low battery detection.
These threshold levels are shown on the table below.

(1)BC	BA1	BA2	V_{BAT-L}
0	0	0	3.00V
0	0	1	3.25V
0	1	0	3.30V
0	1	1	3.45V
1	0	0	(2)Battery Saving
1	1	1	

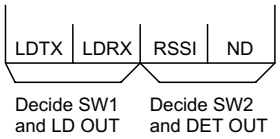
(1) BC bit in REF divider

(2) Only for BATTERY ALARM block

♦ SIG_OUT selection

The SIG_OUT terminal generates combination states of RX and TX lock detectors. The RSSI and NOISE detector are shown in figure 2 below.

SW1 and SW2 in Fig. 3 determine the output on SIG_OUT using selection bits in a control register according to the figure below.



Example: TX lock detector operation

LDTX	LDRX	RSSI	ND
1	0	0	0

Figure 2 SIG_OUT bits

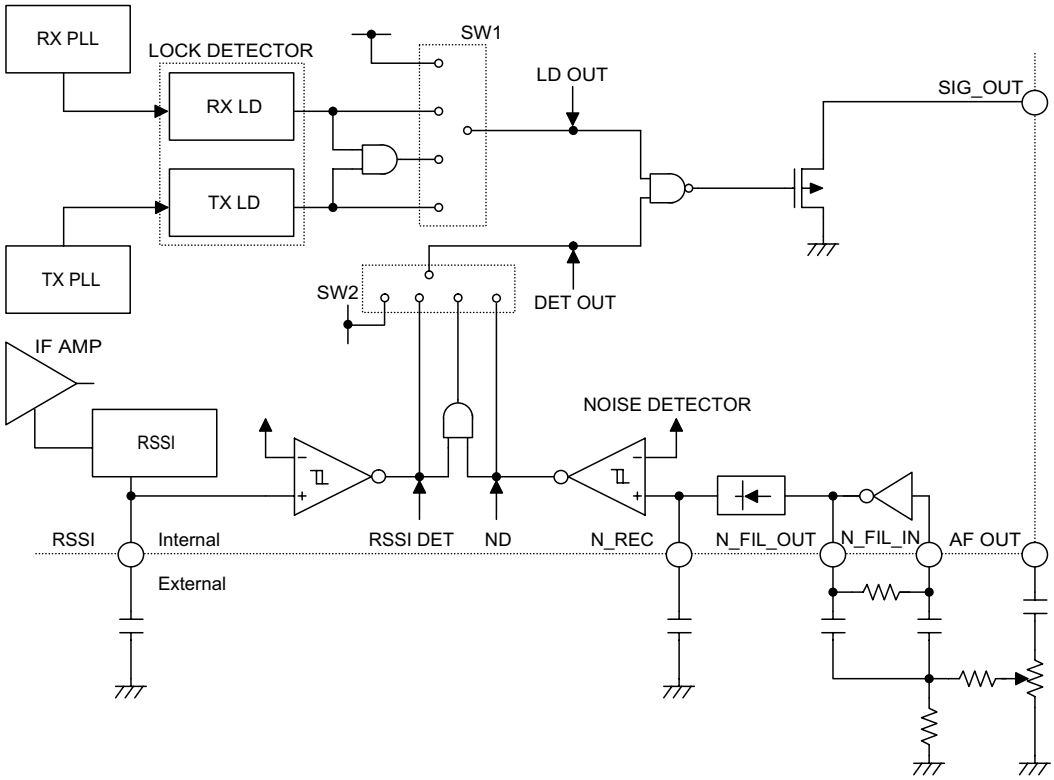


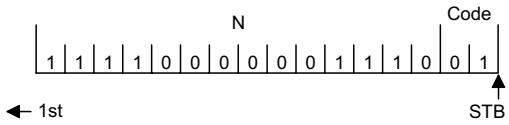
Figure 3 Signal output block diagram

- Example of divider setting

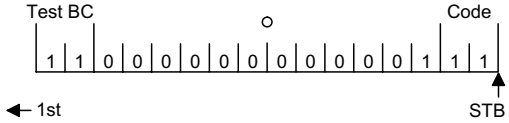
  When the LOCAL OSC frequency is 10.240MHz, RX VCO has to oscillate at frequencies from 35.915MHz in 20kHz or 25kHz step.

  - Reference frequency at the PHASE DETECTOR should be set to 5kHz.
  - 10.240MHz ÷ 5kHz = 2048, ∴ R= 2048
  - Calculate dividing number N for RX divider
  - 35.915MHz ÷ 5kHz = 7183, ∴ N (CH16)= 7183
  - 35.935MHz ÷ 5kHz = 7187, ∴ N (CH17)= 7187
  - Finally you set the following registers.

RX Divider for 7183



REF Divider for R=2048



- The power saving arrangement is one of the features in the HT9015.

  This is achieved through an inside control register to arrange the power consumption of the three major parts (RF. IF. PLL). There are two-pair DC power supplies for the HT9015, V_{CC1}-GND1 and V_{CC3}-GND2. The DC power V_{CC1} provides operating voltage for the IF detector and the compander analog parts.

  The DC power V_{CC3} provides the operating voltage for the PLL and data latch control. It also has a built in 2.0V regulator VCC2 for the RX front end. See the power supply arrangement as shown on the table below.

VCC1	GND1	1st MIX, 2nd MIX, IF AMP, QUAD, NOISE DET. RX-VCO DATA COMP, COMPANDER, RECEIVER AMP, SPLATTER.
VCC3	GND2	RX-PLL, TX-PLL, LOCAL OSC, DATA LATCH CONTROL

Intermediate frequency (IF) decoder part

The figure below shows a simplified block diagram for a double-conversion super heterodyne FM receiver. Heterodyne means to mix two frequencies together in a non linear device or to translate one frequency to another using non linear mixing. The super heterodyne receiver is an improvement over other receiver in gain, selectivity, and sensitivity characteristics.
The super heterodyne receiver is divided into five parts:

- RF section. Generally consists of a preselector and an amplifier stage.
- Mixer conversion section. Includes a radio-frequency oscillator stage (commonly known as a local oscillator) and a mixer conversion stage (commonly known as a frequency detector) to produce the IF signal.
- The IF section. Generally consists of a series of IF amplifiers and bandpass filters and known as the IF strip. Most of the receiver gain and selectivity is achieved in the IF section.
- The FM demodulator section: The quadrature FM demodulator uses a 90° phase shift, a single tuned circuit, and a product detector to demodulate the FM signals.
- The audio amplifier section. The audio section comprises several cascaded audio amplifiers and one or more speakers. The number of amplifiers used depends on the audio signal power desired.

- Mixers

  A Mixer is a non linear device whose purpose is to convert radio frequencies (RF) to intermediate frequency (IF) (RF-to-IF frequency translation). In the frequency conversion process, RF signals are combined with the local oscillator frequency in a non linear device. The output of the mixer contains an infinite number of harmonic and cross-product frequencies which include the sum and the difference between the desired RF carrier and the local oscillator frequencies. The IF band-pass filter are tuned to the different frequencies. Therefore, the IF signal is filtered out by the BPF. In the HT9015 the double conversion method (Figure 4) is applied to produce the lower IF.

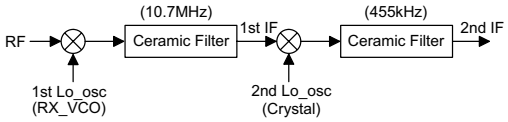


Figure 4 The illustration of mixers

The first IF is a relatively high frequency (10.7MHz), for good image-frequency rejection, while the second IF is a relatively low frequency (455kHz) that allows the IF amplifiers to have a relatively high gain and still not be susceptible to oscillations.

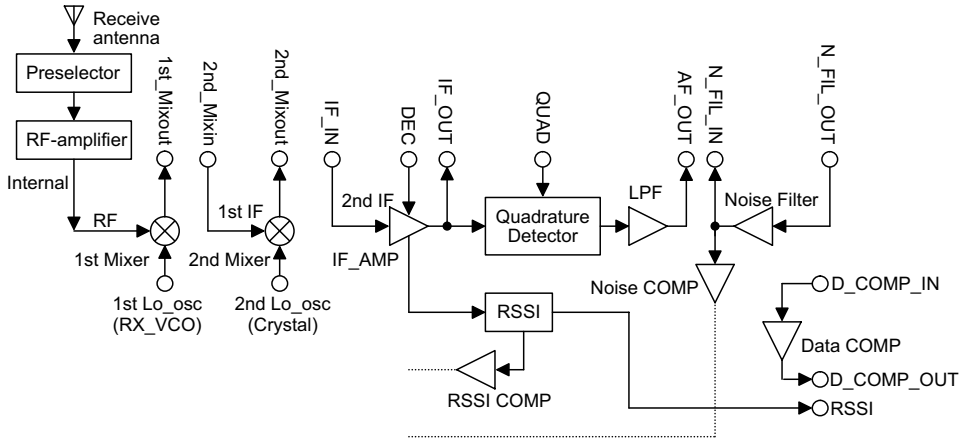


Figure 5 Intermediate frequency decoder block

- Limiting IF Amplifier, RSSI (Received Signal Strength Indicator) and RSSI Comparator

  The basic function of the IF amp is to boost the IF signal and to help handle impulse noise. The IF limiter applies very high gain to the IF frequency such that the top and bottom of the waveform are clipped. This helps in reducing AM and noise intercepted upon reception. The limiting IF amplifier consists of four differential amplifiers (Figure 6).

- Quadrature detector

  Once the signal leaves the IF section, it must be demodulated so that the baseband signal can be separated from the IF signal. This is accomplished by the quadrature detector. A quadrature detector (Figure 7) uses a 90° phase shifter (C_i), an L/C tuned circuit, and a phase comparator to demodulate FM signals.

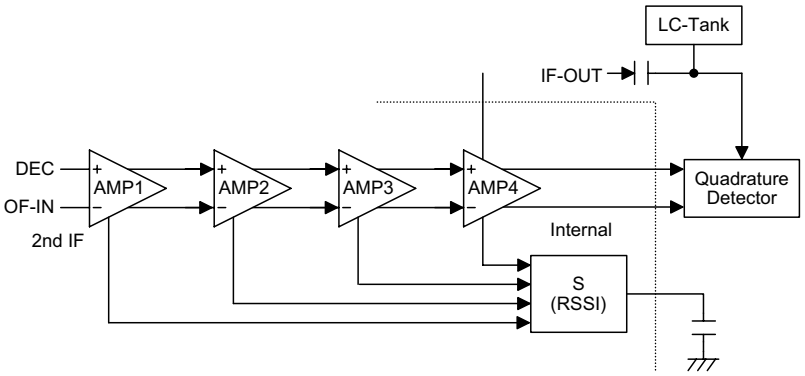


Figure 6 Limiting IF Amplifier, RSSI and RSSI comparator

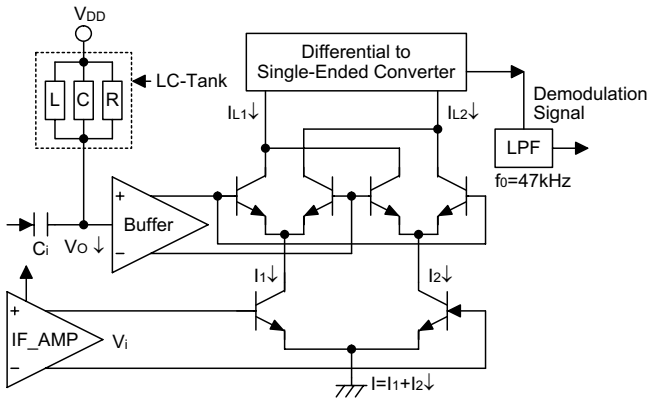


Figure 7 Quadrature detector

• Noise detector

Figure 8 is a band pass filter which can detect noise energy on N_REC pin. There is also a pass through the noise comparator to determine two states on SIG_OUT pin by internal control register setting. The high state expresses noise level more than 0.4V and the low state expresses noise level under 0.4V.

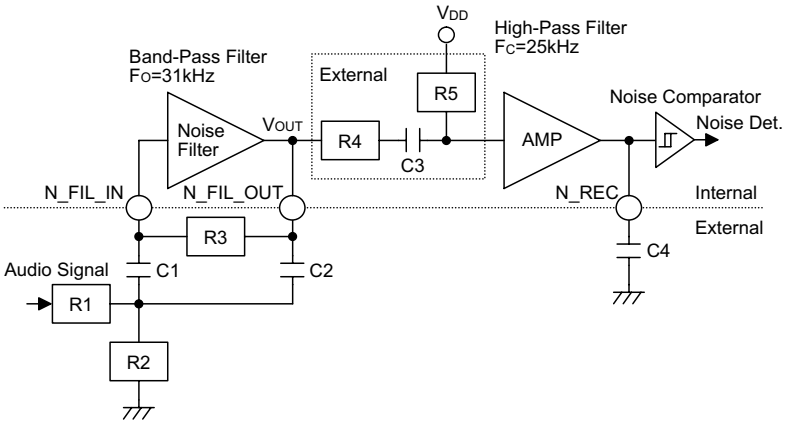


Figure 8 Noise detector

Compander

The compander (compressor and expander) is composed of two variable gain circuits which provide compression and expansion of the signal dynamic range. In consideration of the wide band noise and maximum dynamic range which exist in the transmission medium, the general signal handling technique lowers the general communication quality by reducing the S/N ratio and generating a clipping phenomenon. However the compander improves the communication quality by automatically controlling the gain based on the input signal level to increase the valid dynamic range and to improve the S/N ratio.

In the HT9015, the compressor will take a signal with a 75dB dynamic range (–5dB to –80dB), and reduce it to a 37.5dB dynamic range (–7.5dB to –45dB) by attenuating strong signals,while amplifying low level signals. The expander does the opposite in that the 37.5dB signal range is increased to a dynamic range of 75dB by amplifying strong signals and attenuating low level signals. The 0dB level is internally set at 316.227mVrms – that is the signal level which is neither amplified nor attenuated. See Figure 9 below. Through the action of the compander, the noise of the transmission medium is constant under –80dBV.

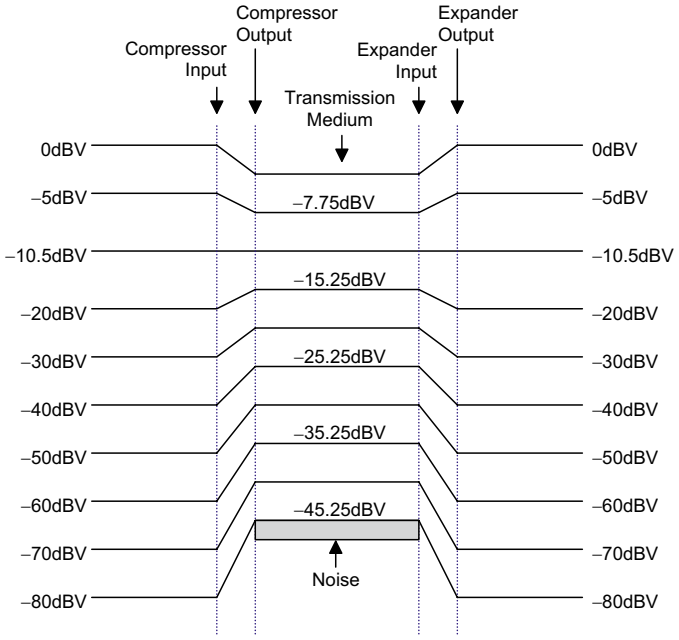


Figure 9 Illustration of compressed and extended signal

PLL

The figure below shows a simplified block diagram of the programmable universal dual phase-locked loop (PLL). It provides accurate channel frequencies for cordless phone.

The PLL contains one 14-bit programmable counter, one phase detector, charge pump, unlock detector and the 2nd local oscillator. The 12-bit programmable counter provides the reference frequency for the receiver (RX) and transmitter (TX) loops.

This dual PLL is fully programmable through the μC serial interface and supports most country channel frequencies including USA, Spain, Australia, Korea, New Zealand, U.K., Netherlands, France, Taiwan, and China.

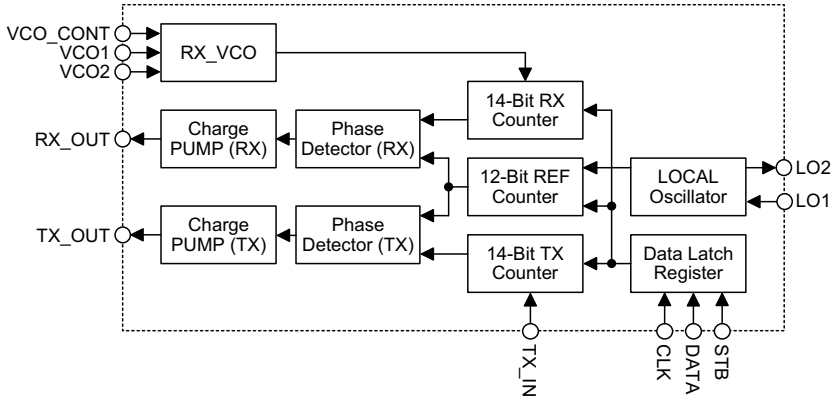
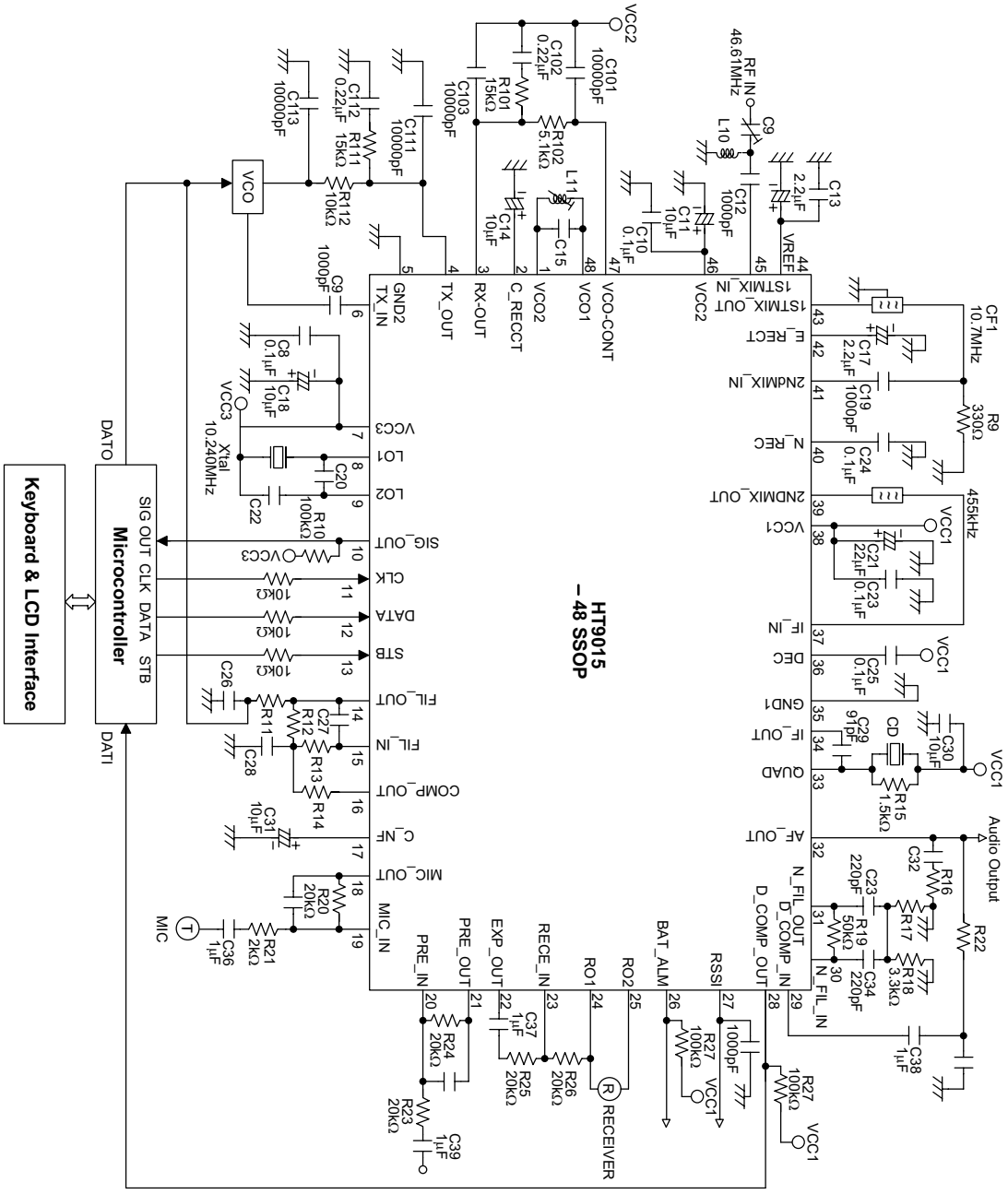


Figure 9 PLL block diagram

Application Circuits



China CT0 frequency

• Base set

Channel Number	TX Channel Frequency (MHz)	TX Counter Value (Ref. Freq.= 5.00kHz	f_{IN}–R Input Frequency (MHz) (1st IF= 10.7MHz)	RX Counter Value (Ref. Freq.= 5.00kHz)
1	45.250	9050	37.550	7510
2	45.275	9055	37.575	7515
3	45.300	9060	37.600	7520
4	45.325	9065	37.625	7525
5	45.350	9070	37.650	7530
6	45.375	9075	37.675	7535
7	45.400	9080	37.700	7540
8	45.425	9085	37.725	7545
9	45.450	9090	37.750	7550
10	45.475	9095	37.775	7555

• Hand set

Channel Number	TX Channel Frequency (MHz)	TX Counter Value (Ref. Freq.= 5.00kHz	f_{IN}–R Input Frequency (MHz) (1st IF= 10.7MHz)	RX Counter Value (Ref. Freq.= 5.00kHz)
1	48.250	9650	34.550	6910
2	48.275	9655	34.575	6915
3	48.300	9660	34.600	6920
4	48.325	9665	34.625	6925
5	48.350	9670	34.650	6930
6	48.375	9675	34.675	6935
7	48.400	9680	34.700	6940
8	48.425	9685	34.725	6945
9	48.450	9690	34.750	6950
10	48.475	9695	34.775	6955

U.S.A. CT0 frequency (10 channels)

• Base set

Channel Number	TX Channel Frequency (MHz)	TX Counter Value (Ref. Freq.= 5.00kHz	f_{IN}–R Input Frequency (MHz) (1st IF= 10.695MHz)	RX Counter Value (Ref. Freq. = 5.00kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	39.150	7830
3	46.670	9334	39.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855

• Hand set

Channel Number	TX Channel Frequency (MHz)	TX Counter Value (Ref. Freq.= 5.00kHz	f_{IN}–R Input Frequency (MHz) (1st IF= 10.7MHz)	RX Counter Value (Ref. Freq. = 5.00kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255

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