Features

- Operating voltage: 3.5V~5.5V
- Bell 202 FSK and V.23 demodulation
- Ring detection input and output
- Carrier detection output
- Power down mode
- High input sensitivity
- HT9032C: 16-pin DIP/SOP package
  HT9032D: 8-pin DIP/SOP package

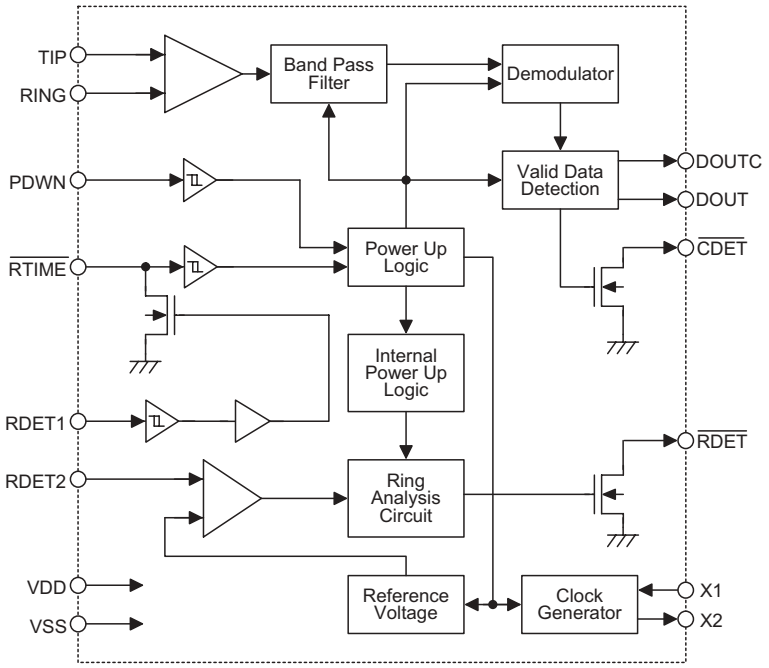
Applications

- Feature phones
- Caller ID adjunct boxes
- Fax and answering machines
- Computer telephony interface products
- ADSI products

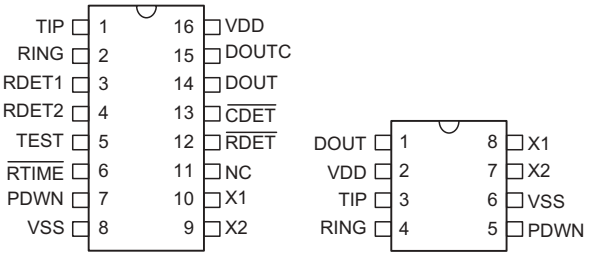
General Description

The HT9032 calling line identification receiver is a low power CMOS integrated circuit designed for receiving physical layer signals transmitted according to Bellcore TR-NWT-000030 and ITU-T V.23 specifications. The primary application of this device is for products used to receive and display the calling number, or message waiting indicator sent to subscribers from the central office facilities. The device also provides a carrier detection circuit and a ring detection circuit for easier system applications.

Block Diagram



Pin Assignment



HT9032C
– 16 DIP-A/SOP-A

HT9032D
– 8 DIP-A/SOP-A

Pin Description

Pin Name	I/O	Description
Power Inputs		
VDD	—	Power-VDD is the input power for the internal logic.
VSS	—	Ground-VSS is ground connection for the internal logic.
PDWN	I	A logic ″1″ on this pin puts the chip in power down mode. When a logic ″0″ is on this pin, the chip in power up mode. This is a Schmitt trigger input.
Clock		
X1	I	A crystal or ceramic resonator should be connected to this pin and X2. This pin may be driven from an external clock source.
X2	O	A crystal or ceramic resonator should be connected to this pin and X1.
Ring Detections		
RDET1	I	It detects ring energy on the line through an attenuating network and enables the oscillator and ring detection. This is a Schmitt trigger input.
RDET2	I	It couples the ring signal to the precision ring detector through an attenuating network. $\overline{\text{RDET}}$=″0″ if a valid ring signal is detected. This is a Schmitt trigger input.
$\overline{\text{RTIME}}$	I/O	An RC network may be connected to this pin in order to hold the pin voltage below 2.2V between the peaks of the ringing signal. This pin controls internal power up and activates the partial circuitry needed to determine whether the incoming ring is valid or not. The input is a Schmitt trigger input. The output cell structure is an NMOS output.
FSK Signal Inputs		
TIP	I	This input pin is connected to the tip side of the twisted pair wires. It is internally biased to 1/2 V_{DD} when the device is in power up mode. This pin must be DC isolated from the line.
RING	I	This input pin is connected to the ring side of the twisted pair wires. It is internally biased to 1/2 V_{DD} when the device is in power up mode. This pin must be DC isolated from the line.
Detection Results		
$\overline{\text{RDET}}$	O	This open drain output goes low when a valid ringing signal is detected. When connected to PDWN pin, this pin can be used for auto power up.
$\overline{\text{CDET}}$	O	This open drain output goes low indicating that a valid carrier is present on the line. A hysteresis is built-in to allow for a momentary drop out of the carrier. When connected to PDWN pin, this pin can be used for auto power up.
DOUT	O	This pin presents the output of the demodulator when chip in power up mode. This data stream includes the alternate ″1″ and ″0″ pattern, the marking, and the data. At all other times, this pin is held high.
DOUTC	O	This output presents the output of the demodulator when chip in power up mode and when an internal validation sequence has been successfully passed. This data stream does not include the alternate ″1″ and ″0″ pattern. This pin is always held high.
TEST	O	Output pin for testing purposes only.
NC	—	No connection

Absolute Maximum Ratings

Voltages are referenced to V_{SS}, except where noted.

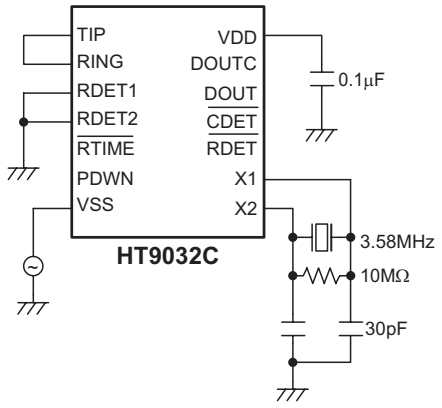
Supply Voltage .....–0.5V to 6.0V
Operating Temperature Range .....0°C to 70°C
All Input Voltages.....25mW
Storage Temperature Range .....–40°C to 150°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Crystal=3.58MHz, Ta=0~70°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Supply Voltage	—	—	3.5	5	5.5	V
I_{DD1}	Supply Current	5V	PDWN=0 (3.58MHz OSC on)	—	3.2	5	mA
I_{DD2}	Supply Current	5V	PDWN=1 and $\overline{RTIME}$=0 (3.58MHz OSC on and internal circuits partially on)	—	1.9	2.5	mA
I_{STBY}	Standby Current	5V	PDWN=1 and $\overline{RTIME}$=1 (3.58MHz OSC off)	—	—	1	μA
V_{IL}	Input Voltage Logic 0	5V	—	—	—	0.2V	V_{DD}
V_{IH}	Input Voltage Logic 1	5V	—	0.8V	—	—	V_{DD}
I_{OL}	Output Voltage Logic 0	5V	I_{OL}=1.6mA	—	—	0.1V	V_{DD}
I_{OH}	Output Voltage Logic 1	5V	I_{OH}=0.8mA	0.9V	—	—	V_{DD}
I_{IN}	Input Leakage Current, All Inputs	5V	—	–1	—	1	μA
V_{T-}	Input Low Threshold Voltage	5V	RDET1, $\overline{RTIME}$, PDWN	2.0	2.3	2.6	V
V_{T+}	Input High Threshold Voltage	5V	RDET1, $\overline{RTIME}$, PDWN	2.5	2.75	3.0	V
V_{TRDET2}	Input Threshold Voltage	5V	RDET2	1.0	1.1	1.2	V
R_{IN}	Input DC Resistance	5V	TIP, RING	—	500	—	kΩ

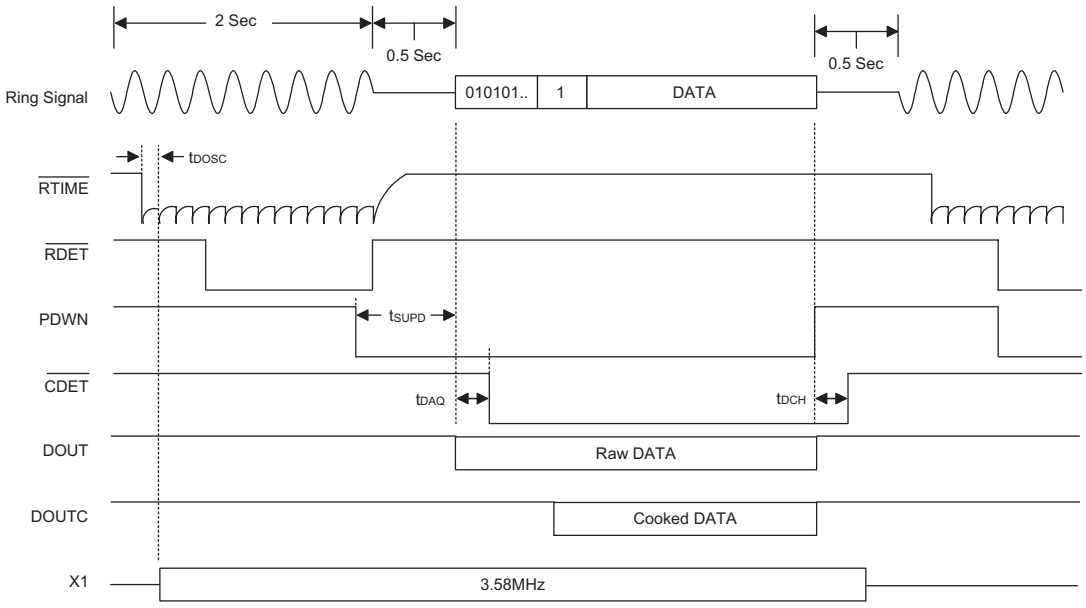


Supply current testing: All, except PDWN and $\overline{RTIME}$, unwired pins are left floating.

A.C. Characteristics – FSK Detection

V_{SS}=0V, Crystal=3.58MHz, Ta=0 to 70°C, 0dBm=0.7746Vrms @ 600Ω

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
	Input Sensitivity: TIP, RING	5V		–40	–45	—	dBm
S/N	Signal to Noise Ratio	5V		—	20	—	dB
	Band Pass Filter 60Hz 550Hz 2700Hz 3300Hz	5V	Frequency Response Relative to 1700Hz @ 0dBm	—	 –64 –4 –3 –34	—	dB
	Carrier Detect Sensitivity	5V		—	–48	—	dBm
t_{DOSC}	Oscillator Start Up Time	5V	—	—	2	—	ms
t_{SUPD}	Power Up to FSK Signal Set Up Time	5V	—	15	—	—	ms
t_{DAQ}	Carrier Detect Acquisition Time	5V	—	—	14	—	ms
t_{DCH}	End of Data to Carrier Detect High	5V	—	8	—	—	ms



Functional Description

The HT9032 is designed to be the physical layer demodulator for products targeted for the caller ID market. The data signaling interface should conform to Bell 202, which is described as follows:

- Analog, phase coherent, frequency shift keying
- Logical 1 (Mark)=1200+/−12Hz
- Logical 0 (Space)=2200+/−22Hz
- Transmission rate=1200bps
- Data application=serial, binary, asynchronous

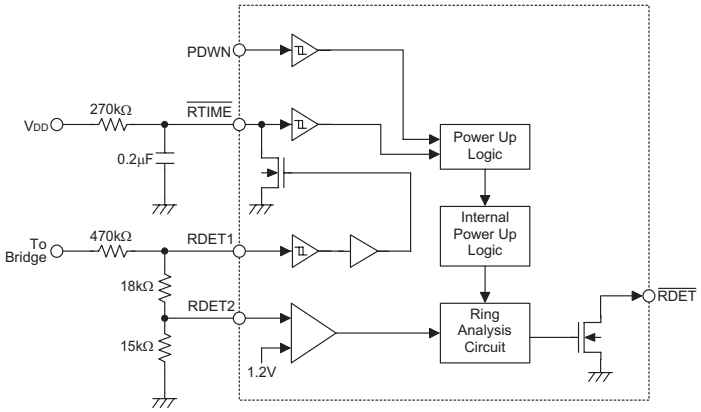
The interface should be arranged to allow simple data transmission from the terminating central office, to the CPE (Customer Premises Equipment), only when the CPE is in an on-hook state. The data will be transmitted in the silent period between the first and second power ring before a voice path is established. The transmission level from the terminating C.O. will be −13.5dBm+/−1.0. The worst case attenuation through the loop is expected to be −20dB. The receiver therefore, should have a sensitivity of approximately −34.5dBm to handle the worst case installations. The ITU-T V.23 is also using the FSK signaling scheme to transmit data in the general switched telephone network. For mode 2 of the V.23, the modulation rate and characteristic frequencies are listed below:

- Analog, phase coherent, frequency shift keying
- Logical 1 (Mark)=1300Hz
- Logical 0 (Space)=2100Hz
- Transmission rate=1200bps

Since the band pass filter of the HT9032 can pass the V.23 signal, hence the HT9032 also can demodulate the V.23 signal.

Ring detection

The data will be transmitted in the silent period between the first and second power ring before a voice path is established. The HT9032 should first detect a valid ring and then perform the FSK demodulation. The typical ring detection circuit of the HT9032 is depicted below. The power ring signal is first rectified through a bridge circuit and then sent to a resistor network that attenuates the incoming power ring. The values of resistors and capacitor given in the figure have been chosen to provide a sufficient voltage at RDET1 pin to turn on the Schmitt trigger input with approximately a 40 Vrms or greater power ring input from tip and ring. When V_{T+} of the Schmitt is exceeded, the NMOS on the pin $\overline{\text{RTIME}}$ will be driven to saturation discharging capacitor on $\overline{\text{RTIME}}$. This will initialize a partial power up, with only the portions of the part involved with the ring signal analysis enabled, including RDET2 pin. With RDET2 pin enabled, a portion of the power ring above 1.2V is fed to the ring analysis circuit. Once the ring signal is qualified, the $\overline{\text{RDET}}$ pin will be sent low.



Operation mode

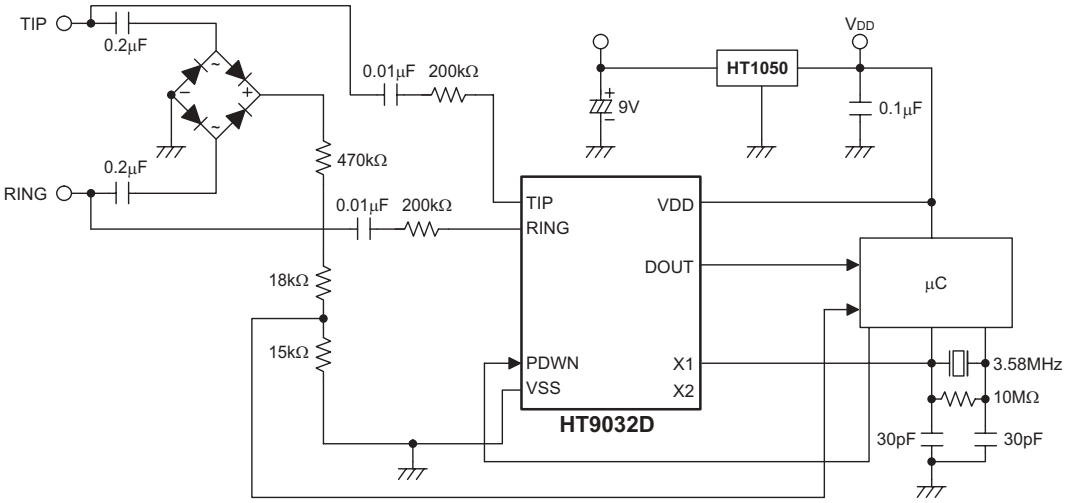
There are three operation modes of the HT9032. They are power down mode, partial power up mode, and power up mode. The three modes are classified by the following conditions:

Modes	Conditions	Current Consumption
Power down	PDWN="1" and $\overline{\text{RTIME}}$="1"	<1μA
Partial power up	PDWN="1" and $\overline{\text{RTIME}}$="0"	1.9mA typically
Power up	PDWN="0"	3.2mA typically

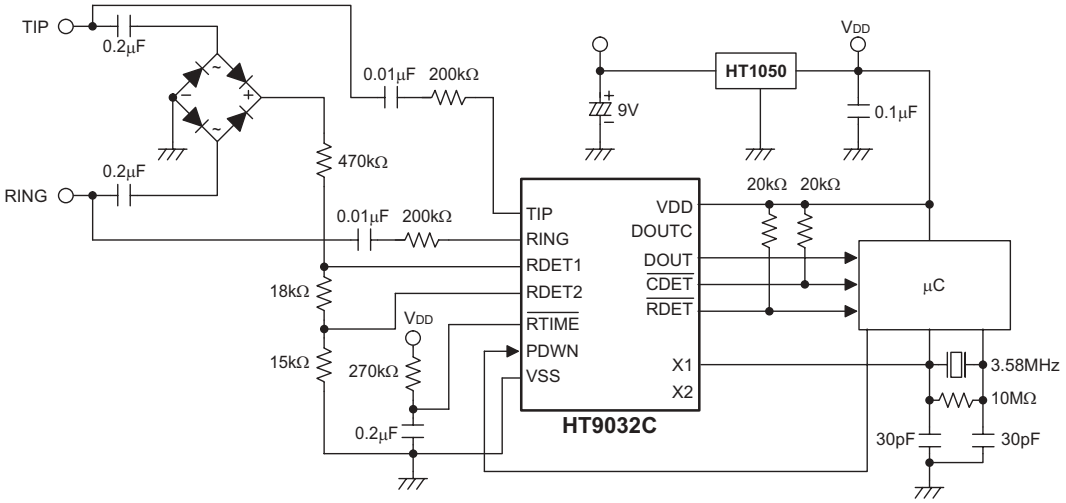
Normally, the PDWN pin and the $\overline{\text{RTIME}}$ pin control the operation mode of the HT9032. When both pins are HIGH, the HT9032 is set at the power down mode, consuming less than 1μA of supply current. When a valid power ring arrives, the $\overline{\text{RTIME}}$ pin will be driven below V_{T-} and the portions of the part involved in the ring signal analysis are enabled. This is partial power up mode, consuming approximately 1.9mA typically. Once the PDWN pin is below V_{T-}, the part will be fully powered up, and ready to receive FSK. During this mode, the device current will increase to approximately 3.2mA (typ). The state of the $\overline{\text{RTIME}}$ pin is now a "don't care" as far as the part is concerned. After the FSK message has been received, the PDWN pin can be allowed to return to V_{DD} and the part will return to the power down mode.

Application Circuits

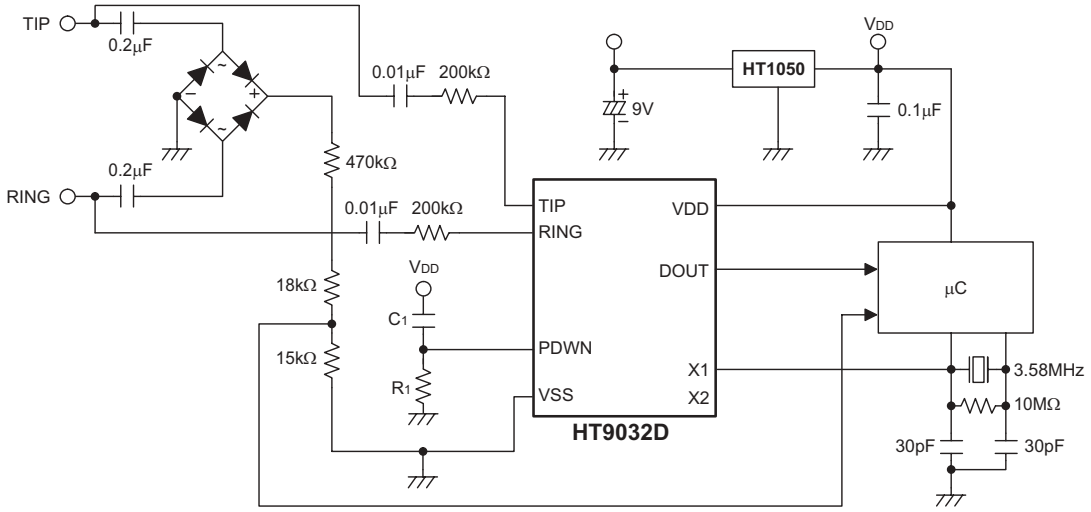
Application circuit 1



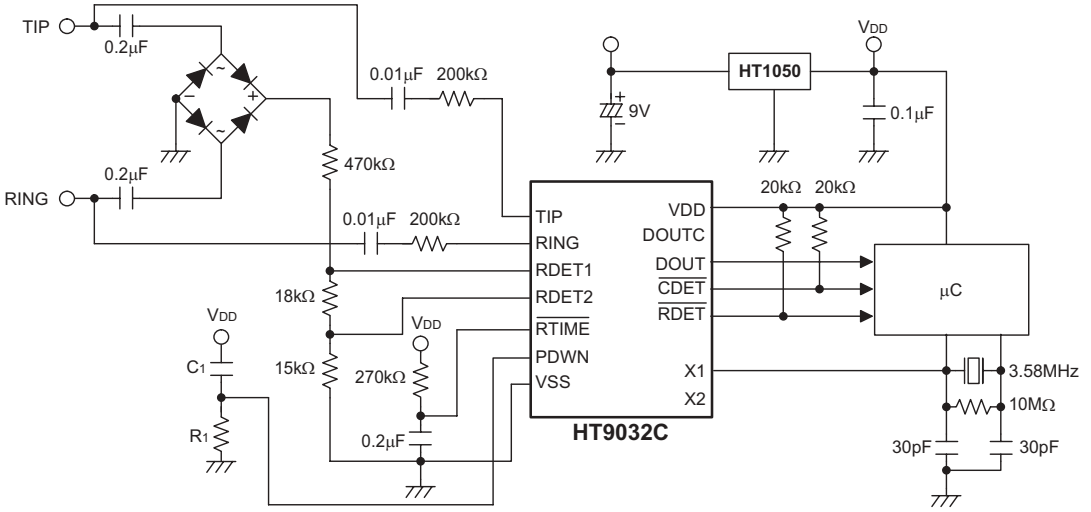
Application circuit 2

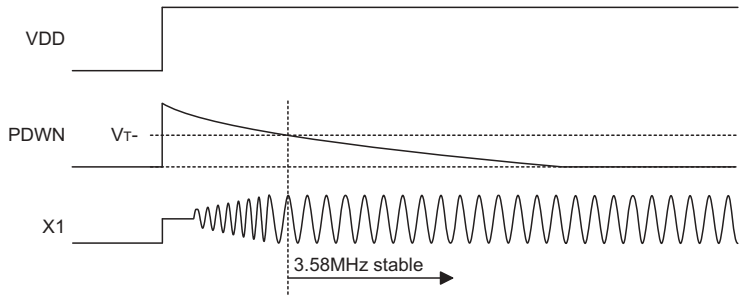


Application circuit 3 — power on reset



Application circuit 4 — power on reset





Note: reference C_1=0.1μF R_1=81kΩ

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