Single-Ended, Analog-Input 24Bit, 96kHz Stereo ADC

FEATURES

- 24Bit Delta-Sigma Stereo ADC
- Single-Ended Voltage Input: 3 Vp-p
- High Performance
  - THD+N: -90dB (Typical)
  - SNR: 99dB (Typical)
  - Dynamic Range: 99dB (Typical)
- Flexible PCM Audio Interface
  - Master- or Slave-Mode Selectable
  - Data Formats: 24Bit I^2S, 24Bit Left-Justified
- Power Down and Reset by Halting System Clock
- Analog Antialias LPF Included
- Sampling Rate: 8 kHz–96 kHz
- System Clock: 256 f_S, 384 f_S, 512 f_S
- Resolution: 24 Bits
- Dual Power Supplies
  - 5V for Analog
  - 3.3V for Digital
- TSSOP14 Package

APPLICATIONS

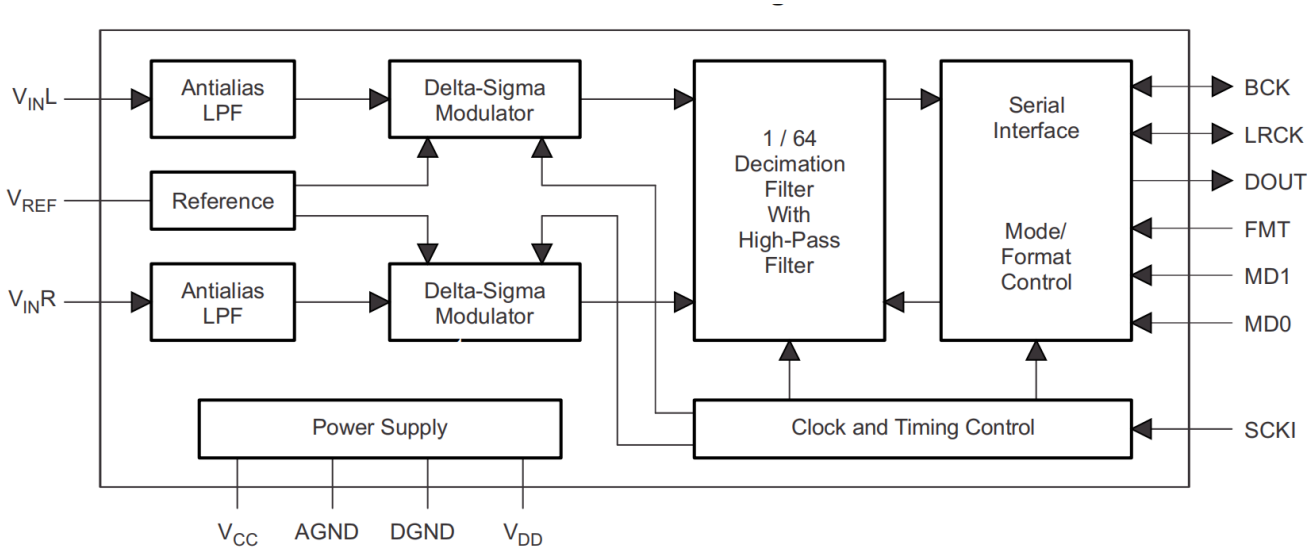
- DVD Recorder
- Digital TV
- AV Amplifier or Receiver
- MD Player
- CD Recorder
- Multitrack Receiver
- Electric Musical Instrument

DESCRIPTION

The HT91808 device is a high-performance, low-cost, single-chip, stereo analog-to-digital converter with single-ended analog voltage input. The HT91808 device uses a delta-sigma modulator with 64-times oversampling and includes a digital decimation filter and high-pass filter that removes the dc component of the input signal. For various applications, the HT91808 device supports master and slave mode and two data formats in serial audio interface.

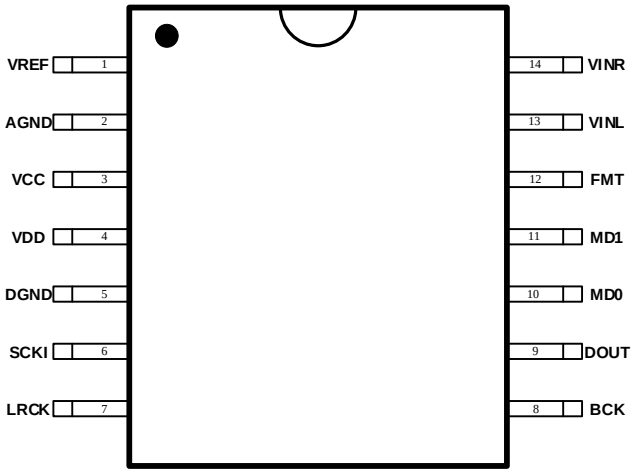
The device is available in TSSOP14 package.

BLOCK DIAGRAM



Contents

■ TERMINAL CONFIGURATION



TSSOP14 Top View

■ TERMINAL FUNCTION

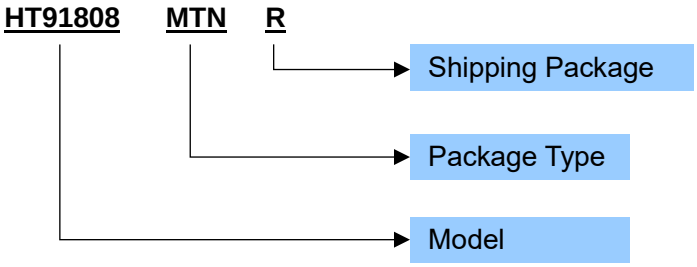
Terminal No.	NAME	I/O[1]	Description
1	VREF	-	Reference-voltage decoupling (= 0.5 VCC).
2	AGND	-	Analog GND
3	VCC	-	Analog power supply, 5V
4	VDD	-	Digital power supply, 3.3V
5	DGND	-	Digital GND
6	SCKI	I	System clock input; 256 f_S, 384 f_S or 512 f_S [2]
7	LRCK	I/O	Audio-data latch-enable input or output [3]
8	BCK	I/O	Audio-data bit-clock input or output [3]
9	DOUT	O	Audio-data digital output
10	MD0	I	Audio-interface mode select 0 [4]
11	MD1	I	Audio-interface mode select 1 [4]
12	FMT	I	Audio-interface format select [4]
13	INL	I	Analog input, L-channel
14	INR	I	Analog input, R-channel

[1] I: input O: output G: GNDP: Power
[2] Schmitt-trigger input, 5V tolerant
[3] Schmitt-trigger input with internal pulldown (100-kΩ, typical)
[4] Schmitt-trigger input with internal pulldown (100-kΩ, typical), 5V tolerant

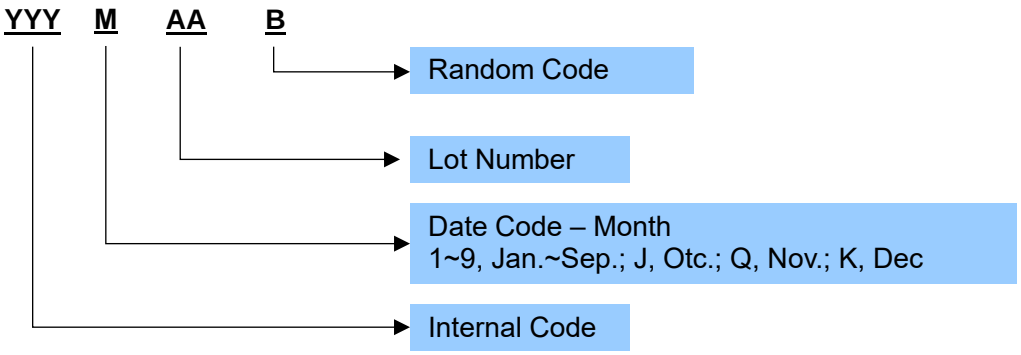
■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	Shipping Package / MOQ
HT91808MTNR	TSSOP14 (MTN)	HT91808 YYYMAAB[5]	-40℃～85℃	Tape and Reel (R) / 3000pcs

Part Number



Production Tracking Code



[5] YYYMAAB is production tracking code

■ ELECTRICAL CHARACTERISTICS[6]

● Absolute Maximum Ratings[7]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Analog supply voltage range	VCC	-0.3	6.5	V
Digital supply voltage range	VDD	-0.3	4	V
Digital input voltage, LRCK, BCK, DOUT	Vin	-0.3	(VDD+0.3)<4	V
Digital input voltage, SCKI, MD0, MD1, FMT	Vin	-0.3	6.5	V
Analog input voltage, INL, INR, VREF	Vin	-0.3	(VCC+0.3)<6.5	V
Input current (any pins except supplies)			±10	mA
Junction temperature range	T_J		150	℃
Storage temperature range	T_{STG}	-50	150	℃

● Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog supply voltage	VCC	4.5	5	5.5	V
Digital supply voltage	VDD	2.7	3.3	3.6	V
Analog input voltage, full scale (-0dB), VCC = 5V	Vin			3	Vpp
High input logic level[8]	V_{IH}	2		VDD	VDC
Low input logic level[7]	V_{IL}	0		0.8	VDC
High input logic level[910]	V_{IH}	2		5.5	VDC
Low input logic level[89]	V_{IL}	0		0.8	VDC
Digital input logic family		TTL compatible			
Digital input clock frequency, system clock		2.048		49.152	MHz
Digital input clock frequency, sampling clock		8		96	kHz
Digital output load capacitance				20	pF
Operating ambient temperature range	T_A	-40		85	℃
Junction temperature	T_J			150	℃

[6] Depending on parts and PCB layout, characteristics may be changed.
[7] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability
[8] Pins 7, 8: LRCK, BCK (Schmitt-trigger input, with 100-kΩ typical pulldown resistor, in slave mode)
[9] Pin 6: SCKI (Schmitt-trigger input, 5V tolerant)
[10] Pins 10–12: MD0, MD1, FMT (Schmitt-trigger input, with 100-kΩ typical pulldown resistor, 5V tolerant)

Data Format

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Resolution				24		Bits
Audio data interface format				I^2S, left-justified		
Audio data bit length				24		Bits
Audio data format				MSB-first, 2s complement		
Sampling frequency	f_S		8	48	96	kHz
System clock frequency		256 f_S	2.048	12.288	24.576	MHz
		384 f_S	3.072	18.432	36.864	MHz
		512 f_S	4.096	24.576	49.152	MHz

Input / output Logic

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
High input logic level[7]	V_{IH}		2		VDD	VDC
Low input logic level[7]	V_{IL}		0		0.8	VDC
High input logic level[89]	V_{IH}		2		5.5	VDC
Low input logic level[89]	V_{IL}		0		0.8	VDC
High input logic current[8]	I_{IH}	VIN = VDD			±10	uA
Low input logic current[8]	I_{IL}	VIN = 0 V			±10	uA
High input logic current[79]	I_{IH}	VIN = VDD		33	50	uA
Low input logic current[79]	I_{IL}	VIN = 0 V			±10	uA
High output logic level[11]	V_{OH}	I_{OUT} = –4 mA	2.8			VDC
Low output logic level	V_{OL}	I_{OUT} = 4 mA			0.5	VDC

DC Accuracy

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Gain mismatch, channel-to-channel				±1		% of FSR
Gain error				±3		% of FSR

Dynamic Performance[12]

T_A = 25°C, VCC = 5V, VDD = 3.3V, master mode, fs = 48kHz, system clock = 512fs, 24-bit data, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Total Harmonic Distortion + Noise	THD+N	VIN = -0.5dB, fs = 48kHz		-90		dB
		VIN = -0.5dB, fs = 96kHz, system clock = 256 f_S,		-80		dB
		VIN = –60 dB, f_S = 48 kHz		-37		dB
		VIN = -60dB, fs = 96kHz, system clock = 256 f_S,		-39		dB
Dynamic Range	DR	fs = 48kHz, A-weighted		99		dBVDC
		fs = 96kHz, system clock = 256 f_S, A-weighted		101		dBVDC
Signal-to-noise ratio	SNR	fs = 48kHz, A-weighted		99		dB
		fs = 96kHz, system clock = 256 f_S, A-weighted		101		dB
Channel separation	CS	fs = 48kHz		97		dB
		fs = 96kHz, system clock = 256 f_S		91		dB

[11] Pins 7–9: LRCK, BCK (in master mode), DOUT

[12] Testing of analog performance specifications uses an audio measurement system by Audio Precision™ with 400Hz HPF and 20kHz LPF in RMS mode.

● Analog Input

T_A = 25°C, VCC = 5V, VDD = 3.3V, master mode, fs = 48kHz, system clock = 512fs, 24-bit data, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input voltage				0.6Vcc		Vpp
Center voltage (VREF)				0.5Vcc		V
Input impedance				70		kΩ
Antialiasing filter frequency response		－3 dB		1.3		MHz

● Digital Filter Performance

T_A = 25°C, VCC = 5V, VDD = 3.3V, master mode, fs = 48kHz, system clock = 512fs, 24-bit data, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Pass band					0.454 f_S	Hz
Stop band			0.583 f_S			Hz
Pass-band ripple					±0.05	dB
Stop-band attenuation			－65			dB
Delay time				17.4 / f_S		
HPF frequency response		－3 dB		0.019f_S /1000		

● Power Supply Requirements

TA = 25°C, VCC = 5V, VDD = 3.3V, master mode, fs = 48kHz, system clock = 512fs, 24-bit data, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Analog supply current	ICC	f_S = 48 kHz or f_S = 96 kHz system clock = 256fs		5.1		mA
		Powered down[13]		1		uA
Digital supply current	IDD	f_S = 48 kHz		5.9		mA
		f_S = 96 kHz, system clock = 256fs		10.2		mA
		Powered down[12]		90		uA
Power dissipation		f_S = 48 kHz		45		mW
		f_S = 96 kHz, system clock = 256fs		59		mW
		Powered down[12]		300		μW

[13] Power-down and reset functions enabled by halting SCKI, BCK, LRCK.

- **Timing Requirements**

PARAMETER	SYMBOL		MIN	TYP	MAX	UNIT
SYSTEM CLOCK TIMING						
System clock pulse duration, HIGH	$t_{w(SCKH)}$		8			ns
System clock pulse duration, LOW	$t_{w(SCKL)}$		8			ns
System clock duty cycle			40%		60%	
CLOCK-HALT POWER-DOWN AND RESET TIMING						
Delay time from SCKI halt to internal reset	$t_{(CKR)}$		4			us
Delay time from SCKI resume to reset release	$t_{(RST)}$				1024SCKI	Us
Delay time from reset release to DOUT output	$t_{(REL)}$				8960fs	Us
AUDIO DATA INTERFACE TIMING (Slave Mode: LRCK and BCK Work as Inputs)[14]						
BCK period	$t_{(BCKP)}$		1 / (64 fs)			ns
BCK pulse duration, HIGH	$t_{(BCKH)}$		1.5 × $t_{(SCKI)}$			ns
BCK pulse duration, LOW	$t_{(BCKL)}$		1.5 × $t_{(SCKI)}$			ns
LRCK setup time to BCK rising edge	$t_{(LRSU)}$		50			ns
LRCK hold time to BCK rising edge	$t_{(LRHD)}$		10			ns
LRCH period	$t_{(LRCP)}$		10			us
Delay time, BCK falling edge to DOUT valid	$t_{(CKDO)}$		-10		40	ns
Delay time, LRCK edge to DOUT valid	$t_{(LRDO)}$		-10		40	ns
Rise time of all signals	t_r				20	ns
Fall time of all signals	t_f				20	ns
AUDIO DATA INTERFACE TIMING (Master Mode: LRCK and BCK Work as Outputs)[15]						
BCK period	$t_{(BCKP)}$		150	1 / (64 fs)	2000	ns
BCK pulse duration, HIGH	$t_{(BCKH)}$		65		1200	ns
BCK pulse duration, LOW	$t_{(BCKL)}$		65		1200	ns
Delay time, BCK falling edge to LRCK valid	$t_{(BCKR)}$		-10		20	ns
LRCK period	$t_{(LRCP)}$		10	1/fs	125	ns
Delay time, BCK falling edge to DOUT valid	$t_{(CKDO)}$		-10		20	ns
Delay time, LRCK edge to DOUT valid	$t_{(LRDO)}$		-10		20	ns
Rise time of all signals	t_r				20	ns
Fall time of all signals	t_f				20	ns
AUDIO CLOCK INTERFACE TIMING (Master Mode: BCK Work as Outputs)[16]						
Delay time, SCKI rising edge to BCK edge	$t_{(SCKBCK)}$		5		30	ns

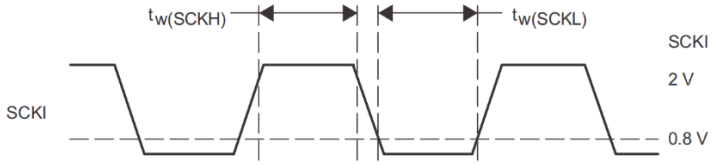


Figure 1 System Clock Timing

[14] Timing measurement reference level is 1.4 V for input and 0.5 VDD for output. Rise and fall times are from 10% to 90% of the input-output signal swing. Load capacitance of DOUT is 20 pF. $t_{(SCKI)}$ is the SCKI period.
[15] Timing measurement reference level is 0.5 VDD. Rise and fall times are from 10% to 90% of the input-output signal swing. Load capacitance of all signals is 20 pF
[16] Timing measurement reference level is 1.4 V for input and 0.5 VDD for output. Load capacitance of BCK is 20 pF. This timing applies when SCKI frequency is less than 25 MHz

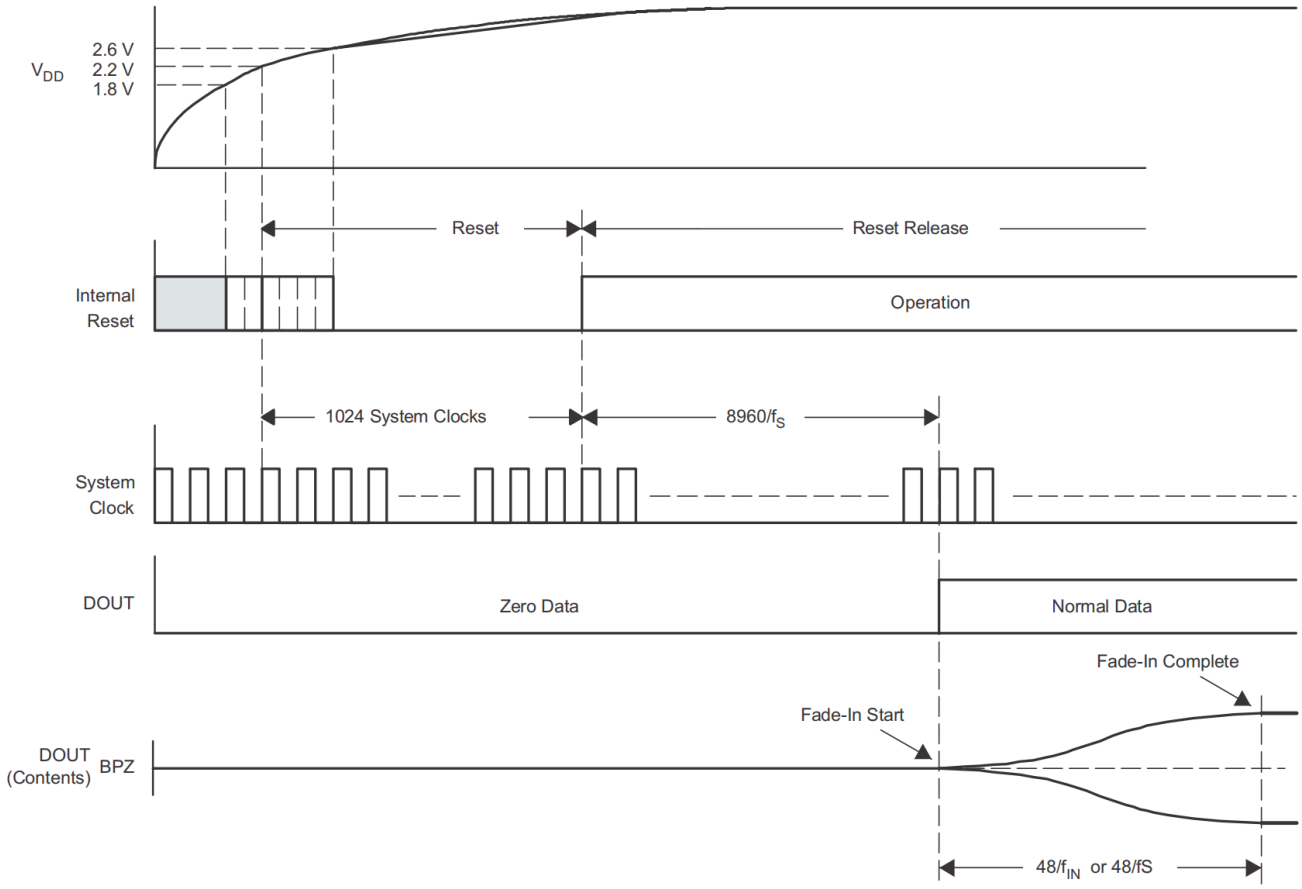


Figure 2 Power-On Timing

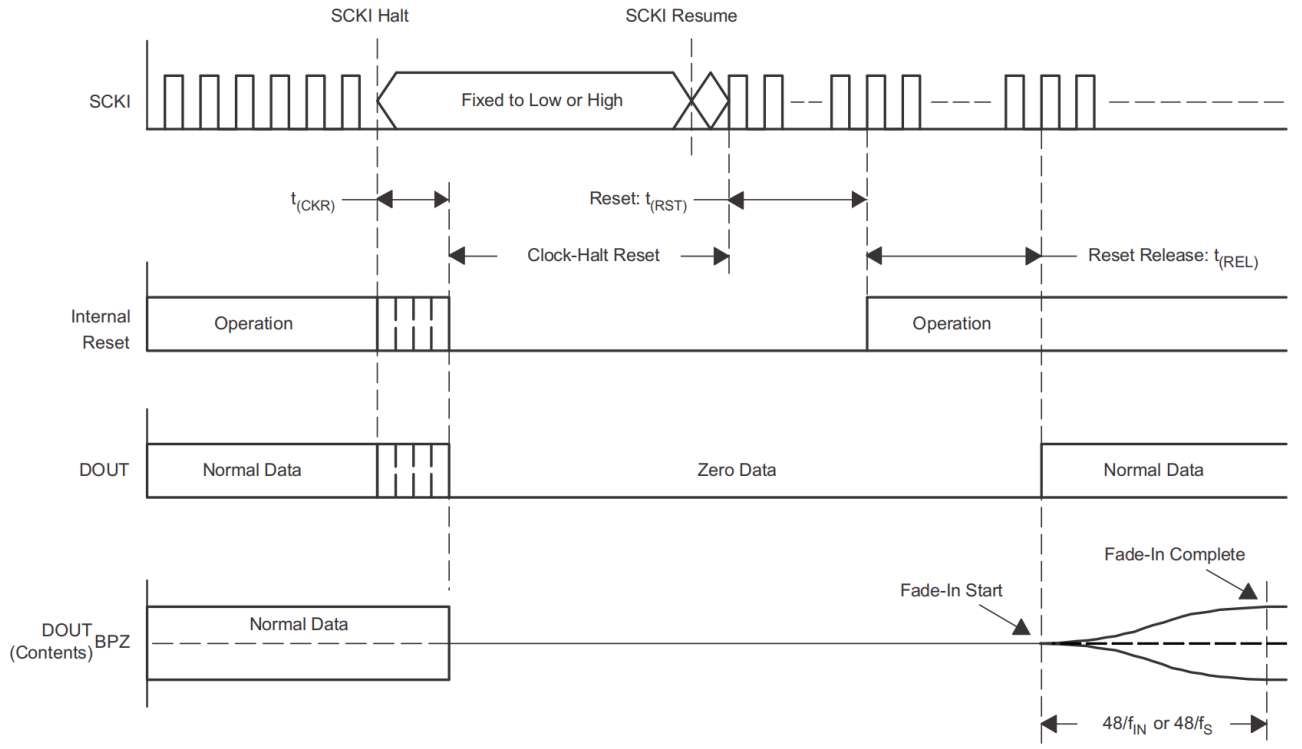


Figure 3 Clock-Halt Power-Down and Reset Timing

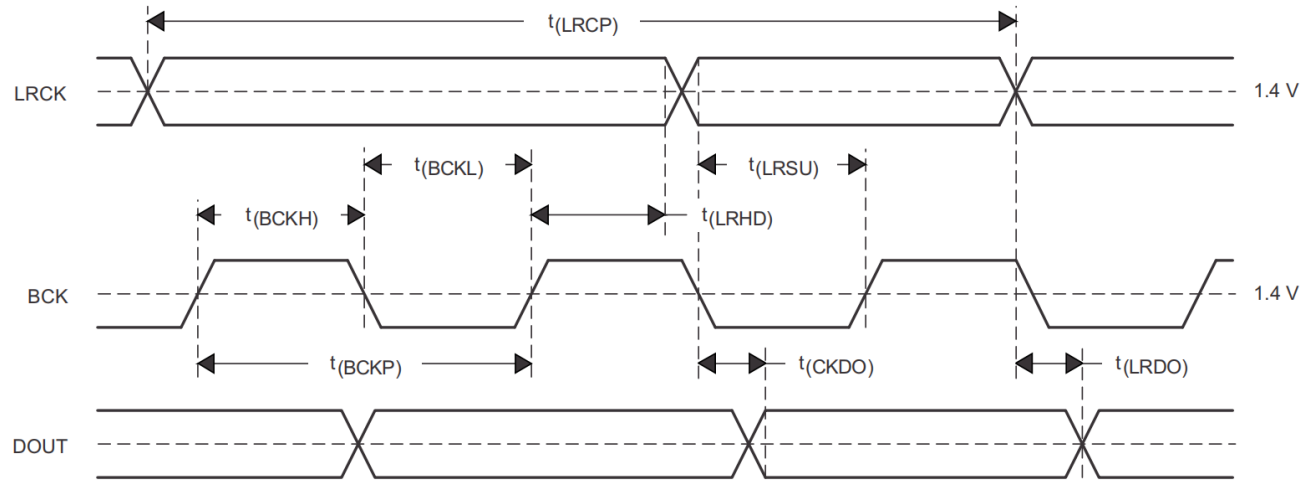


Figure 4 Audio Data Interface Timing (Slave Mode: LRCK and BCK Work as Inputs)

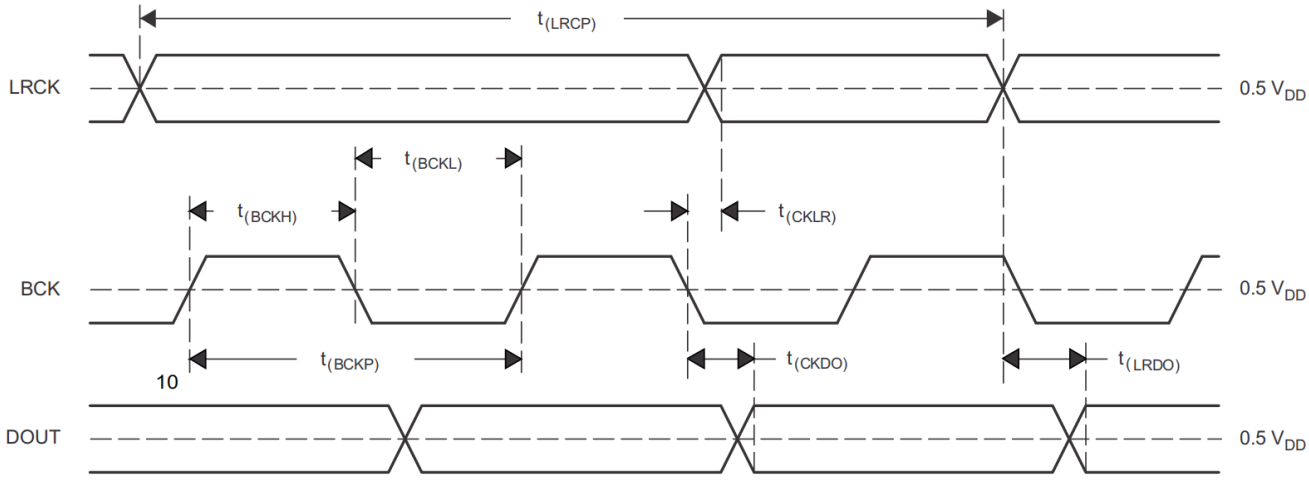


Figure 5 Audio Data Interface Timing (Master Mode: LRCK and BCK Work as Outputs)

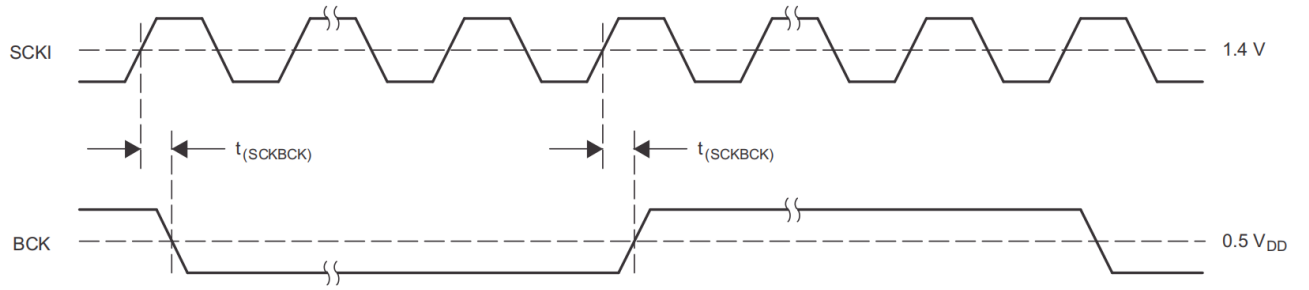


Figure 6 Audio Clock Interface Timing (Master Mode: BCK Works as Output)

■ APPLICATION INFORMATION

The HT91808 is high-performance, low-cost, single-chip, stereo analog-to-digital converter with single-ended analog voltage input. The HT91808 uses a delta-sigma modulator with 64-times oversampling and includes a digital decimation filter and high-pass filter that removes the dc component of the input signal. For various applications, the HT91808 supports master and slave mode and two data formats in serial audio interface up to 96-kHz sampling. These features are controlled through hardware by pulling pins high or low with resistors or a controller GPIO. The HT91808 also supports a power-down and reset function by means of halting the system clock.

1. Feature Description

1.1. Hardware Control

Pins FMT, MD0, and MD1 allow the device to be controlled by either pullup or pulldown resistors as well as GPIO from a digital IC. These controls allow the option of switching between I2S or left-justified, and in which interface mode the device operates

1.2. System Clock

The HT91808 device supports 256 f_S, 384 f_S, and 512 f_S as system clock, where f_S is the audio sampling frequency. The system clock input must be on SCKI (pin 6).

The HT91808 device has a system-clock detection circuit which automatically senses if the system-clock operation is at 256 f_S, 384 f_S, or 512 f_S in slave mode. In master mode, control of the system clock frequency must be through the serial control port, which uses MD1 (pin 11) and MD0 (pin 10). An internal circuit automatically divides down the system clock to generate frequencies of 128 f_S and 64 f_S, which operate the digital filter and the delta-sigma modulator, respectively.

Table 1 shows some typical relationships between sampling frequency and system clock frequency, and Figure 1 shows system clock timing.

MCLK/LRCK must be an integer ratio, as shown in Table 2.

Table 1 Common Clock Frequencies

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	256×fs	384×fs	512×fs
8	2.048	3.072	4.096
16	4.906	6.144	8.192
32	8.192	12.288	16.384
44.1	12.2896	16.9344	22.5792
48	12.288	18.432	24.576
64	16.384	24.576	32.768
88.2	22.5792	33.8688	45.1584
96	24.576	36.864	49.152

1.3. Synchronization with Digital Audio System

In slave mode, the HT91808 device operates under LRCK (pin 7), synchronized with system clock SCKI (pin 6). The HT91808 device does not require a specific phase relationship between LRCK and SCKI, but does

require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 BCK/frame (±5 BCKs for 48 BCK/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within 1 / f_S and digital output goes to zero data (BPZ code) until resynchronization between LRCK and SCKI occurs.

In the case of changes less than ±5 BCKs for 64 BCK/frame (±4 BCKs for 48 BCK/frame), resynchronization does not occur, and the previously described digital output control and discontinuity do not occur.

Figure 7 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, the HT91808 device can generate some noise in the audio signal. Also, the transition of normal data to undefined data creates a discontinuity in the digital output data, which can generate some noise in the audio signal. The digital output is valid after resynchronization completes and the time of 32 / fS has elapsed.

Because the fade-in operation is performed, it takes additional time of 48 / fin or 48 / f_S to obtain the level corresponding to the analog input signal. In the case of loss of synchronization during the fade-in or fade-out operation, the operation stops and DOUT (pin 9) goes to zero data immediately. The fade-in operation resumes from mute after the time of 32 / f_S following resynchronization.

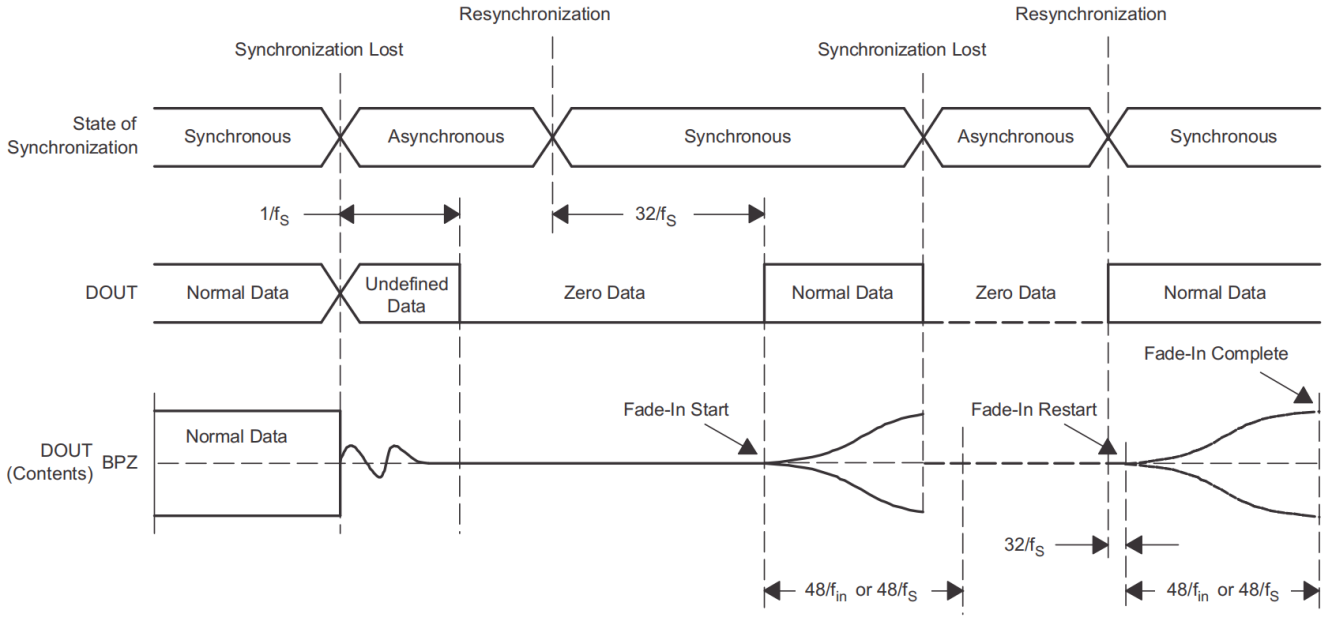


Figure 7 ADC Digital Output for Loss of Synchronization and Resynchronization

1.4. Power On

The HT91808 device has an internal power-on-reset circuit, and initialization (reset) occurs automatically when the power supply (VDD) exceeds 2.2 V (typical). While VDD < 2.2 V (typical), and for 1024 system-clock counts after VDD > 2.2 V (typical), the HT91808 device stays in the reset state and the digital output remains zero. After release of the reset state, 8960 / fS seconds must pass before the digital output becomes valid. Because of the performing of the fade-in operation, it takes additional time of 48 / fin or 48 / fS to obtain the data corresponding to the analog input signal. Figure 2 illustrates the power-on timing and the digital output.

1.5. Serial Audio Data Interface

The HT91808 device interfaces the audio system through LRCK (pin 7), BCK (pin 8), and DOUT (pin 9).

1.5.1 Interface Mode

MD1 (pin 11) and MD0 (pin 10) select master mode and slave mode as interface modes, both of which the HT91808 device supports. Table 2 shows the interface-mode selections. It is necessary to set MD1 and MD0 prior to power on.

In master mode, the HT91808 device provides the timing of serial audio data communications between the HT91808 device and the digital audio processor or external circuit. While in slave mode, the HT91808 device receives the timing for data transfer from an external controller.

Table 2 Interface Modes

MD1 (PIN 11)	MD0 (PIN 10)	INTERFACE MODE
Low	Low	Slave mode (256 f_S, 384 f_S, 512 f_S autodetection)
Low	High	Master mode (512 f_S)
High	Low	Master mode (384 f_S)
High	High	Master mode (256 f_S)

In master mode, BCK and LRCK work as output pins, timing which from the clock circuit of the HT91808 device controls these pins. The frequency of BCK is constant at 64 BCK/frame.

In slave mode, BCK and LRCK work as input pins. The HT91808 device accepts 64BCK/frame or 48BCK/frame format (only for a 384f_S system clock), not 32BCK/frame format.

1.5.2 Data Format

Table 3 Interface Modes

FMT (Pin 12)	INTERFACE MODE
Low	I^2S, 24-bit
High	Left-justified, 24-bit

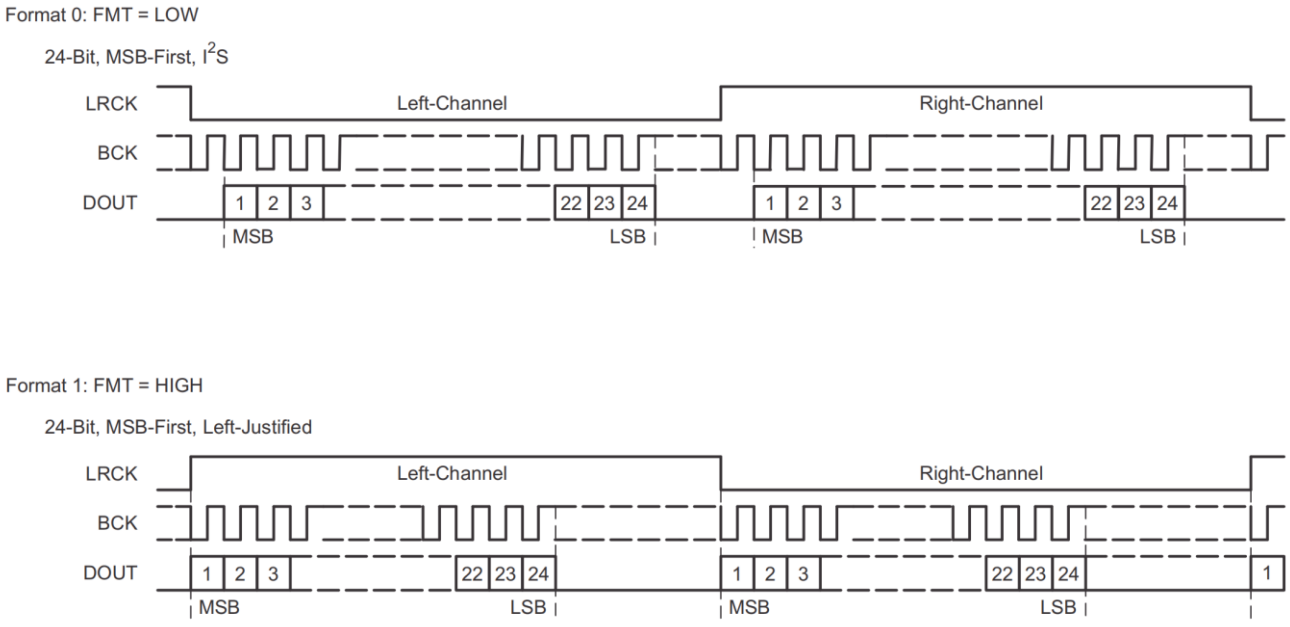


Figure 8 Audio Data Format (LRCK and BCK Work as Inputs in Slave Mode and as Outputs in Master Mode)

1.5.3 Interface Timing

Figure 4 and Figure 5 illustrate the interface timing in slave mode and master mode, respectively.

2. Device Functional Modes

2.1. Fade-In and Fade-Out Functions

The HT91808 device has fade-in and fade-out functions on DOUT (pin 9) to avoid pop noise, and the functions come into operation in some cases as described in several following sections. Performance of the level changes from 0 dB to mute or mute to 0 dB employs calculated pseudo S-shaped characteristics with zero-cross detection. Because of the zero-cross detection, the time needed for the fade-in and fade-out depends on the analog input frequency (fin). It takes 48 / fin to complete the processing. If there is no zero-cross during 8192 / f_S, a forced DOUT fade-in or fade-out occurs during 48 / f_S (TIME OUT). Figure 9 illustrates the fade-in and fade-out operation processing.

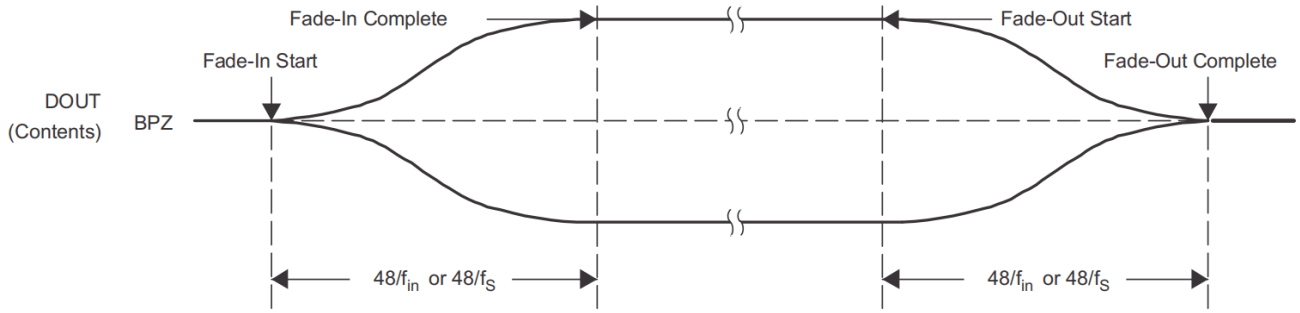


Figure 9 Fade-In and Fade-Out Operations

2.2. Clock-Halt Power-Down and Reset Function

The HT91808 device has a power-down and reset function. Halting SCKI (pin 6) in both master and slave modes triggers this function. The function is available any time after power on. Reset and power down occur automatically 4 μs (minimum) after the halt of SCKI. During assertion of the clock-halt reset, the HT91808 device stays in the reset and power-down mode, with DOUT (pin 9) forced to zero. Release the reset and power-down mode requires the supply of SCKI. The digital output is valid after release of the reset state and elapse of the time of 1024 SCKI + 8960 / f_S. Performing the fade-in operation takes additional time of 48 / fin or 48 / f_S to attain the level corresponding to the analog input signal. Figure 3 illustrates the clock-halt reset timing.

To avoid ADC performance degradation, BCK (pin 8) and LRCK (pin 7) must synchronize with SCKI within 4480 / f_S after the resumption of SCKI. If it takes more than 4480 / f_S for BCK and LRCK to synchronize with SCKI, mask SCKI until it again achieves synchronization, taking care of glitch and jitter. See the typical circuit connection diagram, Figure 10.

To avoid ADC performance degradation, assertion of the clock-halt reset is necessary when changing system clock SCKI or the audio interface clocks BCK and LRCK (sampling rate f_S) on the fly.

3. Application and Implementation

3.1. Application Information

The HT91808 device is suitable for wide variety of cost-sensitive consumer applications requiring good performance and operation with a 5V analog supply and 3.3V digital supply.

3.2. Typical Application

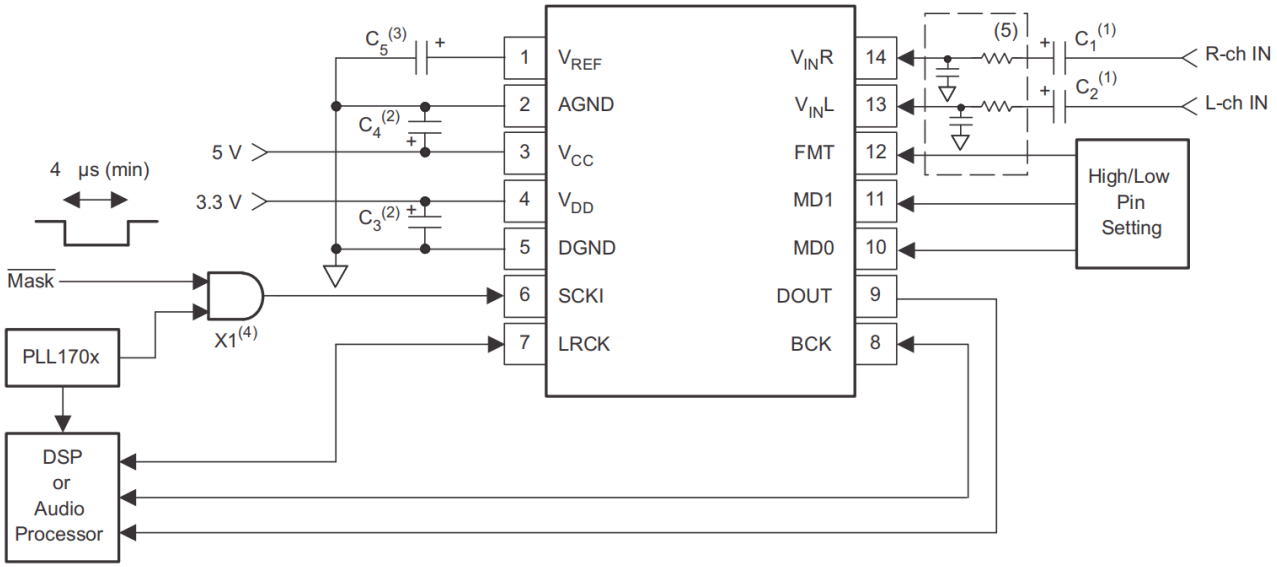


Figure 10 Typical Circuit Connection Diagram

(1) C1, C2: A 1µF electrolytic capacitor gives 2.3 Hz (τ = 1µF × 70 kΩ) cutoff frequency for the input HPF in normal operation and requires a power-on settling time with a 60-ms time constant in the power-on initialization period.

(2) C3, C4: Bypass capacitors, 0.1µF ceramic and 10µF electrolytic, depending on layout and power supply.

(3) C5: Recommended capacitors are 0.1µF ceramic and 10-µF electrolytic.

(4) X1: X1 masks the system clock input when using the clock-halt reset function with external control.

(5) Optional external antialiasing filter could be required, depending on the application.

For this design example, use the parameters listed in Table 4 as the input parameters

Table 4 Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Analog input voltage range	0 Vp-p to 3 Vp-p
Output	PCM audio data
System clock input frequency	2.048 MHz to 49.152 MHz
Output sampling frequency	8 kHz to 96 kHz
Power supply	3.3 V and 5 V

3.2.1 Control Pins

The control pins FMT, MD0, and MD1 should be controlled either by biasing with a 10 kΩ resister to VDD or GND, or by driving with GPIO from the DSP or audio processor.

3.2.2 Master Clock

In this application of the HT91808 device, a PLL170X series device is used as the master clock source to drive both the HT91808 and the DSP or audio processor synchronously. With the addition of the AND gate, the operation of the HT91808 device can be halted by control of the MASK bit. A crystal that operates at the standard audio multiples can also be used.

3.2.3 DSP or Audio Processor

In this application, the DSP or audio processor is acting as the audio master, and the HT91808 is acting as the audio slave. This means the DSP or audio processor must be able to output audio clocks that the HT91808 can use to process audio signals.

3.2.4 Input Filters

For the analog input circuit, an ac coupling capacitor should be placed in series with the input. This will remove the dc component of the input signal. An RC filter can also be implemented to filter out-of-band noise to reduce aliasing. The equation below can be used to calculate the cutoff frequency of the optional RC filter for the input.

$$f_c = \frac{1}{2\Pi RC}$$

4. Power Supply Recommendations

The HT91808 device requires a 5V nominal supply and a 3.3V nominal supply. The 5V supply is for the analog circuitry powered by the VCC pin. The 3.3V supply is for the digital circuitry powered by the VDD pin. The decoupling capacitors for the power supplies should be placed close to the device terminals.

A VCC that varies from the nominal 5 V affects the reference voltage for the input. This has a slight impact on the data conversion of the device.

5. Layout

5.1. VCC, VDD Pins

Bypass the digital and analog power supply lines to the HT91808 device to the corresponding ground pins with both 0.1μF ceramic and 10μF electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC.

5.2. AGND, DGND Pins

To maximize the dynamic performance of the HT91808 device, there are no internal connections to the analog and digital grounds. These grounds should have low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the HT91808 device package to reduce potential noise problems.

5.3. VINL, VINR Pins

VINL and VINR are single-ended inputs. These inputs have integrated antialias low-pass filters to remove the high-frequency noise outside the audio band. If the performance of these filters is not adequate for an application, the application requires appropriate external antialiasing filters. An appropriate choice would typically be a passive RC filter in the range of 100 Ω and 0.01 μF to 1 kΩ and 1000 pF.

5.4. VREF Pin

To ensure low source impedance of the ADC references, the recommended capacitors between VREF and AGND are 0.1μF ceramic and 10μF electrolytic. These capacitors should be located as close as possible to the VREF pin to reduce dynamic errors on the ADC references.

5.5. DOUT Pin

The DOUT pin has a large load-drive capability, but if the DOUT line is long, a recommended practice is to locate a buffer near the HT91808 device and minimize load capacitance to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

5.6. System Clock

The quality of the system clock can influence dynamic performance, as the HT91808 device operates based on a system clock. Therefore, it may be necessary to consider the system clock duty, jitter, and the time difference between system clock transition and BCK or LRCK transition in slave mode.

5.7. Layout Example

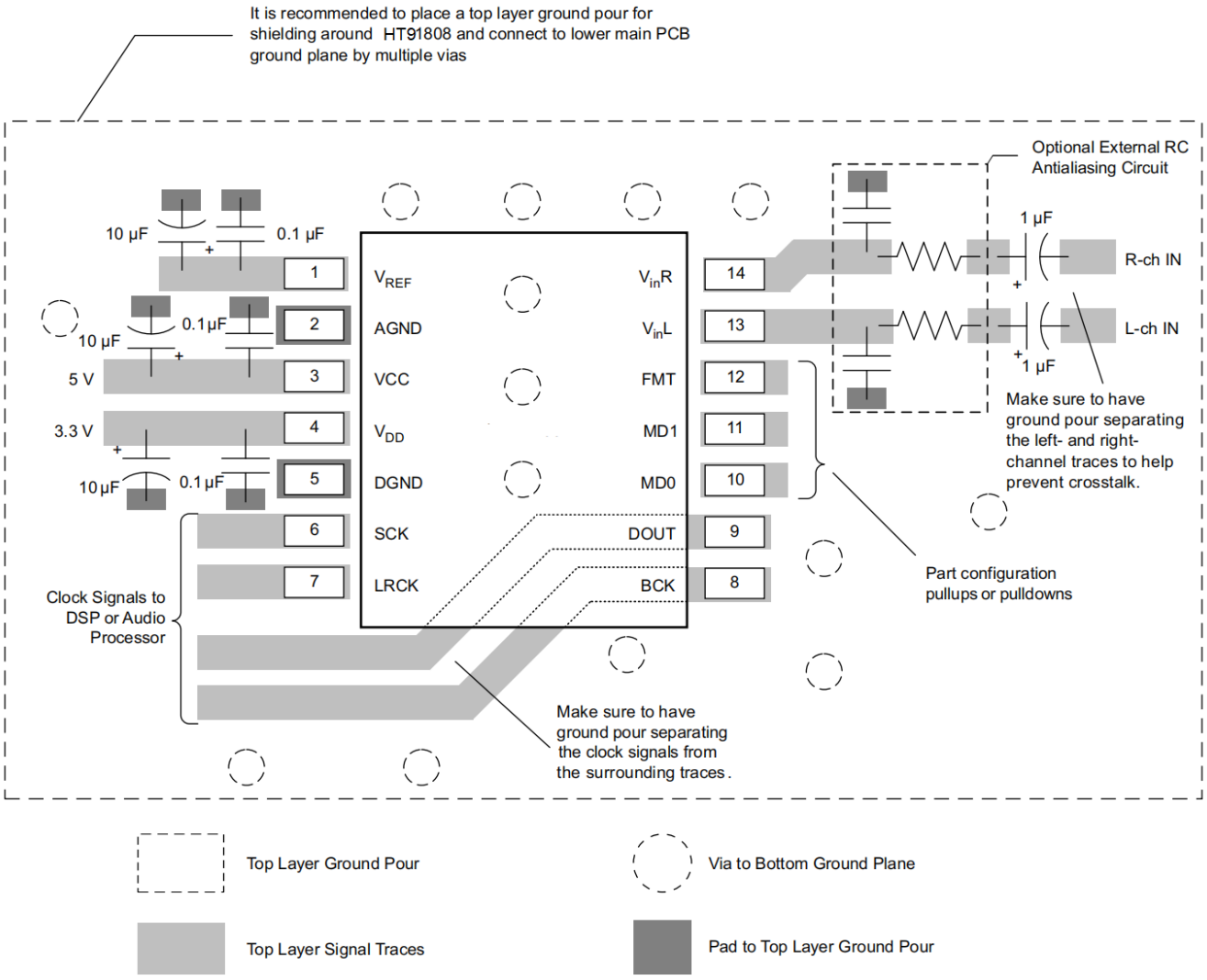
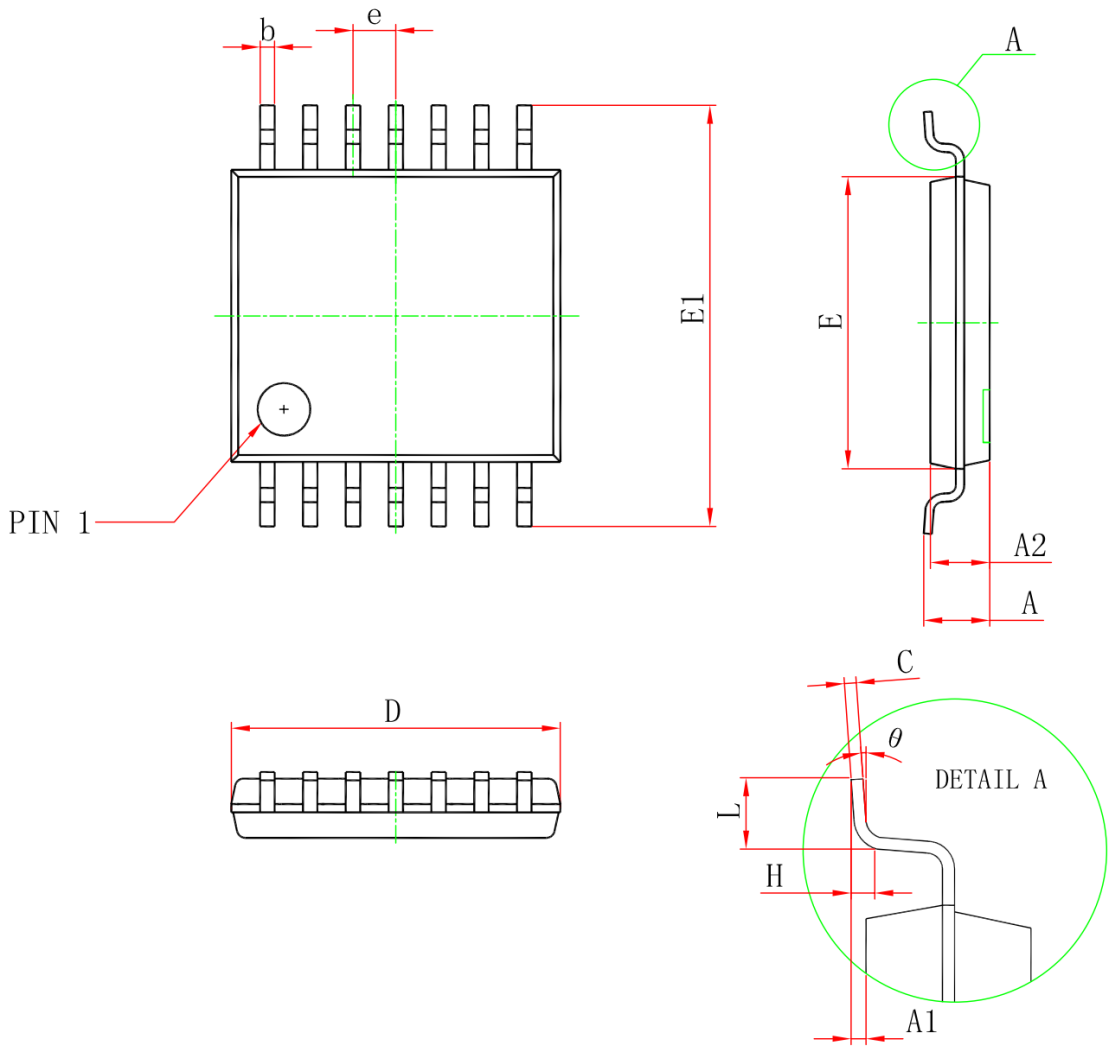


Figure 11 HT91808 Layout Example

■ PACKAGE OUTLINE



Symbol	Dimensions in Millimeters		
	Min.	NOM	Max.
D	4.900	5.000	5.100
E	4.300	4.400	4.500
b	0.200	-	0.280
c	0.130	-	0.170
E1	6.200	6.400	6.600
A			1.200
A2	0.900	1.000	1.050
A1	0.050	-	0.150
e	0.65(BSC)		
L	0.450	0.600	0.750
θ	0°	-	8°

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