Feature

- Logic Operating Voltage:2.4V~5.5V
- Integrated oscillator circuitry
- Bias: 1/2 or 1/3; Duty:1/4
- Internal LCD bias generation with voltage-follower buffers
- External VLCD pin to supply LCD operating voltage
- Support I^2C-bus serial interface
- Selectable LCD Frame Frequencies
- Up to 40×4 bits RAM for display data storage
- Maximum Display patterns: 40×4 patterns - 40 segments and 4 commons
- Versatile blinking modes: off, 0.5Hz, 1Hz, 2Hz
- Write address auto-increment
- Support Power Save Mode for low power consumption
- Manufactured in silicon gate CMOS process
- Package Type: COG and chip

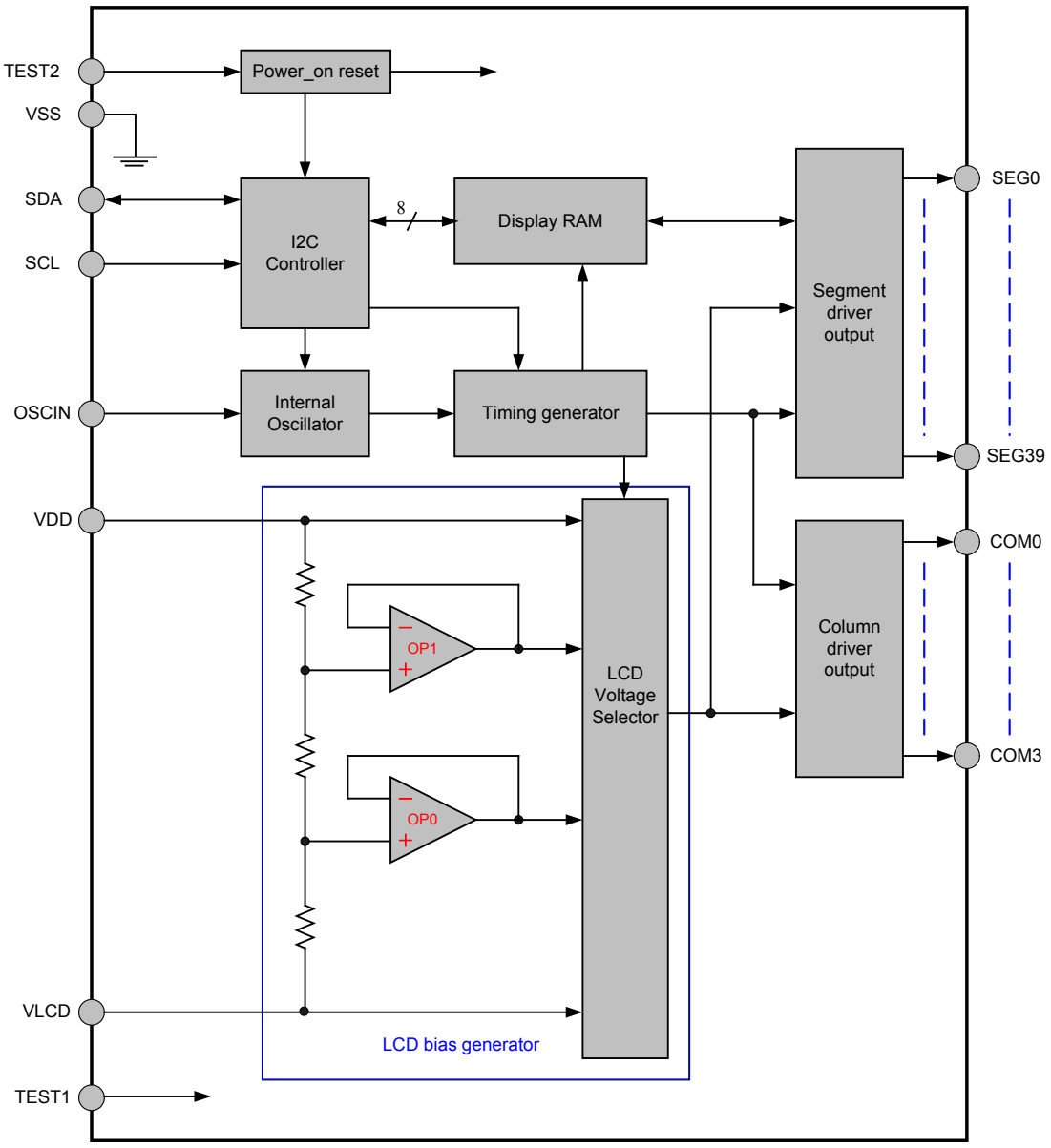
Applications

- Leisure products
- Games
- Telephone display.
- Audio Combo display
- Video Player display
- Kitchen Appliance display
- Measurement equipment display
- Household appliance
- Consumer electronics

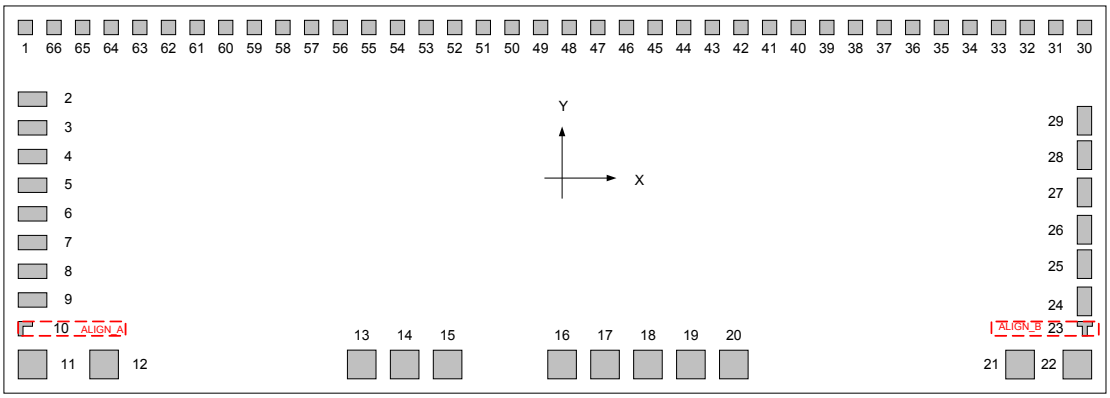
General Description

The device is a memory mapping and multi-function LCD controller driver. The maximum display segments of the device are 160 patterns (40 segments and 4commons) display. The software configuration feature of the HT9B92G device makes it suitable for multiple LCD applications including LCD modules and display subsystems. The device communicates with most microprocessors / microcontrollers via a two-wire bidirectional I^2C-bus interface.

Block Diagram



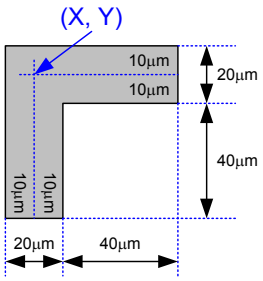
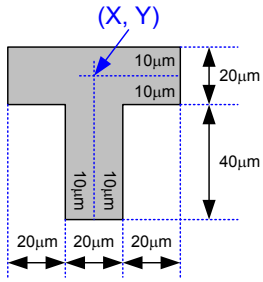
Pad Assignment



Pad Dimensions

Item	Number.		Size		Unit
			X	Y	
Chip size	—		2402	1100	μm
Chip thickness	—		508		μm
Pad pitch	1~9, 30~66		60		μm
	24~29		80		μm
	11~22		85		μm
Bump size	Output pad	2~9	67	47	μm
		31~66	47	67	μm
	Input pad	13~20	74	74	μm
	Dummy pad	11, 12, 21, 22	74	74	μm
		1, 24~30	47	67	μm
Bump height	All pad		18±3		μm

Alignment mark Dimensions

Item	Number	Size	Unit
ALIGN_A	10		μm
ALIGN_B	23		μm

Pad Coordinates

Unit: μm

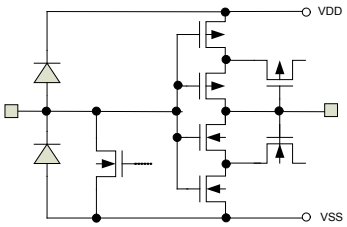
No	Name	X	Y	No	Name	X	Y
1	DUMMY	-1117	455.5	34	SEG3	870.05	455.5
2	SEG36	-1106.5	155.66	35	SEG4	810.05	455.5
3	SEG37	-1106.5	95.66	36	SEG5	750.05	455.5
4	SEG38	-1106.5	35.66	37	SEG6	690.05	455.5
5	SEG39	-1106.5	-24.34	38	SEG7	630.05	455.5
6	COM0	-1106.5	-84.34	39	SEG8	570.05	455.5
7	COM1	-1106.5	-144.34	40	SEG9	510.05	455.5
8	COM2	-1106.5	-204.34	41	SEG10	450.05	455.5
9	COM3	-1106.5	-264.34	42	SEG11	390.05	455.5
10	ALIGN_A	-1124	-340	43	SEG12	330.05	455.5
11	DUMMY	-1104	-452	44	SEG13	270.05	455.5
12	DUMMY	-966.45	-452	45	SEG14	210.05	455.5
13	VLCD	-406.8	-452	46	SEG15	150.05	455.5
14	VDD	-319.8	-452	47	SEG16	90.05	455.5
15	VSS	-234.8	-452	48	SEG17	30.05	455.5
16	TEST1	-12.8	-446.4	49	SEG18	-29.95	455.5
17	OSCIN	72.2	-446.4	50	SEG19	-89.95	455.5
18	SCL	160.9	-446.4	51	SEG20	-149.95	455.5
19	SDA	245.9	-446.4	52	SEG21	-209.95	455.5
20	TEST2	334.6	-446.4	53	SEG22	-269.95	455.5
21	DUMMY	910	-452	54	SEG23	-329.95	455.5
22	DUMMY	1104	-452	55	SEG24	-389.95	455.5
23	ALIGN_B	1104	-340	56	SEG25	-449.95	455.5
24	DUMMY	1117	-278.292	57	SEG26	-509.95	455.5
25	DUMMY	1117	-198.292	58	SEG27	-569.95	455.5
26	DUMMY	1117	-118.292	59	SEG28	-629.95	455.5
27	DUMMY	1117	-38.292	60	SEG29	-689.95	455.5
28	DUMMY	1117	41.708	61	SEG30	-749.95	455.5
29	DUMMY	1117	121.708	62	SEG31	-809.95	455.5
30	DUMMY	1117	455.5	63	SEG32	-869.95	455.5
31	SEG0	1050.05	455.5	64	SEG33	-929.95	455.5
32	SEG1	990.05	455.5	65	SEG34	-989.95	455.5
33	SEG2	930.05	455.5	66	SEG35	-1049.95	455.5

Pad Description

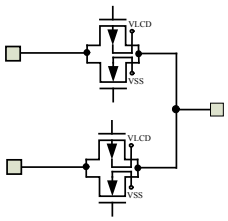
Pin Name	Type	Description
SDA	I/O	Serial Data Input/Output pin Serial Data (SDA) Input/Output for 2-wire I^2C interface is an NMOS open drain structure.
SCL	I	Serial Clock Input pin Serial Data (SCL) is a clock input for 2-wire I^2C interface.
OSCIN	I	External Clock Input pin The external and internal clock mode can be selected by the command. When the internal oscillator circuitry is used, this pin must be connected to V_{SS}.
TEST1	I	Test mode input pin When this pin is connected to V_{DD}, the device will enter the test mode.
TEST2	I	Power on reset control pin The internal power on reset circuitry will be enabled if this pin is connected to V_{SS}. If this pin is connected to V_{DD}, the internal power on reset circuitry will be disabled and the reset function will be performed by executing the software reset command.
COM0~COM3	O	LCD Common outputs.
SEG0~SEG39	O	LCD Segment outputs.
VDD	—	Positive power supply.
VSS	—	Negative power supply, ground.
VLCD	—	LCD power supply pin

Approximate Internal Connections

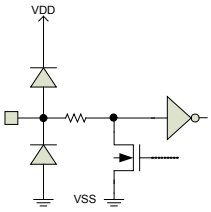
SCL, SDA (for Schmitt trigger type)



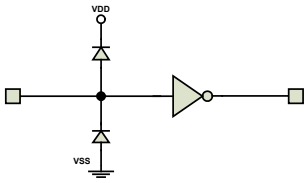
COM0~COM3; SEG0~SEG39



OSCIN



TEST1, TEST2



Absolute Maximum Ratings

SupplyVoltage ..... V_{SS}-0.3V to V_{DD}+6.5V
Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V
Storage Temperature ..... -55°C to 150°C
Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{SS} = 0V; V_{DD} =2.4V to 5.5V; Ta = -40 to +85°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
V_{LCD}	LCD Operating Voltage	—	—	0	—	V_{DD}-2.4	V
V_{IH}	Input High Voltage	—	SCL, SDA, TEST1, TEST2	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input Low Voltage	—	SCL, SDA, TEST1, TEST2	0	—	0.3V_{DD}	V
I_{IL}	Input Leakage Current	—	V_{IN} = V_{SS} or V_{DD}	−1	—	1	μA
I_{OL}	Low Level Output Current	3.3V	V_{OL}=0.4V for SDA pin	6	—	—	mA
		5.0V		9	—	—	mA
I_{DD}	Operating Current	3.3V	No load, 1/3bias, B type inversion, Ta=25°C, LCD display on, f_{LCD}=80Hz, V_{LCD} pin is connected to V_{SS}, Power save mode = Low Current2 mode	—	7.5	15	μA
		5.0V		—	12	20	μA
I_{STB1}	Standby Current	3.3V	No load, 1/3bias, B type inversion, Ta = 25°C, LCD display off, f_{LCD}=80Hz, VLCD pin is connected to V_{SS}, Power save mode = Low Current2 mode	—	—	1	μA
		5.0V		—	—	2	μA
R_{PL}	Pull-Low Resistance	3.3V	For OSCIN pin	2	4	6.5	kΩ
		5.0V		1.5	3	4.5	
I_{OL1}	LCD Common Sink Current	—	V_{DD}-V_{LCD}=3.30V, V_{OL}=0.33V	250	400	—	μA
			V_{DD}-V_{LCD}=5.00V, V_{OL}=0.50V	500	800	—	μA
I_{OH1}	LCD Common Source Current	—	V_{DD}-V_{LCD}=3.30V, V_{OH}=2.97V	−140	−230	—	μA
			V_{DD}-V_{LCD}=5.00V, V_{OH}=4.50V	−300	−500	—	μA
I_{OL2}	LCD Segment Sink Current	—	V_{DD}-V_{LCD}=3.30V, V_{OL}=0.33V	250	400	—	μA
			V_{DD}-V_{LCD}=5.00V, V_{OL}=0.50V	500	800	—	μA
I_{OH2}	LCD Segment Source Current	—	V_{DD}-V_{LCD}=3.30V, V_{OH}=2.97V	−140	−230	—	μA
			V_{DD}-V_{LCD}=5.00V, V_{OH}=4.50V	−300	−500	—	μA

A.C. Characteristics

Ta=-40 to +85°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
f_{LCD1}	LCD Frame Frequency	3.3V	Ta=25°C, internal oscillator is used, Display control command: P[4:3]="00"	72.0	80.0	88.0	Hz
			Ta=25°C, internal oscillator is used, Display control command: P[4:3]="01"	63.9	71.0	78.1	
			Ta=25°C, internal oscillator is used, Display control command: P[4:3]="10"	57.6	64.0	70.4	
			Ta=25°C, internal oscillator is used, Display control command: P[4:3]="11"	47.7	53.0	58.3	
f_{LCD2}	LCD Frame Frequency	2.4V ~ 5.5V	Ta=-40 to 85°C, internal oscillator is used, Display control command: P[4:3]="00"	56.0	80.0	104.0	Hz
			Ta=-40 to 85°C, internal oscillator is used, Display control command: P[4:3]="01"	49.7	71.0	92.3	
			Ta=-40 to 85°C, internal oscillator is used, Display control command: P[4:3]="10"	44.8	64.0	83.2	
			Ta=-40 to 85°C, internal oscillator is used, Display control command: P[4:3]="11"	37.1	53.0	68.9	
t_{SR}	VDD Slew Rate	—	—	0.05	—	—	V/ms
t_{POF}	VDD OFF Times	—	VDD drop down to 0.9V	10	—	—	ms
t_{RSOFF}	Wait Time for Data Transfers	—	2-wire I²C-bus	1	—	—	ms

Note: $f_{LCD}=1/t_{LCD}$

I²C Interface Characteristics

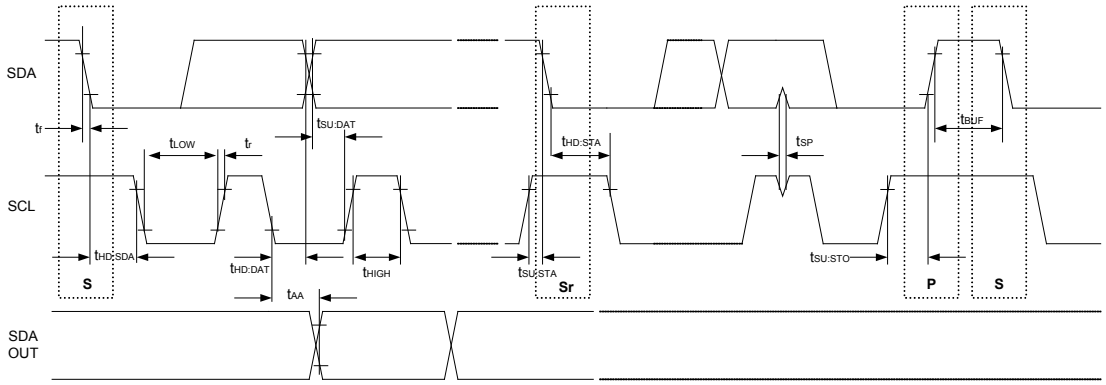
Unless otherwise specified, V_{SS}=0V; V_{DD}=2.4V~5.5V; Ta=-40 to +85°C

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCL}	Clock frequency	—	—	400	kHz
t_{BUF}	bus free time	Time in which the bus must be free before a new transmission can start	1.3	—	μs
$t_{HD:\,STA}$	Start condition hold time	After this period, the first clock pulse is generated	0.6	—	μs
t_{LOW}	SCL Low time	—	1.3	—	μs
t_{HIGH}	SCL High time	—	0.6	—	μs
$t_{SU:\,STA}$	Start condition setup time	Only relevant for repeated START condition	0.6	—	μs
$t_{HD:\,DAT}$	Data hold time	—	0	—	ns
$t_{SU:\,DAT}$	Data setup time	—	100	—	ns
t_R	SDA and SCL rise time	Note	—	0.3	μs
t_F	SDA and SCL fall time	Note	—	0.3	μs
$t_{SU:\,STO}$	Stop condition set-up time	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	50	ns

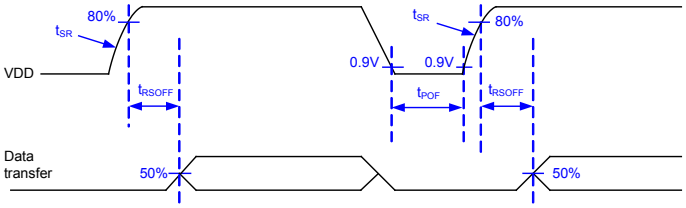
Note: These parameters are periodically sampled but not 100% tested.

Timing Diagrams

I²C Timing



Power On Reset Timing



Note: 1. If the conditions of Reset timing are not satisfied in power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.

2. If the V_{DD} drops lower than the minimum operating voltage during operating, the conditions of Power on Reset timing must also be satisfied. That is the V_{DD} drop to 0.9V and keep at 0.9V for 10ms (min.) before rising to the normal operating voltage.

3. Data transfers on the I²C serial bus should at least be delayed for 1ms after the power-on sequence to ensure that the reset operation is complete.

4. If it is difficult to meet the power on reset timing specifications, users can execute the software reset command after power-on.

Functional Description

Power-On Reset

When the power is applied, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common outputs are set to V_{SS}.
- All segment outputs are set to V_{SS}.
- LCD Driver Output Waveform: A-type inversion.
- Internal oscillator is selected.
- The 1/3 bias drive mode is selected.
- LCD bias generator is in an off state.
- LCD Display and internal oscillator are in off states.
- Power save mode is set to normal current.
- Frame Frequency is set to 80Hz.
- Blinking function is switched off.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

System Oscillator

The timing for the internal logic and the LCD drive signals are generated by the internal oscillator or external clock source input. The System Clock frequency (f_{SYS}) determines the LCD frame frequency. During initial system power on the System Oscillator will be in the stop state.

Segment Driver Outputs

The LCD drive section includes up to 40 segment outputs SEG0~SEG39 which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed common signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit.

Column Driver Outputs

The LCD drive section includes 4 column outputs COM0~COM3 which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit if less than 4 column outputs are required.

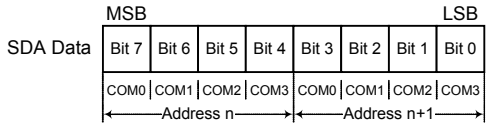
Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the Display Data Input command.

Display Memory – RAM Structure

The display RAM is static 40×4 bits RAM which stores the LCD data. Logic "1" in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly, logic 0 indicates the "off" state.

The contents of the RAM data are directly mapped to the LCD data. The first RAM column corresponds to the segments operated with respect to COM0. In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with COM1, COM2 and COM3 respectively. The following diagram is a data transfer format for I²C interface.



LCD Display Output Data Transfer Format for I²C bus

Address	COM0	COM1	COM2	COM3	Output
00H					SEG0
01H					SEG1
02H					SEG2
03H					SEG3
04H					SEG4
05H					SEG5
06H					SEG6
07H					SEG7
08H					SEG8
09H					SEG9
0AH					SEG10
0BH					SEG11
0CH					SEG12
0DH					SEG13
0EH					SEG14
0FH					SEG15
10H					SEG16
11H					SEG17
12H					SEG18
13H					SEG19
14H					SEG20
15H					SEG21
16H					SEG22
17H					SEG23
18H					SEG24
19H					SEG25
1AH					SEG26
1BH					SEG27
1CH					SEG28
1DH					SEG29
1EH					SEG30
1FH					SEG31
20H					SEG32
21H					SEG33
22H					SEG34
23H					SEG35
24H					SEG36
25H					SEG37
26H					SEG38
27H					SEG39
RAM Data	Bit 3	Bit 2	Bit 1	Bit 0	

Note: 1. The LCD display RAM address is specified by the Address Set command and the address will be automatically incremented by one after a 4-bit data is shifted in.

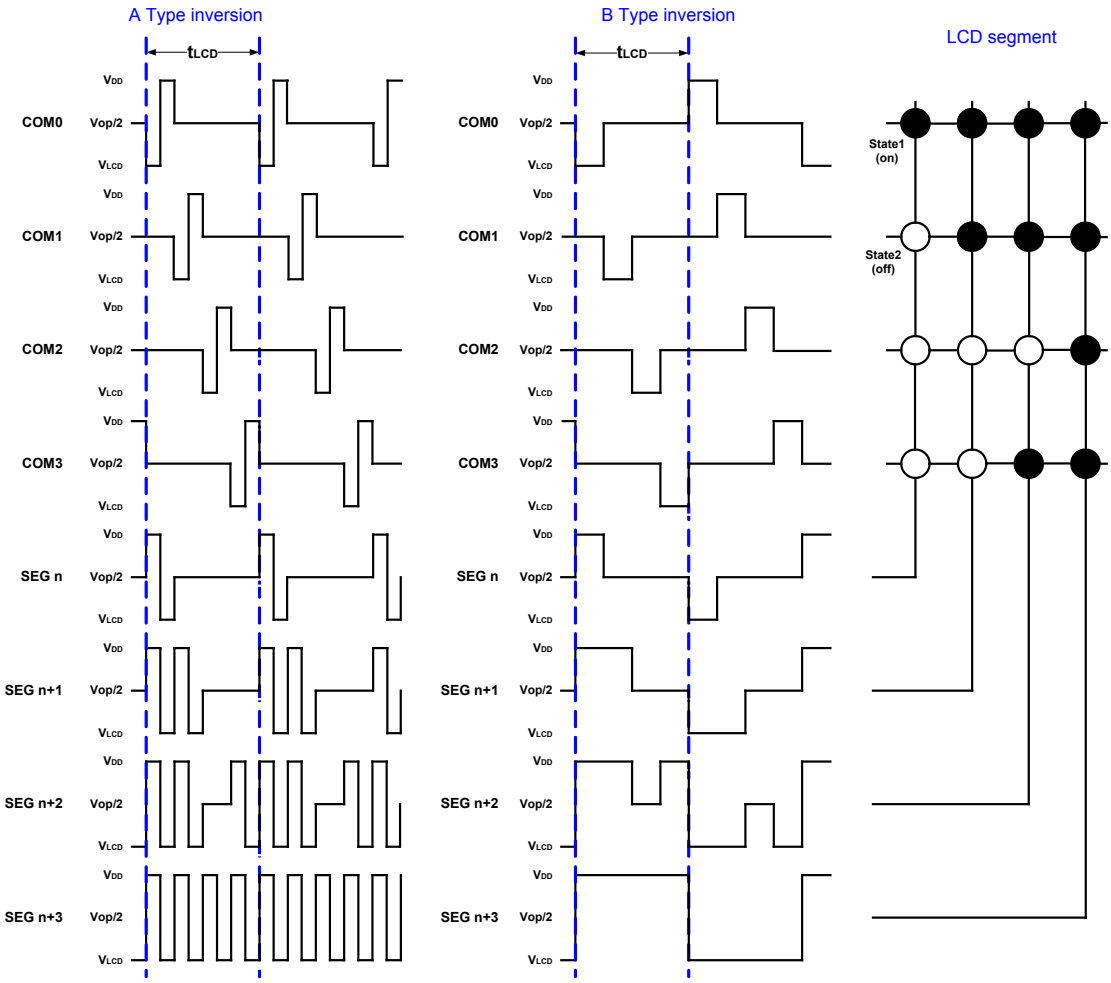
2. The address of the display RAM data is from 00H to 27H.

LCD Bias Generator

Fractional LCD biasing voltages, known as 1/2 or 1/3 bias voltage, are obtained from an internal voltage divider of three series resistors connected between V_{LCD} and V_{DD}. The centre resistor can be switched out of circuits to provide a 1/2 bias voltage level configuration.

LCD Drive Mode Waveforms

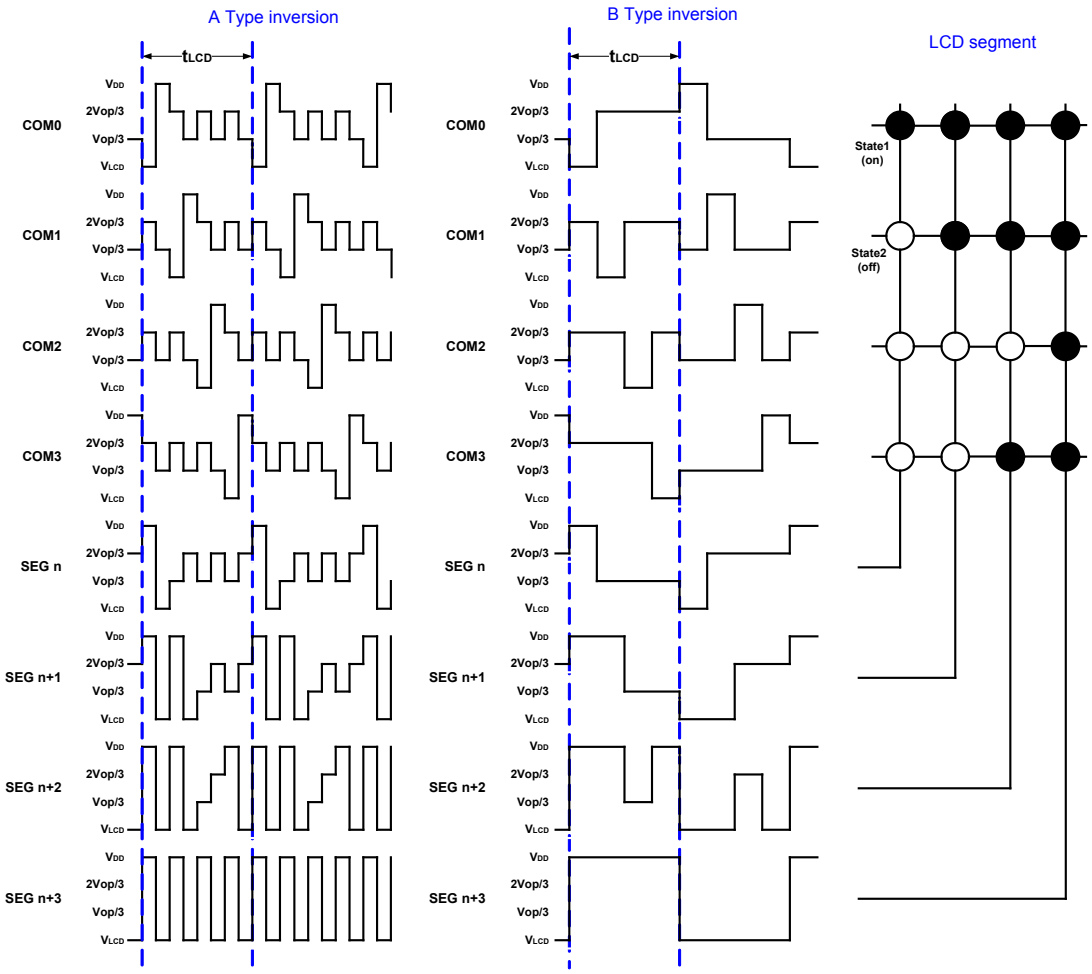
- When the LCD drive mode is selected as 1/4 duty and 1/2 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/4 duty drive mode with 1/2 bias ($V_{OP}=V_{DD}-V_{LCD}$)

Note: $t_{LCD}=1/f_{LCD}$

• When the LCD drive mode is selected as 1/4 duty and 1/3bias, the waveform and LCD display is shown as follows:



Waveforms for 1/4 duty drive mode with 1/2 bias (V_{OP}=V_{DD}-V_{LCD})

Note: t_{LCD}=1/f_{LCD}

Blinking Function

The device contains versatile blinking capabilities. The whole display can be blinked at frequencies selected by the Blinking Frequency command. The blinking frequency is a subdivided ratio of the system frequency. The ratio between the system oscillator and blinking frequencies depends on the blinking mode in which the device is operating, as shown in the following table:

Blinking Mode	Blinking frequency (Hz)
0	Blink off
1	0.5
2	1
3	2

Frame Frequency

The device provides four frame frequencies selected with the Frame Frequency command known as 80Hz, 71Hz, 64Hz and 53Hz respectively.

Mode	Frame frequency (Hz) @ V_{DD}=3.3V
0	80
1	71
2	64
3	53

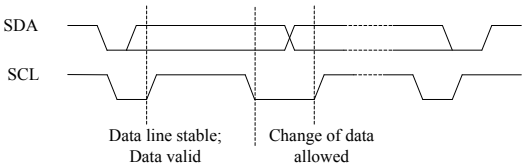
I²C Serial Interface

I²C Operation

The device supports I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors. When the bus is free, both lines are high. Devices connected to the bus must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

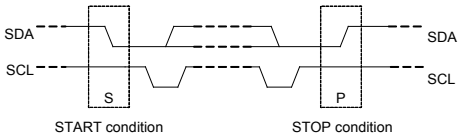
Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only change when the clock signal on the SCL line is Low as shown in the diagram.



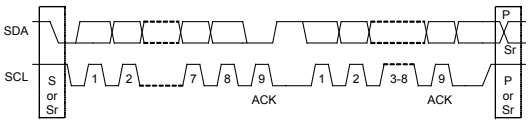
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START(S) and repeated START (Sr) conditions are functionally identical.



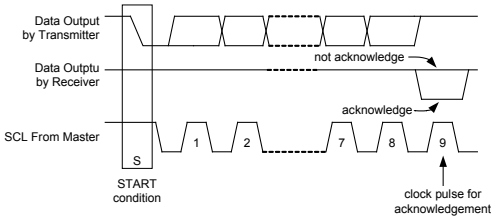
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.



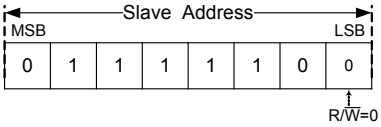
Acknowledge

- Each bytes of eight bits is followed by one acknowledge bit. This Acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an Acknowledge, ACK, after the reception of each byte.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Slave Addressing

- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. This device only supports the write operation and therefore, the eighth data bit, R/$\overline{W}$, which is used to define a read or write operation will be fixed at a "0" state. If the R/$\overline{W}$ bit is set to 1 to execute a read operation, it will result in no operation.
- The device address bits are "0111110". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.



I²C Interface Write Operation

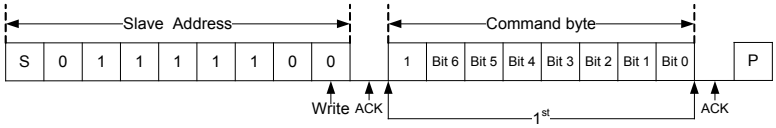
Byte Write Operation

- Single Command Type
  A Single Command write operation requires a START condition, a slave address with a write control bit, a command byte and a STOP condition for a single command write operation.
- Compound Command Type
  A Compound Command write operation requires a START condition, a slave address with a write control bit, a command byte, up to two command setting bytes and a STOP condition for a compound command write operation.
- Display RAM Single Data Byte
  A display RAM data byte write operation requires a START condition, a slave address with a write control bit, a valid Register Address byte, a Data byte and a STOP condition.

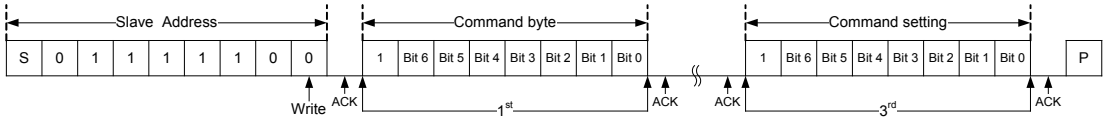
  The start address can only be set from 00H to 1FH. The start address which is greater than 1FH will be regarded as a command. Therefore, it is recommended that the start address should be set from 00H to 1FH.

Display RAM Page Write Operation

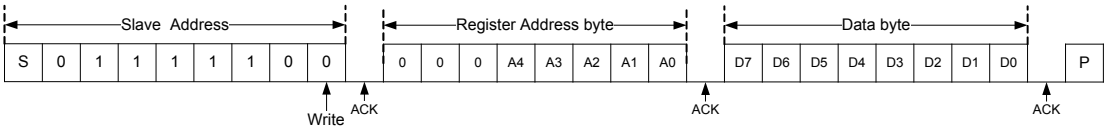
After a START condition the slave address with a write control bit is placed on the bus followed with the specified display RAM Register Address of which the contents are written into the internal address pointer. The data to be written into the memory will be transmitted next. The internal address pointer will be incremented by 1 after a 4-bit data is shifted in. Then the acknowledge clock pulse will be received after an 8-bit data is shifted. After the internal address point reaches the maximum memory address, 27H, the address pointer will be reset to 00H. It is strongly recommended to write the display RAM data from address 00H to 27H using the Display RAM Page Write Operation.



I²C Single Command Type Write Operation



I²C Compound Command Type Write Operation

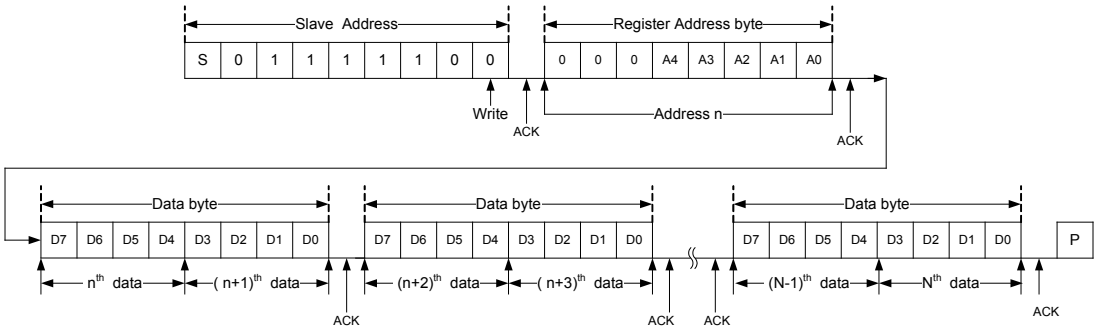


I²C Display RAM Single Data Byte Write Operation

Command Summary

The bit 7 denoted as "C" here is the control bit which is used to determine that the next byte is the display RAM data or command byte.

C bit	Remark
0	Next byte is Display RAM data.
1	Next byte is command.



I²C Interface N Bytes Display RAM Data Write Operation

Display RAM Address Setting Command

This command is used to define the start address of the display RAM.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Address Pointer	C	0	0	A4	A3	A2	A1	A0	Display RAM memory start address

Note: 1. The address ranges from 00H to 1FH.
2. It is strongly recommended to write the display RAM data from address 00H to 27H at one time.
3. Power on status: the address will be set to 00H.
4. If the programmed command is not defined, the function will not be affected.

Drive Mode Setting Command

This command is used to control the LCD bias and display on/off.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Bias and Display on/off setting	C	1	0	X	P3	P2	X	X	—

Note:

P2	Bias
0	1/3 bias (default)
1	1/2 bias

P3	LCD Display On/Off
0	Off (default)
1	On

- Power on status: The 1/3 bias drive mode is selected and the LCD display is switched off.
- If the programmed command is not defined, the function will not be affected.

Display Control Command

This command is used to select the Current mode according to the characteristics of the LCD panel for achieving high display quality and LCD driver output waveform set and frame frequency select.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Display Control Setting	C	0	1	P4	P3	P2	P1	P0	—

Note:

P [1:0]	Power Save Mode	Current Consumption	Remark
00	Low Current2 Mode	x 0.5	• The data listed here is for reference only. The actual data depends upon the panel load. • Please meet the condition: $V_{DD}-V_{LCD}\geq 3V$ when used in High current mode.
01	Low Current1 Mode	x 0.67	
10	Normal Current Mode	x 1 (default)	
11	High Current Mode	x 1.8	

P2	LCD Driver Output Waveform	Remark
0	A Type inversion (default)	
1	B Type inversion	

P [4:3]	Frame Frequency @V_{DD}=3.3V (Hz)	Remark
00	80 (default)	• The data listed here is for reference only. The actual data depends upon the panel load. • Please meet the condition: $V_{DD}-V_{LCD}\geq 3V$ when used in High current mode.
01	71	
10	64	
11	53	

- The setting of the frame frequency, LCD output waveform and current mode will influence the display image qualities. Please select a proper display setting suitable for the current consumption and display image quality with LCD panel.

Mode	Flicker	Image Quality/Contrast
Frame Frequency	O	
LCD Driver Output Waveform	O	O
Power Save Mode		O

- If the programmed command is not defined, the function will not be affected.

Software Reset and Oscillator Mode Setting Command

This command is used to select the system oscillator source and to initiate a software reset.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
System Oscillator Setting and Software Reset	C	1	1	0	1	X	P1	P0	—

P1	Software Reset	Remark
0	No Operation (default)	When a "Software Reset" is executed, the device will be reset to an initial condition. Other settings can be configured after Software reset is completed.
1	Initiate a Software Reset	

P0	Oscillator Mode	Remark
0	Internal Oscillator (default)	● When the internal oscillator is used, the OSCIN pin must be connected to V_{SS} or open-circuit. ● When the external clock mode is selected, the external clock is supplied on the OSCIN pin.
1	External Clock Input Mode	

When the software reset is executed, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common outputs are set to V_{SS}.
- All segment outputs are set to V_{SS}.
- LCD Driver Output Waveform: A-type inversion.
- Internal oscillator source is selected.
- 1/3 bias is selected.
- LCD bias generator is off state.
- LCD Display and system oscillation are off state.
- Power save mode is set to normal current.
- Frame Frequency is set to 80Hz.
- Blinking function is switched off.

Note that if the programmed command is not defined, the function will not be affected.

Blinking Frequency Setting Command

This command defines the blinking frequency of the display modes.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Blinking Frequency setting	C	1	1	1	0	X	P1	P0	—

Note:

P [1:0]	Blinking Frequency	Remark
00	Blinking off (default)	—
01	0.5 Hz	
10	1 Hz	
11	2 Hz	

- Power on status: Blinking function is switched off.
- If the programmed command is not defined, the function will not be affected.

All Pixels On/Off Setting Command

This command controls that all pixels are switched on or off when the LCD normally displays.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
All Pixels On/Off setting	C	1	1	1	1	1	P1	P0	—

Note:

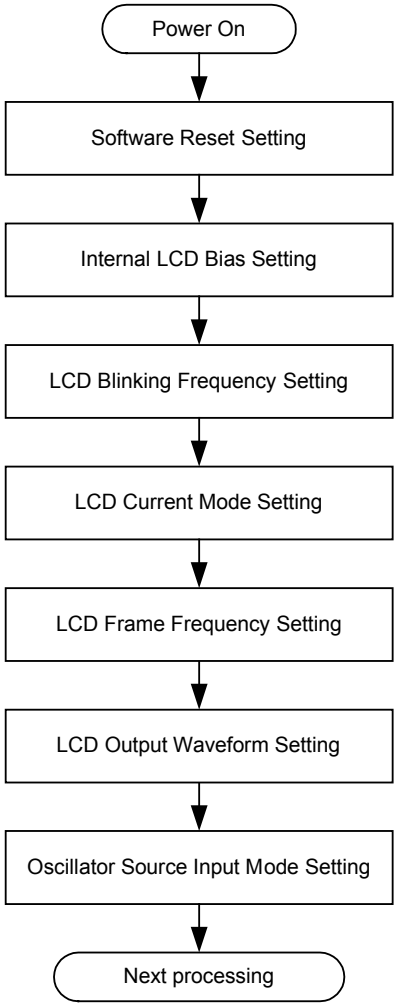
P [1:0]	Blinking Frequency	Remark
00	Normal Display (default)	● This command is only available when the LCD is normally displayed. The display RAM contents will not be changed when this command is executed. ● All pixels are switched on or off regardless of the display RAM data when the relevant setting is selected.
01	All Pixels Off	
10	All Pixels On	
11	All Pixels Off	

● Power on status: Normal display.
● If the programmed command is not defined, the function will not be affected.

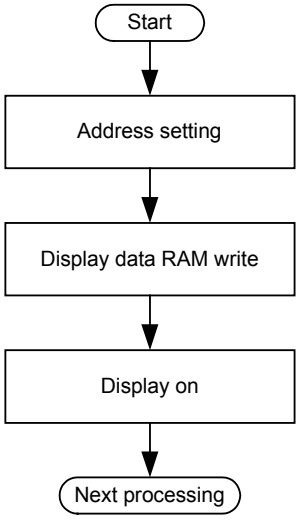
Operation Flow Chart

Access procedures are illustrated below using flowcharts.

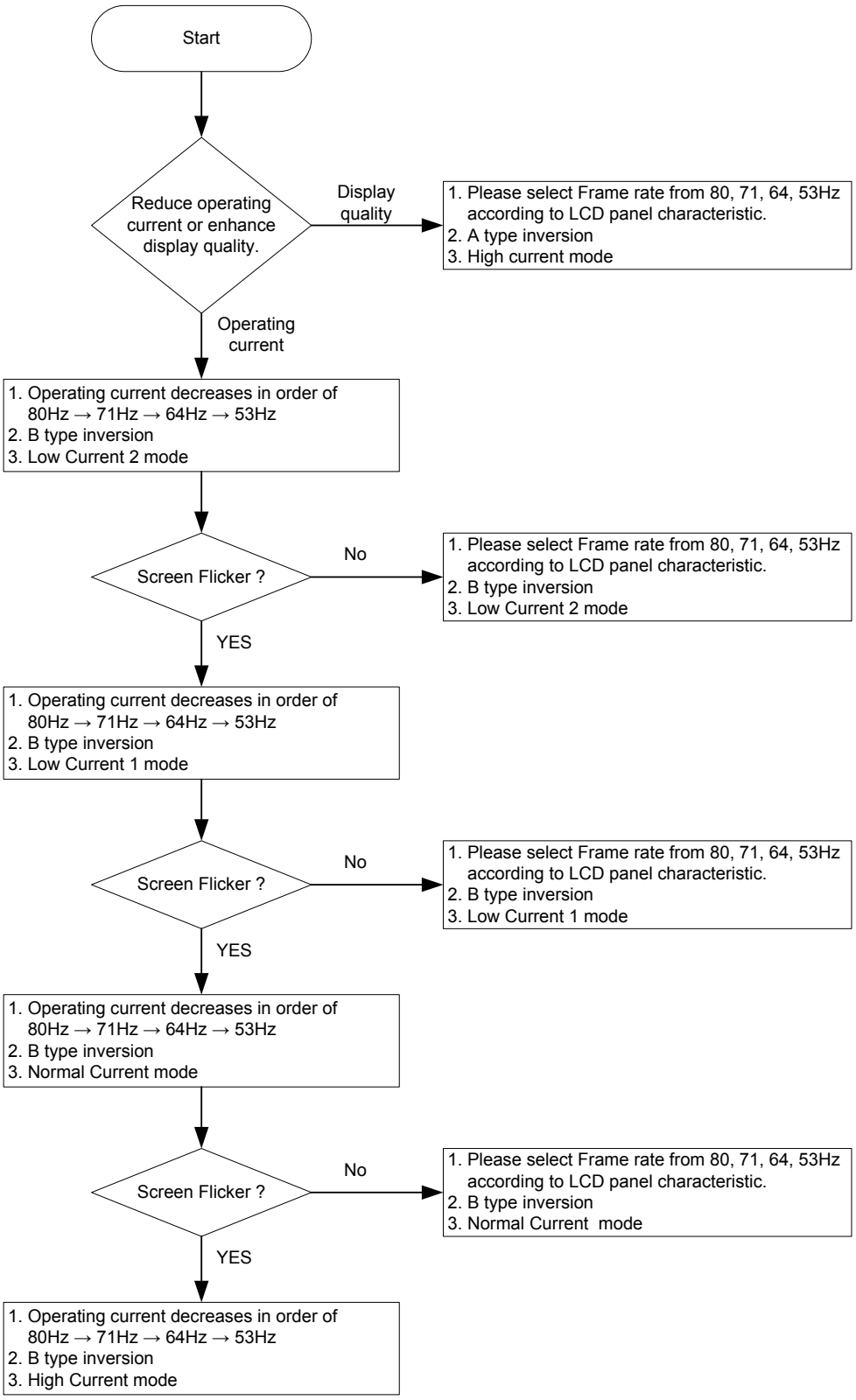
Initialization



Display Data Write (Address Setting)



Display Quality or Operating Current (Power Save Mode) Setting



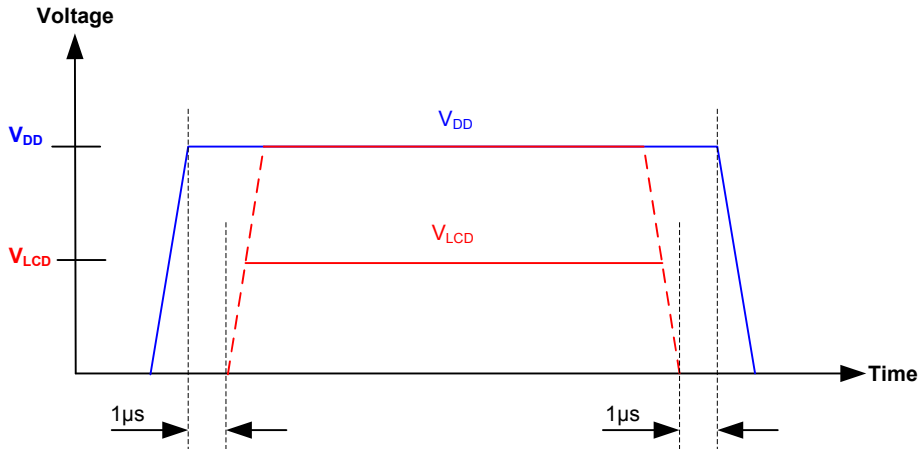
Power Supply Sequence

- If the power is individually supplied on the LCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

Holtek Power Supply Sequence Requirement:

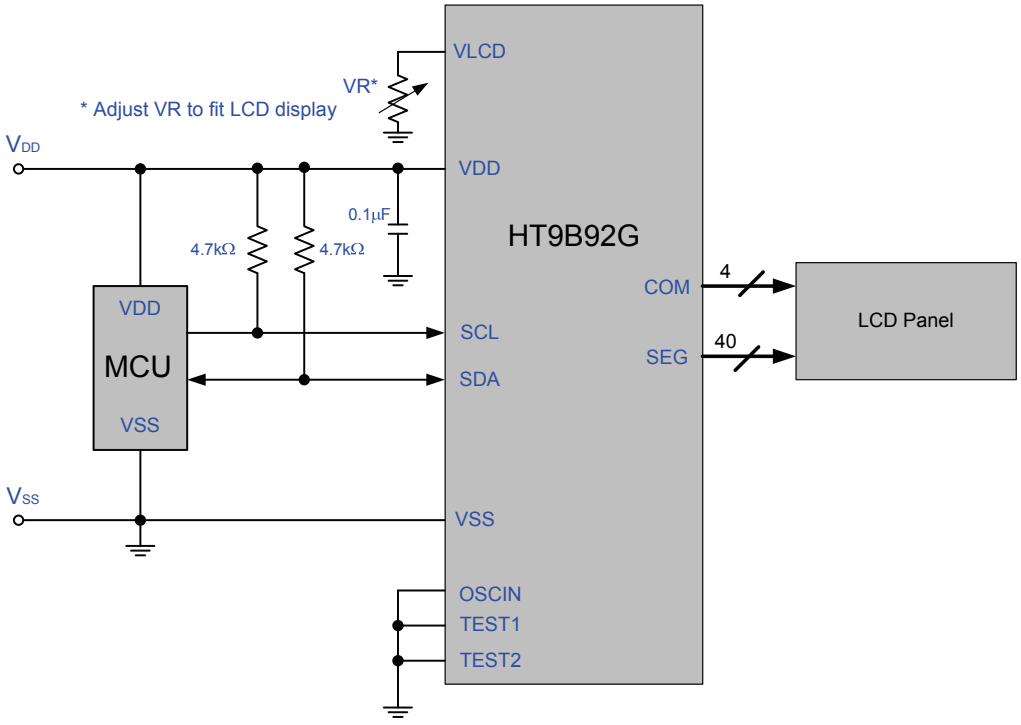
1. Power-on sequence:
   Turn on the logic power supply V_{DD} first and then turn on the LCD driver power supply V_{LCD}.
2. Power-off sequence:
   Turn off the LCD driver power supply V_{LCD}. First and then turn off the logic power supply V_{DD}.
3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the V_{LCD} voltage is higher than the V_{DD} voltage.

- When the V_{LCD} voltage is smaller than or is equal to V_{DD} voltage application



Application Circuit

Internal Oscillator Circuit Mode



External Clock Input Mode