100V P-Ch Power MOSFET

V_{DS}		-100	V
$R_{DS(on),typ}$	V_{GS}=10V	105	mΩ
$I_{D\ (Sillicon\ Limited)}$		-22	A

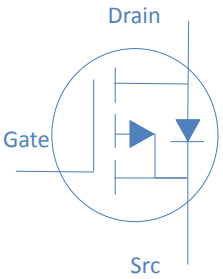
Feature

- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

Application

- ◇ Load Switches
- ◇ Hard Switching and High Speed Circuit
- ◇ BLDC Motor

TO-220F



Part Number	Package	Marking
HTA1K2P10	TO-220F	TA1K2P10

Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	-22	A
		T_C=100℃	-15	
Drain to Source Voltage	V_{DS}	-	-100	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	-75	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25℃	22.5	mJ
Power Dissipation	P_D	T_C=25℃	38	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	62.5	℃/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	3.3	℃/W

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250μA	-100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=-250μA	-1.5	-2.5	-4.0	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=-80V, T_j=25℃	-	-	-1	μA
		V_{GS}=0V, V_{DS}=-70V, T_j=125℃	-	-	-25	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-11A	-	105	120	mΩ
Transconductance	g_{fs}	V_{DS}=-5V, I_D=-11A	-	8	-	S
Gate Resistance	R_G	V_{GS}=15mV, V_{DS}=0V, f=1MHz	-	4.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-25V, f=1MHz	-	3522	-	pF
Output Capacitance	C_{oss}		-	130	-	
Reverse Transfer Capacitance	C_{rss}		-	114	-	
Total Gate Charge	Q_g	V_{DD}=-80V, I_D=-11A, V_{GS}=-10V	-	58	-	nC
Gate to Source Charge	Q_{gs}		-	13.8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	10.5	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=-10V, I_D=-1A, V_{GS}=-10V, R_G=6Ω,	-	15	-	ns
Rise time	t_r		-	67	-	
Turn off Delay Time	$t_{d(off)}$		-	50	-	
Fall Time	t_f		-	50	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=-22A	-		1.3	V
Reverse Recovery Time	t_{rr}	I_F=-5A, dI_F/dt=100A/μs	-	150	-	ns
Reverse Recovery Charge	Q_{rr}		-	830	-	nC

Fig 1. Typical Output Characteristics

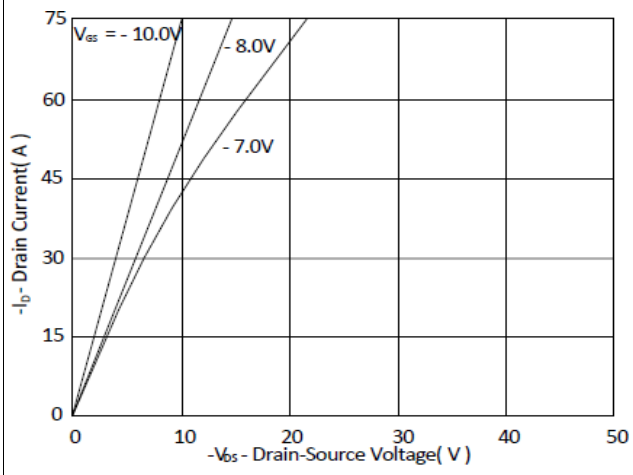


Figure 2. On-Resistance vs. Gate-Source Voltage

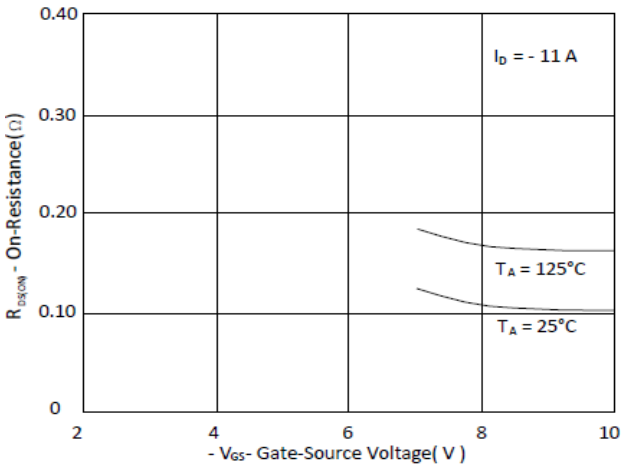


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

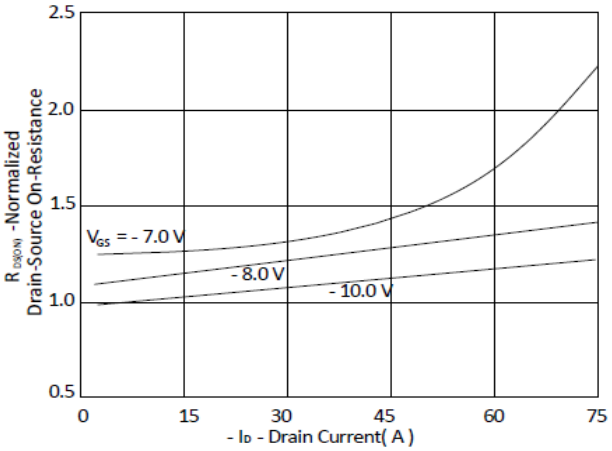


Figure 4. Normalized On-Resistance vs. Junction Temperature

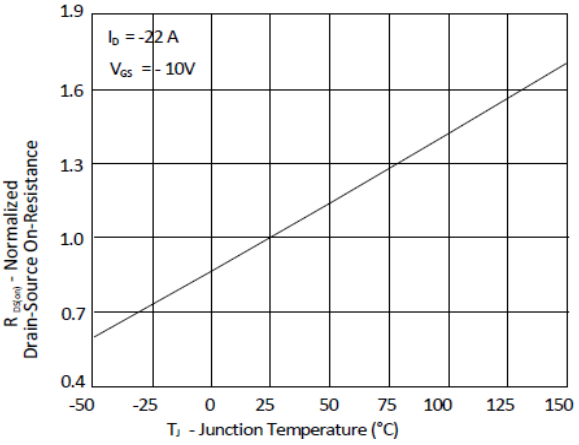


Figure 5. Typical Transfer Characteristics

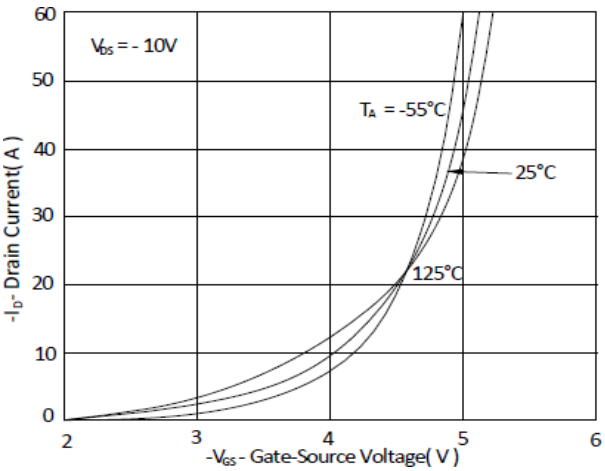


Figure 6. Typical Source-Drain Diode Forward Voltage

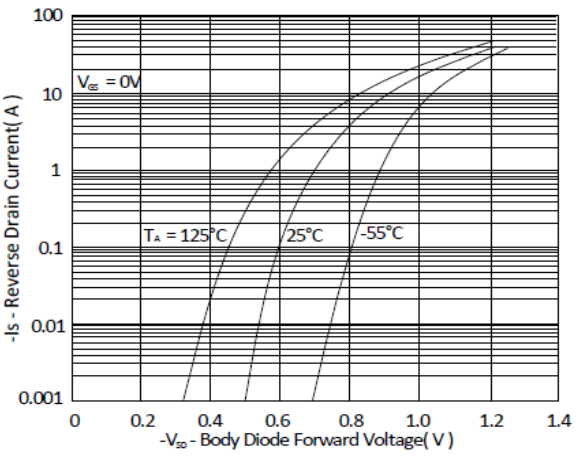


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

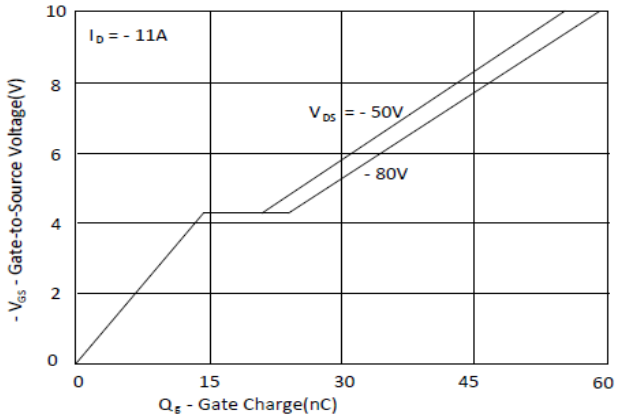


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

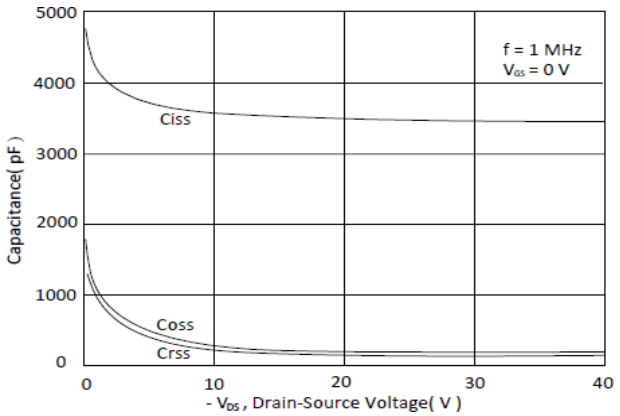


Figure 9. Maximum Safe Operating Area

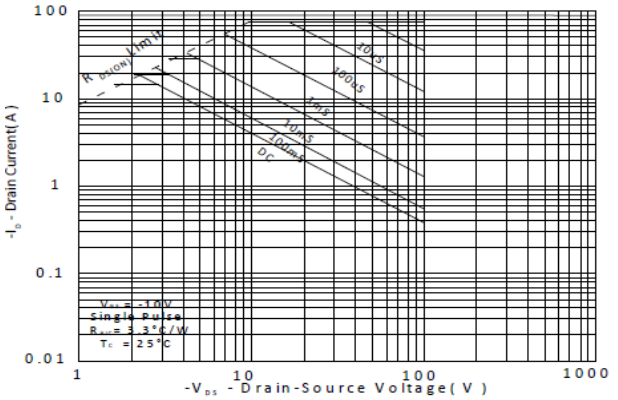


Figure 10. Single Pulse Maximum Power Dissipation

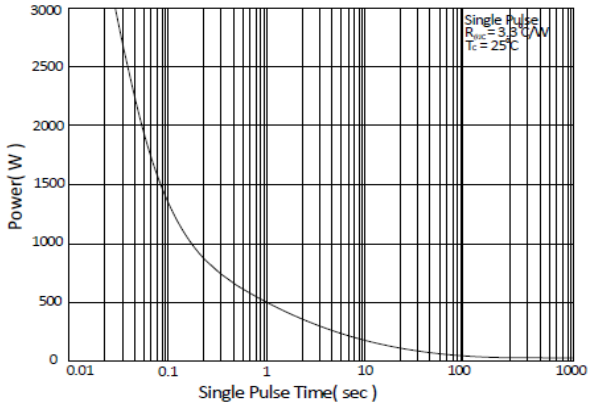
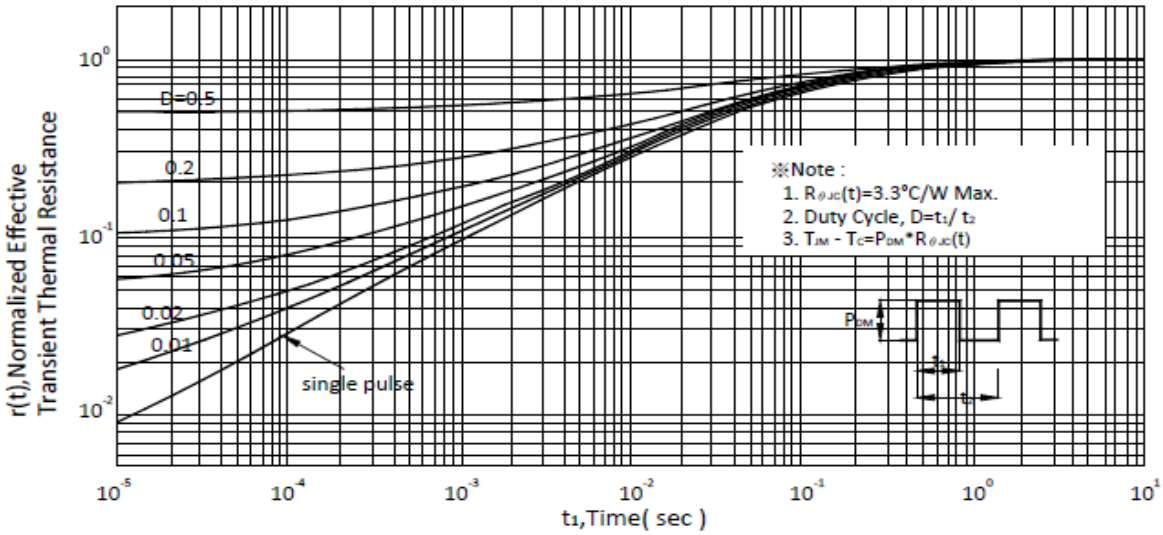
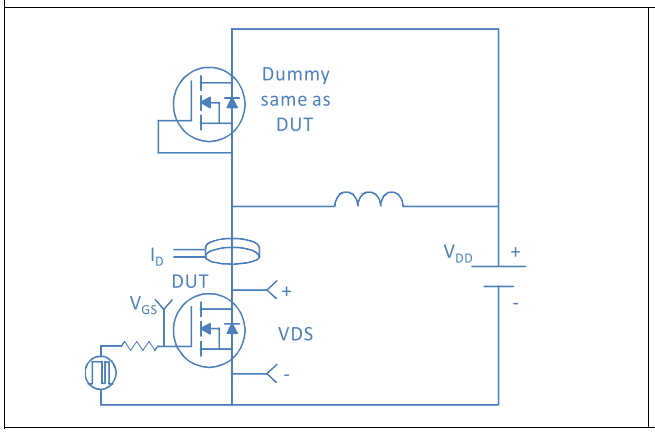
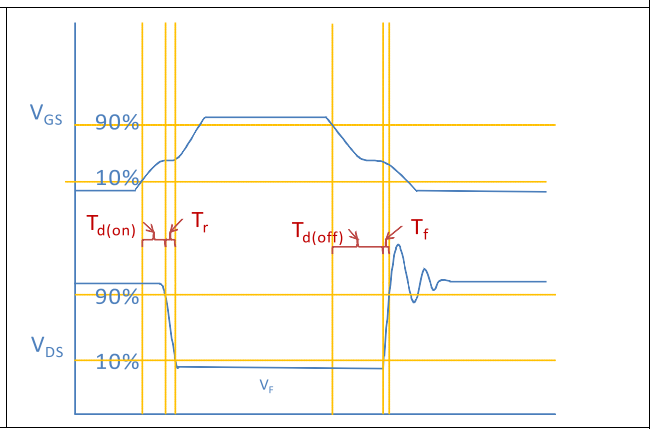


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

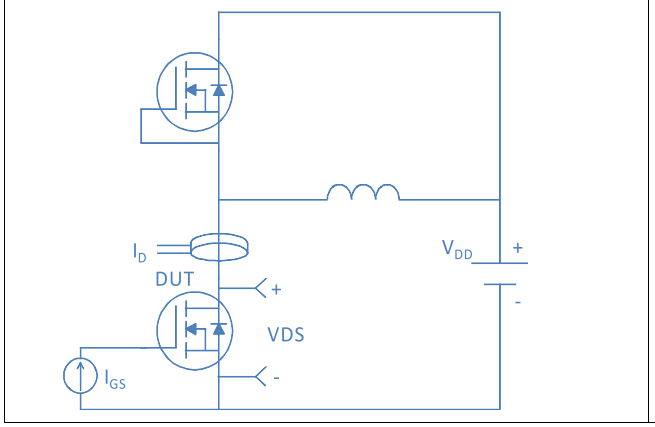


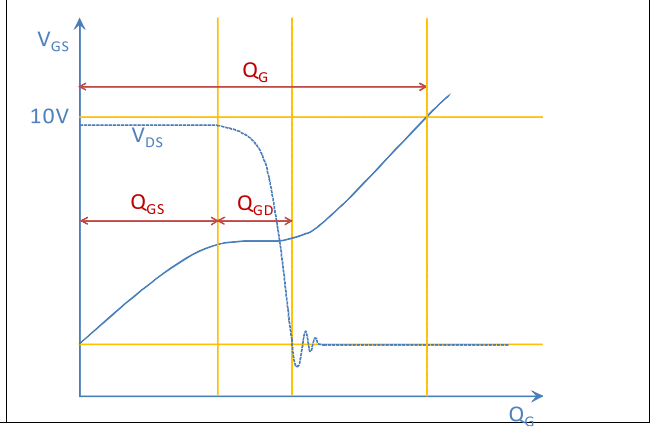
Inductive switching Test



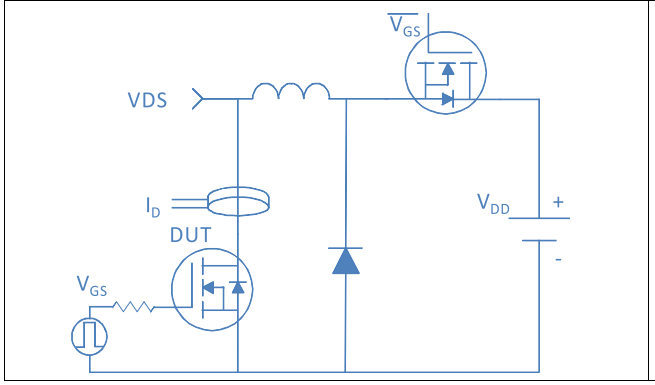


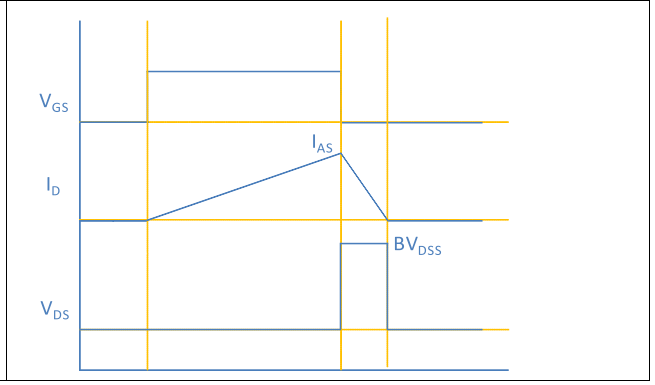
Gate Charge Test



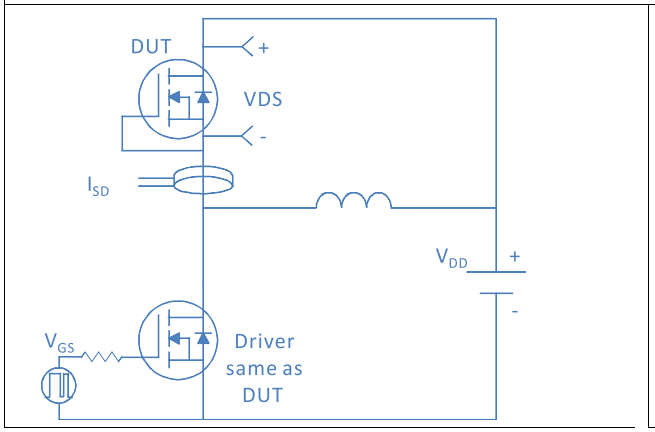


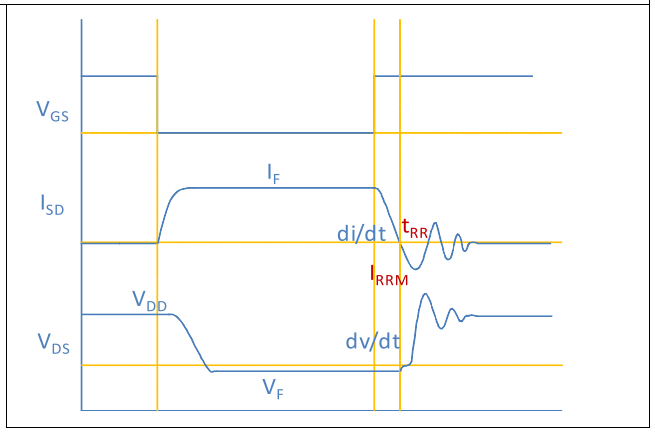
Uclamped Inductive Switching (UIS) Test





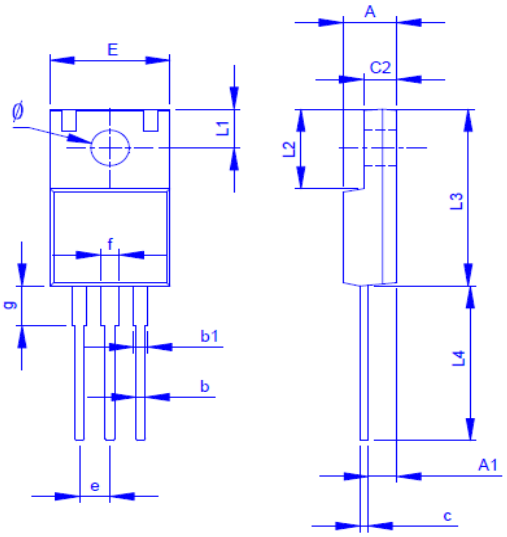
Diode Recovery Test





Package Outline

TO-220F, 3leads



Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L1	L2	L3	L4	ø	e	f	g
Min.	4.20	1.95	0.50	0.90	0.45	2.34	9.70	2.70	6.48	14.80	12.68	3.00	2.35	1.18	3.13
Max.	4.90	2.96	1.05	1.50	0.80	3.20	10.66	3.80	7.50	16.30	14.50	3.50	2.75	1.90	4.00