

20V P-Ch Power MOSFET

Feature

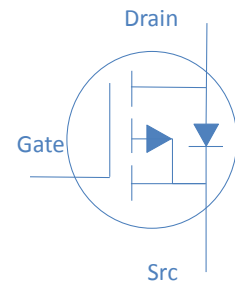
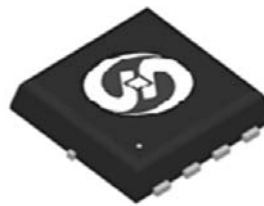
- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

V_{DS}		-20	V
$R_{DS(on),typ}$	$V_{GS}=-4.5V$	7.8	mΩ
$R_{DS(on),typ}$	$V_{GS}=-2.5V$	10.3	mΩ
$R_{DS(on),typ}$	$V_{GS}=-1.8V$	14.5	mΩ
I_D (Silicon Limited)		-15	A

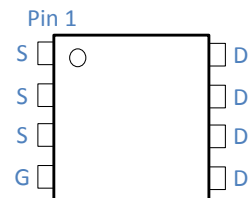
Application

- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial

DFN3x3



Part Number	Package	Marking
HTM095P02	DFN3*3	TM095P02



Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_A=25^\circ\text{C}$	-20	A
		$T_A=70^\circ\text{C}$	-15	
Drain to Source Voltage	V_{DS}	-	-20	V
Gate to Source Voltage	V_{GS}	-	± 8	V
Pulsed Drain Current	I_{DM}	-	-80	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.1\text{mH}, T_C=25^\circ\text{C}$	11.25	mJ
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2.5	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	$^\circ\text{C}$

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	6	$^\circ\text{C/W}$

Electrical Characteristics at $T_J=25^{\circ}\text{C}$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.4	-0.75	-1.2	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-16V, T_J=25^{\circ}\text{C}$	-	-	-1	μA
		$V_{GS}=0V, V_{DS}=-12V, T_J=125^{\circ}\text{C}$	-	-	-10	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 8V, V_{DS}=0V$	-	-	± 100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-15A$	-	7.8	9.5	m Ω
		$V_{GS}=-2.5V, I_D=-8A$	-	10.3	12.5	
		$V_{GS}=-1.8V, I_D=-5A$	-	14.5	18	
Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-15A$	-	32	-	S
Gate Resistance	R_G	$V_{GS}=15mV, V_{DS}=0V, f=1MHz$	-	3.0	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=-10V, f=1MHz$	-	7660	-	pF
Output Capacitance	C_{oss}		-	596	-	
Reverse Transfer Capacitance	C_{rss}		-	510	-	
Total Gate Charge	$Q_g(4.5V)$	$V_{DD}=-10V, I_D=-15A, V_{GS}=-4.5V$	-	51	-	nC
	$Q_g(2.5V)$		-	32	-	
Gate to Source Charge	Q_{gs}		-	4.9	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	13	-	
Turn on Delay Time	$t_{d(on)}$		-	25	-	
Rise time	t_r	$V_{DD}=-10V, I_D=-1A, V_{GS}=-4.5V,$	-	55	-	
Turn off Delay Time	$t_{d(off)}$	$R_G=6\Omega,$	-	150	-	
Fall Time	t_f		-	65	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=-3.5A$	-		-1.2	V
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Fig 1. Typical Output Characteristics

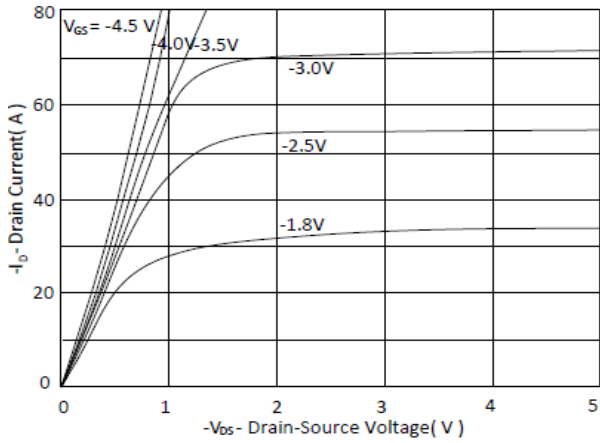


Figure 2. On-Resistance vs. Gate-Source Voltage

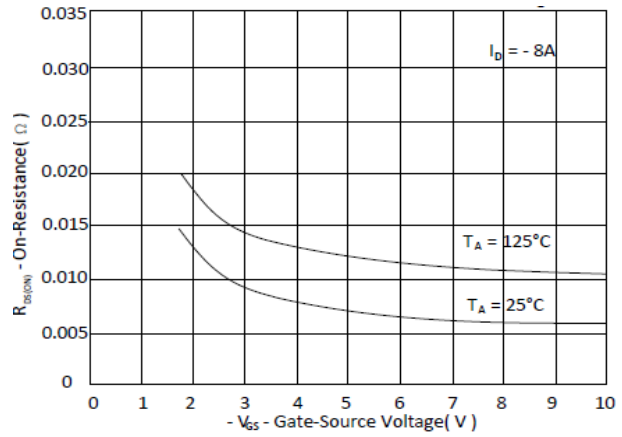


Figure 3. Gate Threshold Voltage v.s. Junction Temperature

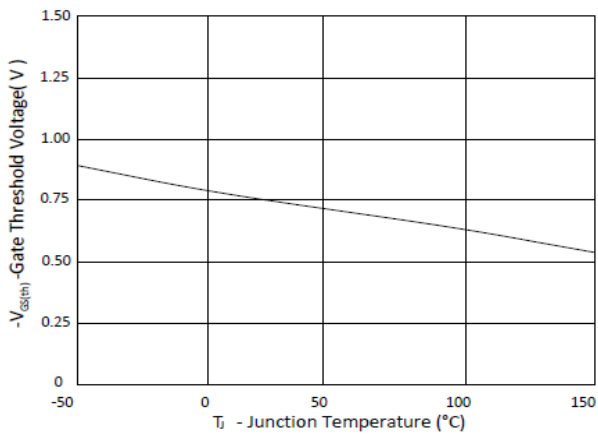


Figure 4. Normalized On-Resistance vs. Junction Temperature

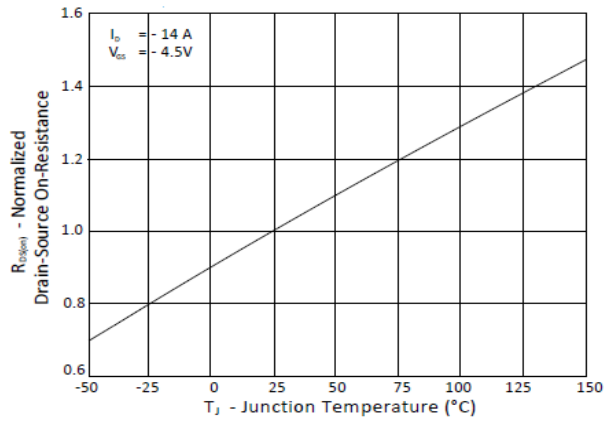


Figure 5. Typical Source-Drain Diode Forward Voltage

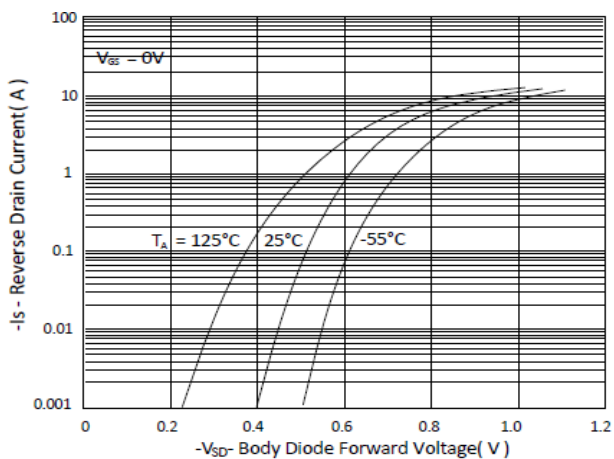


Figure 6. Typical Gate-Charge vs. Gate-to-Source Voltage

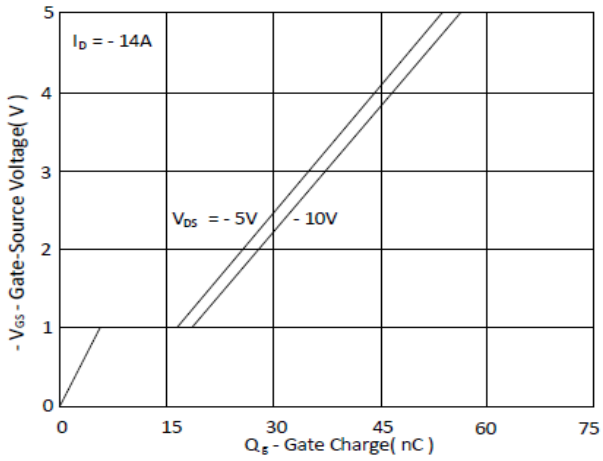


Figure 7. Typical Capacitance vs. Drain-to-Source Voltage

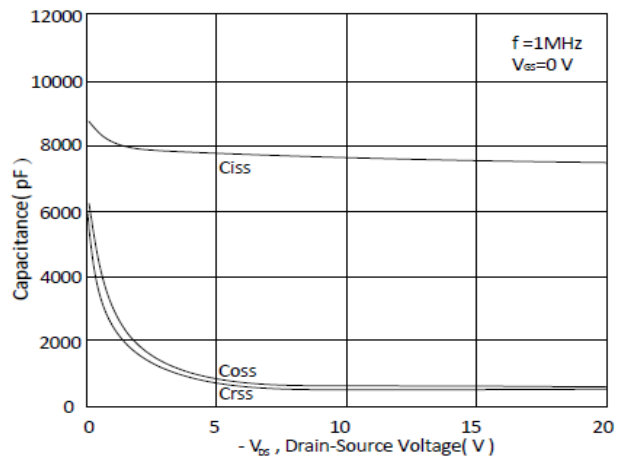


Figure 8. Maximum Safe Operating Area

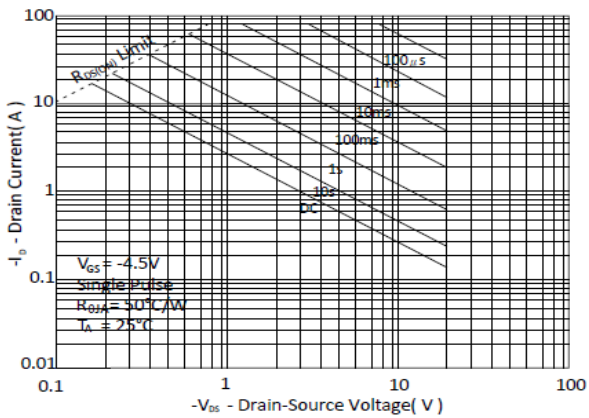


Figure 9. Single Pulse Maximum Power Dissipation

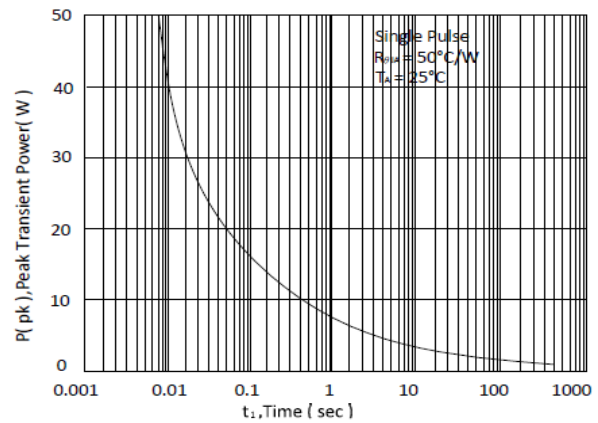
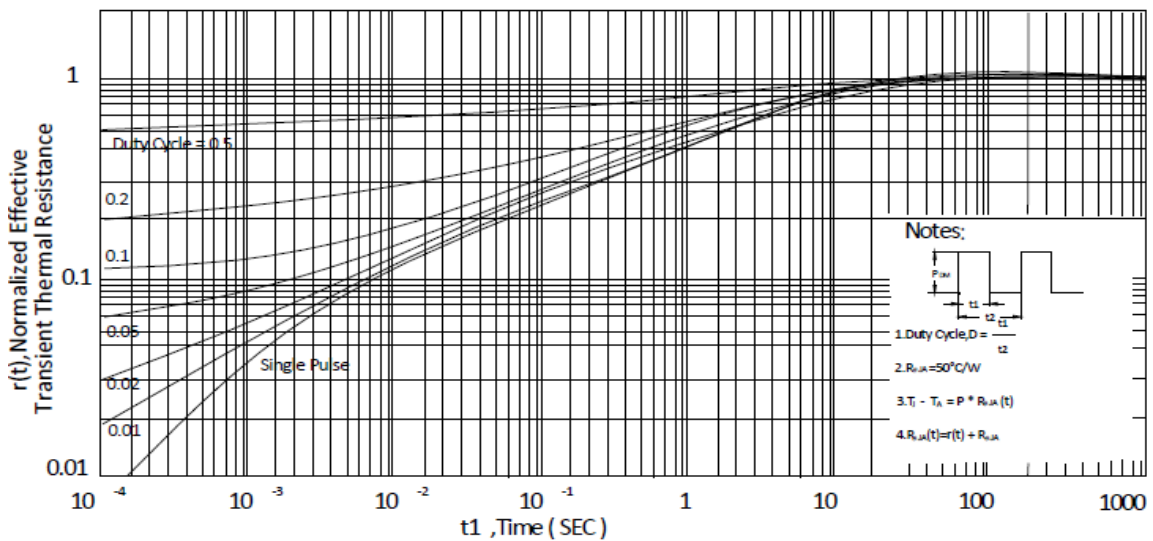
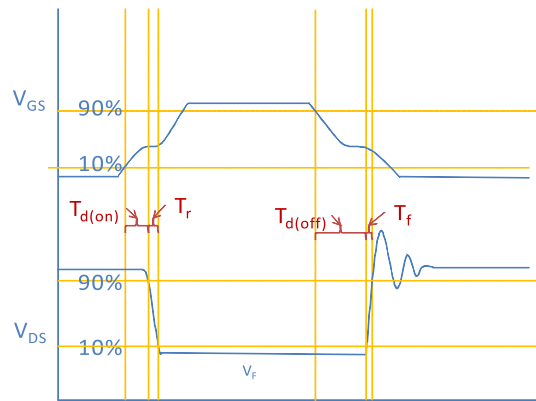


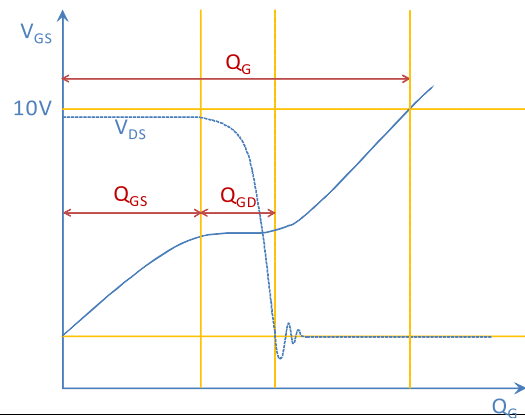
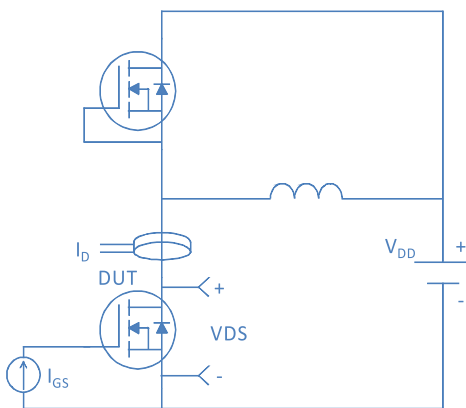
Figure 10. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



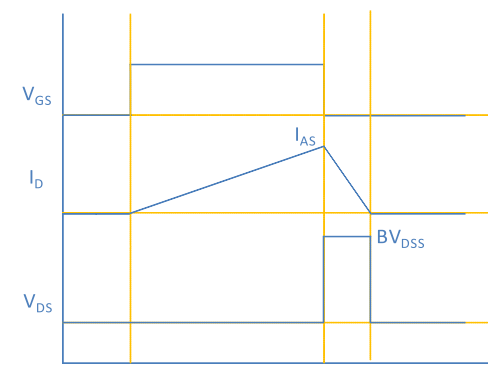
Inductive switching Test



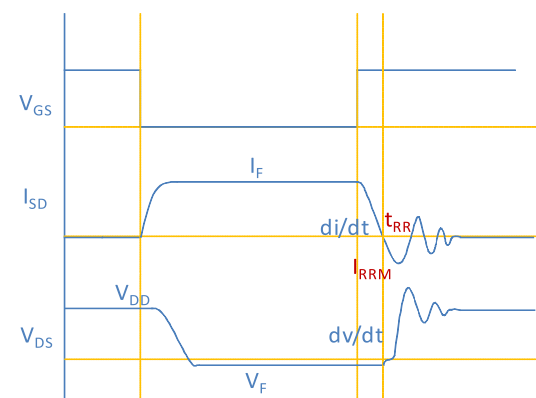
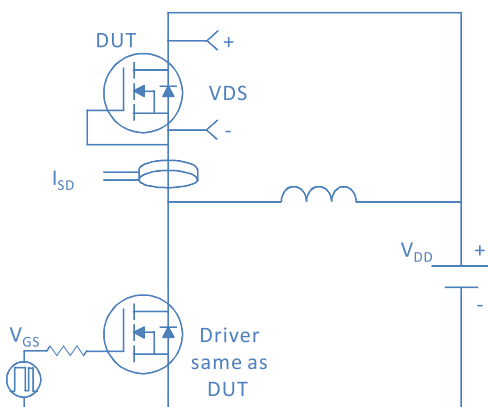
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

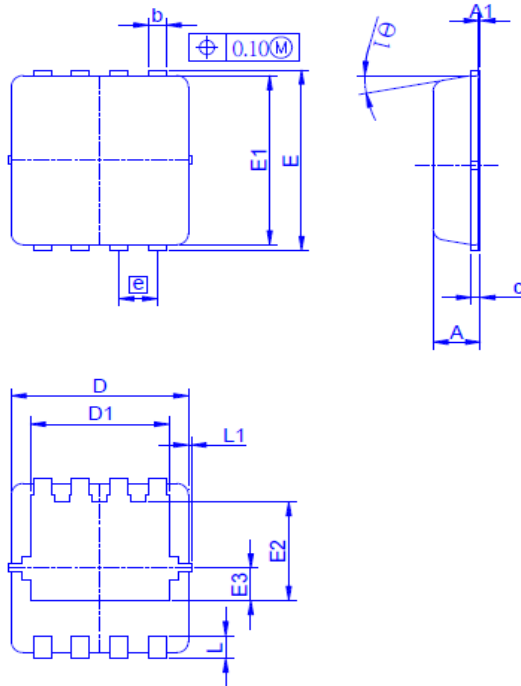


Diode Recovery Test



Package Outline

DFN3*3, 8leads



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	$\theta 1$
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°