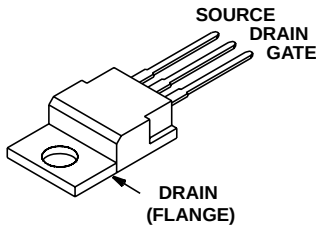
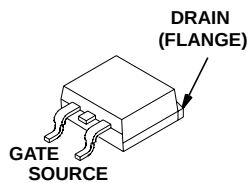
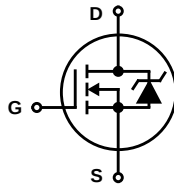


64A, 60V, 0.017 Ohm, N-Channel, Logic Level UltraFET Power MOSFET

Packaging
JEDEC TO-220AB

HUF76437P3
JEDEC TO-263AB

HUF76437S3S
Symbol

Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.014\Omega$, $V_{GS} = 10V$
 - $r_{DS(ON)} = 0.017\Omega$, $V_{GS} = 5V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER® Electrical Models
 - Spice and SABER® Thermal Impedance Models
 - www.Intersil.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76437P3	TO-220AB	76437P
HUF76437S3S	TO-263AB	76437S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF76437S3ST.

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	HUF76437P3, HUF76437S3S	UNITS
Drain to Source Voltage (Note 1)	60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	60	V
Gate to Source Voltage	± 16	V
Drain Current		
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 5V$)	64	A
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10V$) (Figure 2)	71	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 5V$)	45	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 4.5V$) (Figure 2)	44	A
Pulsed Drain Current	Figure 4	I_{DM}
Pulsed Avalanche Rating	Figures 6, 17, 18	UIS
Power Dissipation	155	W
Derate Above 25°C	1.03	W/ $^\circ\text{C}$
Operating and Storage Temperature	-55 to 175	T_J, T_{STG} $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	300	T_L $^\circ\text{C}$
Package Body for 10s, See Techbrief TB334.	260	T_{pkg} $^\circ\text{C}$

NOTES:

1. $T_J = 25^\circ\text{C}$ to 150°C .

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

HUF76437P3, HUF76437S3S

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	60	-	-	V	
		I _D = 250μA, V _{GS} = 0V , T _C = -40 ⁰ C (Figure 12)	55	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 50V, V _{GS} = 0V, T _C = 150 ⁰ C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 71A, V _{GS} = 10V (Figures 9, 10)	-	0.012	0.014	Ω	
		I _D = 45A, V _{GS} = 5V (Figure 9)	-	0.014	0.017	Ω	
		I _D = 44A, V _{GS} = 4.5V (Figure 9)	-	0.015	0.018	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	TO-220 and TO-263	-	-	0.97	⁰ C/W	
Thermal Resistance Junction to Ambient	R _{θJA}		-	-	62	⁰ C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 44A V _{GS} = 4.5V, R _{GS} = 5.6Ω (Figures 15, 21, 22)	-	-	350	ns	
Turn-On Delay Time	t _{d(ON)}		-	16	-	ns	
Rise Time	t _r		-	216	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	33	-	ns	
Fall Time	t _f		-	64	-	ns	
Turn-Off Time	t _{OFF}		-	-	145	ns	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 71A V _{GS} = 10V, R _{GS} = 5.6Ω (Figures 16, 21, 22)	-	-	215	ns	
Turn-On Delay Time	t _{d(ON)}		-	9	-	ns	
Rise Time	t _r		-	133	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	43	-	ns	
Fall Time	t _f		-	24	-	ns	
Turn-Off Time	t _{OFF}		-	-	100	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 30V, I _D = 45A, I _{g(REF)} = 1.0mA (Figures 14, 19, 20)	-	59	71	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	32	39	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	2	2.4	nC
Gate to Source Gate Charge	Q _{gs}			-	7.6	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	18	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 13)	-	2230	-	pF	
Output Capacitance	C _{OSS}		-	695	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	145	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 45\text{A}$	-	-	1.25	V
		$I_{SD} = 22\text{A}$	-	-	1.0	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 45\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	100	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 45\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	295	nC

Typical Performance Curves

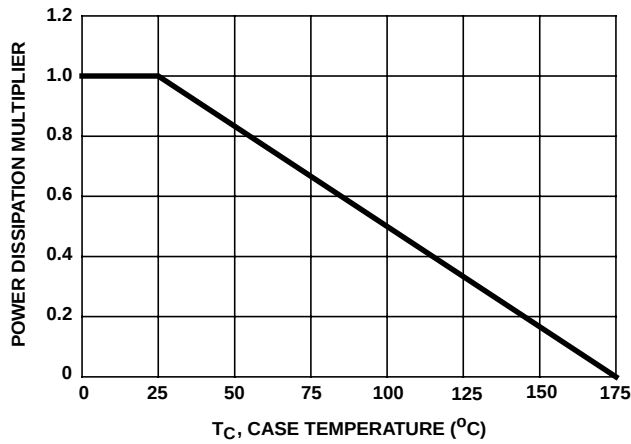


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

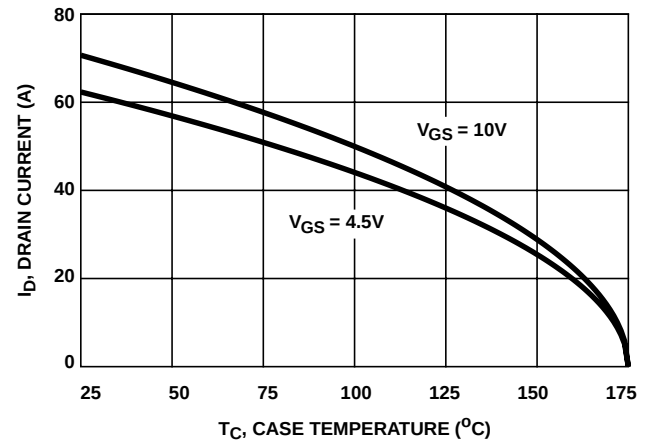


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

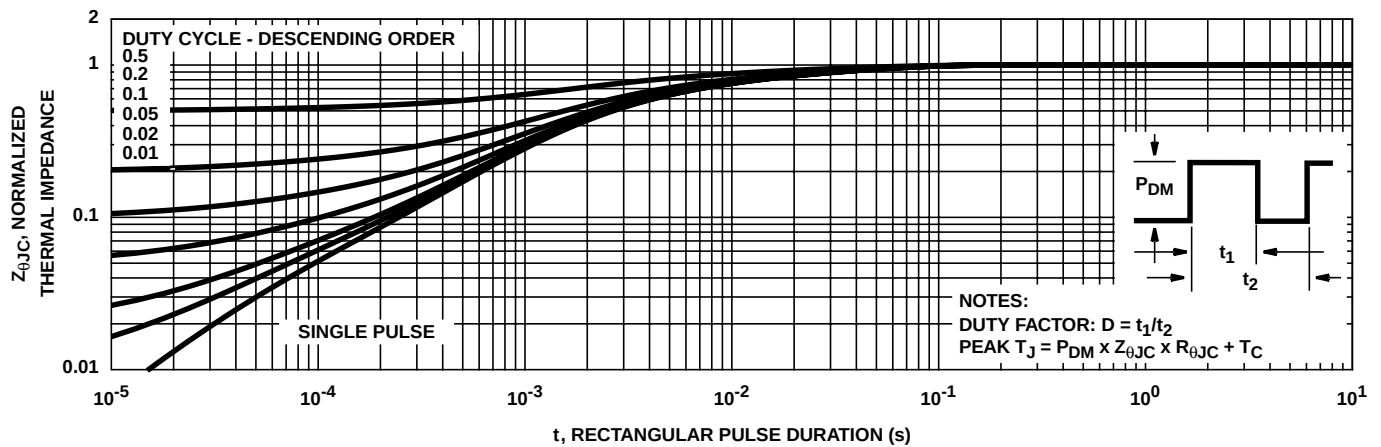


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

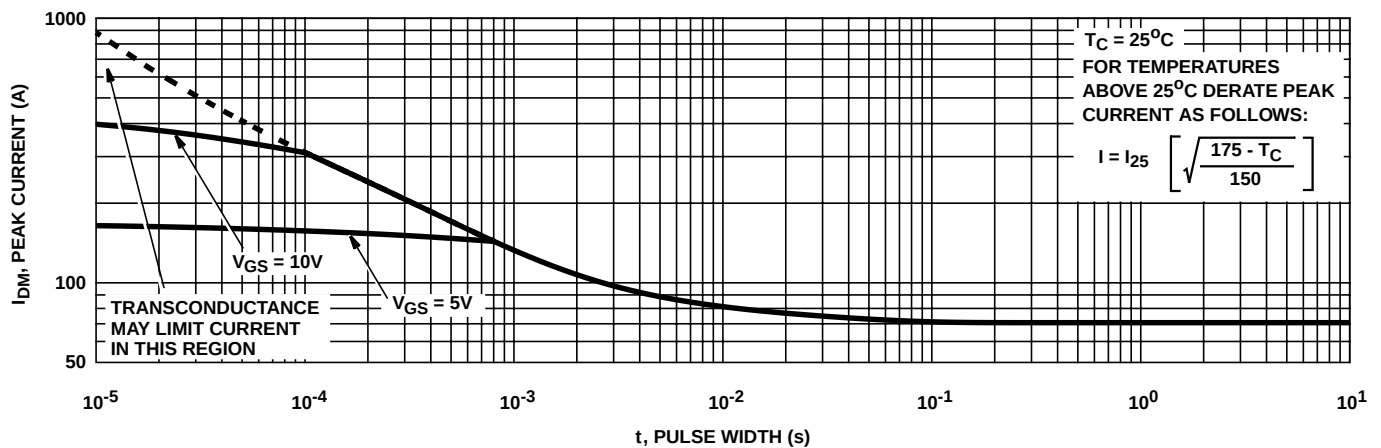


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

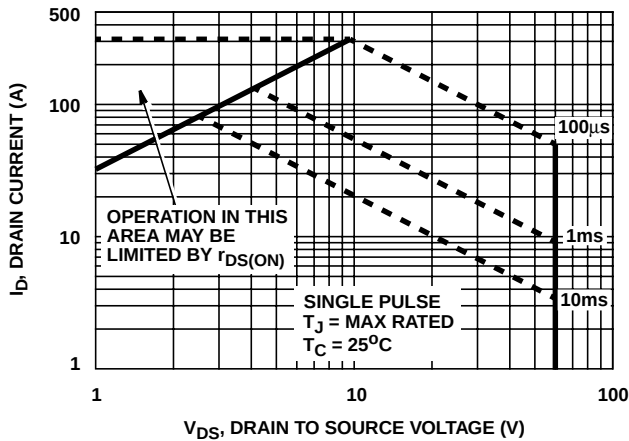
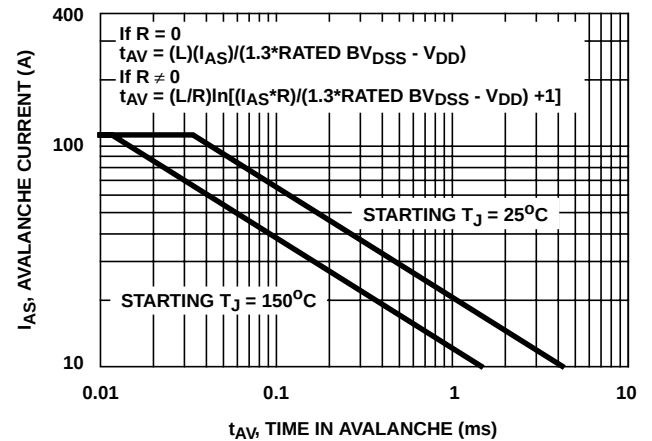


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

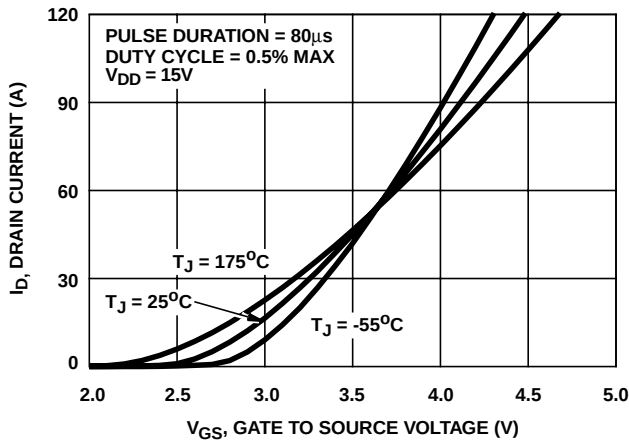


FIGURE 7. TRANSFER CHARACTERISTICS

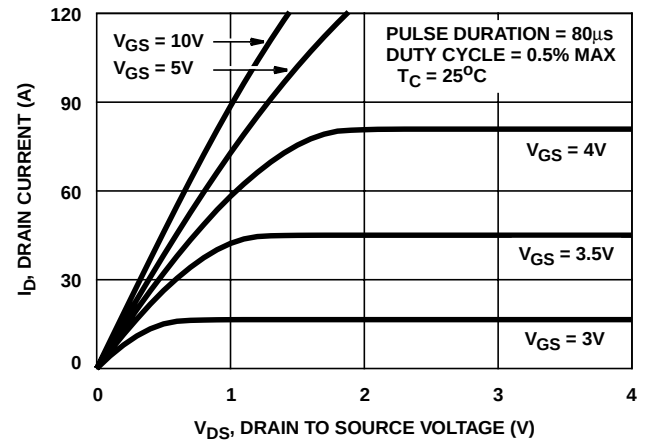


FIGURE 8. SATURATION CHARACTERISTICS

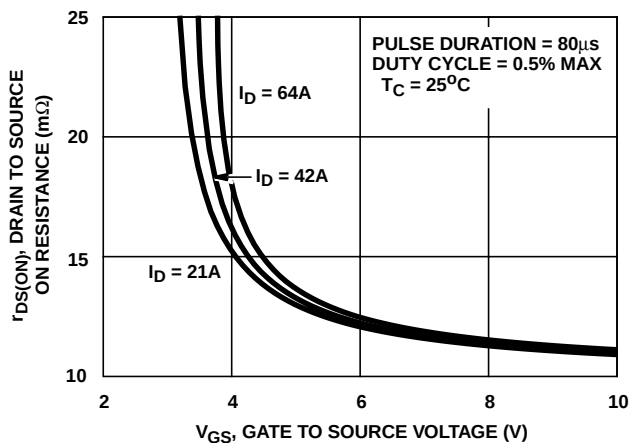


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs. GATE VOLTAGE AND DRAIN CURRENT

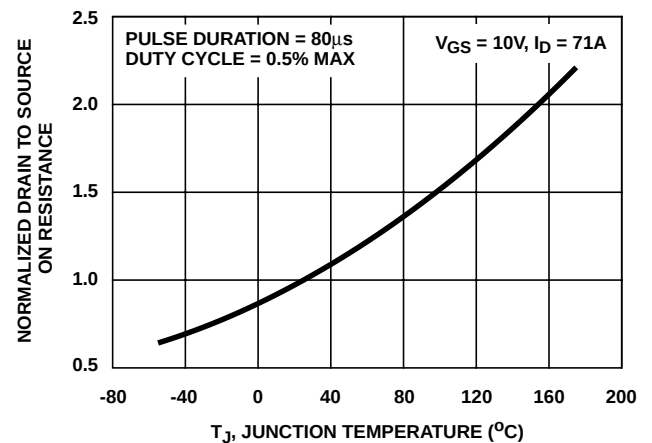


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs. JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

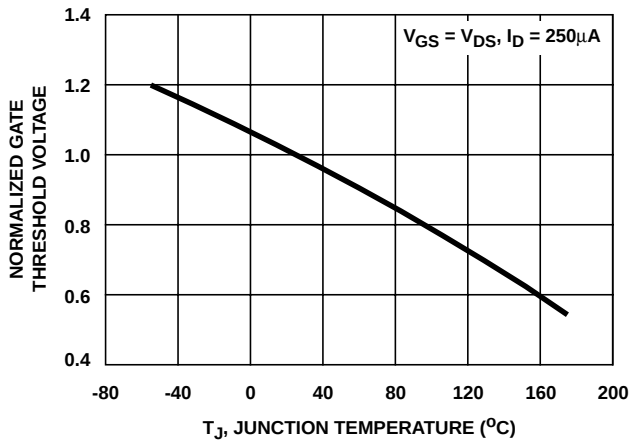


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

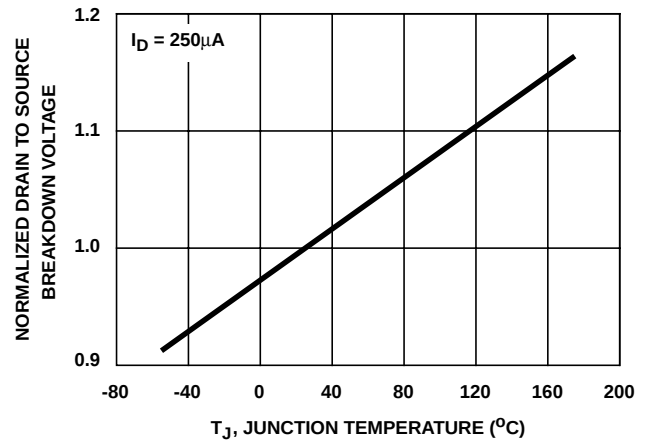


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

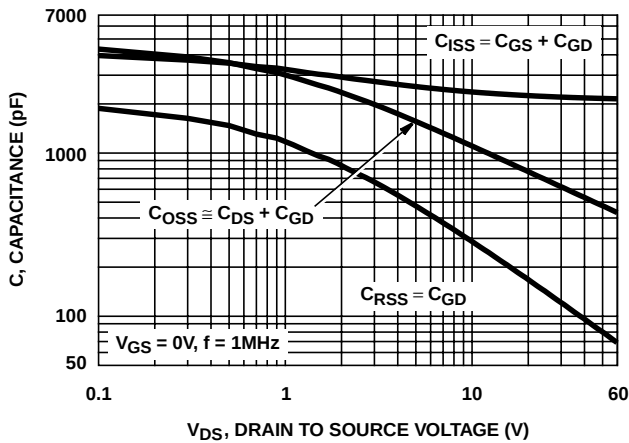
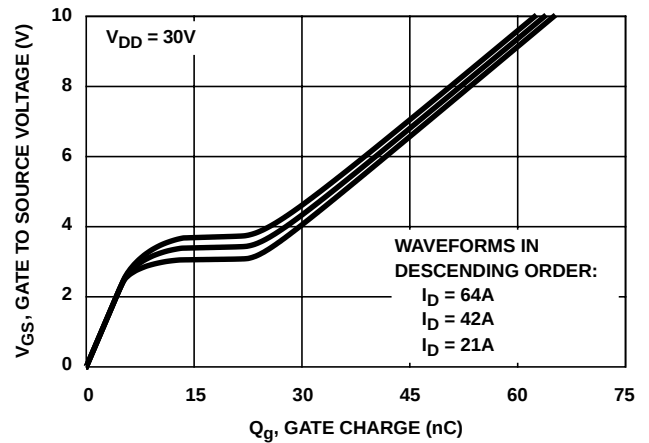


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

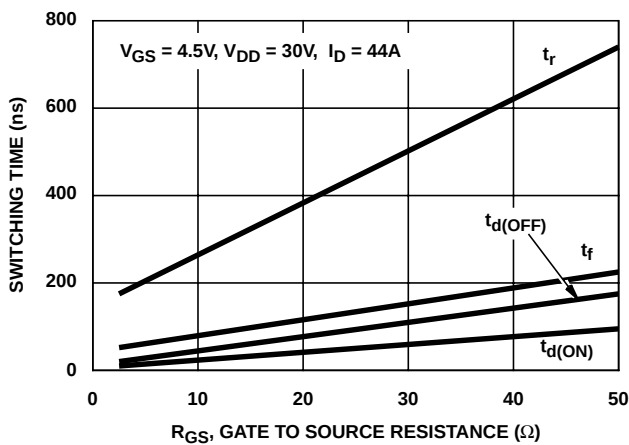


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

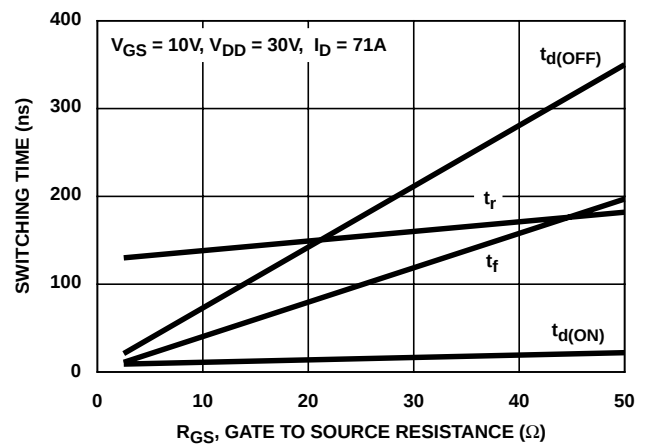


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

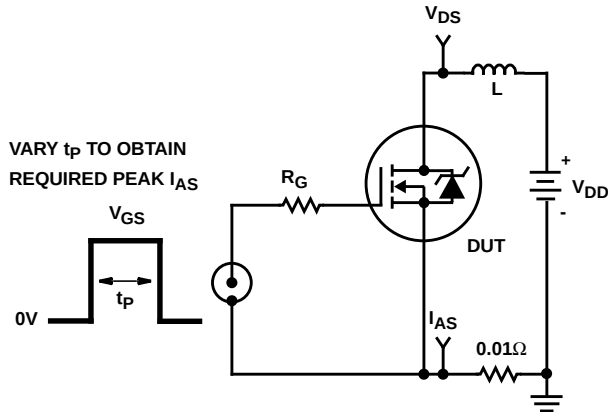


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

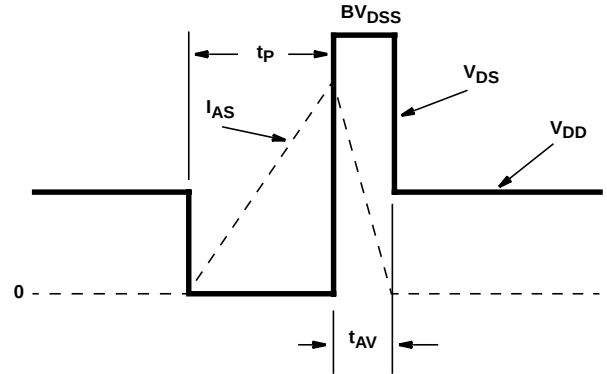


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

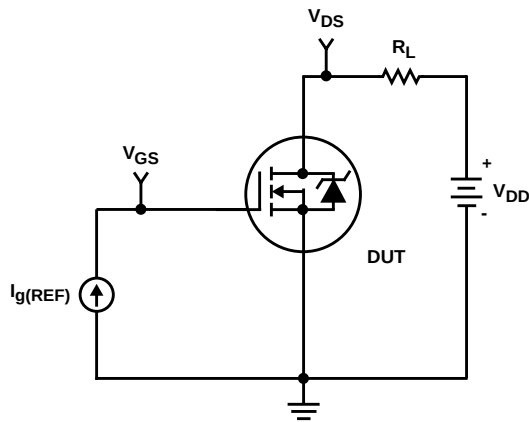


FIGURE 19. GATE CHARGE TEST CIRCUIT

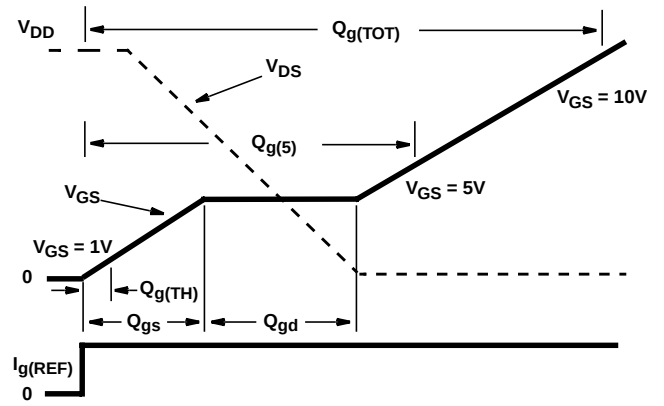


FIGURE 20. GATE CHARGE WAVEFORMS

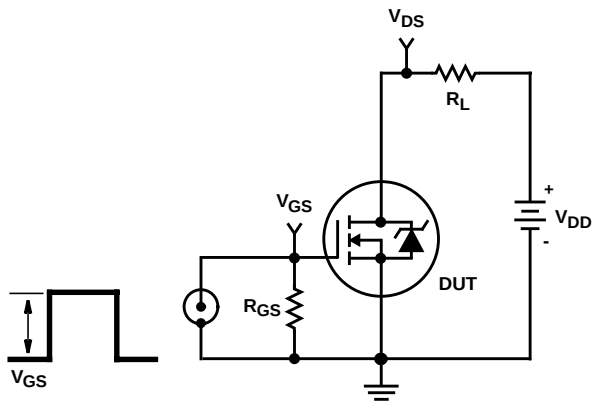


FIGURE 21. SWITCHING TIME TEST CIRCUIT

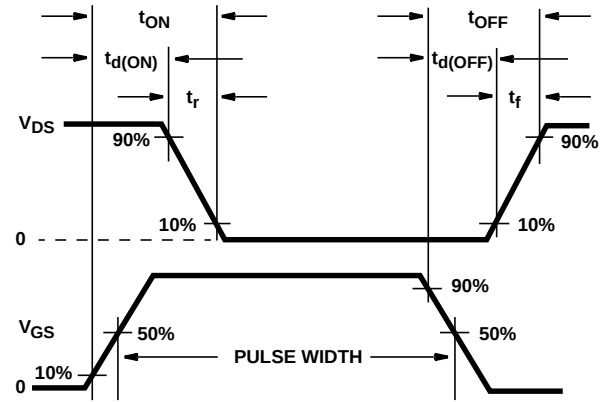


FIGURE 22. SWITCHING TIME WAVEFORM

SPICE Thermal Model

REV 1 September 1999

HUF76437T

CTHERM1 th 6 3.15e-3
CTHERM2 6 5 1.10e-2
CTHERM3 5 4 1.14e-2
CTHERM4 4 3 1.65e-2
CTHERM5 3 2 3.65e-2
CTHERM6 2 tl 1.90e-1

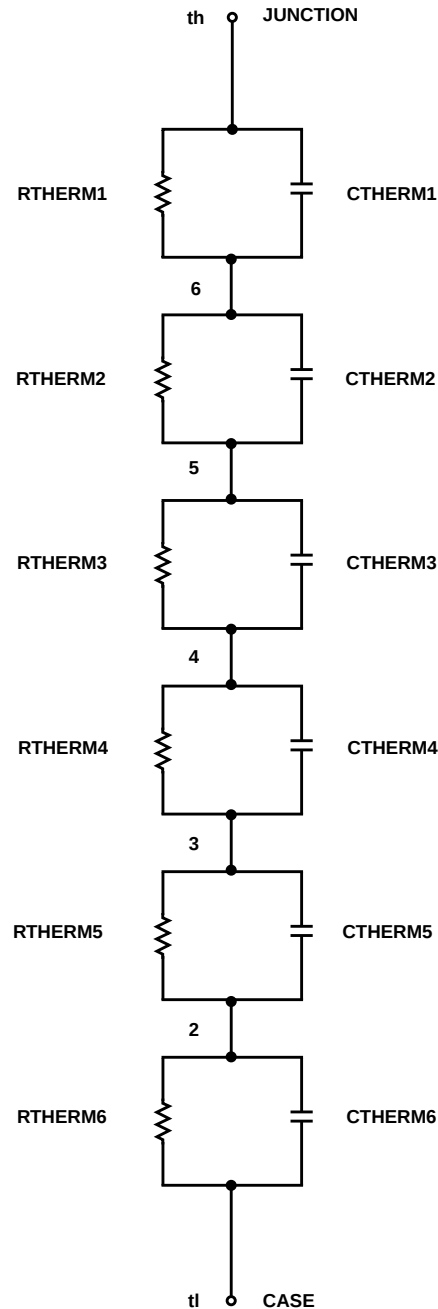
RTHERM1 th 6 1.60e-2
RTHERM2 6 5 9.30e-2
RTHERM3 5 4 1.30e-1
RTHERM4 4 3 1.60e-1
RTHERM5 3 2 1.85e-1
RTHERM6 2 tl 1.89e-1

SABER Thermal Model

SABER thermal model HUF76437T

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template thermal_model th tl
thermal_c th, tl
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  ctherm.ctherm2 6 5 = 1.10e-2
  ctherm.ctherm3 5 4 = 1.14e-2
  ctherm.ctherm4 4 3 = 1.65e-2
  ctherm.ctherm5 3 2 = 3.65e-2
  ctherm.ctherm6 2 tl = 1.90e-1

  rtherm.rtherm1 th 6 = 1.60e-2
  rtherm.rtherm2 6 5 = 9.30e-2
  rtherm.rtherm3 5 4 = 1.30e-1
  rtherm.rtherm4 4 3 = 1.60e-1
  rtherm.rtherm5 3 2 = 1.85e-1
  rtherm.rtherm6 2 tl = 1.89e-1
}
```



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