Type-C DRP Controller with 32-bit RISC-V MCU

Hynetek Semiconductor Co., Ltd.

HUSB251

FEATURES

- USB Type-C DRP with PD protocol Supported
  - Compliant with USB Type-C Specification Reversion 2.1
  - Compliant with USB PD Specification Reversion 3.1
- Bidirectional PD protocol for Type-C with 28 V EPR FPDO and EPR AVS Supported
- Integrated VCONN Power for eMarker Detection
- Integrated N-MOSFET drive with soft start
- Multiple DPDM Charging Protocols Implemented
  - BC1.2 DCP and Divider 3
  - QC2.0, QC3.0, AFC, FCP, UFCS
- Up to 35 V Maximum Voltage Rating at USB Type-C Connector Pins
- Programmable Constant Voltage and Constant Current Control
- Integrated dead battery function for power requesting as SINK
- Fault Protections including VIN OCP, SCP, UVP, OVP and CC OVP, OCP, DPDM OVP, OTP, TSD and so on
- 32-bit RISC-V MCU with 32 kB MTP Memory
- Integrated I^2C and UART module for system communication
- Integrated deep sleep mode for power saving
- ±4 kV HBM ESD Rating for all of Type-C Connector Pins

APPLICATIONS

Travel Adaptor

Car Charger

Battery Powered Devices

GENERAL DESCRIPTION

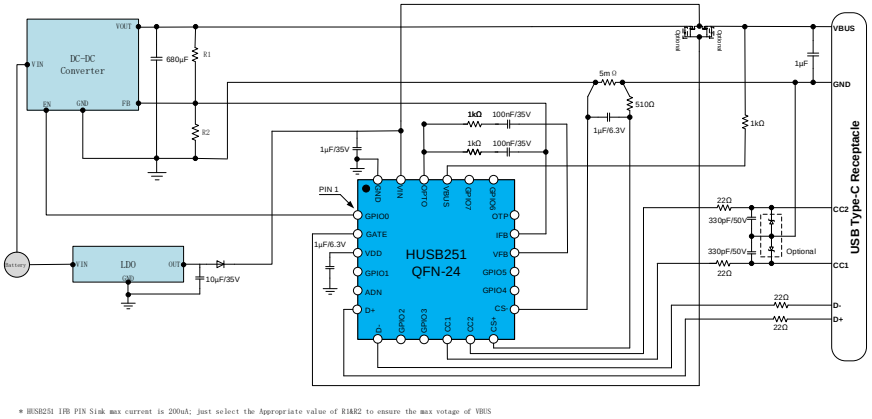
HUSB251 is designed for a USB Type-C DRP product. It can support up to multiple PDOs with programmable voltage and current for different applications, such as PPS PDOs, EPR PDOs. All of PDOs are fully compliant with USB PD 3.1 Specification Rev.1.8

Besides, HUSB251 implements DPDM charging protocols for source. Both D+ and D- pins can be configured to support QC2.0, QC3.0, AFC, FCP, UFCS and divider 3 mode which provide excellent compatibility for the legacy devices.

It integrates an GATE driver to enable between VBUS and VIN to protect the devices connected with Type-C connector.

The high voltage tolerance and protections at CC1, CC2, D+ and D- pins provides more reliability for the system.

TYPICAL APPLICATION CIRCUIT



* HUSB251 IFB PIN Sink max current is 200uA; just select the Appropriate value of R1&R2 to ensure the max votage of VBUS

Figure 1. Typical Application Circuit for DRP

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REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	06/2023	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

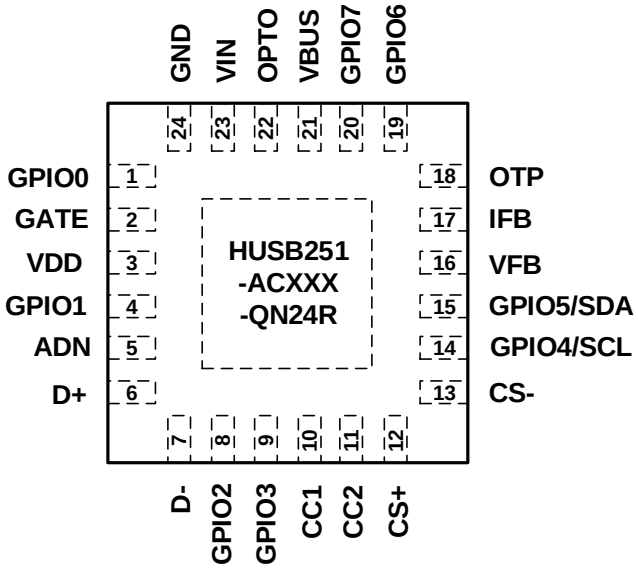


Figure 2. HUSB251 Pin Assignment

Table 1. HUSB251-ACXXX-QN24R Pin Function Descriptions

Pin No.	Pin Name	Type	Description
1	GPIO0	AO	General purpose pin 0.
2	GATE	AO	N-MOSFET Gate driver output for VBUS load switch.
3	VDD	P	Internal 1.5 V regulator output for system power. Connect a 1 μF ceramic capacitor at this pin.
4	GPIO1	AO	General purpose pin 1. This pin is only open drain output.
5	ADN	AI	ADC input pin for voltage detection.
6	D+	DIO	USB D+ line.
7	D-	DIO	USB D- line.
8	GPIO2	DIO	General purpose pin 2. This pin can be configured as ADC input, digital input, digital output, pull up or pull down function by firmware.
9	GPIO3	DIO	General purpose pin 3. This pin can be configured as ADC input, digital input, digital output, pull up or pull down function by firmware.
10	CC1	AIO	USB Type-C CC1 line.
11	CC2	AIO	USB Type-C CC2 line.
12	CS+	AI	Positive input of the current sense amplifier.
13	CS−	AI	Negative input of the current sense amplifier.
14	GPIO4	AO	Multiplex PIN. One is general purpose pin 4. Other is SCL of I^2C.
15	GPIO5	AO	Multiplex PIN. One is general purpose pin 5. Other is SDA of I^2C.
16	VFB	AI	Feedback point of Constant Voltage (CV) loop, connect CV compensation network to this pin.
17	IFB	AI	Feedback point of Constant Current (CC) loop, connect CC compensation network to this pin.
18	OTP	AI	External temperature sensing pin. An internal pull up current source is connected at this pin. A NTC thermistor is recommended to be place at this pin.
19	GPIO6	DIO	General purpose pin 6. This pin can be configured as ADC input, digital input, digital output, pull up or pull down function by firmware.
20	GPIO7	DIO	General purpose pin 7. This pin can be configured as ADC input, digital input, digital output, pull up or pull down function by firmware.
21	VBUS	AI	VBUS sense and discharge pin.

Pin No.	Pin Name	Type	Description
22	OPTO	AI	OPTO driver. Connect to the opto-coupler in isolated ACDC applications.
23	VIN	P	Supply voltage input. Connect this pin to GND via a recommended 1 μF ceramic capacitor.
24	GND	P	Power ground.
-	PAD	-	QFN package pad. It is recommended to connect this pin to GND.

1 Legend:

A = Analog Pin

P = Power Pin

D = Digital Pin

I = Input Pin

O = Output Pin

RECOMMENDED OPERATING CONDITIONS

Table 2.

Parameter	Rating
VIN Input Voltage	3.15 V to 29.4 V
Operating Junction Temperature Range (T_J)	−40 °C to 125 °C
Ambient Temperature Range (T_A)	-40 °C to 85 °C

SPECIFICATIONS

V_{IN} = 3.15 V to 29.4 V, T_J = −40°C to 125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Power Supply						
Supply Voltage UVLO Threshold	V_{IN_UVLO}	Rising edge		3.3		V
Supply Voltage UVLO Hysteresis	$V_{IN\_UVLO\_HYS}$			300		mV
Operation Mode Supply Current	I_{CC_OPR}	CC is attached with a R_d, normal operation		4		mA
Sleep Mode Supply Current	I_{CC_SLP}	CC is attached with a R_d, configured in sleep mode			1.5	mA
Internal Regulator (VDD)						
Output Voltage	V_{DD}			1.5		V
Type C Pull up current source (CC1, CC2)						
Default Current Source	I_{RP_DFT}		64	80	96	µA
1.5 A Current Source	$I_{RP\_1.5A}$		166	180	194	µA
3 A Current Source	I_{RP_3A}		304	330	356	µA
Rd Detection Threshold 1	$v_{Rd\_OPEN\_1.5A}$	Default or 1.5 A R_p current source is enabled, T_A = 25°C	1.55	1.6	1.65	V
Rd Detection Threshold 2	$v_{Rd\_OPEN\_3A}$	3 A R_p current source is enabled, T_A = 25°C	2.50	2.6	2.70	V
Ra Detection Threshold 0	v_{Ra_DEF}	Default R_p current source is enabled, T_A = 25°C	0.15	0.2	0.25	V
Ra Detection Threshold 1	$v_{Ra\_1.5A}$	1.5 A R_p current source is enabled, T_A = 25°C	0.35	0.4	0.45	V
Ra Detection Threshold 2	v_{Ra_3A}	3 A R_p current source is enabled, T_A = 25°C	0.75	0.8	0.85	V
CC Impedance in Disable Mode	R_{P_DIS}	CC impedance with R_P is disabled	2			MΩ
VCONN Output Voltage	v_{VCONN}	VCONN is enabled	3	5	5.5	V
VCONN Output Current Limit	I_{VCONN}	V_{IN} = 3.3 V to 5.5 V and VCONN is enabled	20			mA
Type C Pull down resistor (CC1, CC2)						
Sink Pull Down Resistor	Rd	Vin>V_{IN_UVLO}	4.6	5.1	5.6	kΩ
Ra Detection Threshold as Sink	V_{Ra_SNK}	Configured as Sink		0.15	0.20	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Rd Detection Threshold as Sink	V_{Rd_SNKDEF}	Configured as Sink with IRP_DEF attached	0.25	0.61	0.66	V
	$V_{Rd\_SNK1.5A}$	Configured as Sink with IRP_DEF attached	0.70	1.16	1.23	V
	$V_{Rd\_SNk3.0A}$	Configured as Sink with IRP_DEF attached	1.31	2.04	2.18	V
Type C PD BMC Receiver						
Noise Amplitude when BMC is Active	$v_{NoiseActive}$	Peak-to-peak noise after Rx filter has been applied			165	mV
Noise Amplitude when BMC is Idle	$v_{NoiseIdle}$	Peak-to-peak noise after Rx filter has been applied			300	mV
Receiver Input Impedance	z_{BmcRx}	Input impedance of Rx	2			MΩ
Rx Bandwidth Limiting Filter	$t_{RxFilter}$	Time constant of a single pole filter	100			ns
Type C PD BMC Transmitter						
Bit Rate	$f_{BitRate}$	Refer the average bit rate of the last 32b of the Preamble	270	300	330	kbps
Unit Interval	UI		3.03	3.33	3.7	μs
Bitrate Drift	$p_{BitRate}$				0.25	%
Fall Time	t_{Fall}	10% and 90% amplitude points, unloaded condition	300			ns
Rise Time	t_{Rise}	10% and 90% amplitude points, unloaded condition	300			ns
Voltage Swing	v_{Swing}	CC pull down resistor >800 Ω	1.05	1.125	1.2	V
Voltage Low	v_{Low}	CC pull down resistor >800 Ω	-75	0	75	mV
Transmitter output impedance	z_{Driver}		33	50	75	Ω
BC1.2 DCP MODE as Source						
D+ and D- Shorting Resistance	R_{DPM_SHORT}	V_{D+} = 0.6 V		30		Ω
D+ Leakage Resistance	R_{DP_LKG}	V_{D+} = 0.6 V		800		kΩ
D- Leakage Resistance	R_{DM_LKG}	V_{D-} = 0.6 V		800		kΩ
DIVIDER 3 MODE as Source						
D+ Output Voltage	$V_{DP\_2.7V}$	V_{IN} = 5 V		2.7		V
D- Output Voltage	$V_{DM\_2.7V}$	V_{IN} = 5 V		2.7		V
D+ Output Impedance	R_{DP_PAD}	I_{D+} = −5 μA		30		kΩ
D- Output Impedance	R_{DM_PAD}	I_{D-} = −5 μA		30		kΩ
HVDCP MODE as Source						
Output Voltage Selection Reference	V_{SEL_REF}			2.0		V
Data Detect Voltage	V_{DAT_REF}			0.325		V
D- Pull-Down Resistance	R_{DM_DWM}			15		kΩ
FCP and UFCS MODE as Source						
D+/D- TX Valid Output High	V_{TX_VOH}		2.55		3.6	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
D-/D+ TX Valid Output Low	V_{TX_VOL}				0.3	V
D-/D+ RX Valid Input High	V_{RX_VIH}		1.4		3.6	V
D-/D+ RX Valid Input Low	V_{RX_VIL}				1	V
Unit Interval for FCP	UI			160		μs
BC1.2 Detection						
DCD Source Current	I_{DP_SRC}		7	10	12	μA
BC1.2 Source Voltage	V_{DPM_SRC}		0.55	0.6	0.65	V
BC1.2 Sink Current	I_{DPM_SNK}		25	75	125	μA
Voltage Regulation						
VDAC LSB	LSB_VDAC			10		Bit
Default Voltage	$V_{DEFAULT}$		4.75	5.1	5.5	V
Regulation Accuracy	$v_{SRCValid}$	T_A = 25°C	99	100	101	%
		T_J = -40°C to 125°C	97	100	103	%
Active Load for Discharge	R_{ALD}	ALD option 0 is selected		70		mA
		ALD option 1 is selected		100		mA
		ALD option 2 is selected		140		mA
		ALD option 3 is selected		170		mA
Current Control						
Constant Current Accuracy		Operating current is less than 3 A	-0.15	0	0.15	A
		Operating current is higher than 3 A, refer to nominal operation current	95	100	105	%
Current Sensing Resistor	R_{CS}			5		mΩ
Gate Driver and VBUS						
Gate Driver Output Voltage	V_{GATE}	V_{IN} ≤ 21 V	5	7	10	V
		V_{IN} > 21 V	4.5	5.5	6.5	V
Gate Driver Output Current	I_{GATE_ON}			20		μA
Gate Discharge Current	I_{GATE_DSG}			20		mA
VBUS Discharge Current	I_{VBUS_DSG}			20		mA
Fault Protection						
Over-voltage Protection Threshold	V_{IN_OV}	OVP threshold option 0, refer to nominal V_{IN}		110		%
		OVP threshold option 1, refer to nominal V_{IN}		115		%
		OVP threshold option 2, refer to nominal V_{IN}		120		%
		OVP threshold option 3, refer to nominal V_{IN}		125		%
Over-current Protection Threshold	I_{IN_OCP}	Nominal output current = 3 A		3.6		A
Short-circuit Protection Threshold	I_{IN_SCP}			12		A
OTP Current Source	I_{OTP}			80		μA
Thermal Shut Down Threshold	T_{SD}			150		°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Thermal Shut Down Hysteresis	T_{SDHys}			20		°C
ADC						
ADC Resolution	N_{ADC}			11		Bit
ADC Reference Voltage	V_{ADC}			2.5		V
ADC Sample Rate	f_{ADC}			125		kHz
GPIO						
Digital Output High Voltage	V_{OH_D}	Source current = 2 mA		3.3		V
Digital Output Low Voltage	V_{OL_D}	Sink current = 2 mA			0.4	V
Digital Input High Voltage	V_{IH_D}		1.4			V
Digital Input Low Voltage	V_{IL_D}				1	V
Internal Pull-up Resistor	R_{GPIO_PU}			35		kΩ
Internal Pull-down Resistor	R_{GPIO_PD}			35		kΩ
I^2C(SDA，SCL)						
Input Leakage Current	I_{LKG_I2C}	VDD=3.3 V	-3		3	mA
Output Low Voltage	V_{OL_I2C}	Sink current is 2 mA			0.4	V
Input Low Voltage	V_{OL_I2C}	I^2C Pull up voltage is 3.3 V			0.99	V
Input High Voltage	V_{HL_I2C}	I^2C Pull up voltage is 3.3 V	2.31			V
Input High Hysteresis	V_{HYS_I2C}	I^2C Pull up voltage is 3.3 V	0.17			V
SCL Clock Frequency	F_{SCL_I2C}		50		400	kHz
UART(UTX，URX)						
Output Low Voltage	V_{OL_UART}	Sink current is 0.5 mA			0.4	V
Output High Voltage	V_{OH_UART}	Source current is 0.5 mA			0.9V	V
Output Impedance	R_{O_UART}		35		75	Ω
Input Low Voltage	V_{IL_UART0}				0.99	V
	V_{IL_UART1}				0.54	V
Input High Voltage	V_{HL_UART0}		1.4			V
	V_{HL_UART1}		2.31			V
Input High Hysteresis	V_{HYS_UART}		0.2			V
UATR Tx Baud Rate	F_{BR_UART0}		103.7	115.2	126.7	kHz
	F_{BR_UART1}		51.84	57.6	63.36	kHz
	F_{BR_UART2}		34.56	38.4	42.24	kHz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN, VBUS, OPTO, GATE to GND	−0.3 V to 35 V
CC1, CC2, D+, D-, CS+, CS- to GND	−0.3 V to 30 V
VFB, IFB, ADN, OTP, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7 to GND	−0.3 V to 7 V
VDD to GND	−0.3 V to 2 V
Junction Temperature Range	−40°C to 125°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model (ALL Other PINS to GND)	±6000 V
Human Body Model (ALL Other PINS to VDD)	±6000 V
Human Body Model (ALL Other PINS to VIN)	±2500 V
Charged Device Model	±2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN4x4-24L	46	23	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

FUNCTIONAL BLOCK DIAGRAM

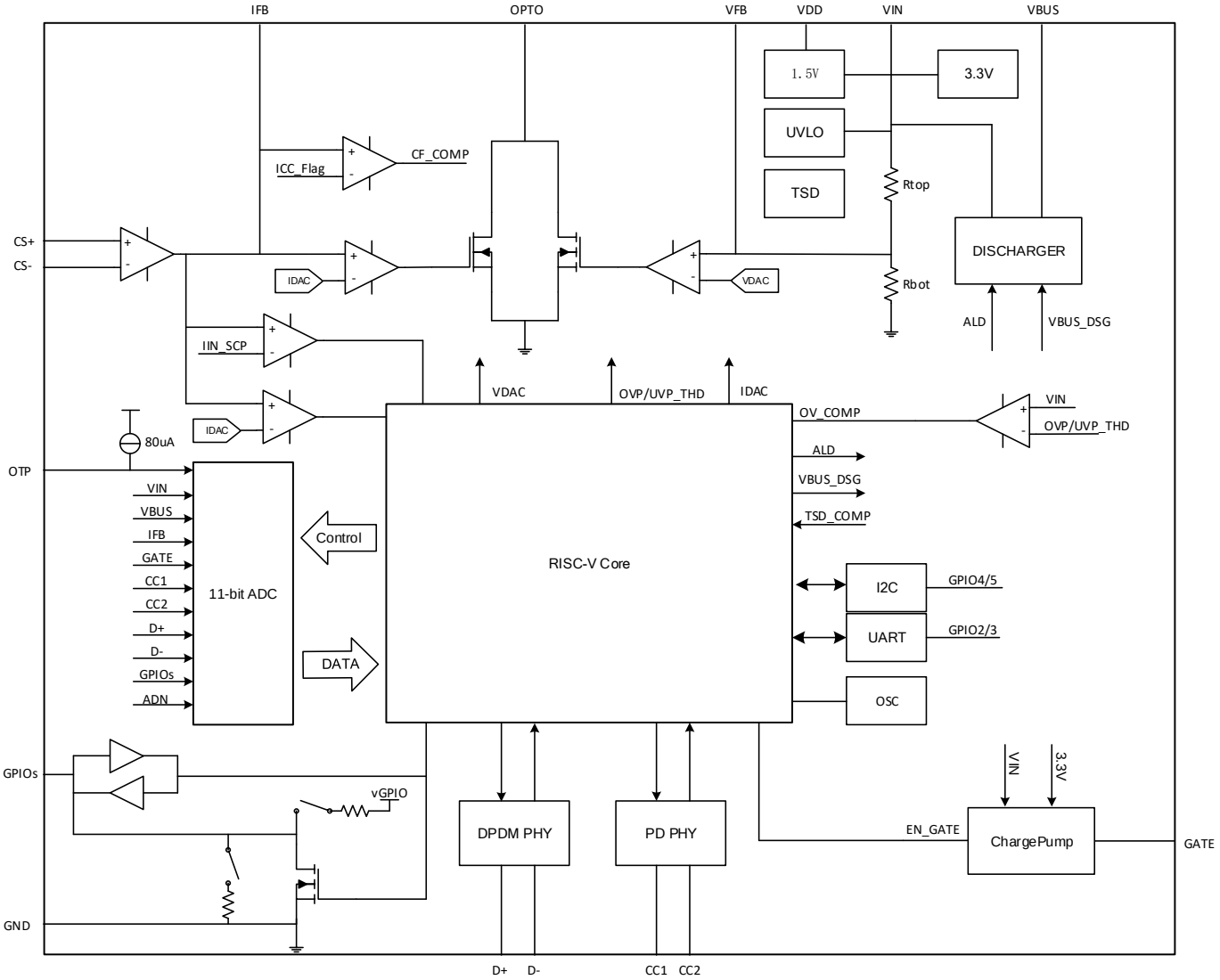


Figure 3. HUSB251 Functional Block Diagram

THEORY OF OPERATION

HUSB251 is a MCU-based USB PD DRP controller. It integrates a MCU core with necessary functions for USB PD protocol, legacy charging protocols and power regulation. By modifying the firmware, the HUSB251 can be employed in different applications. The integrated protections including OCP, OVP, UVP, SCP, OTP, CCOV, TSD and DPDMOV can enhance the system reliability significantly.

MCU

HUSB251 integrates a 32-Bit RISC-V MCU core for the main operation. This subsystem implements the standard RISC-V structure. It features:

- Support RV32 commands
- Support the programs in C format
- Support interruptions
- Internal communication BUS
- With 8 kB ROM, 8 kB RAM, 32 kB Flash peripherals

VIN PIN

VIN pin is the power supply input, which is derived from the output of the AC-DC or DC-DC converter. Connect a 1 μF decoupling MLCC between VIN pin and GND pin.

The VIN pin is also connected to an internal MOSFET and discharge resistor, which is used as a bleeder to help discharge the energy stored in the output capacitor. With this bleeder, VIN can be regulated to vSafe5V upon the detachment of a connected device, or to a lower desired output voltage level upon a request command received from the Sink, such as from 20 V to 5 V.

VDD PIN

An internal liner regulator is used to provide 1.5 V for internal circuits. Connect a 1 μF MLCC to VDD pin for decoupling.

CONTROL LOOP COMPENSATION CIRCUIT (VFB, CS+, CS−, IFB, OPTO PINS)

In the HUSB251, the constant voltage loop (CV loop) compensation and constant current loop (CC loop) compensation are implemented. VIN voltage is scaled by a resistor divider to be as the feedback voltage. It is compared with the internal voltage reference to generate an error signal. The CV loop can compensate this error signal. And then the compensated signal is employed to drive the primary side of the opto-coupler and control the AC-DC power loop.

CURRENT SENSE RESISTOR

The recommended current sense resistor is 5 mΩ. The sensed current information is employed to perform OCP, SCP and Constant Current Control.

CC1 AND CC2 PINS

CC1 and CC2 pins are used to detect Type-C connection, BMC communication.

TYPE-C CC FUNCTION

CC1 and CC2 are the Configuration Channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable.

The HUSB251 monitors the status of CC1 and CC2 pins and decide which state should enter.

CC1 and CC2 can be configured as Source, Sink and DRP by firmware. And default state of CC with Rd resistor.

CC1 and CC2 are configured as Source only mode with 1.5 A and 3 A current advertising. The default R_p current on CC1 and CC2 is I_{CC_3P0}, which means 3 A current advertising.

The CC1 and CC2 can tolerance a voltage up to 30V. This is helpful for the HUSB251 to survive in the failure when the CC1 or CC2 is shorted to the VBUS pin.

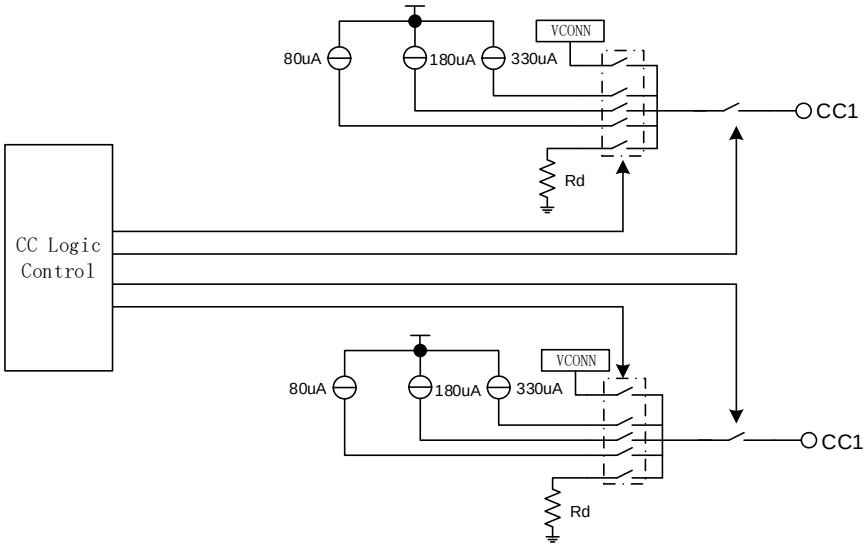


Figure 4. CCx Hardware Diagram

BMC DRIVER

Through the Type-C detection, one of the CC pins will be connected to the internal BMC block to achieve PD communication.

VBUS PIN

This pin is used to sense VBUS presence and discharge VBUS voltage on USB Type-C receptacle side.

The VBUS pin is also connected to an internal MOSFET and discharging circuitry, which is used as a bleeder to help dissipate the energy stored in the VBUS capacitor. With this bleeder, VBUS is discharged to vSafe0V upon the detachment of a connected device, or to a lower desired output voltage level upon a request command received from the Sink, such as from 20 V to 5 V.

GATE PIN

The GATE pin of the HUSB251 is designed to drive an external N-MOSFET. When the HUSB251 is attached and is ready to enable VBUS. The GATE pin outputs a voltage to turn on the external N-MOSFET. The turn on time of the external N-MOSFET may impacted by the external N-MOSFET's characteristics.

OVER VOLTAGE PROTECTION

The HUSB251 detects the VIN pin voltage to achieve over-voltage protection function. The threshold to trigger over-voltage protection can be configured as 4 options. When the over-voltage condition occurs, the firmware is notified to handle this fault.

OVER CURRENT PROTECTION

When the current sensed by the sense resistor exceeds the pre-set threshold in firmware. The threshold to trigger over-current protection can be configured by firmware. When the over-current condition occurs, the firmware is notified to handle this fault.

SHORT CIRCUIT PROTECTION

The HUSB251 integrates SCP protection function. When the VBUS is hard shorted to GND by fault, the output current increases sharply. When the output current reaches the SCP threshold, the firmware is notified to handle this fault.

OVER TEMPERATURE PROTECTION

The HUSB251 integrates a current source at OTP pin. When the OTP function is preferred, a NTC thermistor is recommended to be place at OTP pin. In addition, the internal current source outputs the current to the GND through the external thermistor. The voltage at the OTP pin can be sampled by ADC to identify the actual temperature.

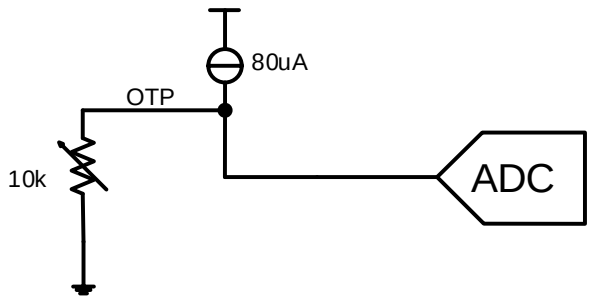


Figure 5. OTP Detection

THERMAL SHUT DOWN

When the junction temperature rises across T_{TSD}, thermal shut down takes action and the GATE is disabled. When the junction temperature falls across T_{TSD}-T_{TSD_HYS}, the HUSB251 is reset to default mode and will automatic recover again.

ANALOG-DIGITAL CONVERTER

Configured as Source or Toggled as Source:

The HUSB251 supports various fast charging protocols including PD2.0,PD3.0, BC1.2 DCP, Divider 3, QC 2.0/3.0 Class A, AFC, FCP, SCP and UFCS. According to the different status of D+ and D- pins, the HUSB251 recognizes the attached Sinks and apply the fast charging protocol automatically.

Configured as Source or Detected as Source:

Configured as Sink or Toggled as Sink:

The HUSB251 supports PD2.0, PD3.1, BC1.2;

GPIO

GPIO pins are for general purpose. GPIO pins can be configured in different work mode per the firmware settings. GPIO pins can be worked as:

Interrupt Input: the GPIO pin is a digital input pin, any digital logic level transition of GPIO pin can be configured a interrupt source to notify the MCU.

Output Pin: the GPIO pin is a digital output pin, the output state can be determined by the firmware.

ADC Input: the GPIO pin is an analog input pin, the input voltage can be sampled by ADC and reported to the MCU.

	INT	ADC	Pull UP	Pull Down	Open Drain	Direct output	I^2C	UART
GPIO0	○	○			○	○		
GPIO1	○				○	○		
GPIO2	○	○	○	○	○	○		○
GPIO3	○	○	○	○	○	○		○
GPIO4	○				○	○	○	
GPIO5	○				○	○	○	
GPIO6	○	○	○	○	○	○		
GPIO7	○	○	○	○	○	○		

I²C FUNCTION

The HUSB251 implements a Fast-mode I²C interface. This I²C can be using as master or slave just setting by firmware.

When configure GPIO as the I²C, GPIO4 as SCL and GPIO5 as SDA. It can detect the status of the input signals and drive the I²C bus when needed

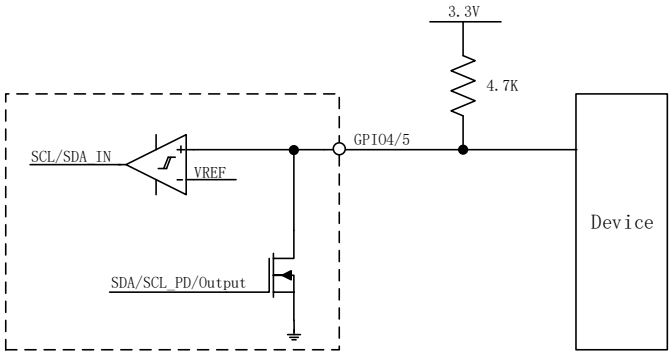
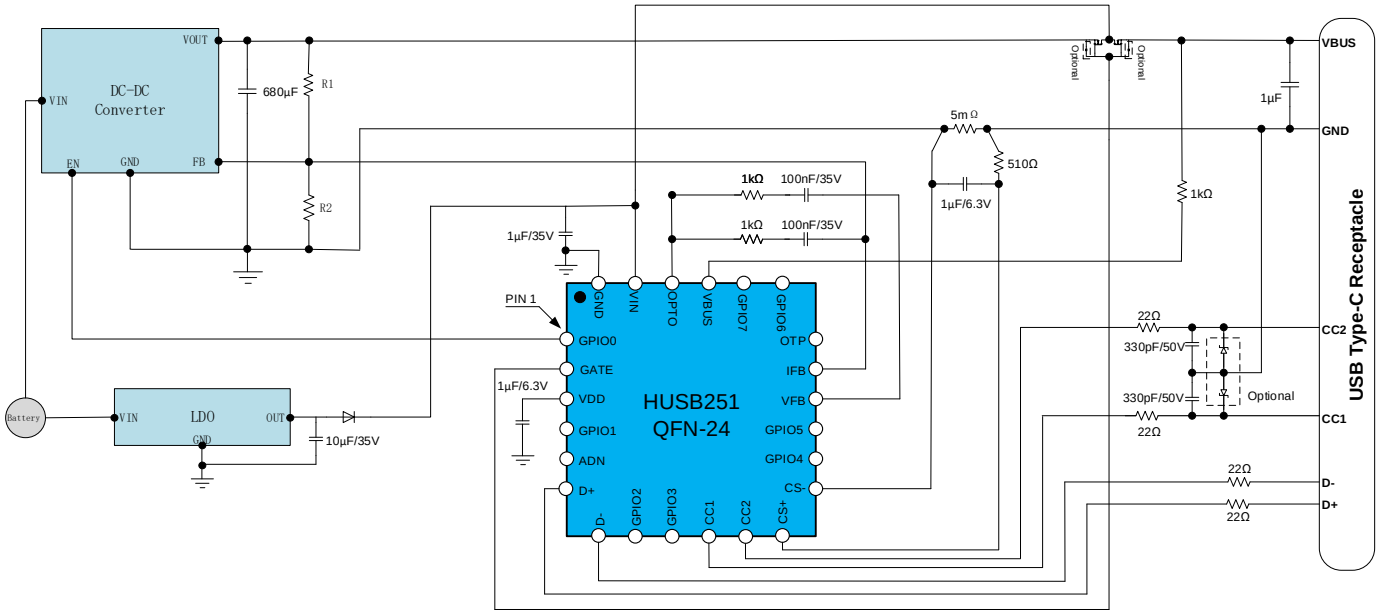


Figure 6. I²C Connection Diagram

SLEEP MODE

The HUSB251 supports deep sleep mode, and customizable sleep time. The current of VIN is not more than 1.5 mA on toggling as the DRP, when configured the appropriate sleep timer.

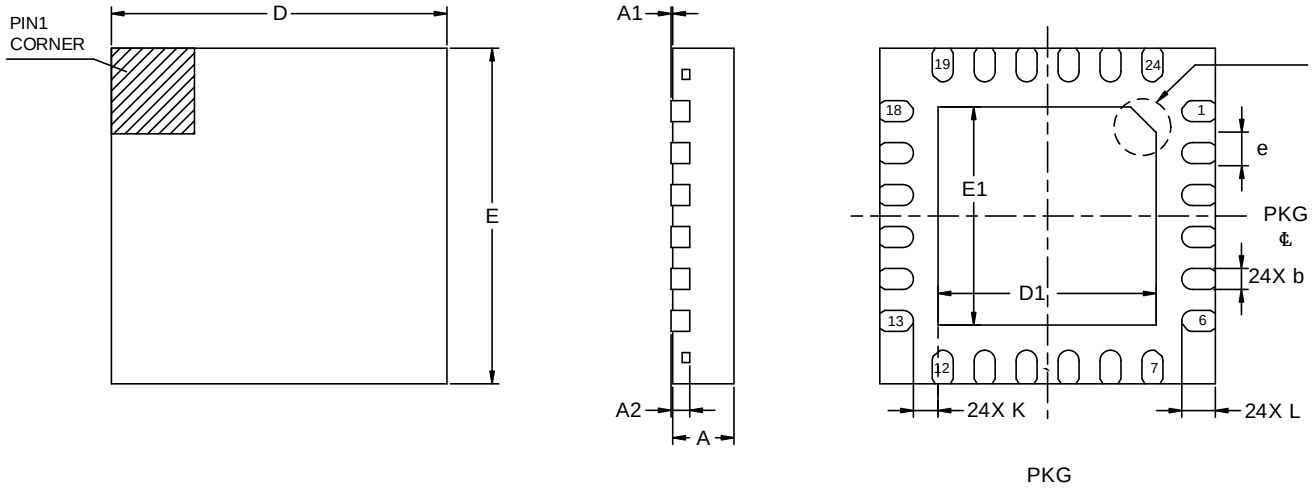
TYPICAL APPLICATION CIRCUITS



* HUSB251 IFB PIN Sink max current is 200uA; just select the Appropriate value of R1&R2 to ensure the max votage of VBUS

Figure 7. Typical Application Circuit for DRP

PACKAGE OUTLINE DIMENSIONS



TOP VIEW **SIDE VIEW**

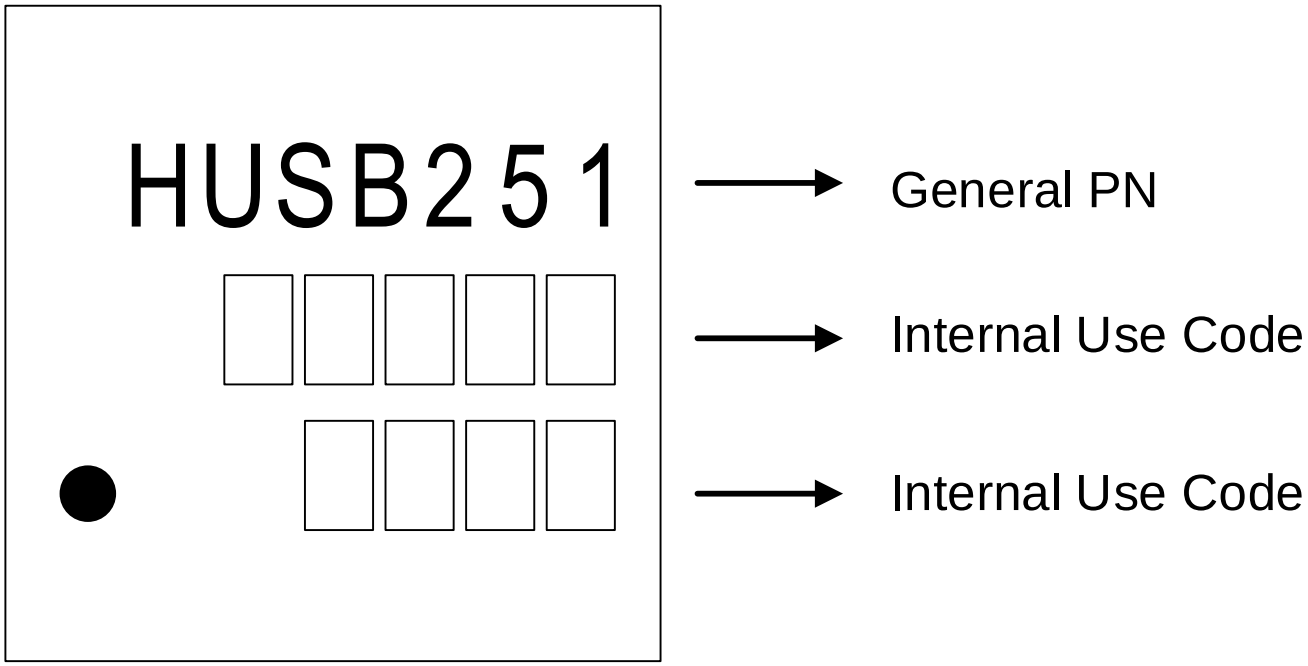
ALTERNATE A-1 ALTERNATE A-2

DETAIL A: ALTERNATE PIN#1 ID. CONSTRUCTIONS

SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.000	0.02	0.05
A2		0.203 REF	
b	0.20	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
D1	2.40	2.50	2.80
E1	2.40	2.70	2.80
e		0.50 BSC	
L	0.30	0.40	0.50
k		0.20 MIN	

Figure 8. QFN4x4-24L Package of Dimension

PACKAGE TOP MARKING



QFN4X4-24L

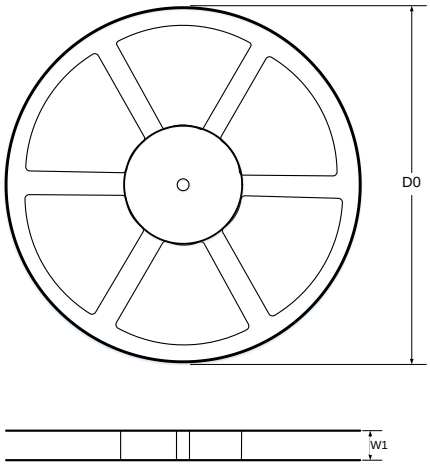
Figure 9. marking

ORDERING GUIDE

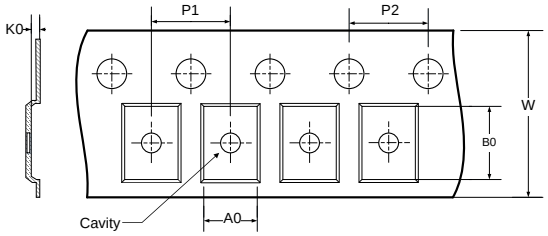
Model	Temperature Range	MSL	Package Type	Package Option	Package Qty
HUSB251-BCXXX-QN24R	-40 to 125°C	MSL3	QFN-24L, 4 mm x 4 mm	Tape & Reel	5000

TAPE AND REEL INFORMATION

REEL DIMENSIONS

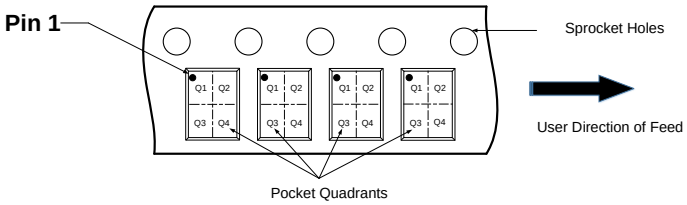


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel Diameter
W1：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
HUSB251-BC000-QN24R	QFN4X4-24L	330.00	12.40	4.30	4.30	1.10	8.00	4.00	12.00	Q1	5000

All dimensions are nominal

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