USB Type-C Port Controller with GPIO Control

Hynetek Semiconductor Co., Ltd.

HUSB320-AA000

FEATURES

- Fully Autonomous USB Type-C Port Controller
- Support USB Type-C Specification Reversion 2.1
- Source, Sink and DRP Port Role Configuration with Optional Accessary Support
- Try.SRC and Try.Snk Modes for User Configurations
- VDD Operating Range: 2.85 V to 5.5 V
- Multiple IO Voltage Support: 1.2 V, 1.8 V and 3.3 V
- Typical Low Power Operation: I_{VDD_STBY}< 30 μA
- GPIO Mode
- Maximum 28 V DC Tolerance on ID, VBUS_DET, CC1 and CC2 Pins
- Dead Battery Support
- 4 kV HBM ESD Rating for USB IO Pins
- Small Package, 12 Lead QFN (1.6 mm x1.6 mm)

APPLICATIONS

Accessories
Industrial
Power Banks

GENERAL DESCRIPTION

The HUSB320-AA000 is designed for a USB Type-C port. It integrates the CC logic detection and output the connection results per the different connection combinations. The HUSB320-AA000 is freely to be configured by user as a Source, Sink or DRP. Additionally, the debug accessories and audio accessories are both supported to be recognized.

The HUSB320-AA000 is run in GPIO mode, the configuration is achieved via the pins and the detection results are presented at these pins.

The ultra-low operation current of the HUSB320-AA000 helps the system to reduce the total power dissipation and suitable for a battery application.

TYPICAL APPLICATION CIRCUIT

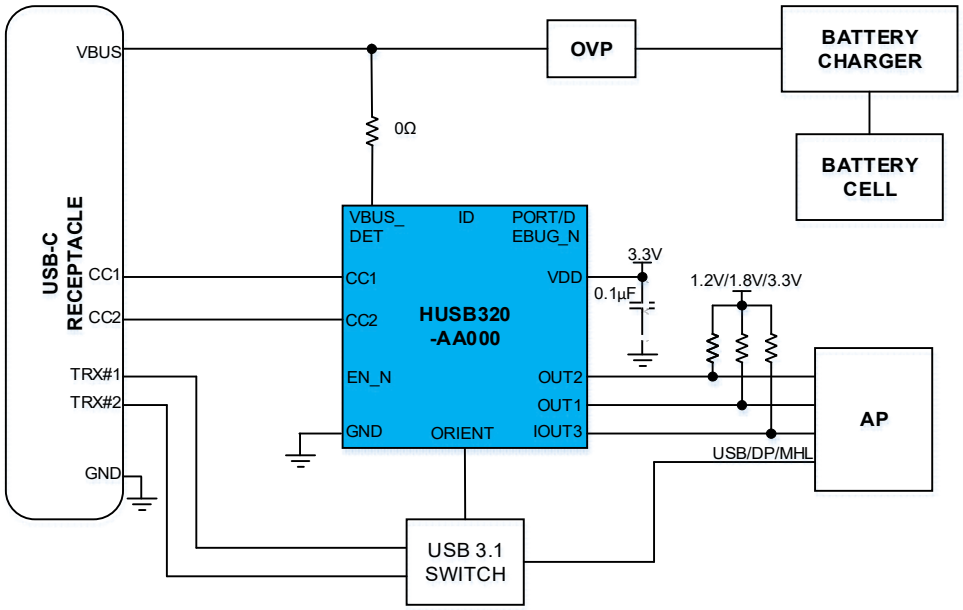


Figure 1. Typical Application Circuit

TABLE OF CONTENTS

REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	11/2022	Initial version
Rev. 1.1	01/2023	Update ORDERING GUIDE
Rev. 1.2	02/2023	Update Typical Application Circuit

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

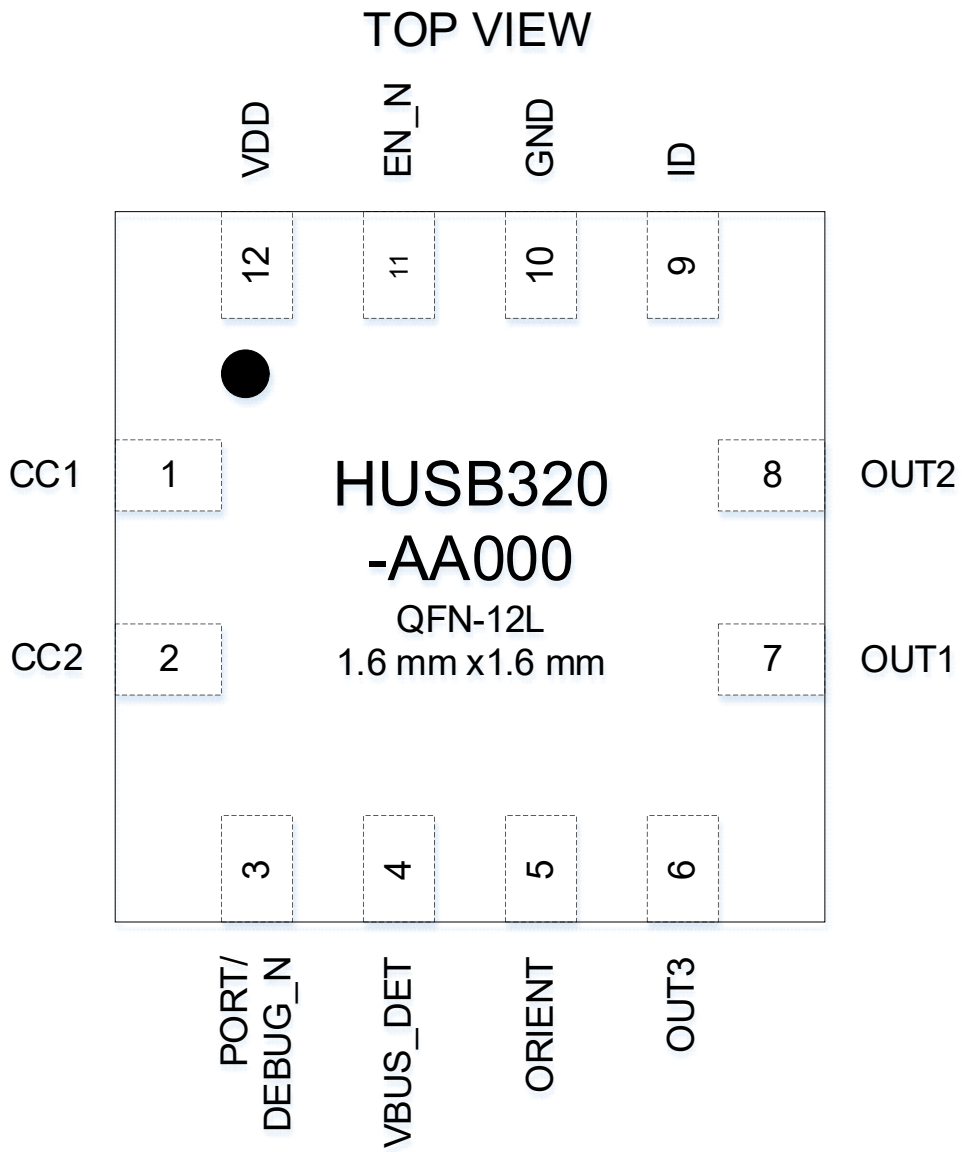


Figure 2. Pin Assignment

Table 1. Pin Function Descriptions

Pin No.	Pin Name	Type[1]	Description
1	CC1	DIO	Type-C configuration channel signal 1
2	CC2	DIO	Type-C configuration channel signal 2
3	PORT/DEBUG_N	IO	Dual function pin. In input mode, this pin (PORT) is a 3 state input to set the port role. The port role is defined as: Connected to VDD via a 900 kΩ resistor = Source Only Connected to GND via a 900 kΩ resistor = Sink Only Float = Dual Role Port (DRP) In output mode, this pin (DEBUG_N) is push-pull output to indicate the Debug Accessory Detection results.

Pin No.	Pin Name	Type[1]	Description
			Low = Debug Accessory detected
			High = Debug Accessory not detected
4	VBUS_DET	AI	VBUS voltage detection pin. It could be connected to the VBUS pin at type-C connector. It is employed for attach and detach detection. It is also the discharge path for VBUS pin when detachment happened
5	ORIENT	IO	Dual function pin. In input mode, the working mode is defined as:
			Float = GPIO mode
			In output mode, this pin (ORIENT) is push-pull output to indicate the connection status.
			Low = CC1 of USB Type-C receptacle is connected
			High = CC2 of USB Type-C receptacle is connected
6	OUT3	IO	This pin (OUT3) is an open-drain output to indicate Audio Accessory detection results:
			Low = Audio Accessory is detected
			High-Z = Audio Accessory is not detected
7	OUT1	IO	Open-drain output pin. This pin (OUT1) combined with OUT2 and ID pins to indicate the connection status
8	OUT2	IO	Open-drain output pin. This pin (OUT2) combined with OUT1 and ID pins to indicate the connection status
9	ID	O	Open-drain output pin. This pin combined is used to indicate the connection status
10	GND	P	Ground connection point
11	EN_N	AI	Chip enabled pin. It is pulled up internally and the HUSB320-AA000 is enabled by pulling this pin to GND
12	VDD	P	Input supply for internal circuitry

1 Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

RECOMMENDED OPERATING CONDITIONS

Table 2. Recommended Operating Conditions

Parameter	Rating
VDD Input Voltage	2.85 V to 5.5 V
VBUS_DET Input Voltage	4 V to 22 V
Operating Temperature Range (Junction)	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

SPECIFICATIONS

V_{VDD} = 2.85 V to 5.5 V, T_A = 25°C for typical specifications, unless otherwise noted.

Table 3. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Power Supply						
VDD UVLO Rising Threshold	$V_{VDD\_UVLO\_R}$	Power Up to normal operation		2.75	2.9	V
VDD UVLO Hysteresis	$V_{VDD\_UVLO\_HYS}$	Hysteresis Voltage to shutdown		0.08		V
VDD Leakage Current	$I_{VDD\_DISABLE}$	V_{VDD}>$V_{VDD\_UVLO\_R}$ and EN_N=High or V_{VDD}< $V_{VDD\_UVLO\_R}$ - $V_{VDD\_UVLO\_HYS}$			5	μA
VDD Standby Current	I_{VDD_STBY}	EN_H=Low and configured in Sink without attachment, V_{VDD}=4.5 V		15	30	μA
		EN_H=Low and configured in Source or DRP without attachment, V_{VDD}=4.5 V		15	30	μA
VDD Operating Current	I_{VDD_OP}	EN_H=Low and attached as a Sink or Source, V_{VDD}=4.5 V		15	30	μA
Open Drain Output Pins (ID, OUT1, OUT2 OUT3)						
Output Low Voltage	V_{OL_OD}	Sink current=2 mA			0.4	V
Output Low Resistance	R_{OL_OD}				200	Ω
Input Pin (EN_N)						
Internal Pull Up Resistance	R_{PU_EN}	To VDD pin		6		MΩ
Low Level Input Threshold	V_{IL_EN}				0.4	V
High Level Input Threshold	V_{IH_EN}		0.8			V
Enable Time	t_{EN}	From EN_N=Low to HUSB320-AA000 is ready to output stable status			100	ms
Input and Output Pins (PORT/DEBUG_N, ORIENT)						
Low Level Input Threshold	V_{IL_ORIENT}				0.2·V_{VDD}	V
Middle Level Input Threshold	V_{IM_ORIENT}		0.44·V_{VDD}		0.56·V_{VDD}	V
High Level Input Threshold	V_{IH_ORIENT}		0.8·V_{VDD}			V
Impedance to VDD	Z_{float}	Pins are floating		3.3		MΩ
Output Low Voltage	V_{OL_PP}	Sink current=1 mA			0.2·V_{VDD}	V
Output High Voltage	V_{OH_PP}	Source current=1 mA	0.8·V_{VDD}			V
Type-C Pins (CC1, CC2)						
Default R_p Current	I_{RP_DEF}	V_{VDD} ≥ 3.5 V	64	80	96	μA
1.5 A R_p Current	$I_{RP\_1.5A}$	V_{VDD} ≥ 3.5 V	165.6	180	194.4	μA
3 A R_p Current	I_{RP_3A}	V_{VDD} ≥ 3.5 V	303.6	330	356.4	μA
Dead Battery Clamp Voltage	V_{SNKDB0}	Configured as Sink with 80 μA ±20% R_p Current from Source, V_{VDD}< $V_{VDD\_UVLO\_R}$	0.25		1.5	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
	V_{SNKDB1}	Configured as Sink with 180 µA ±8% R_p Current from Source, V_{VDD} < $V_{VDD\_UVLO\_R}$	0.45		1.5	V
	V_{SNKDB2}	Configured as Sink with 330 µA ±8% R_p Current from Source, V_{VDD} < $V_{VDD\_UVLO\_R}$	0.85		2.18	V
Sink Pull Down Resistor	R_d		4.6	5.1	5.6	kΩ
CC Impedance	z_{OPEN}	CC1 or CC2 are disabled from applying R_p or R_d	1000			kΩ
R_a Detection Threshold as Source	$vRa_{\_SRCDEF}$	Configured as Source with I_{RP_DEF}	0.15	0.2	0.25	V
	$vRa_{\_SRC1.5A}$	Configured as Source with $I_{RP\_1.5A}$	0.35	0.4	0.45	V
	$vRa_{\_SRC3A}$	Configured as Source with I_{RP_3A}	0.75	0.8	0.85	V
R_d Detection Threshold as Source	$vRd_{\_SRCDEF}$	Configured as Source with I_{RP_DEF}	1.55	1.6	1.65	V
	$vRd_{\_SRC1.5A}$	Configured as Source with $I_{RP\_1.5A}$	1.55	1.6	1.65	V
	$vRd_{\_SRC3A}$	Configured as Source with I_{RP_3A}	2.45	2.6	2.75	V
R_a Detection Threshold as Sink	$vRa_{\_SNK}$	Configured as Sink	0.15	0.2	0.25	V
R_d Detection Threshold as Sink	$vRd_{\_SNKDEF}$	Configured as Sink with I_{RP_DEF} attached	0.61	0.66	0.7	V
	$vRd_{\_SNK1.5A}$	Configured as Sink with $I_{RP\_1.5A}$ attached	1.16	1.23	1.31	V
	$vRd_{\_SNK3A}$	Configured as Sink with I_{RP_3A} attached	2.04	2.11	2.18	V
VBUS Present Rising Threshold	vVB_{PRS_R}	Rising edge to set VBUSOK=1b	3.67	4	4.4	V
VBUS Present Hysteresis	vVB_{PRS_HYS}	Hysteresis voltage to set VBUSOK=0b		0.7		V
VBUS Present Debounce	t_{DEB_VB}	Debounce time for valid VBUSOK flag	250	375	500	µs
vSafe0V Falling Threshold	v_{Safe0V_F}	Falling edge to set vSafe0V=1b		0.8		V
vSafe0V Hysteresis	v_{Safe0V_HYS}	Hysteresis Voltage to set vSafe0V=0b		20		mV
vSafe0V Debounce	$t_{DEB\_vSafe0V}$	Debounce time for valid VBUSOK flag	250	375	500	µs
VBUS_DET Discharge Resistance	R_{DSCHG_VB}	VBUS_DET to GND path resistance when detachment event happens		2		kΩ
AUTOSNK Threshold	$v_{AUTOSNKth0}$	CONTROL1[6:5]=00b	2.9	3.0	3.1	V
	$v_{AUTOSNKth1}$	CONTROL1[6:5]=01b	3.0	3.1	3.2	V
	$v_{AUTOSNKth2}$	CONTROL1[6:5]=10b	3.1	3.2	3.3	V
	$v_{AUTOSNKth3}$	CONTROL1[6:5]=11b	3.2	3.3	3.4	V

Table 4. Timing Parameters

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Global Timing						
Input Lock Time	t_{IOLOCK}	Time for input and output pins to sample input signal		10		ms
AUTOSNK Debounce Time	$t_{AUTOSNK}$	Debounce time for entering or exiting AUTOSNK mode if it is enabled		15		ms
Enable Time	t_{EN}	From EN_N=Low to HUSB320-AA000 is ready to output stable status			100	ms
Type-C Timing						
CC Attach Debounce Time	$t_{CCDebounce0}$			150		ms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
WaitSink Debounce Time for Detach	$t_{PDDebounce}$		10	15	20	ms
AttachedSink Debounce Time for Detach	$t_{SinkDisconnect2}$			0		ms
Wait time for Attach in Try Action	$t_{TryCCDebounce}$		10		20	ms
Sink Detection Time for R_p Change	$t_{RpValueChange}$		10		20	ms
Source Debounce Time for Detach	$t_{SRCDisconnect}$				20	ms
Error Recovery Duration	$t_{ErrorRecovery}$		25	50	100	ms
Toggling Period	t_{DRP1}			70		ms
SNK Duration in DRP Toggling	$t_{DRPtogSNK0}$			60		%
SRC Duration in DRP Toggling	$t_{DRPtogSRC0}$			40		%

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
VDD, PORT/DEBUG_N, ORIENT, EN_N, OUT3 Pins	-0.3 V to 6.5 V
CC1, CC2, VBUS_DET, ID Pins	-0.3 V to 28 V
OUT1, OUT2 Pins	-0.3 V to 6.5 V
Operating Temperature Range (Junction)	−40°C to 125°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model (CC1, CC2, VBUS_DET Pins)	±4000 V
Human Body Model (Other Pins)	±2000 V
Charged Device Model	±500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN1.6x1.6-12L	164.4	47.1	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

FUNCTIONAL BLOCK DIAGRAM

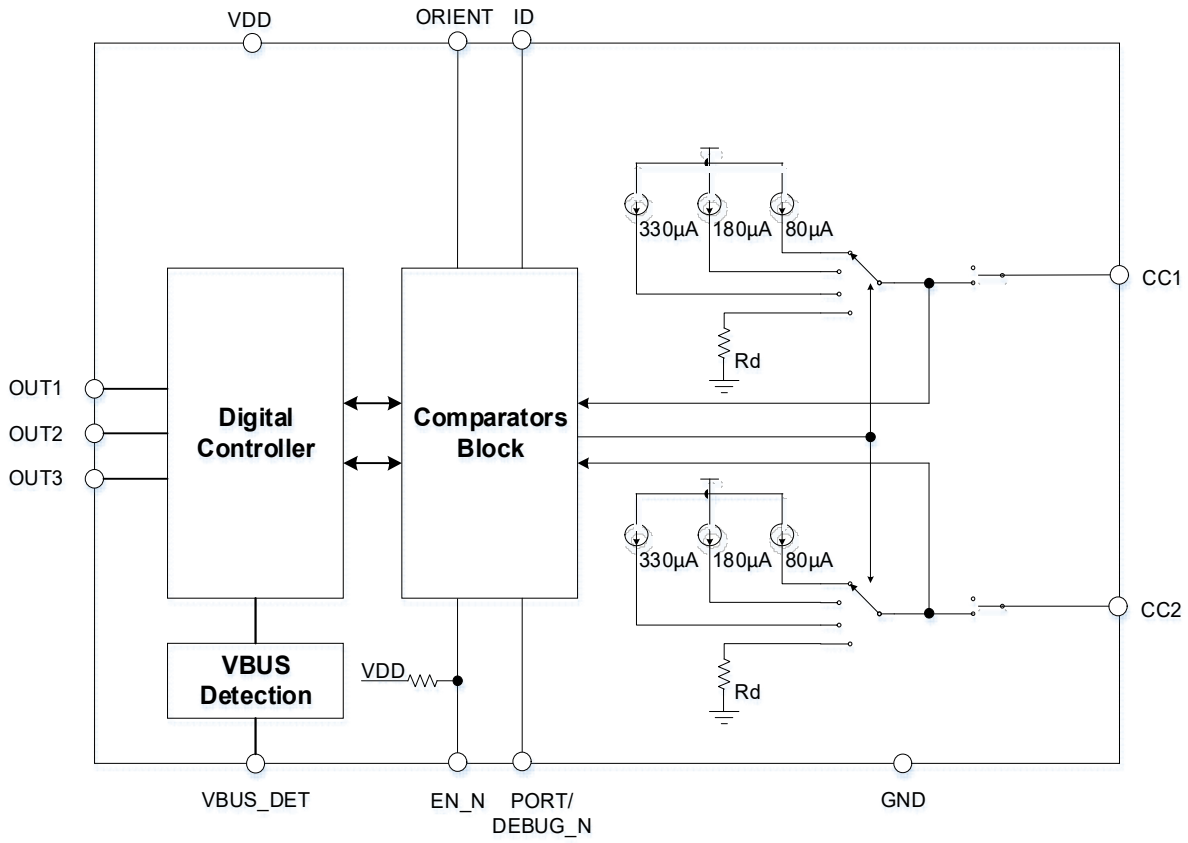


Figure 3. HUSB320-AA000 Functional Block Diagram

THEORY OF OPERATION

The HUSB320-AA000 is a CC logic controller, which can support most of the Type-C functions. It integrates all of necessary function blocks which are necessary in Type-C mode. Besides the typical Type-C roles functions including Source, Sink and DRP, the HUSB320-AA000 also supports to detect a Type-C port with accessories.

ENABLE CONTROL

The HUSB320-AA000 has an enable pin (EN_N) for the whole system control. This pin is pulled up by R_{PU_EN} internally. There is an input comparator implemented for this input voltage. This output of this comparator is going to enable the whole system control.

VDD AND INITIALIZATION

The HUSB320-AA000 is powered by VDD pin. It has an internal UVLO for its power input VDD voltage (V_{VDD}). When V_{VDD} is lower than $V_{VDD\_UVLO\_R}$, all of pins are in HIZ mode (not include CC pins configured as Sink or DRP). With the increase of VDD voltage to exceed the $V_{VDD\_UVLO\_R}$, the HUSB320-AA000 start initialization.

DOWNLOAD

With the ready status of VDD and the HUSB320-AA000 is enabled, the digital core start to download the trim values and default settings for the internal memory and registers. Only when download is completed, the HUSB320-AA000 starts to configure the blocks by the download values.

INITIALIZATION

After the download, the HUSB320-AA000 enables initialization. The input function of input and output pins (PORT/DEBUG_N and ORIENT pins) is selected during this initialization process. The HUSB320-AA000 samples the input status of these pins in t_{IOLOCK} and updates port role configuration register. Then the HUSB320-AA000 switches these pins to output status, the HUSB320-AA000 is ready to run normal operation and the initialization is done.

During initialization, PORT/DEBUG_N is an input pin for determining the role of the HUSB320-AA000. With different connections, the role of the HUSB320-AA000 is set as Table 7.

Table 7. Port Role Configuration

PORT/DEBUG_N Connection	HUSB320-AA000 Role Configured
Connected to VDD via a 900 kΩ Resistor	Source only
Floating	DRP
Connected to GND via a 900 kΩ Resistor	Sink only

With the sampled status of PORT/DEBUG_N pin, the role settings are updated at Register PORTROLE[2:0].

For ORIENT pin, it is employed to select whether the HUSB320-AA000 works as GPIO mode. As shown in Table 8 :

Table 8. Work Mode Configuration

ORIENT Connection	HUSB320-AA000 Role Configured
Floating	**GPIO mode**

POWER OFF

If the VDD falls under ($V_{VDD\_UVLO\_R}$-$V_{VDD\_UVLO\_HYS}$) any time, all of the internal circuit would be reset and wait for the next rising of VDD.

VBUS_DET PIN

The VBUS_DET pin is employed to sense the VBUS pin of USB type-C port. It can indicate the VBUS voltage status per two signals. The signals of VBUSOK and vSafe0V are sent to digital block to help determine the attach or detach status.

Besides, VBUS_DET pin has implemented an internal discharge resistor to dissipate the energy stored in the VBUS capacitors when needed.

GPIO PINS

After the initialization, the HUSB320-AA000 is able to output the status of current connection. When ORIENT pin is floating during initialization, the HUSB320-AA000 is in GPIO mode. In this mode, the OUT1, OUT2, OUT3 pins are repopulated as output pins.

OUT3

The OUT3 pin is an open drain output pin, which indicates the Audio Accessory detection results in Table 9:

Table 9. OUT3 Pin Definition

OUT3 Status	Description
Low	HUSB320-AA000 enters AudioAccessory State
High-Z	HUSB320-AA000 is not in AudioAccessory State

OUT2 AND OUT1

The OUT2 and OUT1 pin are combined to indicate the attached status in Table 9 and Table 9:

Table 10. OUT1 and OUT2 Pin Definition when Enable the PORT pin output mode

ID Status	OUT1 Status	OUT2 Status	Description
High-Z	High-Z	Low	Unattached
High-Z	High-Z	High-Z	SNK with Default R_p
High-Z	Low	High-Z	SNK with 1.5A R_p
High-Z	Low	Low	SNK with 3A R_p
Low	High-Z	High-Z	SRC with Default R_p
Low	Low	High-Z	SRC with 1.5A R_p
Low	Low	Low	SRC with 3A R_p
Low	High-Z	Low	Reserved

ID PIN

The ID pin is an open drain output that indicate the HUSB320-AA000 connection status in Table 9:

Table 11. ID Pin Definition

ID Status	Description
Low	Attached as a Source
High-Z	Attached as a Sink or unattached

DEBUG_N PIN

The DEBUG_N pin is a push-pull output that indicate the HUSB320-AA000 connection status in Table 9:

Table 12. DEBUG_N Pin Definition

DEBUG_N Status	Description
Low	Debug Accessory detected
High	Debug Accessory not detected

ORIENT PIN

The ORIENT pin is a push-pull output that indicate the HUSB320-AA000 connection status.

DEAD BATTERY

DB STATE

When the VDD voltage is lower than $V_{VDD\_UVLO\_R,}$ the HUSB320-AA000 supports the dead battery features on both CC1 and CC2 pins. In DB State, The CC1 and CC2 pin is clamped to be lower than V_{SNKDB} when there is an R_p connected to CC1 or CC2 pins (R_d/R_d). There is not any other function enabled expect the EN_N detection.

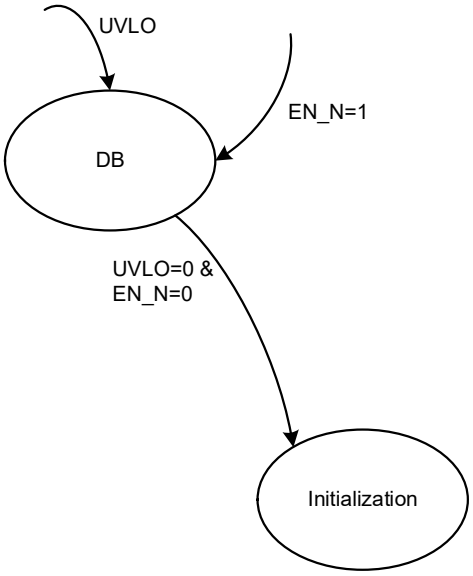


Figure 4. Dead Battery Timing

CC LOGIC

The HUSB320-AA000 is able to support the USB Type-C Rev.2.1. It integrates the necessary function blocks for all of Type-C operations. CC1 and CC2 pins are used to detect the attachment/detachment with the external devices.

With different configurations, the HUSB320-AA000 is possible connected with different terminations. These possible termination could be R_p current source when the HUSB320-AA000 is configured as a Sink, R_d when the HUSB320-AA000 is configured as a Source or R_a in a eMarker cable or accessory.

The valid Ra, Rd or R_p are defined as below:

Table 13. Possible Connected External Terminations

External Termination	Min	Typ	Max	Unit
R_a	0.8	1	1.2	kΩ
R_d	4.6	5.1	5.6	kΩ
Default R_p Current Source	64	80	96	μA
Resistor to 3.3 V	28.8	36	43.2	kΩ
Resistor to 5 V	44.8	56	67.2	kΩ
1.5 A R_p Current Source	166	180	194	μA
Resistor to 3.3 V	11.4	12	12.6	kΩ
Resistor to 5 V	20.9	22	23.1	kΩ
3 A R_p Current Source	304	330	356	μA
Resistor to 3.3 V	4.46	4.7	4.93	kΩ
Resistor to 5 V	9.5	10	10.5	kΩ

AUTOSNK FUNCTION

The HUSB320-AA000 monitors the VDD voltage. There is an internal comparator connected to VDD pin, if the VDD voltage is lower than AUTOSNK_TH, the HUSB320-AA000 will trigger the port role transition. If VDD voltage rises back to be higher than AUTOSNK_TH, AUTOSNK function is deactivated.

TYPICAL APPLICATION CIRCUITS

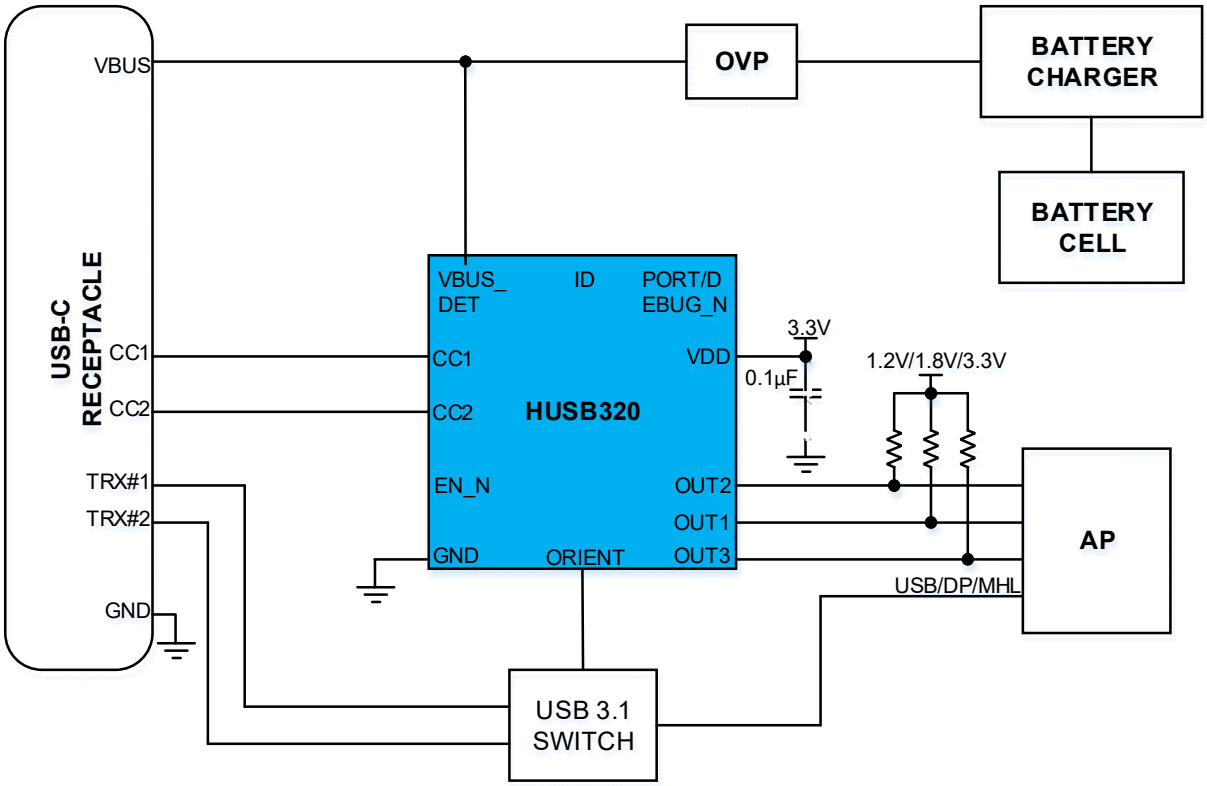
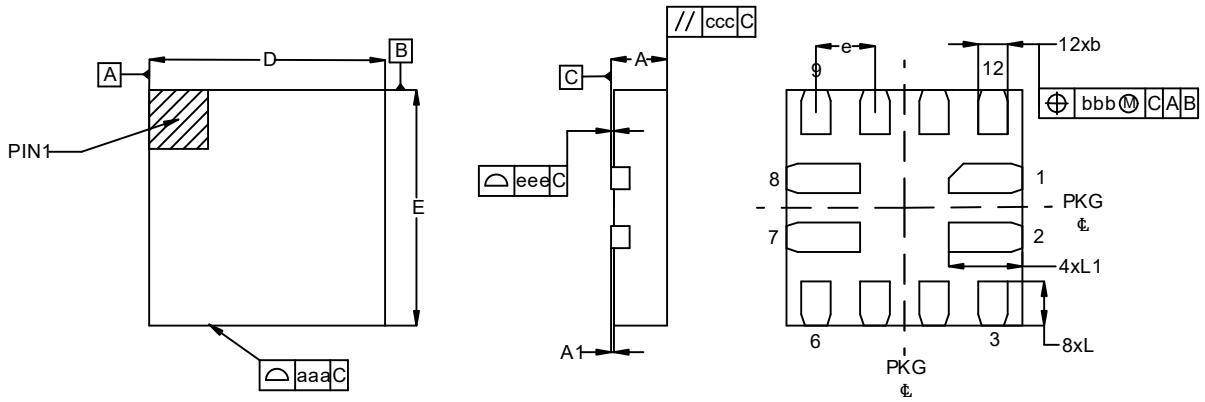


Figure 5. Typical Application

PACKAGE OUTLINE DIMENSIONS



TOP VIEW SIDE VIEW BOTTOM VIEW

	DIMENSION IN MILLIMETERS		
SYMBOLS	MIN	NOM	MAX
A	0.31	0.37	0.40
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D		1.60 BSC	
E		1.60 BSC	
e		0.40 BSC	
L	0.25	0.30	0.35
L1	0.45	0.50	0.55
aaa		0.10	
bbb		0.07	
ccc		0.10	
eee		0.08	

Figure 6. QFN1.6x1.6-12L Package of Dimension

PACKAGE TOP MARKING

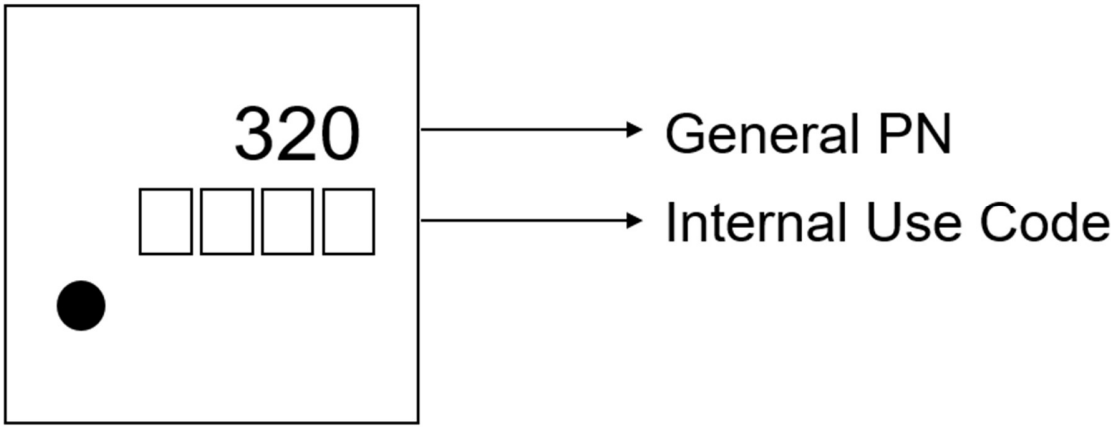
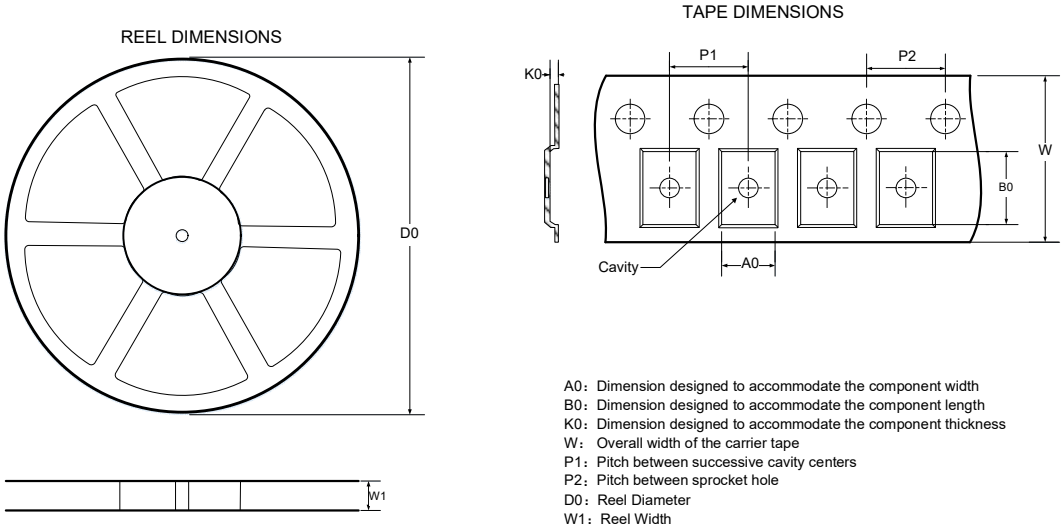


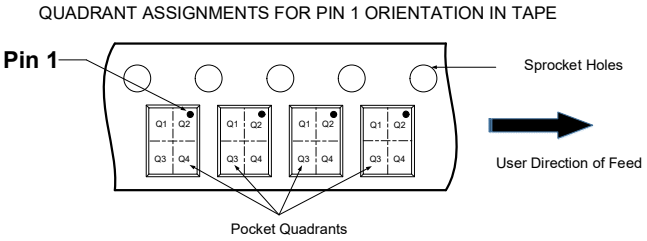
Figure 7. Package Top Marking

ORDERING GUIDE

Model	Configurations	T_J Temp (°C)	Package Type	Package Option
HUSB320-AA000-QN12R	VBUS_DET pin External resistor 0 Ω ; Enable the ORIENT and PORT pin output mode	-40 to 125	QFN1.6x1.6-12L	T&R, 3k

TAPE AND REEL INFORMATION





DIMENSIONS AND PIN1 ORIENTATION

D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
178.00	9.50	1.80	1.80	0.45	4.00	4.00	8.00	Q2	3000

All dimensions are nominal

Figure 8. Tape and Reel Information

IMPORTANT NOTICE

Hynetek Semiconductor Co., Ltd. and its subsidiaries (Hynetek) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to Hynetek’s terms and conditions of sale supplied at the time of order acknowledgment.

Hynetek warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in Hynetek’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent Hynetek deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

Hynetek assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using Hynetek components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Hynetek does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Hynetek components or services are used. Information published by Hynetek regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Hynetek under the patents or other intellectual property of Hynetek.

Reproduction of significant portions of Hynetek information in Hynetek data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Hynetek is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of Hynetek components or services with statements different from or beyond the parameters stated by Hynetek for that component or service voids all express and any implied warranties for the associated Hynetek component or service and is an unfair and deceptive business practice.

Hynetek is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Hynetek components in its applications, notwithstanding any applications-related information or support that may be provided by Hynetek. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify Hynetek and its representatives against any damages arising out of the use of any Hynetek components in safety-critical applications.

In some cases, Hynetek components may be promoted specifically to facilitate safety-related applications. With such components, Hynetek’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No Hynetek components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those Hynetek components which Hynetek has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of Hynetek components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

Hynetek has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, Hynetek will not be responsible for any failure to meet ISO/TS16949.

Please refer to below URL for other products and solutions of Hynetek Semiconductor Co., Ltd.