USB Type-C and PD Source Controller

Hynetek Semiconductor Co., Ltd.

HUSB338C

FEATURES

- **USB Type-C 2.0 and USB PD3.0 Compliance Certified, TID: 1000189, XID: 0005399**
  - **Support 5V, 9V and 12V FPDOs**
  - **Support 5V Prog and 9V Prog APDOs**
- **Support BC1.2 DCP and HVDCP Protocols**
  - **BC1.2 DCP Mode**
  - **Apple Divider 3 Mode**
  - **QC2.0/3.0 Class A**
  - **AFC**
  - **FCP and SCP**
- **External N-MOSFET Supported**
- **Support Constant Voltage Loop (CV) and Constant Current Loop (CC) Operation**
- **Additional 7 Power Levels Configured by PS0, PS1 Pins**
- **Integrated OVP, UVP, UVLO, OCP, FOCP and TSD Protections**
- **16-Lead Plastic QFN (3mm × 3mm) Package**
- **±4kV HBM ESD Rating for USB IO Pins**

APPLICATIONS

AC-DC Power Adaptor
Car Charger

GENERAL DESCRIPTION

The HUSB338C is a high performance, high integration USB Type-C Power Delivery source controller. The HUSB338C supports PD2.0, PD3.0, PPS, QC2.0/3.0, BC1.2 DCP, AFC, FCP and SCP protocols. It supports 5V, 9V and 12V three FPDOs and 5V Prog, 9V Prog two APDOs which are fully compliant with USB Power Delivery Specification Revision 3.0, version 2.0.

The HUSB338C integrates all required protections such as Over Voltage Protection (OVP), Under Voltage Protection (UVP), Under Voltage Lock Out (UVLO), Over Current Protection (OCP), Fast Over Current Protection (FOCP) and Thermal Shut Down (TSD).

It is available in QFN-16L, 3mm x 3mm package.

TYPICAL APPLICATION CIRCUIT

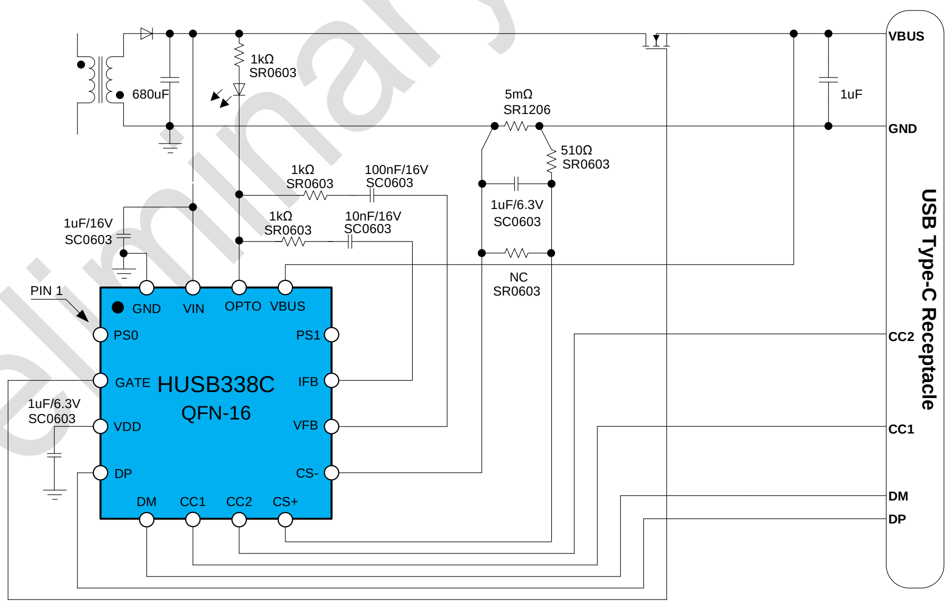

Figure 1. Typical Application Circuit

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REVISION HISTORY

Version	Date	Owner	Descriptions
Rev. 0.0	10/2021	Yingyang Ou	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

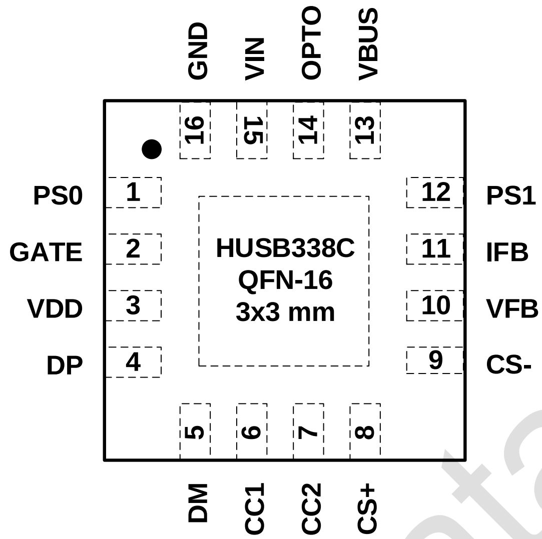


Figure 2. Pin Configuration (Top View)

Table 1. Pin Function Descriptions

Pin No.	Pin Name	Type[1]	Description
1	PS0	AI	Power selection input 0. Connect to ground or VDD, or keep floating can determine the output power level, combined with PS1 pin.
2	GATE	AO	N-MOSFET Gate driver output for VBUS load switch.
3	VDD	P	Internal 3.3V regulator output for system power.
4	DP	DIO	USB D+ line.
5	DM	DIO	USB D- line.
6	CC1	AIO	USB Type-C CC1 line.
7	CC2	AIO	USB Type-C CC2 line.
8	CS+	AI	Positive input of the current sense amplifier.
9	CS−	AI	Negative input of the current sense amplifier.
10	VFB	AI	Feedback point of Constant Voltage (CV) loop, connect CV compensation network to this pin.
11	IFB	AI	Feedback point of Constant Current (CC) loop, connect CC compensation network to this pin.
12	PS1	AI	Power selection input 1. Connect to ground or VDD, or keep floating can determine the output power level, combined with PS0 pin.
13	VBUS	AI	VBUS sense and discharge pin.
14	OPTO	AI	OPTO driver.
15	VIN	P	Supply voltage input. Connect this pin to GND via a recommended 1μF ceramic capacitor.
16	GND	P	Power ground.

1 Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

SPECIFICATIONS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Supply Voltage	V_{IN}		3.3		12	V
Supply Voltage UVLO Threshold	V_{IN_UVLO}	Rising edge		3.0		V
Supply Voltage UVLO Hysteresis	$V_{IN\_UVLO\_HYS}$			250		mV
Supply Current	I_{CC}	CC is attached, normal operation		2.6		mA
Quiescent Current	I_Q	CC1 and CC2 pins are floating		550		μA
VDD						
Internal Regulator Output	V_{DD}			3.3		V
Type-C						
1.5A Mode Pull-Up Current Source	I_{CC_1P5}		166	180	194	μA
3.0A Mode Pull-Up Current Source	I_{CC_3P0}		304	330	356	μA
UFP Detection Threshold at 1.5A Current	V_{TH_1A5}		1.51	1.6	1.64	V
UFP Detection Threshold at 3.0A Current	V_{TH_3A0}		2.46	2.6	2.74	V
BMC COMMAN PARAMETERS						
Bit Rate	$f_{BitRate}$		270	300	330	Kbps
BMC TX PARAMETERS						
Falling Time	t_{Fall}	10% and 90% amplitude points, unloaded condition	300			ns
Rising Time	t_{Rise}	10% and 90% amplitude points, unloaded condition	300			ns
Voltage Swing	V_{Swing}	CC pull down resistor > 800Ω	1.05	1.125	1.2	V
Transmitter Low Voltage	V_{Low}	CC pull down resistor > 800Ω	-75		75	mV
Transmitter Output Impedance	Z_{Driver}	Source output impedance at 750kHz with CC attached	35	55	75	Ω
BMC RX PARAMETERS						
RX Bandwidth Limiting Filter	$t_{RXFilter}$	Time constant of a single pole filter	100			ns
Input Signal Hysteresis				160		mV
Receiver Input Impedance	Z_{BMC_RX}		1			MΩ
BC1.2 DCP MODE						
DP and DM Shorting Resistance	R_{DPM_SHORT}	V_{DP} = 0.6V		20	40	Ω
DP Leakage Resistance	R_{DP_LKG}	V_{DP} = 0.6V		800		kΩ
DM Leakage Resistance	R_{DM_LKG}	V_{DM} = 0.6V		800		kΩ
APPLE DIVIDER3 MODE						
DP Output Voltage	V_{DP_APP}	V_{IN} = 5V		2.7		V
DM Output Voltage	V_{DM_APP}	V_{IN} = 5V		2.7		V
DP Output Impedance	R_{DP_PAD}	I_{DP} = −5μA		30		kΩ
DM Output Impedance	R_{DM_PAD}	I_{DM} = −5μA		30		kΩ
HVDCP MODE						
Output Voltage Selection Reference	V_{SEL_REF}			2.0		V
Data Detect Voltage	V_{DAT_REF}			0.325		V
DP High Glitch Filter Time	$T_{GLITCH\_BC\_MODE}$		1	1.25	1.5	S
DM Low Glitch Filter Time	$T_{GLITCH\_DM\_LOW}$		1	2		ms
Output Voltage Glitch Filter Time	$T_{GLITCH\_V\_CHANGE}$		20	40	60	ms
DM Pull-Down Resistance	R_{DM_DWM}			15		kΩ
QC MODE						

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Pulse Glitch Filter Time	$T_{GLITCH\_CONT\_CHANGE}$	For QC3.0 in continues mode	100	150	200	µs
FCP MODE						
DM FCP TX Valid Output High	V_{TX_VOH}		2.55		3.6	V
DM FCP TX Valid Output Low	V_{TX_VOL}				0.3	V
DM FCP RX Valid Input High	V_{RX_VIH}		1.4		3.6	V
DM FCP RX Valid Input Low	V_{RX_VIL}				1	V
DM Output Pull-Low Resistance	R_{DMPL}			500		Ω
Unit Interval for FCP	UI			160		µs
VOLTAGE CONTROL (VFB PIN)						
Voltage Sense Scaling Factor				10		
VIN Step LSB				20		mV
Default Voltage	V_{IN_DEF}	CC is unattached		5.1		V
VIN Regulation Accuracy		VIN=3.3-12V	-5		5	%
CURRENT CONTROL (CS+, CS−, IFB PINs)						
Current Sense Resistor				5		mΩ
GATE PIN						
Driver Voltage		Refer to VIN		5		V
Sourcing Current		EN_GATE = 1		20		µA
Pull Down Resistance		EN_GATE transition from 1 to 0		200		Ω
OPTO PIN						
Minimum OPTO Current				30		µA
Maximum Pull Down Current				3		mA
OVER VOLTAGE PROTECTION						
OVP Protection Threshold	V_{IN_OV}	Reference to internal V_{IN} reference	115	120	125	%
OVP De-bounce Time	t_{OV_DEB}			10		µs
UNDER VOLTAGE PROTECTION						
UVP Protection Threshold	V_{IN_UV}	Reference to internal V_{IN} reference	75	80	85	%
UVP De-bounce Time	t_{UV_DEB}			1		ms
OVER CURRENT PROTECTION						
OCP Protection Threshold	I_{IN_OC}	Reference to internal I_{IN} reference	115	120	125	%
OCP De-bounce Time	t_{OC_DEB}			2.5		ms
FOCP Protection Threshold	I_{IN_SCP}			6		A
THERMAL SHUT DOWN						
Thermal Shut Down Threshold	T_{TSD}			150		ºC
Thermal Shut Down Hysteresis	T_{TSD_HYS}			20		ºC

RECOMMENDED OPERATING CONDITIONS

Table 3.

Parameter	Rating
VIN Input Voltage	3.15V to 12.6V
Operating Junction Temperature Range (T_J) Ambient Temperature Range (T_A)	−40°C to 125°C -40°C to 85°C

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN, VBUS, OPTO	−0.3V to 16V
GATE	−0.3V to 24V
CC1, CC2	−0.3V to 16V
VDD, DP, DM, CS+, CS−, VFB, IFB	−0.3V to 7V
Junction Temperature Range	−40°C to +150°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Mode (CC1, CC2, DP, DM and VBUS pins)	4000V
Human Body Mode (Other pins)	2000V
Machine Mode	500V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

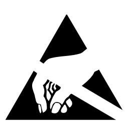
θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN-16L, 3mm x 3mm	TBD	TBD	°C/W

ESD CAUTION



Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

VIN PIN

VIN pin is the power supply input, which is derived from the output of the AC-DC or DC-DC converter. Connect a 1µF decoupling MLCC between VIN pin and GND pin.

The VIN pin is also connected to an internal MOSFET and discharge resistor, which is used as a bleeder to help discharge the energy stored in the output capacitor. With this bleeder, VIN can be regulated to vSafe5V upon the detachment of a connected device, or to a lower desired output voltage level upon a request command received from the Sink, such as from 12V to 5V.

VDD PIN

An internal liner regulator is used to provide 3.3V for internal circuits. Connect a 1µF MLCC to VDD pin for decoupling.

CONTROL LOOP COMPENSATION CIRCUIT (VFB, CS+, CS−, IFB, OPTO PINS)

In the HUSB338C, the constant voltage loop (CV loop) compensation and constant current loop (CC loop) compensation are implemented. VIN voltage is scaled by a resistor divider to be as the feedback voltage. It is compared with the internal voltage reference to generate an error signal. The CV loop can compensate this error signal. And then the compensated signal is employed to drive the primary side of the opto-coupler and control the AC-DC power loop.

SLEW RATE CONTROL

The HUSB338C implements a fixed voltage slew rate, which is 83mV/ms.

IR COMPENSATION

IR compensation is only available when VIN is set to 5V. If PPS function is enabled, IR compensation will be disabled even if 5V APDO is selected.

Four options of IR compensation are available: 0mV/A, 50mV/A, 100mV/A and 150mV/A. IR compensation can be customized by Hynetek. The default IR compensation is 100mV/A.

For example, if 100mV/A IR compensation is selected, then for the 5V/3A condition (except 5V APDO), the actual VIN voltage is:

$$5V + 3A \times 100mV/A = 5.3V$$

CURRENT SENSE RESISTOR

The recommended current sense resistor is 5mΩ. The sensed current information is employed to perform OCP, FOCP and Constant Current Control.

CC1 AND CC2 PINS

CC1 and CC2 pins are used to detect Type-C connection, BMC communication.

TYPE-C CC FUNCTION

CC1 and CC2 are the Configuration Channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable.

The HUSB338C monitors the status of CC1 and CC2 pins and decide which state the HUSB338C should enter.

CC1 and CC2 are configured as Source only mode with 1.5A and 3A current advertising. The default R_p current on CC1 and CC2 is I_{CC_3P0}, which means 3A current advertising.

The CC1 and CC2 can tolerance a voltage up to 16V. This is helpful for the HUSB338C to survive in the failure when the CC1 or CC2 is shorted to the VBUS pin.

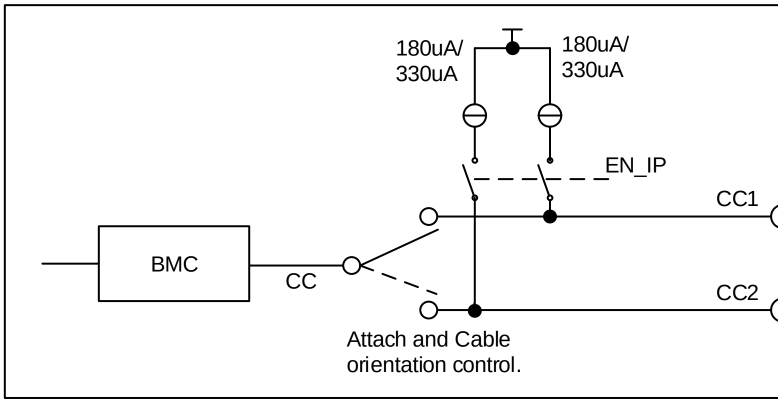


Figure 3. CCx Hardware Diagram

BMC DRIVER

Through the Type-C detection, one of the CC pins will be connected to the internal BMC block to achieve PD communication.

VBUS PIN

This pin is used to sense VBUS presence and discharge VBUS voltage on USB Type-C receptacle side.

VSAFE0V DETECTION

When the HUSB338C is attached with a Sink, it detects whether the VBUS voltage is within vSafe0V. If yes, the HUSB338C enters Attached.SRC state. If no, it will stay at AttachWait.SRC state.

VBUS DISCHARGE

The VBUS pin is also connected to an internal MOSFET and discharging circuitry, which is used as a bleeder to help dissipate the energy stored in the VBUS capacitor. With this bleeder, VBUS is discharged to vSafe0V upon the detachment of a connected device, or to a lower desired output voltage level upon a request command received from the Sink, such as from 12V to 5V.

GATE PIN

The GATE pin of the HUSB338C is designed to drive an external N-MOSFET. When the HUSB338C is attached and is ready to enable VBUS. The GATE pin outputs a voltage to turn on the external N-MOSFET. The turn on time of the external N-MOSFET may impacted by the external N-MOSFET's characteristics.

POWER SELECTION

The source output power can be set into different power levels and different PDP options through different combination of the configurations of the PS0 and PS1 pins, as shown in Table 6.

Table 6. Source Power Selection

PS0	PS1	Source Power Level
Floating	Floating	30W (5V/3A, 9V/3A, 12V/2.5A)
Floating	GND	18W (5V/3A, 9V/2A, 12V/1.5A)
Floating	VDD	18W (5V/3A, 9V/2A, 12V/1.5A, 3.3V~5.9V/3A, 3.3V~11V/2A)
GND	Floating	20W (5V/3A, 9V/2.22A)
GND	GND	20W (5V/3A, 9V/2.22A, 12V/1.66A)
GND	VDD	20W (5V/3A, 9V/2.22A, 12V/1.66A, 3.3V~5.9V/3A, 3.3V~11V/2.2A)
VDD	Floating	25W (5V/3A, 9V/2.77A, 3.3V~5.9V/3A, 3.3V~11V/2.75A)
VDD	GND	27W (5V/3A, 9V/3A, 12V/2.25A)
VDD	VDD	27W (5V/3A, 9V/3A, 12V/2.25A, 3.3V~11V/3A)

OVER VOLTAGE PROTECTION

The HUSB338C detects the VIN pin voltage to achieve over-voltage protection function. The threshold to trigger over-voltage protection is 120% of the VIN_REF. When the over-voltage condition occurs, the HUSB338C disables the

GATE pin. When the over-voltage condition is removed, the HUSB338C is reset to default mode and will automatic recover again.

UNDER VOLTAGE PROTECTION

The HUSB338C detects the VIN pin voltage to achieve under-voltage protection function. The threshold to trigger under-voltage protection is 80% of the VIN_REF. When the under-voltage condition occurs, the HUSB338C disables the GATE pin. When the over-voltage condition is removed, the HUSB338C is reset to default mode and will automatic recover again.

OVER CURRENT PROTECTION

When the current sensed by the sense resistor exceeds the 120% of IIN_REF, the over-current protection takes action and the GATE is also disabled. When the over-current condition is removed, the HUSB338C is reset to default mode and will automatic recover again.

FAST OVER CURRENT PROTECTION

The HUSB338C integrates FOCP protection function. When the VBUS is hard shorted to GND by fault, the output current increases sharply. When the output current reaches the FOCP threshold, the protections circuit takes action and turns off the external load switch. When the short condition is removed, the HUSB338C is reset to default mode and will automatic recover again.

THERMAL SHUT DOWN

When the junction temperature rises across T_{TSD}, thermal shut down takes action and the GATE is disabled. When the junction temperature falls across T_{TSD}-T_{TSD_HYS}, the HUSB338C is reset to default mode and will automatic recover again.

CHARGING PROTOCOLS AUTO SELECTION (DP AND DM PIN)

The HUSB338C supports various fast charging protocols including BC1.2 DCP, Apple Divider 3, QC 2.0/3.0 Class A, AFC, FCP and SCP. According to the different status of DP and DM pins, the HUSB338C recognizes the attached Sinks and apply the fast charging protocol automatically.

DPDM_APP MODE

The DPDM_APP mode is the mode that the HUSB338C supports the Apple Divider 3 charging protocol. In the DPDM_APP mode, the HUSB338C outputs 2.7 V DC voltage on both DP and DM pins. The 2.7 V can be pulled down by the attached Sink. If DP or DM pin is pulled down below V_{SEL_REF}, the HUSB338C exits the DPDM_APP mode and enters into DPDM_DCP mode.

DPDM_DCP MODE

The DPDM_DCP mode is the mode that the HUSB338C supports BC1.2 DCP protocol. The 2.7 V DC sources are removed and the DP and DM pins are shorted through R_{DPM_SHORT} resistor. It is possible for the attached Sink to start primary, secondary and HVDCP detection processes when the HUSB338C is in DPDM_DCP mode.

DPDM_HVDCP MODE

After successful detection of the DCP, the HUSB338C notify the Sink that the HUSB338C enters into HVDCP mode.

In the HVDCP mode, the HUSB338C monitors the DP/DM status and enters into different modes depending on the status of DP/DM pins.

TYPICAL APPLICATION CIRCUITS

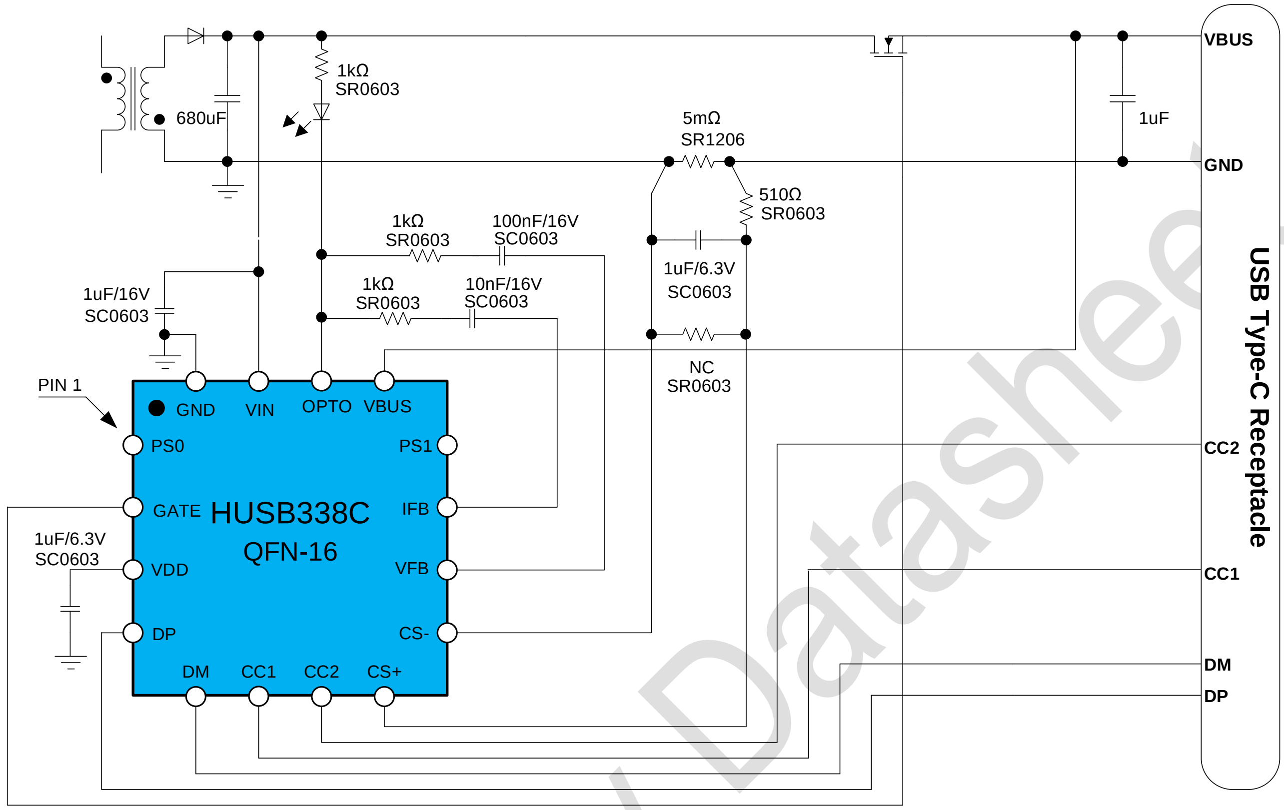
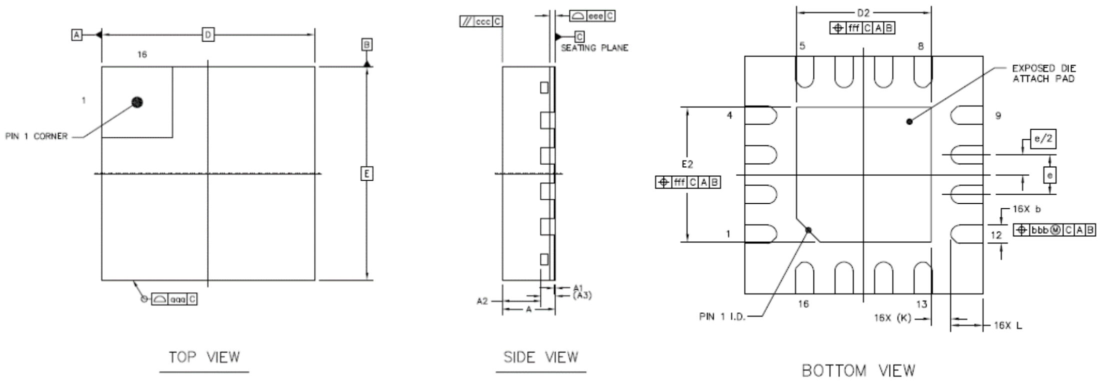


Figure 4. HUSB338C Typical Application Diagram

PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
b	0.18	0.30
D	2.90	3.10
E	2.90	3.10
e	0.5BSC	
D2	1.60	1.80
E2	1.60	1.80
L	0.25	0.50

Figure 5. QFN-16L Package, 3mm x 3mm

PACKAGE TOP MARKING

Figure 6. HUSB338C Package Top Marking

ORDERING GUIDE

Model	Package	5V[1]	9V	12V	3.3-5.9V	3.3-11V	Package Option
HUSB338C_001UA	QFN-16L, 3mm x 3mm	3A	3A	2.5A	-	-	Tape & Reel, 5k

[1] For more configuration info, please contact Hynetek.

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