FEATURES

- USB PD2.0 certified, TID 1000151, XID 0005398
- USB PD3.0 certified, TID 1000189, XID 0005399
- USB Type-C 1.2 and USB PD2.0/3.0 compliant
  - Support up to 5V, 9V, 12V and 15V four FPDOs.
  - Support one PPS APDO. Voltage adjustable in 20mV step. Current adjustable in 50mV step
- Support BC1.2 DCP and HVDCP fast charge protocols
  - BC1.2 DCP mode
  - 5V, 9V and 12V discrete mode voltage adjustment
  - 3.6V ~ 12V continuous mode voltage adjustment at 200mV step
- Integrate voltage l loop compensation and current loop compensation
  - Integrate secondary side compensation circuit, such as TL431
- VBUS and VIN pins fast discharge
- Voltage operating range: 3.3V to 20V
- Low power consumption - 250μA
- Cable voltage drop compensation
- CC pin support 20V high voltage to protect the CC pin and VBUSs pin short risk
- Support constant voltage loop (CV) and constant current loop (CC)
- Integrated VCONN power and eMarker detection
- OTP, VIN OVP, VIN UVP, VIN UVLO and OCP protections
- SOP-14L, QFN-16L and SSOP-10L packages
- ±5kV ESD HBM

APPLICATIONS

- AC-DC power adapter
- Car charger
- USB-PD converter

GENERAL DESCRIPTION

HUSB338L is a high performance, high integration USB Type-C Power Delivery source controller. HUSB338L supports PD3.0, PD2.0, PPS, QC2.0/3.0， BC1.2 DCP etc. The HUSB338 incorporates all required protections, like Over-temperature Protection (OTP), Over-voltage Protection (OVP), Under-voltage Protection (UVP), and Under-voltage Lock-Out (UVLO). It is available in SOP-14L, QFN-16L and SSOP-10L package options.

TYPICAL APPLICATION CIRCUIT

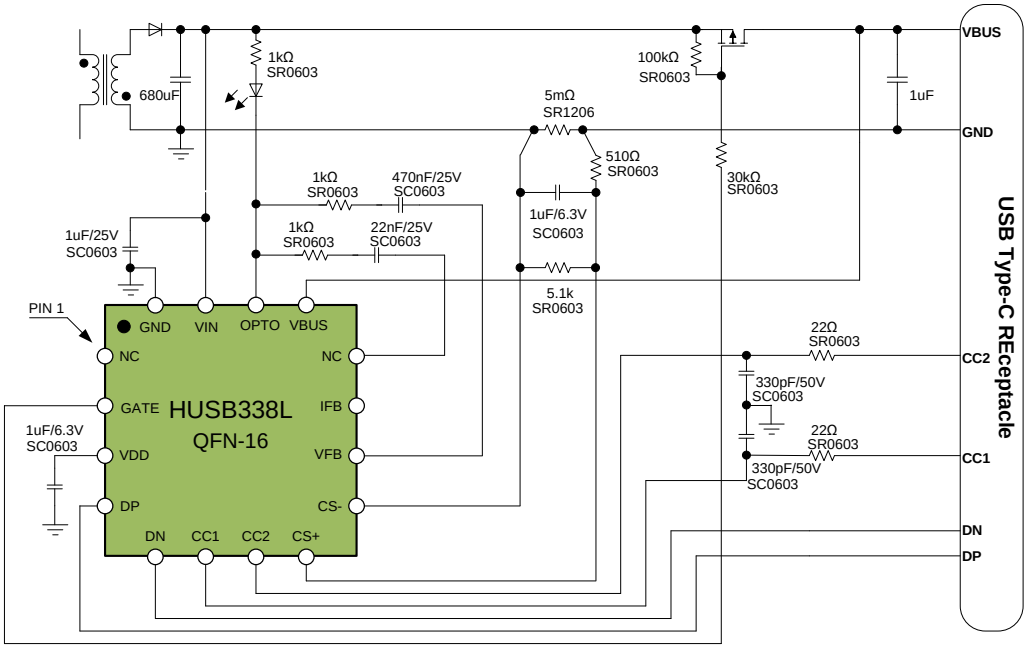


Figure 1.HUSB338L Typical Application Circuit

REVISION HISTORY

Version	Date	Descriptions
V1.0	July 25, 2018	Initial version
V1.1	August 20, 2018	Add USB PD3.0 certification information. Add 5V PDO voltage sense accuracy data. Remove SSOP-10 package information.
V1.2	August 19, 2019	Update the voltage sense accuracy in Table 1. Update the ordering guide Update package top marking
V1.3	September 14, 2019	Add SSOP-10L package
V1.4	October 31, 2019	Update Fig. 1 and Fig. 5
V1.5	June 20, 2020	Update Fig. 7

Contents

SPECIFICATIONS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GENERAL PARAMETERS						
Supply Voltage	V_{IN}		3.3		20	V
Supply Voltage UVLO Threshold	V_{IN_UVLO}	Rising		2.85		V
		Falling		2.75		V
Supply Current at Normal Operating	I_{CC_OPR}			1		mA
Supply Current at Sleep Mode	I_{CC_SLEEP}	GATE pin is not pulled low. CC1 and CC2 floating		250		μA
Regulator Voltage	V_{DD}			1.8		V
Operating Junction Temperature	T_J		-40		125	°C
Operating Ambient Temperature	T_A		-40		105	°C
Type-C						
Default Mode Pullup Current Source	I_{CC_DEF}		64	80	96	μA
1.5A Mode Pullup Current Source	I_{CC_1P5}		166	180	194	μA
3.0A Mode Pullup Current Source	I_{CC_3P0}		304	330	356	μA
UFP Detecting threshold at Default Current	V_{TH_DEF}		1.51	1.6	1.64	V
UFP Detecting threshold at 1.5A current	V_{TH_1A5}		1.51	1.6	1.64	V
UFP Detecting threshold at 3.0A current	V_{TH_3A0}		2.46	2.6	2.74	V
BMC COMMON PARAMETERS						
Bit Rate	$f_{BitRate}$		270	300	330	Kbps
BMC TX PARAMETERS						
Maximum Difference between the Bit-rate during the Part of the Packet Following the Preamble and the Reference Bit-rate.	$p_{BitRate}$				0.25	%
Time to Cease Driving the Line after the End of the Last bit of the Frame.	$t_{EndDriveBMC}$				23	μs
Fall Time	t_{Fall}		300			ns
Time to cease driving the line after the final high-to-low transition.	$t_{HoldLowBMC}$		1			μs
Time from the End of Last Bit of a Frame until the Start of the First bit of the Next Preamble.	$t_{InterFrameGap}$		25			μs
Rise Time	t_{Rise}		300			ns
Time Before the Start of the First Bit of the Preamble when the Transmitter shall Start Driving the Line.	$t_{StartDrive}$		-1		1	μs
Voltage Swing	v_{Swing}		1.05	1.125	1.2	V
Transmit Low Voltage			-75		75	mV
Transmitter Output Impedance	z_{Driver}		33	54	75	Ω
BMC RX PARAMETERS						
Hysteresis				160		mV
Time Window for Detecting Bus Non-idle	$t_{TransitionWindow}$		12		20	μs
Number to Count to Detect Bus Non-idle	n_{Count}		3			
Time Constant of a Single Pole Filter to Limit Broad-band Noise Ingression1	$t_{RxFilter}$		100			ns
Receiver Input Impedance	z_{BmcRx}		1			MΩ
D+ AND D- PINS						
Output Voltage Selection Reference	V_{SEL_REF}		1.8	2.0	2.2	V
Data Detect Voltage Reference	V_{DAT_REF}		0.25	0.325	0.4	V
DatLine Leakage Resistance	R_{DAT_LKG}		300	-	1500	kΩ
D- Pulldown Resistance during HVDCP Mode	R_{DM_DWM}		14.25	19	24.5	kΩ
D+ to D- Resistence During DCP mode	R_{DCP_DAT}			100	200	Ω
D+ High Gitch Filter Time	$T_{GLITCH\_BC\_DONE}$		1000	1250	1500	ms
D- Low Glitch Filter Time	$T_{GLITCH\_DM\_LOW}$		1	2		ms
Output Voltage Glitch Filter Time	$T_{GLITCH\_V\_CHANGE}$		20	40	60	ms
Glitch Filter for D+/- Continuous Change	$T_{GLITCH\_CONT\_CHANGE}$	Continuous Mode	100	150	200	us

VOLTAGE CONTROL(VFB PIN)						
Voltage Sense Scaling Factor				10		
Voltage Sense Accuracy		5V with no load	5.1		5.25	V
Time from Source issue GoodCRC to Start Voltage Transition	$t_{SrcTransition}$			30		ms
CURRENT CONTROL (CS+, CS-, IFB PINS)						
Current Sense Resistor				5		mΩ
GATE PIN						
Maximum Sinking Current			2		20	mA
Pull Low Impedance				50	150	Ω
OPTO PIN						
Min OPTO Current				30		μA
Max Pull Down Current				3		mA
OV AND OC PROTECTIONS						
Over-voltage Protection Threshold	V_{IN_OV}	With respect to V_{IN_REF}	115	120	125	%
Under-voltage Protection Threshold	V_{IN_UV}	With respect to V_{IN_REF}	75	80	85	%
Over-current Protection Threshold	I_{IN_OC}	With respect to I_{IN_REF}	110	125	140	%
Thermal Shutdown Risng	t_{TSD_RISE}			130		°C
Thermal Shutdown Falling	t_{TSD_FALL}			80		°C

ABSOLUTE MAXIMUM RATING

Table 2.

Parameter	Rating
VIN, GATE, VBUS, OPTO	−0.5V to +20V
CC1, CC2	−0.5V to +20V
VDD, D+, D-, CS+, CS-, VFB, IFB	−0.5V to +6V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
ESD HBM (Human Body Model)	±5kV
ESD MM (Machine Model)	500V
Soldering Conditions	JEDEC J-STD-020

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
SOP-14	83.5	37.7	°C/W
QFN-16	47	4.5	°C/W
SSOP-10L	88	37	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

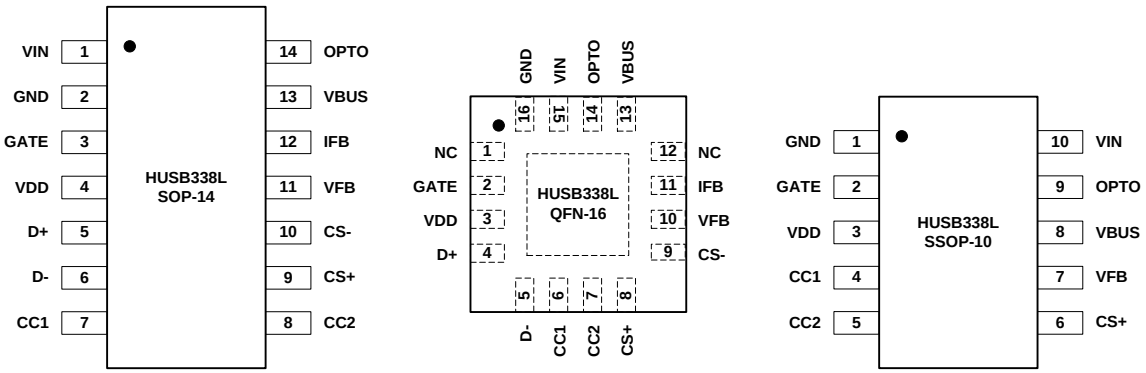


Figure 2. Pin Configuration, View from Top.

Table 4. HUSB338L Pin Function Description

SOP-14 Pin No.	QFN-16 Pin No.	SSOP-10 Pin No.	Pin Name	Pin Type	Voltage Type	Pin Description
1	15	10	VIN	P	HV	Supply input voltage. Connect this pin to GND via the recommended ceramic capacitor.
2	16	1	GND	P	-	Power ground.
-	1	-	NC	-	-	Not connection.
3	2	2	GATE	OD	HV	Open drain gate drive output.
4	3	3	VDD	P	LV	1.8 V regulator output for system power.
5	4	-	D+	DIO	LV	USB D+ line.
6	5	-	D-	DIO	LV	USB D- line.
7	6	4	CC1	AIO	HV	Type-C CC1 line.
8	7	5	CC2	AIO	HV	Type-C CC2 line.
9	8	6	CS+	AI	LV	Positive input of the current sense amplifier.
10	9	-	CS-	AI	LV	Negative input of the current sense amplifier. Provide a low ohmic connection to GND.
11	10	7	VFB	AI	LV	Voltage loop feedback.
12	11	-	IFB	AI	LV	Current loop feedback.
-	12	-	NC	-	-	Not connection.
13	13	8	VBUS	AI	HV	VBUS sense and discharge sink.
14	14	9	OPTO	AI	HV	OPTO driver.

Legend:

HV=High Voltage Pin (Max 20V)

LV=Low Voltage Pin (Max 6V)

OD=Open Drain Pin

A=Analog Pin

P= Power Pin

D=Digital Pin

I=Input Pin

O=Output Pin

THEORY OF OPERATION

VIN AND VDD PINS

VIN Power System

VIN pin is the power supply input, which is derived from the output of the AC-DC or DC-DC converter. Connect a 1μF decoupling MLCC between VIN pin and GND pin, as closer so possible.

VIN Discharge

The VIN pin is also connected to an internal MOSFET and discharging resistor, which is used as a bleeder to help discharge the output capacitor to vSafe5V upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as from 15V to 5V.

VIN Voltage Sense

See the Control Loop Compensation Circuit (VFB, CS+, CS-, IFB, OPTO Pins) section。

VDD System Supply

An internal liner regulator is used to provide 1.8V system voltage. Connect a 1μF MLCC to VDD pin for decoupling.

CONTROL LOOP COMPENSATION CIRCUIT (VFB, CS+, CS-, IFB, OPTO PINS)

In the HUSB338L, the constant voltage loop compensation (CV loop) and constant current loop (CC loop) compensation are implemented. The output of the compensator is used to drive the primary side of the opto-coupler and control the AC-DC power loop.

Constant Voltage Loop Compensation Circuit (CV Loop)

The input of CV loop is connected to VFB pin, which is derived from the internal 90kΩ and 10kΩ voltage divider. The voltage divider sense the VIN voltage. Therefore, the VFB voltage is 10% of VIN voltage. The CV loop compensator is implemented by the resistor and capacitor network between OPTO pin and VFB pin.

Constant Current Loop Compensation Circuit (CC Loop)

In HUSB338L, the CC loop input is derived from a 5mΩ current sense resistor. The current signal is filtered by an RC network and fed to the CS+ and CS- differential inputs. The CC loop compensator is implemented by the resistor and capacitor network between OPTO pin and IFB pin.

Cable Voltage Drop Compensation (IR Compensation)

The cable voltage drop compensation is implemented in HUSB338L. Once it is enabled, the output voltage increases with 100mV/A according to the load current. For example, for the 5V 3A condition, the actual output voltage is:

5V+3A*100mV/A=5.3V。

CC1 AND CC2 PINS

Type-C CC Function

CC1 and CC2 are the Configuration Channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable. CC1 and CC2 only support DFP mode with 500mA, 1.5A and 3A current advertising. The CC1 and CC2 supports 20V high voltage. This is used for protection when the CC1 or CC2 is shorted to the VBUS pin.

BCM Driver

Through the Type-C detection, one of CC1or CC2 pins will be connect to the internal BMC block to achieve PD communication.

VBUS PIN

This pin is used to sense VBUS presence, monitor VBUS voltage and discharge VBUS on USB Type-C receptacle side. Connect directly to VBUS at the Type-C Receptacle.

vSafe0V Detection

When the HUSB338 enter AttachWait.SRC for $t_{CCDebounce}$, it detects whether the VBUS voltage is within vSafe0V. If yes, HUSB338 pulls low GATE pin and enters Attached.SRC state. If no, it will stay at AttachWait.SRC state.

VBUS Discharge

The VBUS pin is also connected to an internal MOSFET and discharging resistor, which is used as a bleeder to help discharge the output capacitor to vSafe0V upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as from 15V to 5V.

GATE PIN

GATE pin is open–drain output allows to drive directly a PMOS load switch. When HUSB338L enters Type-C attached state (Attached.SRC), GATE pin is pulled low. When HUSB338 exits from Type-C attached state, the GATE pin is removed from being pulled low.

OVER-VOLTAGE PROTECTION (VIN_OV)

The HUSB338L detects the VIN pin voltage to achieve over-voltage protection function. The threshold to trigger over-voltage protection is 120% of the V_{IN_REF}. When the over-voltage condition occurs, the HUSB338L stops to pull the GATE pin low. When the over-voltage condition is removed, HUSB338L is reset to standby mode and will automatic recover again.

UNDER-VOLTAGE PROTECTION (VIN_UV)

The HUSB338L detects the VIN pin voltage to achieve under-voltage protection function. The threshold to trigger under-voltage protection is 80% of the V_{IN_REF}. When the under-voltage condition occurs, the HUSB338L stops to pull the GATE pin low. When the over-voltage condition is removed, HUSB338L is reset to standby mode and will automatic recover again.

OVER-TEMPERATURE PROTECTION (OT)

When the junction temperature rises across 130°C, over-temperature protection takes action and the load switch is turned off. When the junction temperature falls across 80°C, HUSB338L is reset to standby mode and will automatic recover again.

OVER-CURRENT PROTECTION (IIN_OC)

When the current sensed by the sense resistor exceeds the 125% of I_{IN_REF}, the over-current protection takes action and the load switch is turned off. When the over-current condition is removed, the HUSB338L is reset to standby mode and will automatic recover again.

D+ AND D- PINS

The HUSB338L with SOP-14L package and QFN-16L package supports BC1.2 DCP and HVDCP fast charger protocols. The HVDCP hardware diagram is shown in Figure 3. The voltage scaling truth cable is shown is Table 5.

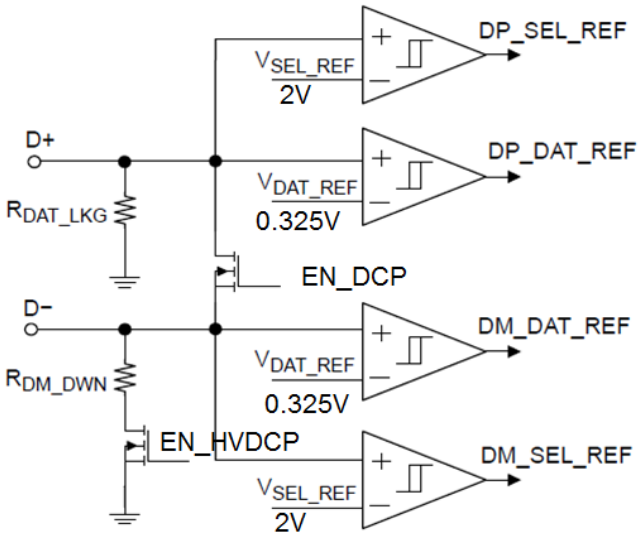


Figure 3. HVDCP Hardware Implementation

Table 5. HVDCP Voltage Scaling Truth Table

Portable Device		Class A HVDCP
D+	D−	Adapter Output Voltage

0.6V	0.6V	12V
3.3 V	0.6 V	9V
0.6 V	3.3 V	Continuous Mode
0.6 V	GND	5V

TYPICAL APPLICATIONS CIRCUITS

Figure 4 to Figure 5 provide some application circuits where the HUSB338Ldrives an optocoupler.

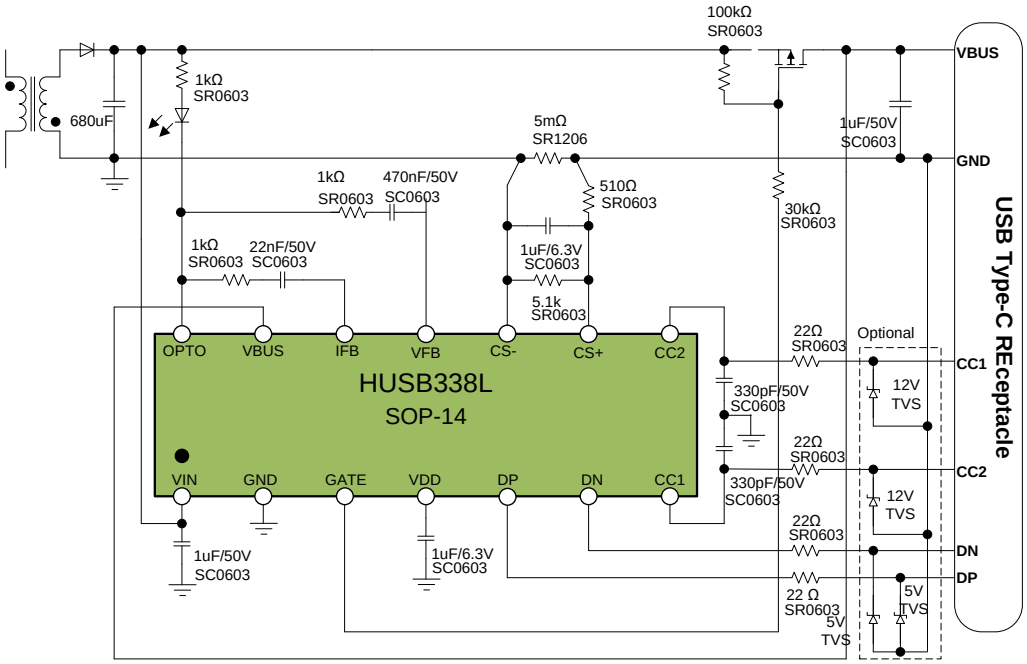


Figure 4. HUSB338L SOP-14L Package Application Circuit

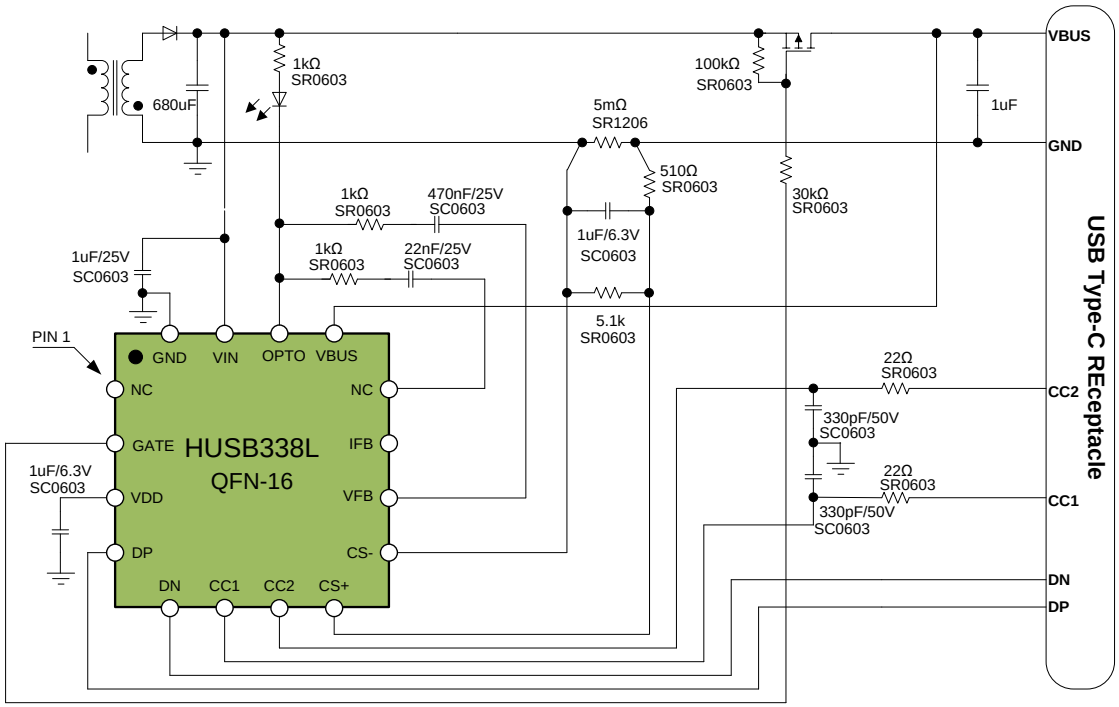
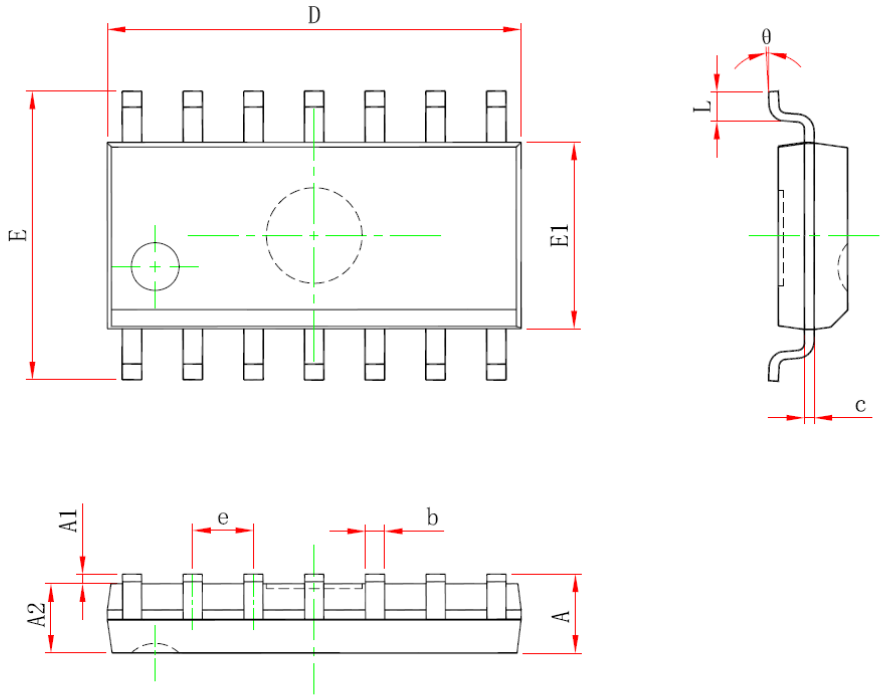


Figure 5. HUSB338L QFN-16L Package Application Circuit

PACKAGE OUTLINE DEMENSIONS

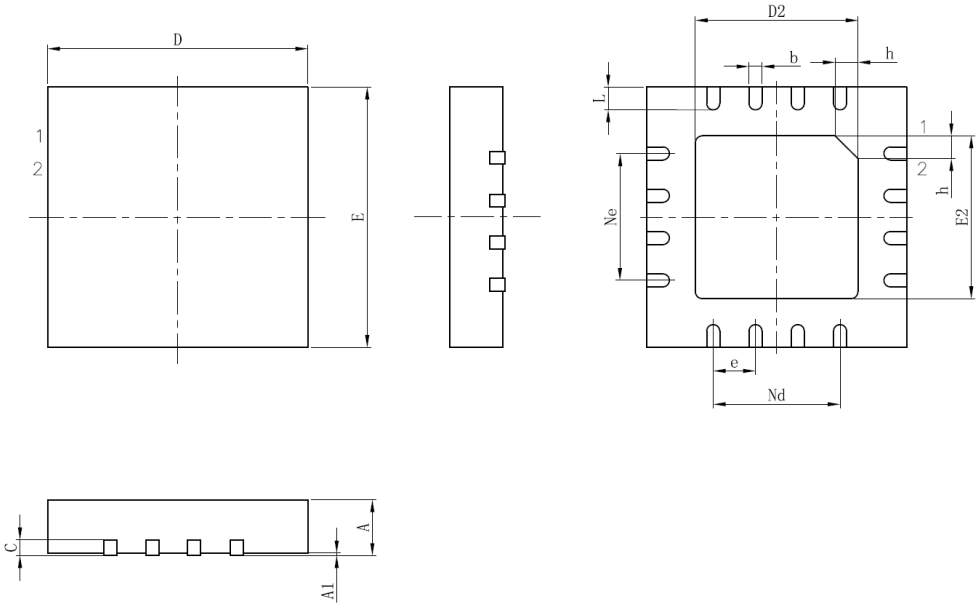
SOP-14L PACKAGE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Figure 6. SOP-14L Package, 8.65 mm × 6 mm

QFN-16L PACKAGE

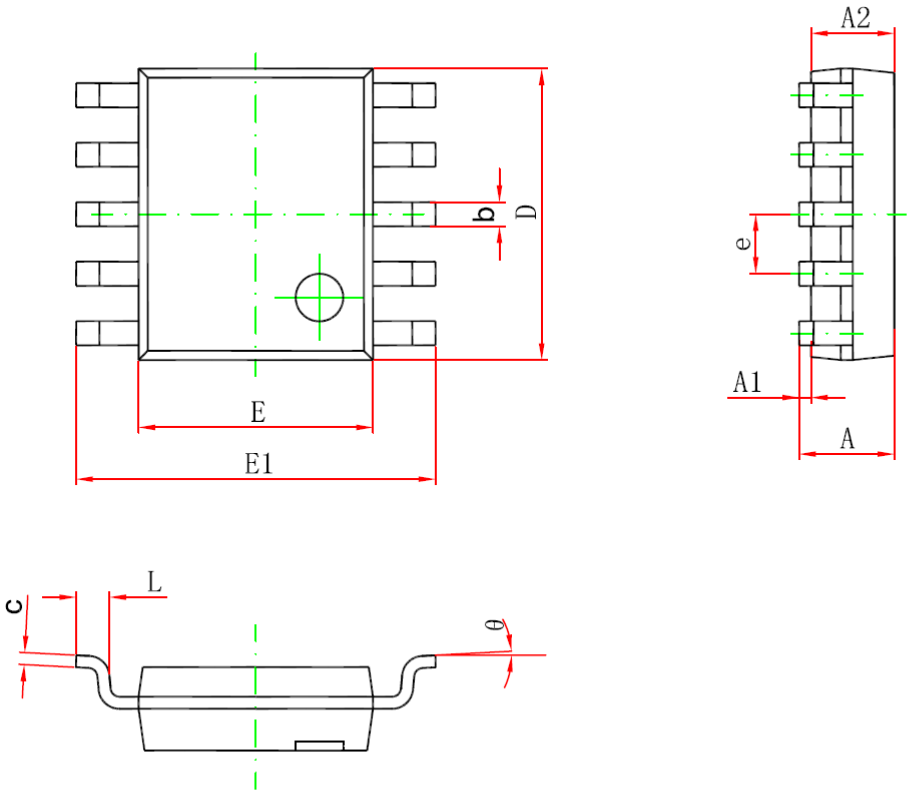


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	——	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.00	2.15	2.30
e	0.650BSC		
Ne	1.95BSC		
Nd	1.95BSC		
E	3.90	4.00	4.10
E2	2.00	2.15	2.30
L	0.45	0.55	0.65
h	0.30	0.35	0.40

Figure 7. QFN-16L Package, 4 mm × 4 mm

SSOP-10L PACKAGE

SSOP-10L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.300	0.450	0.012	0.018
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.000(BSC)		0.039(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	1°	8°

PACKGE TOP MARKING

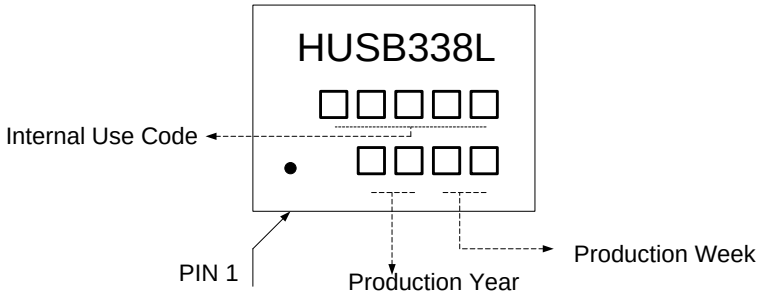


Figure 8. Package Top Marking

ORDERING GUIDE

Package	Model	Power	FPDO	APDO	QC2.0/3.0	Package Option
SOP-14L	See HUSB338L model list	Configurable	Configurable	Configurable	Configurable	Tape & Reel, 4k
QFN-16L	See HUSB338L model list	Configurable	Configurable	Configurable	Configurable	Tape & Reel, 5k
SSOP-10L	See HUSB338L model list	Configurable	Configurable	Configurable	Configurable	Tape & Reel, 4k

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