FEATURES

- USB PD3.0 certified, TID 62
- USB Type-C 1.2 and USB PD3.0 compliant
- Support up to five FPDOs
  - Typical 5V, 9V, 12V, 15V and 20V PDOs
  - Support 5V~23.5V user-defined FPDOs, 5A maximum current and 115W maximum output power
- Support two APDOs
  - Support 5V Prog, 9V Prog, 15V Prog and 20V Prog
  - Constant power control
- Support QC2.0/QC3.0, BC1.2 DCP protocols
  - Apple 5V, 2.4A mode
  - BC1.2 DCP mode
  - QC2.0 5V, 9V and 12V discrete mode voltage adjustment
  - QC3.0 3.6V ~ 12V continuous mode voltage adjustment at 200mV step
- Integrate constant voltage (CV) loop compensation and constant current (CC) loop compensation network
  - Integrate secondary side compensation circuit, such as TL431
- VBUS and VIN pins fast discharge
- Voltage operating range: 3.3V to 25V
- Support cable voltage drop compensation - 0, 50mΩ, 100mΩ or 150mΩ
- Support Smart Power Derating function
- Integrated VCONN power and eMarker detection for USB-C + USB-A dual-port charger or two USB-C ports charger
- OTP, VIN OVP, VIN UVP, VIN UVLO and OCP protections
- CC pin support 28V high voltage to protect the CC pin and VBUSs pin short risk
- SOP-14L and QFN-16L packages
- ±5kV ESD HBM

APPLICATIONS

- AC-DC power adapter
- Car charger
- USB-PD converter

GENERAL DESCRIPTION

The HUSB339 is a high performance, high-integrated USB Type-C Power Delivery source controller. The HUSB339 supports PD3.0, PD2.0, PPS, QC2.0/QC3.0, BC1.2 DCP etc. The HUSB339 incorporates all required protections, like Over-temperature Protection (OTP), Over-voltage Protection (OVP), Under-voltage Protection (UVP), and Under-voltage Lock-Out (UVLO). The HUSB339 supports smart power derating function for dual-port charger applications. It is available in SOP-14L and QFN-16L package options.

TYPICAL APPLICATION CIRCUIT

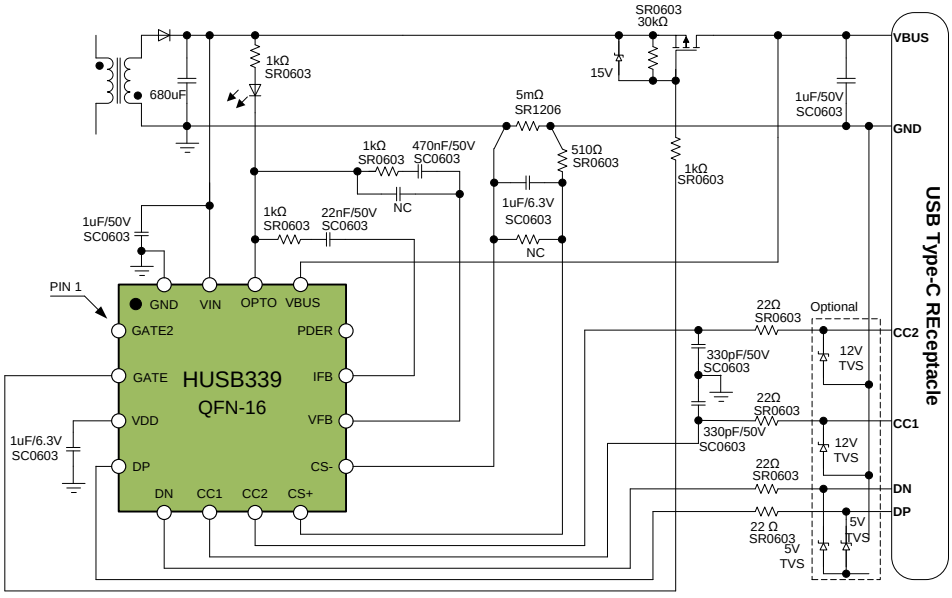


Figure 1. HUSB339 Typical Application Circuit

REVISION HISTORY

Version	Date	Descriptions
V1.0	Jan 21, 2019	Initial version
V1.1	May 28, 2019	Update Fig. 1 and add Fig. 6. Update descriptions of pins high voltage rating. Update descriptions of PDER pin function.
V1.2	Aug 19, 2019	Update package top marking
V1.3	June 20, 2020	Update Fig. 16

Contents

SPECIFICATIONS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GENERAL PARAMETERS						
Supply Voltage	V_{IN}		3.3		25	V
Supply Voltage UVLO Threshold	V_{IN_UVLO}	Rising		2.85		V
		Falling		2.75		V
Supply Current at Normal Operating	I_{CC_OPR}			1		mA
Supply Current at Sleep Mode	I_{CC_SLEEP}	CC1 and CC2 floating		250		µA
	I_{CC_SLEEP}	CC1 and CC2 Clamped		0.9		mA
Regulator Voltage	V_{DD}			1.8		V
Operating Junction Temperature	T_J		-40		125	°C
Operating Ambient Temperature	T_A		-40		105	°C
Type-C						
Default Mode Pullup Current Source	I_{CC_DEF}		64	80	96	µA
1.5A Mode Pullup Current Source	I_{CC_1P5}		166	180	194	µA
3.0A Mode Pullup Current Source	I_{CC_3P0}		304	330	356	µA
UFP Detecting threshold at Default Current	V_{TH_DEF}		1.51	1.6	1.64	V
UFP Detecting threshold at 1.5A current	V_{TH_1A5}		1.51	1.6	1.64	V
UFP Detecting threshold at 3.0A current	V_{TH_3A0}		2.46	2.6	2.74	V
BMC COMMON PARAMETERS						
Bit Rate	$f_{BitRate}$		270	300	330	Kbps
BMC TX PARAMETERS						
Maximum Difference between the Bit-rate during the Part of the Packet Following the Preamble and the Reference Bit-rate.	$p_{BitRate}$				0.25	%
Time to Cease Driving the Line after the End of the Last bit of the Frame.	$t_{EndDriveBMC}$				23	µs
Fall Time	t_{Fall}		300			ns
Time to cease driving the line after the final high-to-low transition.	$t_{HoldLowBMC}$		1			µs
Time from the End of Last Bit of a Frame until the Start of the First bit of the Next Preamble.	$t_{InterFrameGap}$		25			µs
Rise Time	t_{Rise}		300			ns
Time Before the Start of the First Bit of the Preamble when the Transmitter shall Start Driving the Line.	$t_{StartDrive}$		-1		1	µs
Voltage Swing	v_{Swing}		1.05	1.125	1.2	V
Transmit Low Voltage			-75		75	mV
Transmitter Output Impedance	z_{Driver}		33	54	75	Ω
BMC RX PARAMETERS						
Hysteresis				160		mV
Time Window for Detecting Bus Non-idle	$t_{TransitionWindow}$		12		20	µs
Number to Count to Detect Bus Non-idle	n_{Count}		3			
Time Constant of a Single Pole Filter to Limit Broad-band Noise Ingression1	$t_{RxFilter}$		100			ns
Receiver Input Impedance	z_{BmcRx}		1			MΩ
D+ AND D- PINS						
D+ and D- Floating Voltage		Mode 1		2.7		V
D- and D-		Mode 1		2.7		V
Output Voltage Selection Reference	V_{SEL_REF}		1.8	2.0	2.2	V
Data Detect Voltage Reference	V_{DAT_REF}		0.25	0.325	0.4	V
DatLine Leakage Resistance	R_{DAT_LKG}		300	-	1500	kΩ
D- Pulldown Resistance during HVDCP Mode	R_{DM_DWM}	Mode 3	14.25	19	24.5	kΩ
D+ to D- Resistence During DCP mode	R_{DCP_DAT}	Mode 2		100	200	Ω
D+ High Gitch Filter Time	$T_{GLITCH\_BC\_DONE}$		1000	1250	1500	ms
D- Low Glitch Filter Time	$T_{GLITCH\_DM\_LOW}$		1	2		ms

Output Voltage Glitch Filter Time	$T_{GLITCH\_V\_CHANGE}$		20	40	60	ms
Glitch Filter for D+/- Continuous Change	$T_{GLITCH\_CONT\_CHANGE}$	Mode 3, Continuous Mode	100	150	200	us
VOLTAGE CONTROL(VFB PIN)						
Voltage Sense Scaling Factor				10		
Time from Source issue GoodCRC to Start Voltage Transition	$t_{SrcTransition}$			30		ms
CURRENT CONTROL (CS+, CS-, IFB PINS)						
Current Sense Resistor				5		mΩ
GATE PIN						
Maximum Sinking Current			2		20	mA
Pull Low Impedance				50	150	Ω
GATE2 PIN						
Maximum Sinking Current			2		20	mA
Pull Low Impedance				50	150	Ω
PDER PIN						
Low Level Input Voltage	V_{IL}				0.8	V
High Level Input Voltage	V_{IH}	To trigger power derating	1.4			V
OPTO PIN						
Min OPTO Current				30		µA
Max Pull Down Current				3		mA
OV AND OC PROTECTIONS						
Over-voltage Protection Threshold	V_{IN_OV}	With respect to V_{IN_REF}	115	120	125	%
Under-voltage Protection Threshold	V_{IN_UV}	With respect to V_{IN_REF}	75	80	85	%
Over-current Protection Threshold	I_{IN_OC}	Default, With respect to I_{IN_REF}		115		%
Thermal Shutdown Risng	t_{TSD_RISE}			130		°C
Thermal Shutdown Falling	t_{TSD_FALL}			80		°C

ABSOLUTE MAXIMUM RATING

Table 2.

Parameter	Rating
VIN, GATE, VBUS, OPTO	−0.5V to +28V
CC1, CC2, PDER	−0.5V to +28V
GATE2, D+, D-, CS+, CS-, VFB, IFB	−0.5V to +6V
VDD	-0.5V to +2V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
ESD HBM (Human Body Model)	±5 kV
ESD MM (Machine Model)	500 V
Soldering Conditions	JEDEC J-STD-020

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
SOP-14L	83.5	37.7	°C/W
QFN-16L	47	4.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

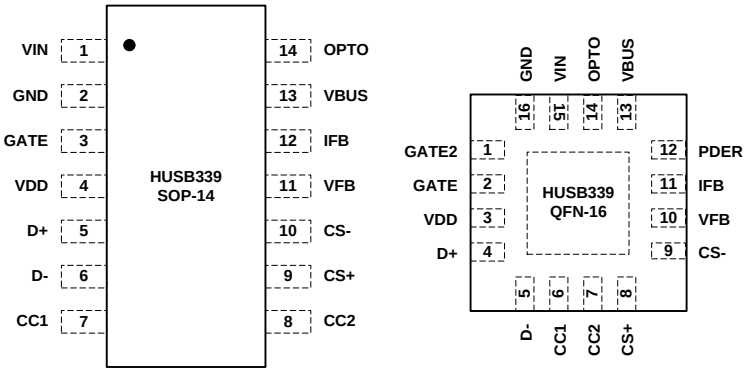


Figure 2. Pin Configuration, View from Top.

Table 4. HUSB339 Pin Function Description

SOP-14 Pin No.	QFN-16 Pin No.	Pin Name	Pin Type	Voltage Type	Pin Description
1	15	VIN	P	HV	Supply input voltage. Connect this pin to GND via the recommended ceramic capacitor.
2	16	GND	P	-	Power ground.
-	1	GATE2	OD	LV	Second gate driver pin.
3	2	GATE	OD	HV	Open drain gate drive output.
4	3	VDD	P	-	1.8 V regulator output for system power.
5	4	D+	DIO	LV	USB D+ line.
6	5	D-	DIO	LV	USB D- line.
7	6	CC1	AIO	HV	Type-C CC1 line.
8	7	CC2	AIO	HV	Type-C CC2 line.
9	8	CS+	AI	LV	Positive input of the current sense amplifier.
10	9	CS-	AI	LV	Negative input of the current sense amplifier. Provide a low ohmic connection to GND.
11	10	VFB	AI	LV	Voltage loop feedback.
12	11	IFB	AI	LV	Current loop feedback.
-	12	PDER	AI	HV	Power derating control pin. High level to trigger power derating.
13	13	VBUS	AI	HV	VBUS sense and discharge sink.
14	14	OPTO	AI	HV	OPTO driver.

Legend:

HV=High Voltage Pin (Max 28V)

LV=Low Voltage Pin (Max 6V)

OD=Open Drain Pin

A=Analog Pin

P= Power Pin

D=Digital Pin

I=Input Pin

O=Output Pin

THEORY OF OPERATION

VIN AND VDD PINS

VIN Power System

VIN pin is the power supply input, which is derived from the output of the AC-DC or DC-DC converter. Connect a 1μF decoupling MLCC between VIN pin and GND pin, as closer so possible.

VIN Discharge

The VIN pin is also connected to an internal MOSFET and discharging resistor, which is used as a bleeder to help discharge the output capacitor to vSafe5V upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as from 20V to 5V.

VIN Voltage Sense

See the Control Loop Compensation Circuit (VFB, CS+, CS-, IFB, OPTO Pins) section。

VDD System Supply

An internal liner regulator is used to provide 1.8V system voltage. Connect a 1μF MLCC to VDD pin for decoupling, as closer so possible.

CONTROL LOOP COMPENSATION CIRCUIT (VFB, CS+, CS-, IFB, OPTO PINS)

In the HUSB339, the constant voltage loop compensation (CV loop) and constant current loop (CC loop) compensation are implemented. The output of the compensator is used to drive the primary side of the opto-coupler and control the AC-DC power loop.

Constant Voltage Loop Compensation Circuit （CV Loop）

The input of CV loop is connected to VFB pin, which is derived from the internal 90kΩ and 10kΩ voltage divider. The voltage divider sense the VIN voltage. Therefore, the VFB voltage is 10% of VIN voltage. The CV loop compensator is implemented by the resistor and capacitor network between OPTO pin and VFB pin.

Constant Current Loop Compensation Circuit (CC Loop）

USB PD3.0 PPS defines current limit function clearly. In the HUSB339, the CC loop input is derived from a 5mΩ current sense resistor. The current signal is filtered by an RC network and fed to the CS+ and CS- differential inputs. The CC loop compensator is implemented by the resistor and capacitor network between OPTO pin and IFB pin.

Voltage Shift Slew Rate

During PD voltage shift, to make sure the voltage shift smoothly and to reduce inrush during voltage shift, the HUSB339 has a fixed voltage shift slew rate setting.

Cable Voltage Drop Compensation （IR Compensation）

The cable voltage drop compensation is implemented in the HUSB339. Once it is enabled, the output voltage increases with 0mV/A, 50mV/A, 100mV/A or 150mV/A according to the load current. It is equivalent to adding a negative resistance to cancel or reduce the cable resistance. The negative resistance can be programmed as 0mΩ, -50mΩ, -100mΩ or -150mΩ.

For example, for the 5V 3A condition, the actual output voltage is: 5V+3A*100mV/A=5.3V.

CC1 AND CC2 PINS

Type-C CC Function

CC1 and CC2 are the Configuration Channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable. CC1 and CC2 only support DFP mode with 500mA, 1.5A and 3A current advertising. CC1 and CC2 can support 28V high voltage. This is used for protection when the CC1 or CC2 is shorted to the VBUS pin.

BCM Driver

Through the Type-C detection, one of CC1or CC2 pins will be connect to the internal BMC block to achieve PD communication.

VCONN Power and eMarker Detection

The HUSB339 supports VCONN power and USB eMarker (such as HUSB330, HUSB331 or HUSB332) detection function. The USB PD protocol defines that if an adapter is not with a captive cable, when the adapter has a PD output current more than 3A, it's PD controller must support VCONN power supply and eMarker detection function.

For example, in a 90W PD power adapter, when the HUSB339 detects the eMarker IC in the cable which indicates that the cable current rating is 5A current, the HUSB339 can broadcast a preset 20V/4.5A output capability, and then the sink device can draw 90W power. If the HUSB339 does not detect an eMarker IC or the current rating indicated by the eMarker IC is only 3A, the HUSB339 can only broadcast maximum 3A output current capability, and the sink device can only draw maximum power of 60W.

D+ AND D- PINS

The HUSB339 has D+ Pin and D- Pin, which can support three charge modes as below:

Mode1: 5V/2.4A charge mode

The HUSB339 support 5V/2.4A charge mode.

Mode2: USB BC1.2 DCP charge mode

The HUSB339 support USB BC1.2 DCP charge protocol.

Mode3: QC2.0/QC3.0 quick charge mode

The QC2.0/QC3.0 hardware diagram is shown in Figure 3. The voltage scaling truth cable is shown is Table 5.

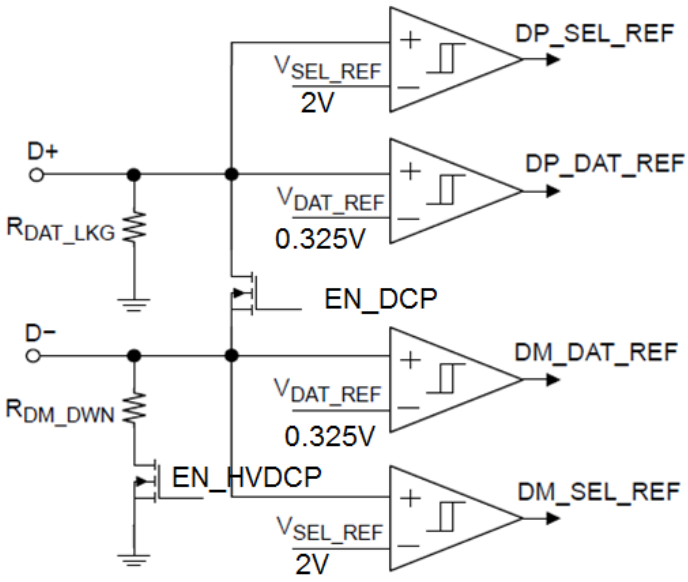


Figure 3. QC3.0 Hardware Implementation

Table 5. QC3.0 Voltage Scaling Truth Table

Portable Device		Class A HVDCP
D+	D−	Adapter Output Voltage
0.6V	0.6V	12V
3.3 V	0.6 V	9V
0.6 V	3.3 V	Continuous Mode
0.6 V	GND	5V

VBUS PIN

This pin is used to sense VBUS presence, monitor VBUS voltage and discharge VBUS on USB Type-C receptacle side. Connect directly to VBUS at the Type-C Receptacle.

vSafe0V Detection

When the HUSB339 enter AttachWait.SRC for $t_{CCDebounce}$, it detects whether the VBUS voltage is within vSafe0V. If yes, the HUSB339 pulls low GATE pin and enters Attached.SRC state. If no, it will stay at AttachWait.SRC state.

VBUS Discharge

The VBUS pin is also connected to an internal MOSFET and discharging resistor, which is used as a bleeder to help discharge the output capacitor to vSafe0V upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as from 20V to 5V.

GATE PIN

The GATE pin is open–drain output allows to drive directly a PMOS load switch. When the HUSB339 enters Type-C attached state (Attached.SRC), GATE pin is pulled low. When the HUSB339 exits from Type-C attached state, the GATE pin is removed from being pulled low.

GATE2 PIN

The GATE2 pin is open-drain output which is used to enable a load for the power adapter under a certain condition. If this function is enabled, the GATE2 pin turns high to control an external circuit when VIN<3.6V and current sense value is below 0.5A.

The HUSB339 SOP-14L package does not support this function.

PDER PIN

The HUSB339 with QFN-16L package supports Smart Power Derating (SPD) function, which can optimize output power distribution when used in a USB-A + USB-C dual-port charger or USB-C +USB-C dual-port charger. When the Smart Power Derating is enabled, USB-A port plug-in and plug-out signal goes to the HUSB339 through the PDER pin. And then the HUSB339 derates or recover it's source power capability announcement and actual power output rating. The range of derating power can be preset to any value such as 10W, 12W, 15W, 18W, 20W or 30W. Below is how the HUSB339 Smart Power Derating function works:

- If the HUSB339 PDER pin is at low level before it enters to PD mode, the HUSB339 will send out source capability with preset normal PD power to enter PD mode.
- If the HUSB339 PDER pin is at high level before it enters to PD mode, the HUSB339 will send out source capability with preset normal PD power subtracted by a preset derating power value to enter PD mode. The derating power value can be set to any value.
- In PD mode, if the HUSB339 PDER pin voltage state changes from low level to high level, the HUSB339 will re-enter to new PD mode source capability with preset normal PD power subtracted by a preset derating power value.
- In PD mode, if the HUSB339 PDER pin voltage state changes from high level to low level, the HUSB339 will re-enter to new PD mode source capability with preset normal PD power.

The HUSB339 SOP-14L package does not support this function.

PROTECTION FUNCTIONS

OVER-VOLTAGE PROTECTION (VIN_OV)

The HUSB339 detects the VIN pin voltage to achieve over-voltage protection function. The threshold to trigger over-voltage protection is 120% of the V_{IN_REF}. When the over-voltage condition occurs, the HUSB339 stops to pull the GATE pin low. When the over-voltage condition is removed, the HUSB339 is reset to standby mode and will automatic recover again.

UNDER-VOLTAGE PROTECTION (VIN_UV)

The HUSB339 detects the VIN pin voltage to achieve under-voltage protection function. The threshold to trigger under-voltage protection is 80% of the V_{IN_REF}. When the under-voltage condition occurs, the HUSB339 stops to pull the GATE pin low. When the over-voltage condition is removed, the HUSB339 is reset to standby mode and will automatic recover again.

According to PD protocol, under-voltage protection is turned off when it works in PPS mode.

OVER-TEMPERATURE PROTECTION (OT)

When the junction temperature rises across 130°C, over-temperature protection takes action and the load switch is turned off. When the junction temperature falls across 80°C, the HUSB339 is reset to standby mode and will automatic recover again.

OVER-CURRENT PROTECTION (IIN_OC)

When the current sensed by the sense resistor exceeds protection threshold, the over-current protection takes action and the load switch is turned off. When the over-current condition is removed, the HUSB339 is reset to standby mode and will automatic recover again.

TYPICAL APPLICATIONS CIRCUITS

Figure 4 to Figure 5 provide some application circuits where the HUSB339 drives an opto-coupler. Figure 6 shows the typical application of car charger.

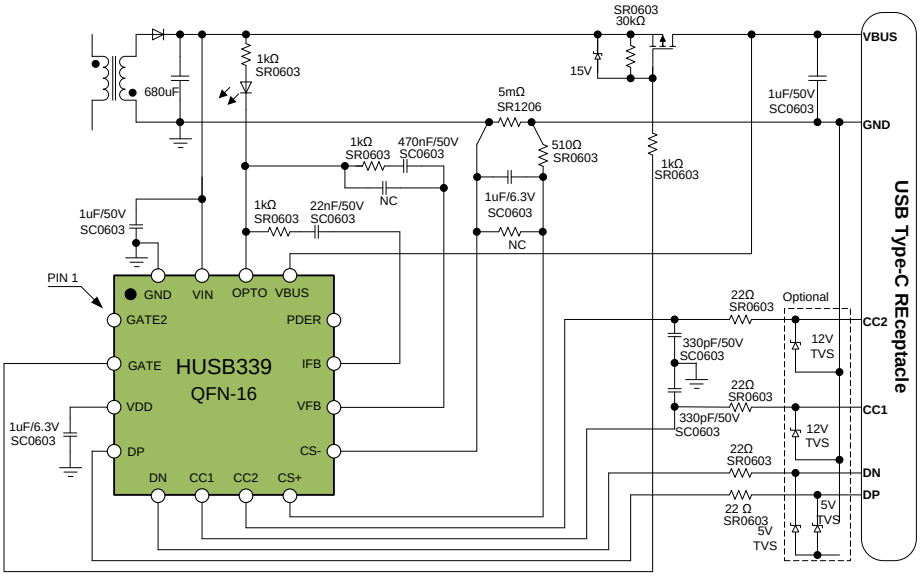


Figure 4. HUSB339 QFN-16L Package Application Circuit

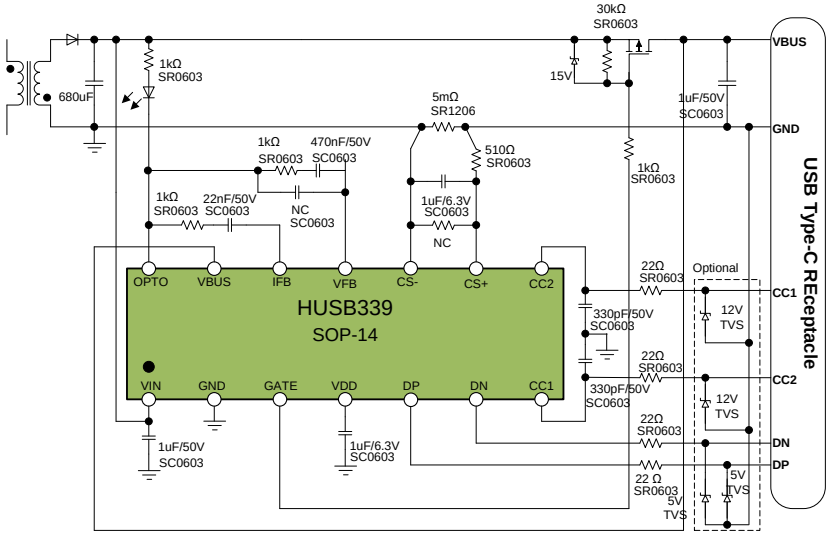


Figure 5. HUSB339 SOP-14L Package Application Circuit

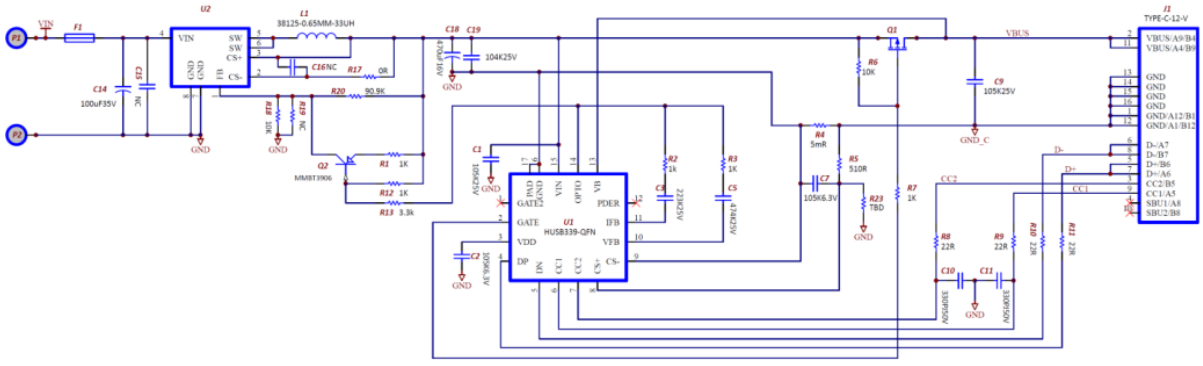


Figure 6. HUSB339 typical car charger application

CIRCUIT DESIGN OF SYSTEM AND APPLICATION

Constant voltage loop compensation design

The CV loop compensation is the network between OPTO pin and VFB pin, as shown in Figure 7. A 1kΩ resistor and a 470nF capacitor placed in series are recommended. Increasing the capacitance value can achieve more stable loop, but the voltage transient response may be slowed down. The “NC” marked device is an optional capacitor to optimize high frequency loop characteristics. We suggest debug the HUSB339 circuit and main power supply circuit together to achieve best loop performance.

Constant current loop compensation design

The CC loop compensation is the network between OPTO pin and IFB pin used in constant current control mode, as show in Figure 7. A 1kΩ resistor and a 22nF capacitor in series are recommended. Change of capacitance value can get different constant current response speed. We suggest debug the HUSB339 circuit and main power supply circuit together to achieve best loop performance.

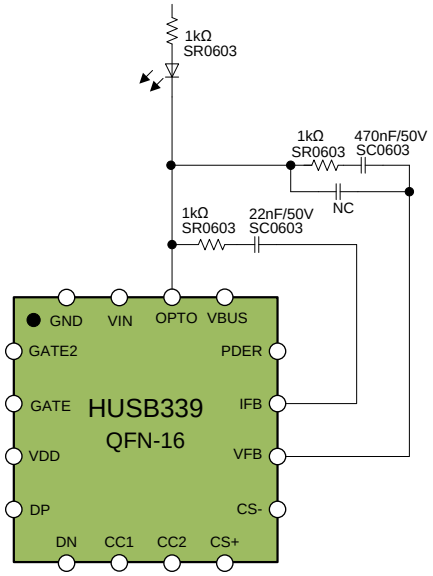


Figure 7. HUSB339 compensation loop circuit

CC1 and CC2 design

The CC1 and CC2 pins can sustain 28V high voltage and 5kV HBM ESD. In extremely conditions, even CC1/CC2 shorts to 25V VBUS voltage will not cause chip to be damaged. To improve high reliability, we suggest adding filter circuit and ESD protection devices shown in Figure 8. The resistor and capacitor values are recommended to be 22Ω and 330pF respectively. This circuit can meet USB PD eye diagram test requirement.

The filter capacitor should connect to the HUSB339 ground. 12V voltage rating TVS devices are recommended, and the TVS devices should be connect to Type-C connector power ground closely.

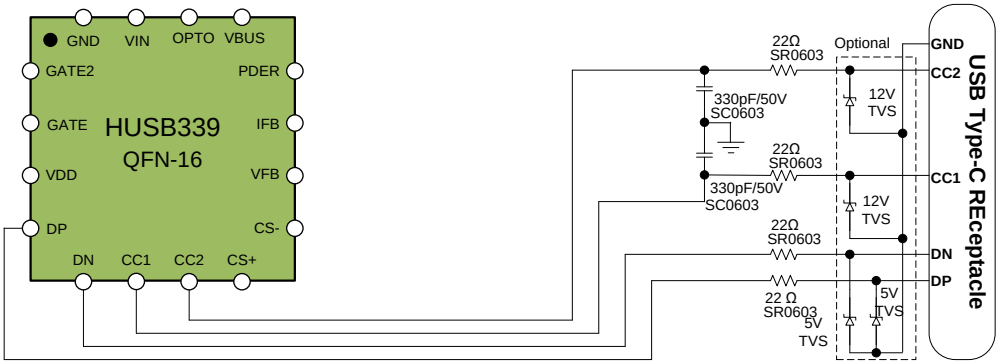


Figure 8. CC1/CC2 and D+/D- circuit

D+/D- design

In the HUSB339, D+/D- pins support 5kV ESD HBM. To improve high reliability, we suggest adding filter circuit and ESD protection device in Figure 8. A 22Ω resistor is recommended. In addition, 5V TVS deviced are recommended, and should be connect to Type-C connector power ground closely.

PMOS gate driver design

To select a suitable PMOS, we need to consider about below points:

- Select -30V rated Vds PMOS to meet more than 20V VBUS output.
- Calculate maximum current by maximum nominal current x1.3, select a proper Rdson specification, and then calculate maximum power dissipation and temperature rise.
- If PPS is needed, the lowest VBUS is 3.15V, then Vgs(th) spec should be considered to make sure the PMOS can be normally driven and output rated current when VBUS is 3.15V.

The driver divided resistor value is recommended with 30kΩ and 1kΩ, as shown in Figure 9. 15V rated TVS in Figure 9 is used when the maximum output voltage is 20V. The PMOS specification can be changed according to real application situation. For example, when the power adapter does not support 20V PDO, then the 15V TVS is not required. When the power adapter does not support PPS, the 1kΩ resistance can be changed to 10kΩ, and no TVS is required.

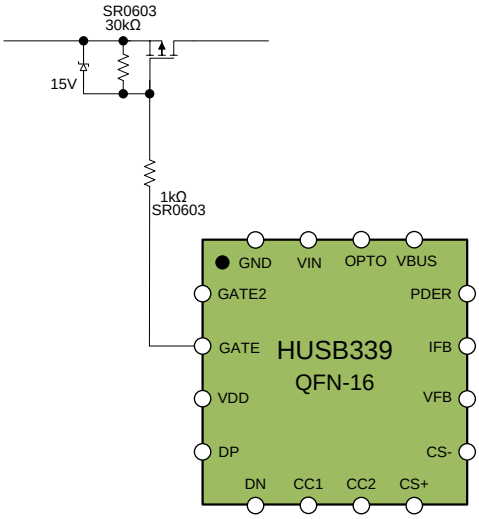


Figure 9. PMOS typical driver circuit

Current sense design

As shown in Figure 10, the current sense resistor is 5mΩ. 1% accuracy and 1206 package are recommended. In normal situation, 0.25W power dissipation rating is enough for this resistor. To reduce the interference of the current ripple, we recommend adding a 510Ω and 1uF RC filter network. The current sense signal should goes to CS+ pin and CS- pin with differential routing. Please refer to PCB Layout Guide section to design current sense layout on PCB. If the overcurrent protection threshold is lower than the setting value caused by poor PCB layout, the “NC” marked resistor in Figure 10 can be added to fine adjust the overcurrent protection threshold.

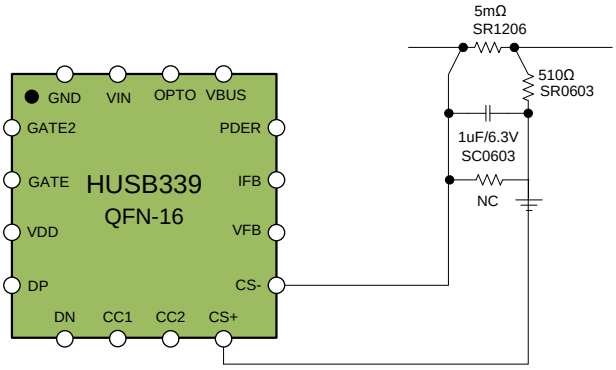


Figure 10. Current sense circuit

PCB LAYOUT GUIDE

The PCB layout guide is described based on the reference design of HUSB339 SOP-14L package PD daughter card. When the HUSB339 is placed on AC-DC power board, the guide should also be followed.

CC1 AND CC2 PINS ESD PROTETCION

As shown in Figure 11, capacitors C7 and C8, resistors R6 and R10 should be placed closely to the HUSB339. The ground connection of capacitors C7 and C8 should be close to GND pin of the HUSB339. The TVS devices D1 and D4 should be close to Type-C connector power ground.

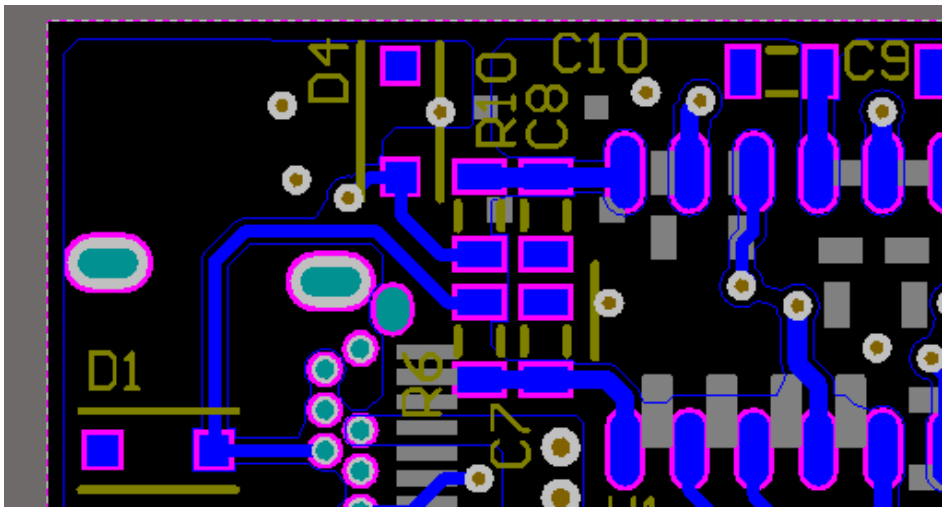


Figure 11. CC1 and CC2 routing

D+ AND D- PINS ESD PROTETCION

As shown in Figure 12, D+ and D- connects to Type-C connector by resistors R12 and R11 respectively. The TVS devices D2 and D3 should be close to Type-C connector power ground.

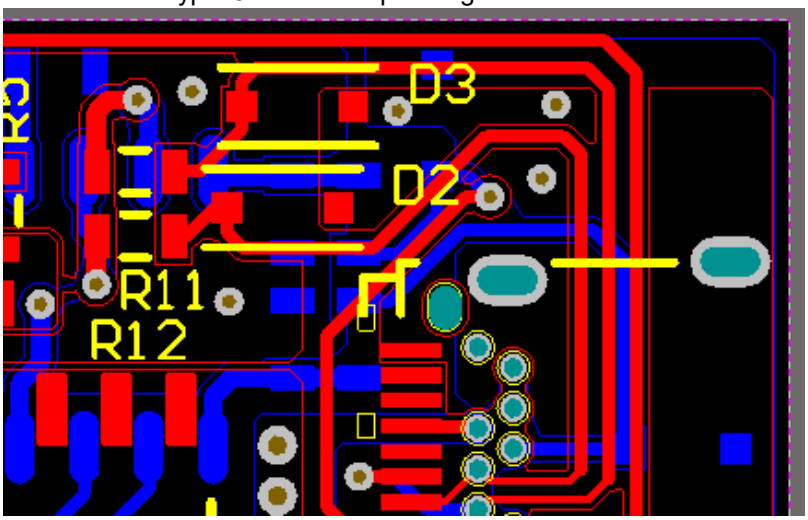


Figure 12. D+ and D- routing

CURRENT SENSE CIRCUIT PCB ROUTING

As shown in Figure 13, the GND pin of the HUSB339 connects to the power ground with the sense resistor R3. Try to avoid the HUSB339 ground and CS- grounding connecting together. If the HUSB339 ground connects to CS- pin unavoidably, the connection between the HSB339 ground and grounding end of R3 should be short and thick as much as possible. The capacitor filter C2 should be as close to the CS+ and CS- pins of the HUSB339 as possible, we suggest using Kelvin Connect to connect current sense resistor by leading a differential pair signal from the sense resistor pads. The current sense resistor connects power ground and Type-C connector ground, the routing should be short and thick. No inductance device is allowed in this path.

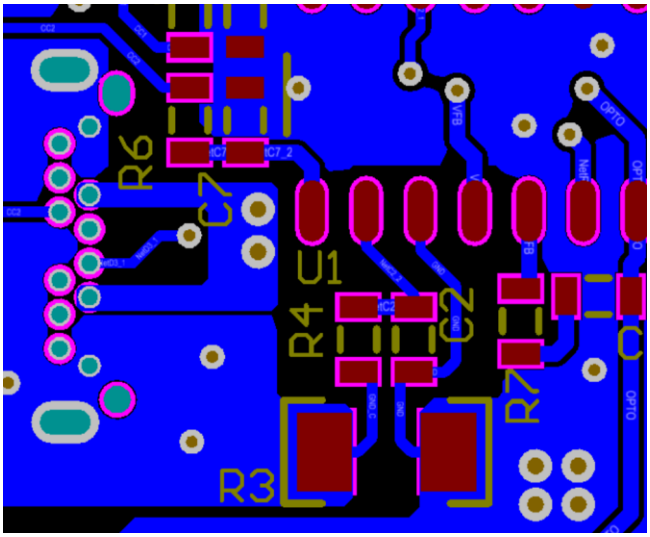


Figure 13. Current sense routing

DECOUPLING CAPACITOR PLACEMENT

As shown in Figure 14, the decoupling capacitor C9 should be placed as closer to VIN pin of the HUSB339 as possible. The power input goes from the daughter card VIN pin and goes to the C9 first, then goes to the VIN pin of the HUSB339. The VDD decoupling capacitor should be placed as closer to the VDD pin as possible.

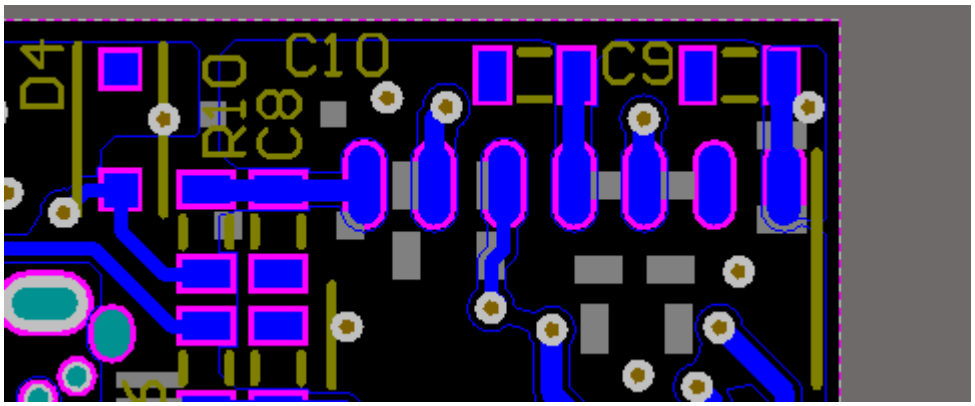
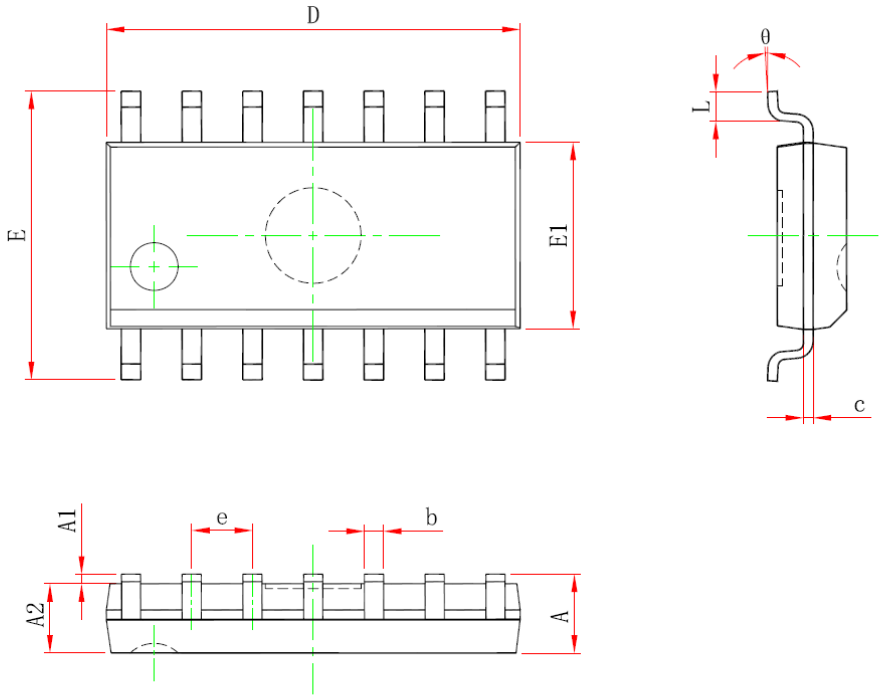


Figure 14. HUSB339 decoupling capacitor placement

PACKAGE OUTLINE DEMENSIONS

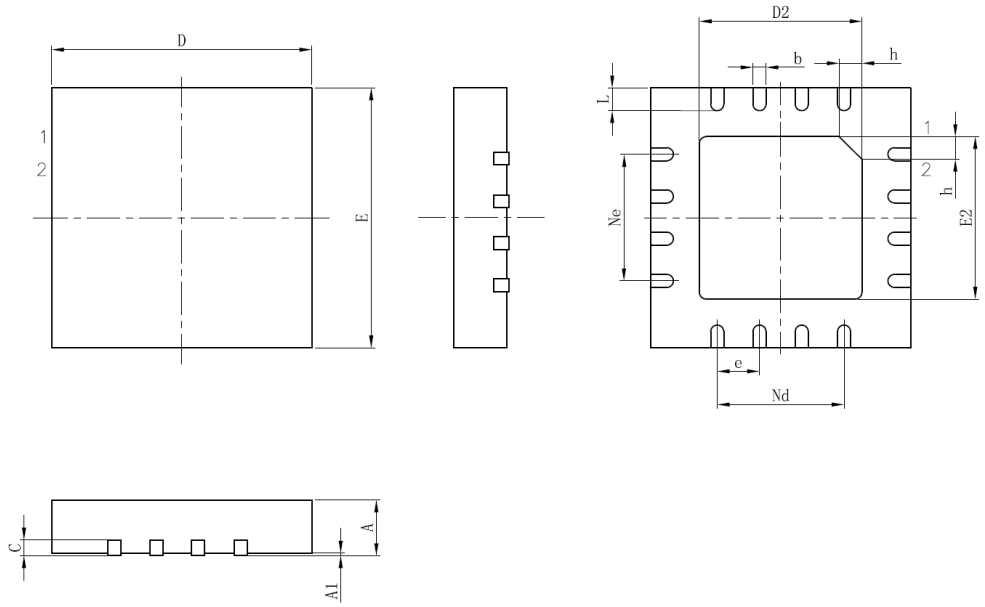
SOP-14L PACKAGE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Figure 15. SOP-14L Package, 8.65 mm × 6 mm

QFN-16L PACKAGE



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	——	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.00	2.15	2.30
e	0.650BSC		
Ne	1.95BSC		
Nd	1.95BSC		
E	3.90	4.00	4.10
E2	2.00	2.15	2.30
L	0.45	0.55	0.65
h	0.30	0.35	0.40

Figure 16. QFN-16L Package, 4 mm × 4 mm

PACKGE TOP MARKING

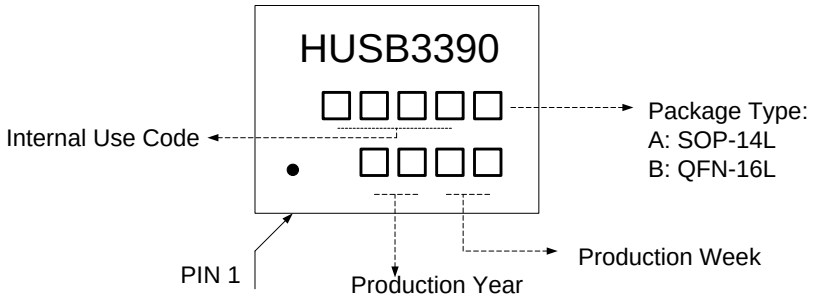


Figure 17. Package Top Marking

ORDERING GUIDE

Package	Model	Power	FPDO	APDO	QC	Shipping Option
SOP-14L	Configurable	Configurable	Configurable	Configurable	Configurable	Tape & Reel, 4k
QFN-16L	Configurable	Configurable	Configurable	Configurable	Configurable	Tape & Reel, 5k

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