64-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options					
		84-Pad Ceramic Leadless Chip Carrier	84-J Lead Plastic Chip Carrier	80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die
HV03	220V	HV0322LC	HV0322PJ	HV0322DG	HV0322PG	HV0322T	HV0322X
	300V	HV0330LC	HV0330PJ	HV0330DG	HV0330PG	HV0330T	HV0330X
HV05	220V	HV0522LC	HV0522PJ	HV0522DG	HV0522PG	HV0522T	HV0522X
	300V	HV0530LC	HV0530PJ	HV0530DG	HV0530PG	HV0530T	HV0530X

Features

- ☐ HVCMOS® Technology
- ☐ Output voltages up to 300V using a ramped supply
- ☐ Sink current minimum 100 mA
- ☐ Shift register speed 8 MHz
- ☐ Latched outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}	-0.5V to +15V
Supply voltage, V_{PP}[2]	-0.5V to +225V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[3]	6.0A
Continuous total power dissipation[4]	1900mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Notes: 1. All voltages are referenced to V_{SS}.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV03 and HV05 are low voltage serial to high voltage parallel converters with open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic printheads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV03 shifts in the counterclockwise direction when viewed from the top of the package and the HV05 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

The HV03 and HV05 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or limit the current through each output.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All V_{IN} = 0V
$I_{O(OFF)}$	Off State Output Current				100	µA	All outputs high, All SWS parallel
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_I = 0V
V_{OH}	High-Level Output Data Out		V_{DD} -1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			15	V	IHV_{OUT} = +100mA
		Data Out			1	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				-1.5	V	I_{OL} = -100mA

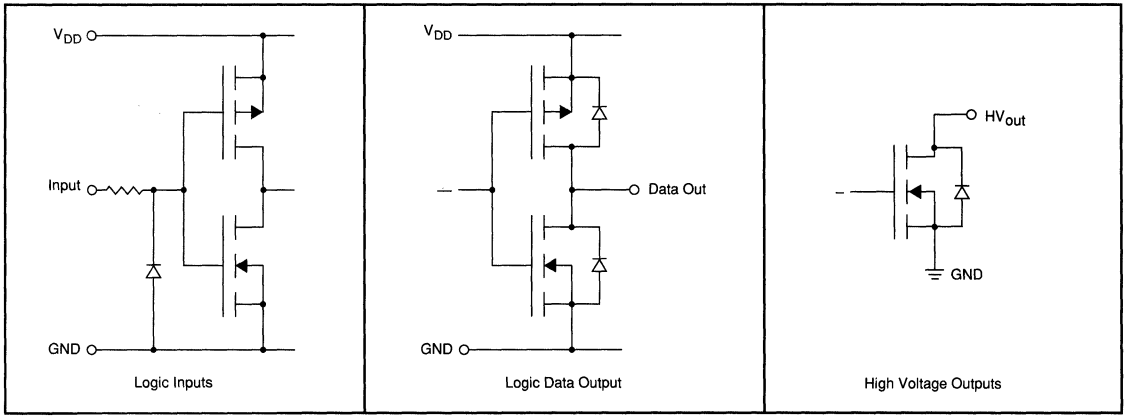
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Falls	25			ns	
t_H	Data Hold Time After Clock Falls	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	LE Delay Time Falling Edge of Clock	25			ns	
t_{SLE}	LE Setup Time Before Falling Edge of Clock	30			ns	
t_D	Delay Time from V_{PP} Low Until Change in LE, $\overline{POL}$, $\overline{BL}$ Is Allowed	100			ns	
t_{SL}	Setup Time from Falling Edge $\overline{LE}$ to V_{PP} Rise	200			ns	
t_{SB}	Setup Time from $\overline{BL}$ Selected to V_{PP} Rise	150			ns	
t_{SP}	Setup Time from $\overline{POL}$ Selected to V_{PP} Rise	100			ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLK}	Delay Time Clock to Data Low to High			100	ns	

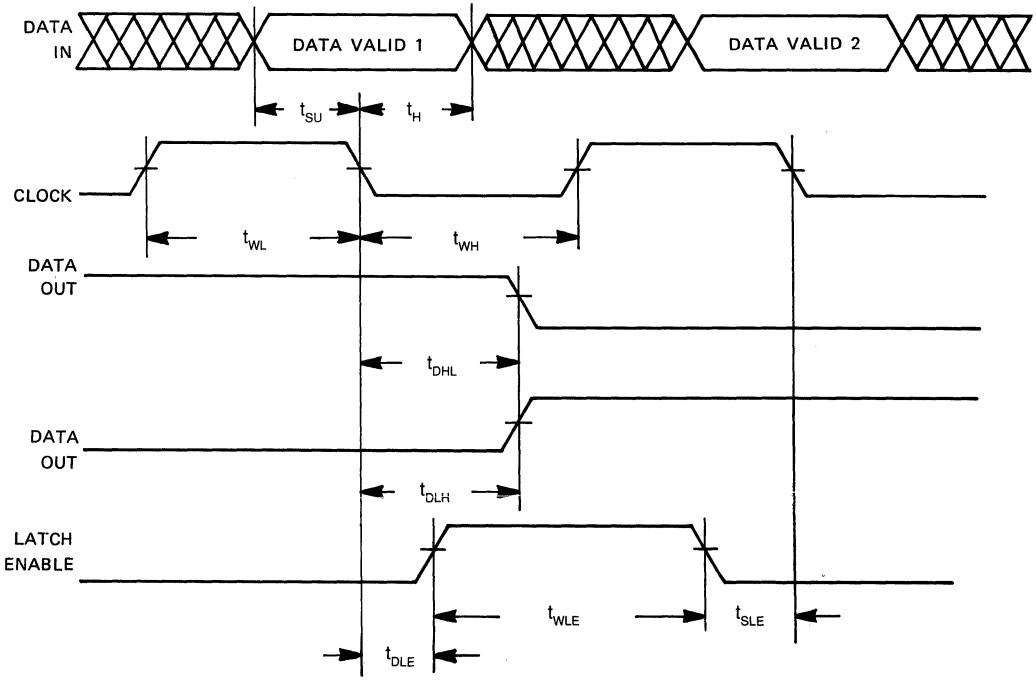
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage		10.8	12	13.2	V
V_{PP}	High voltage supply	HV0320/HV0520	-0.3		200	V
		HV0330/HV0530	-0.3		300	V
V_{IH}	High-level input voltage		V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage		0		2.0	V
dV/dt	V_{PP} ramp rate				80	V/µs
T_A	Operating free-air temperature		-40		+85	°C

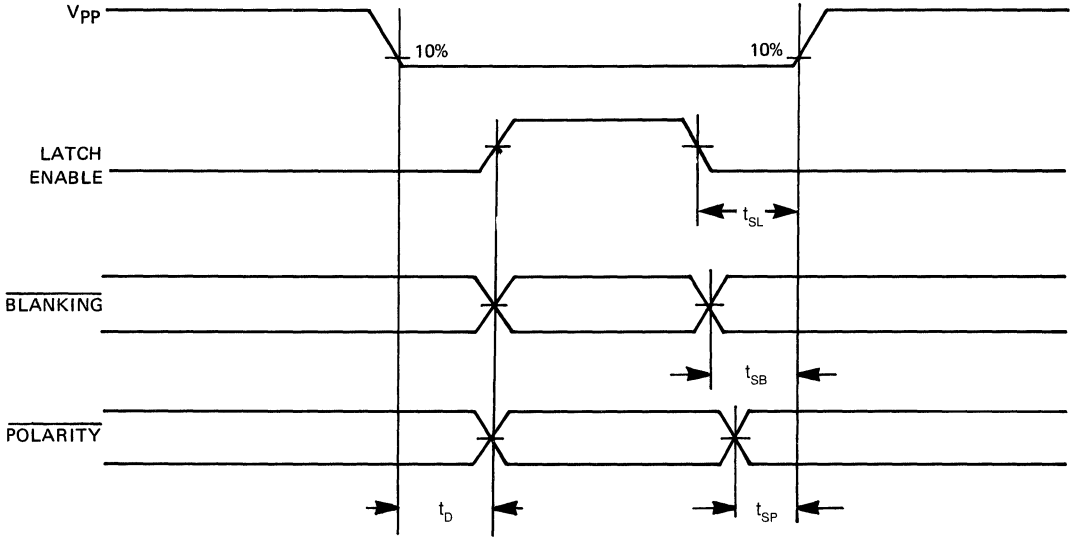
Input and Output Equivalent Circuit



Switching Waveforms

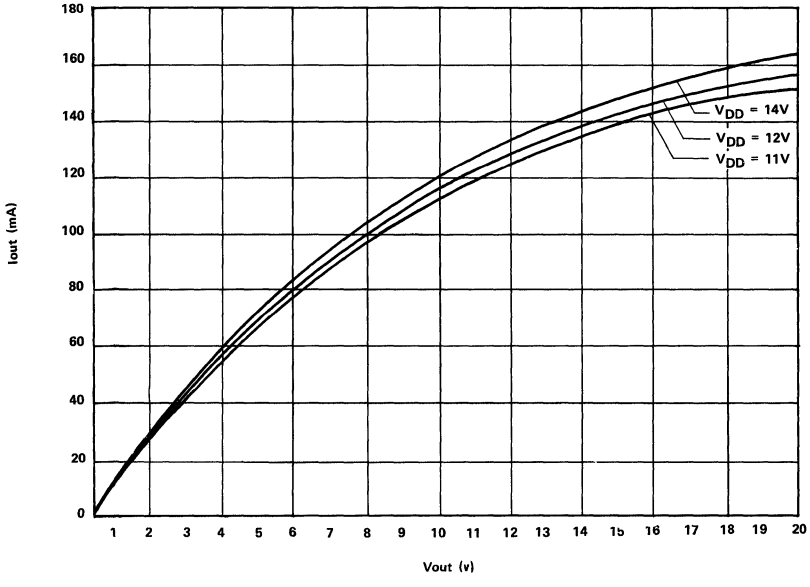


Output Control Waveforms

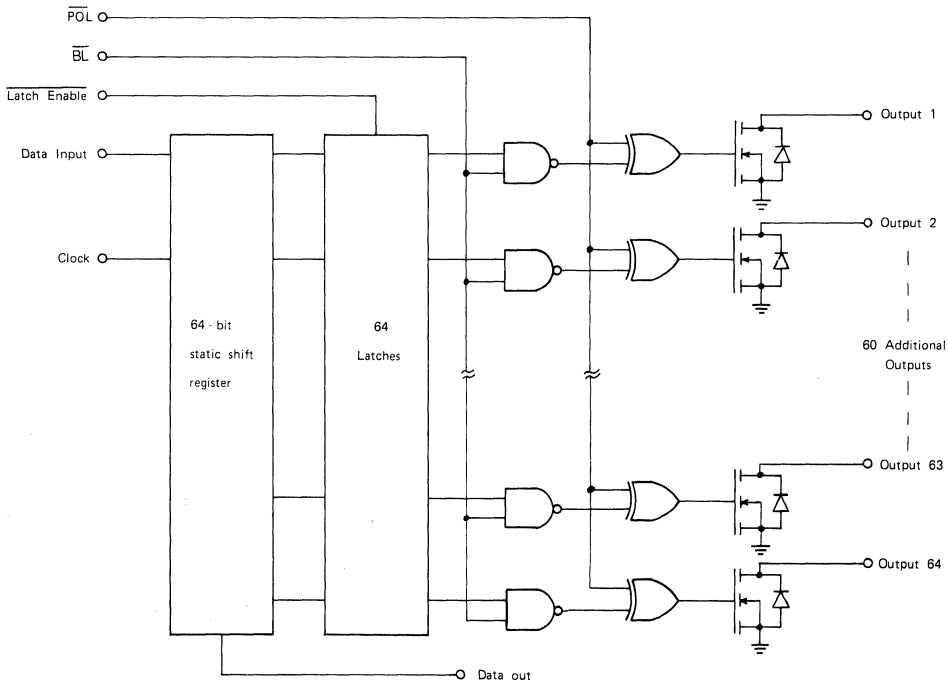


Typical Operating Conditions

SINK CURRENT @ 25C



Functional Block Diagram



Function Table

Function	Inputs					Outputs			
	DI	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1 2.....64	Latch 1 2.....64	HV Outputs 1 2.....64	Data Out
All on	X	X	X	L	L	* *..... *	* *..... *	L L..... L	*
All off	X	X	X	L	H	* *..... *	* *..... *	H H..... H	*
Invert mode	X	X	L	H	L	* *..... *	* *..... *	$\overline{*}$ $\overline{*}$..... $\overline{*}$	*
Load S/R	HorL	↓	L	H	H	HorL *..... *	* *..... *	* *..... *	*
Load latches	X	X	H	X	X	* *..... *	* *..... *	* *..... *	*
Transparent Latch mode	L	↓	H	H	H	L *..... *	L *..... *	H *..... *	*
	H	↓	H	H	H	H *..... *	H *..... *	L *..... *	*

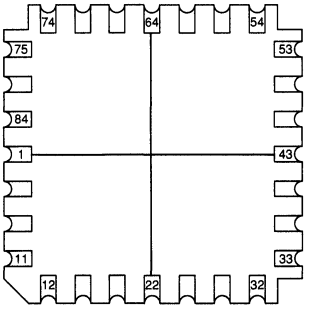
X = Don't care
* = Dependent on previous stage's state before the last CLK : or last LE high
↓ = High to low transition
H = High level
L = Low level

Pin Configurations

PJ and LC Packages

HV03				HV05			
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	V_{DD}	43	HVout 33	1	V_{DD}	43	HVout 32
2	$\overline{LE}$	44	HVout 34	2	$\overline{LE}$	44	HVout 31
3	Data In	45	HVout 35	3	Data In	45	HVout 30
4	$\overline{BL}$	46	HVout 36	4	$\overline{BL}$	46	HVout 29
5	HVout 1	47	HVout 37	5	HVout 64	47	HVout 28
6	HVout 2	48	HVout 38	6	HVout 63	48	HVout 27
7	HVout 3	49	HVout 39	7	HVout 62	49	HVout 26
8	HVout 4	50	HVout 40	8	HVout 61	50	HVout 25
9	HVout 5	51	HVout 41	9	HVout 60	51	HVout 24
10	HVout 6	52	HVout 42	10	HVout 59	52	HVout 23
11	N/C	53	N/C	11	N/C	53	N/C
12	GND	54	GND	12	GND	54	GND
13	GND	55	GND	13	GND	55	GND
14	HVout 7	56	HVout 43	14	HVout 58	56	HVout 22
15	HVout 8	57	HVout 44	15	HVout 57	57	HVout 21
16	HVout 9	58	HVout 45	16	HVout 56	58	HVout 20
17	HVout 10	59	HVout 46	17	HVout 55	59	HVout 19
18	HVout 11	60	HVout 47	18	HVout 54	60	HVout 18
19	HVout 12	61	HVout 48	19	HVout 53	61	HVout 17
20	HVout 13	62	HVout 49	20	HVout 52	62	HVout 16
21	HVout 14	63	HVout 50	21	HVout 51	63	HVout 15
22	HVout 15	64	HVout 51	22	HVout 50	64	HVout 14
23	HVout 16	65	HVout 52	23	HVout 49	65	HVout 13
24	HVout 17	66	HVout 53	24	HVout 48	66	HVout 12
25	HVout 18	67	HVout 54	25	HVout 47	67	HVout 11
26	HVout 19	68	HVout 55	26	HVout 46	68	HVout 10
27	HVout 20	69	HVout 56	27	HVout 45	69	HVout 9
28	HVout 21	70	HVout 57	28	HVout 44	70	HVout 8
29	HVout 22	71	HVout 58	29	HVout 43	71	HVout 7
30	GND	72	GND	30	GND	72	GND
31	GND	73	GND	31	GND	73	GND
32	N/C	74	N/C	32	N/C	74	N/C
33	HVout 23	75	HVout 59	33	HVout 42	75	HVout 6
34	HVout 24	76	HVout 60	34	HVout 41	76	HVout 5
35	HVout 25	77	HVout 61	35	HVout 40	77	HVout 4
36	HVout 26	78	HVout 62	36	HVout 39	78	HVout 3
37	HVout 27	79	HVout 63	37	HVout 38	79	HVout 2
38	HVout 28	80	HVout 64	38	HVout 37	80	HVout 1
39	HVout 29	81	$\overline{POL}$	39	HVout 36	81	$\overline{POL}$
40	HVout 30	82	Data Out	40	HVout 35	82	Data Out
41	HVout 31	83	CLK	41	HVout 34	83	CLK
42	HVout 32	84	GND	42	HVout 33	84	GND

Package Outline



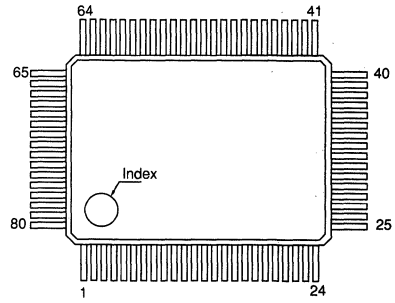
84-Pin Ceramic LCC

Pin Configurations

PG and DG Packages

HV03				HV05			
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	GND	41	GND	1	GND	41	GND
2	GND	42	GND	2	GND	42	GND
3	HVout 59	43	HVout 23	3	HVout 6	43	HVout 42
4	HVout 60	44	HVout 24	4	HVout 5	44	HVout 41
5	HVout 61	45	HVout 25	5	HVout 4	45	HVout 40
6	HVout 62	46	HVout 26	6	HVout 3	46	HVout 39
7	HVout 63	47	HVout 27	7	HVout 2	47	HVout 38
8	HVout 64	48	HVout 28	8	HVout 1	48	HVout 37
9	POL	49	HVout 29	9	POL	49	HVout 36
10	Data Out	50	HVout 30	10	Data Out	50	HVout 35
11	CLK	51	HVout 31	11	CLK	51	HVout 34
12	GND	52	HVout 32	12	GND	52	HVout 33
13	V_{DD}	53	HVout 33	13	V_{DD}	53	HVout 32
14	LE	54	HVout 34	14	LE	54	HVout 31
15	Data In	55	HVout 35	15	Data In	55	HVout 30
16	$\overline{BL}$	56	HVout 36	16	$\overline{BL}$	56	HVout 29
17	HVout 1	57	HVout 37	17	HVout 64	57	HVout 28
18	HVout 2	58	HVout 38	18	HVout 63	58	HVout 27
19	HVout 3	59	HVout 39	19	HVout 62	59	HVout 26
20	HVout 4	60	HVout 40	20	HVout 61	60	HVout 25
21	HVout 5	61	HVout 41	21	HVout 60	61	HVout 24
22	HVout 6	62	HVout 42	22	HVout 59	62	HVout 23
23	GND	63	GND	23	GND	63	GND
24	GND	64	GND	24	GND	64	GND
25	HVout 7	65	HVout 43	25	HVout 58	65	HVout 22
26	HVout 8	66	HVout 44	26	HVout 57	66	HVout 21
27	HVout 9	67	HVout 45	27	HVout 56	67	HVout 20
28	HVout 10	68	HVout 46	28	HVout 55	68	HVout 19
29	HVout 11	69	HVout 47	29	HVout 54	69	HVout 18
30	HVout 12	70	HVout 48	30	HVout 53	70	HVout 17
31	HVout 13	71	HVout 49	31	HVout 52	71	HVout 16
32	HVout 14	72	HVout 50	32	HVout 51	72	HVout 15
33	HVout 15	73	HVout 51	33	HVout 50	73	HVout 14
34	HVout 16	74	HVout 52	34	HVout 49	74	HVout 13
35	HVout 17	75	HVout 53	35	HVout 48	75	HVout 12
36	HVout 18	76	HVout 54	36	HVout 47	76	HVout 11
37	HVout 19	77	HVout 55	37	HVout 46	77	HVout 10
38	HVout 20	78	HVout 56	38	HVout 45	78	HVout 9
39	HVout 21	79	HVout 57	39	HVout 44	79	HVout 8
40	HVout 22	80	HVout 58	40	HVout 43	80	HVout 7

Package Outline



top view

80-pin Gullwing Package